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Capacitor ESR and C Monitoring in Modular Multilevel Converters

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Abstract- The capacitor is one of the weakest components in the module multilevel converter (MMC). The rise of equivalent series resistance (ESR) is a prominent character to monitor the lapsed capacitor, but current researches only focus on capacitance and neglect ESR of capacitors in the MMC. This paper proposed a sorting-based monitoring strategy for capacitors in the MMC, which monitors not only the capacitance but also the ESR of capacitor. This paper reveals the relationship among the capacitor's ESR, capacitance, current and energy. Based on the relationship, the ESRs and capacitances of submodule (SM) capacitors in the arm are indirectly sorted, respectively, and only the capacitor with biggest ESR and the capacitor with smallest capacitance in the arm are monitored. The proposed strategy not only realizes both ESR and capacitance monitoring in the MMC, but also proposes a simplified monitoring algorithm for MMCs with large number of capacitors. The simulation and experimental results confirm the effectiveness of the proposed monitoring strategy for MMCs.

***Index Terms*- Capacitance, monitoring, equivalent series resistance, modular multilevel converter.**

I. Introduction

The modular multilevel converter (MMC) has become an attractive topology for medium/high-voltage and high-power applications due to its modularity and scalability [1, 2]. The MMC not only produces a multilevel voltage with the flexible operation but also reduces average switching frequency without depressing the power quality [3]. Owing to the easy construction, assembling and flexibility, the MMC becomes promising for motor drives [4], energy storage [5], electric railway supplies [6] and microgrid [7], etc.

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The capacitor is one of the weakest components in the MMC [8]. Due to the advantages of high energy density and low cost [9], the electrolytic capacitor is popular for MMCs in some applications, such as microgrid and motor drives [10-12]. Owing to chemical process, aging, etc., the capacitor would gradually deteriorate and the capacitor's parameters would be changed [13]. Normally, the capacitor is needed to be replaced with the new one when its capacitance drops below 80% of rated value or its equivalent series resistance (ESR) is over 2 times of rated value [14]. Therefore, the condition monitoring for capacitors in the MMC is essential.

To date, several studies have paid attention to the capacitor monitoring in the MMC. Reference [15] presents a monitoring scheme for the submodule (SM) capacitors in the MMC, where each SM capacitance is estimated by a recursive least square algorithm based on the information of capacitor voltage, arm current and SM switching state. However, an ac current is injected into the circulating current, which increases the capacitor voltage ripple and affects the MMC performance. Reference [16] presents a Kalman filter algorithm to estimate the SM capacitance in the MMC, where each SM capacitance is estimated based on the capacitor voltage and current. Reference [14] presents a simplified condition monitoring algorithm to estimate the capacitance based on the relationship between the arm average capacitance and the capacitance of each SM. Reference [17] proposes the reference SMs for capacitor condition monitoring in the MMC, where the SM capacitance can be estimated based on the relationship between the monitoring SM capacitor voltage and the reference SM capacitor voltage. The above capacitor monitoring methods still have some limitations as 1) the capacitor is seen as an ideal one, which only considers the capacitance without considering another important parameter, ESR; 2) all SM capacitors in the MMC are monitored, which occupies a large amount of computing resources, especially for the MMC with a large amount of SMs.

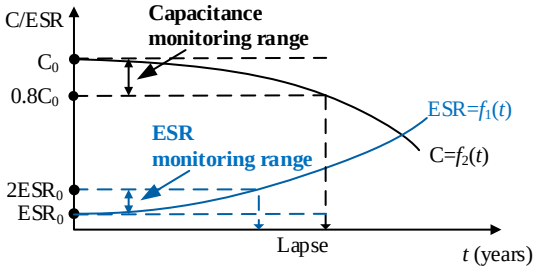

Fig. 1 Capacitor deterioration curve.

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The ESR is an important parameter in the capacitor. In comparison with the reduction of capacitance, the increase of ESR is normally more pronounced in the deteriorated capacitor [18-20], as shown in Fig. 1, because the ESR normally has already increased to over 2 times of its rated value when the capacitance declines to 80% of its rated value, which means that the existing methods cannot detect the lapsed capacitor in time. To make up this gap, the capacitor monitoring method considering not only the capacitance but also the ESR is needed urgently, which can improve the reliability of the MMC. To date, several ESR monitoring methods have been reported such as recursive least square algorithm [21], discrete Fourier transform algorithm [22], Newton-Raphson algorithm [23], short time least square Prony's algorithm [24] and the artificial neural network algorithm [25], etc. However, the above methods are suitable for the converters with few capacitors, which are not suitable for the MMC with large number of capacitors because of complicated computation.

In this paper, a sorting-based condition monitoring strategy is proposed for the MMC to estimate capacitor's ESR and capacitance. The ESRs and capacitances of SM capacitors in the arm are indirectly sorted based on the relationship among capacitor's ESR, capacitance, current and energy, and only the capacitor with biggest ESR and the capacitor with smallest capacitance in the arm are estimated. The advantages of the proposed strategy are 1) estimating not only the capacitance but also the ESR of capacitors, which has not been considered in [14-17]; 2) studying the characteristics of ESR, capacitance, voltage, current, and energy variety of capacitors in the MMC; 3) simplifying monitoring algorithm.

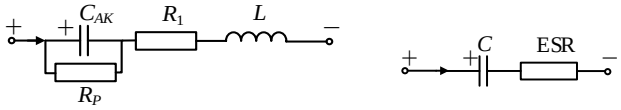
This paper is organized as follows. Section II introduces the characteristics of capacitors in the MMC. Section III introduces the operation principles of the MMC. Section IV analyzes the capacitor characteristics of the MMC. Section V proposes the sorting-based condition monitoring strategy for capacitors in the MMC. Sections VI and VII present the system simulation and experimental tests, respectively, to verify the effectiveness of the proposed monitoring strategy. Finally, the conclusions are presented in Section VIII.

II. CAPACITORS IN MMCS

The detailed equivalent circuit of the electrolytic capacitor is shown in Fig. 2(a) [24,26]. The C_{AK} is the ideal anode-cathode capacitance, which equals to $\varepsilon S/d$ and is independent of capacitor current frequency f. ε is the dielectric constant. S is the plate surface area. d is the thickness of the dielectric between the plates. R_p is the parallel resistance due to leakage current. R_1 is the series resistance of connections, frames and separator, which decreases with the increase of frequency. L is the series equivalent inductance of connections and windings, which is independent of frequency. The L of the capacitor is normally on the order of nH [26] and the main frequencies of the capacitor current in the MMC are low, which results in that the inductive reactance of the capacitor in MMC can be negligible. As a result, the capacitor in the MMC can be simplified as the capacitance in series with the ESR, as shown in Fig. 2(b), which can be expressed as

$$\begin{cases} C = C_{AK} \cdot (1 + \dfrac{1}{4\pi^2 \cdot R_P^2 \cdot C_{AK}^2 \cdot f^2}) \\ \mathrm{ESR} = R_1 + \dfrac{R_P}{1+4\pi^2 \cdot R_P^2 \cdot C_{AK}^2 \cdot f^2} \end{cases} \tag{1}$$

In the MMC, the capacitance is normally on the order of mF [1, 3, 5], which makes the parallel resistance R_P is on the order of MΩ [26]. Accordingly, the C can be considered to be the same as C_{AK} and ESR can be considered to be the same as R_1, which means that C is independent of frequency and ESR decreases with the rise of frequency.



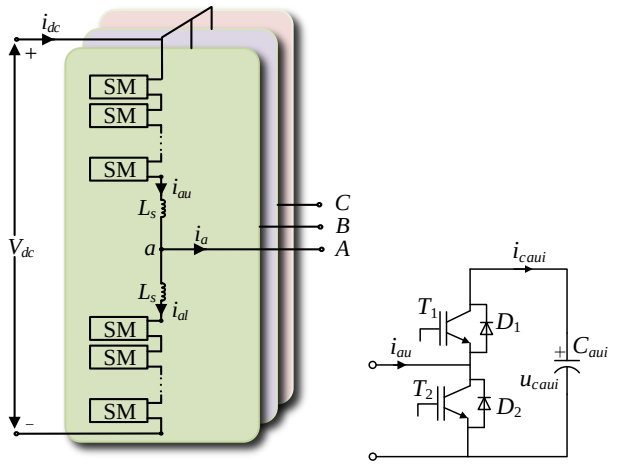
(a) (b)

Fig. 2 (a) Capacitor equivalent circuit. (b) Simplified capacitor equivalent circuit in the MMC.

III. OPERATION PRINCIPLES OF MMCS

A three-phase MMC is shown in Fig. 3(a), which consists of six arms and each arm contains n identical SMs and an arm inductor L_s. Fig. 3(b) shows the i-th SM (i=1, 2, …, n) in the upper arm of phase A, which consists of two switches T_1, T_2, two diodes D_1, D_2 and a dc capacitor C [27]. Normally, the i-th SM is controlled with a switching function S_{aui}, which determines the state of the SM, as shown in Table I. When S_{aui} equals 1, the SM is at "ON" state. Here, the charge or discharge of the capacitor C_{aui} relies on the direction of the arm current i_{au}. If i_{au}>0, the capacitor is charged and capacitor voltage u_{caui} increases; otherwise, the capacitor is discharged and the u_{caui} decreases. When S_{aui} equals 0, the SM is at "OFF" state. Here, the capacitor is bypassed and the capacitor voltage remains unchanged [28]. As a result, the capacitor current i_{caui} of the i-th SM is

$$i_{caui} = S_{aui} \cdot i_{au} \,. \tag{2}$$



(a) (b)

Fig. 3 (a) Structure of a three-phase MMCs. (b) Structure of a SM.

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TABLE I
TWO OPERATION STATES OF SMS

SM state	S_{aui}	i_{au}	C_{aui}	u_{caui}
On	1	≥0	Charge	Increased
		<0	discharge	Decreased
Off	0	≥0 or <0	Bypass	Unchanged

IV. MMC CAPACITOR CHARACTERISTICS BASED ON ESR AND C

The chemical process, aging, etc. would cause capacitor deterioration, which results in not only the drop of capacitance but also the increase of ESR [13]. The ESR is one of the important capacitor parameters, while the current researches on the capacitor monitoring of MMCs [14-17] only consider the capacitance and neglect the ESR in the capacitor, which cannot distinguish the lapsed capacitor in time.

A. Capacitor Current Characteristics

Fig. 4 shows the upper arm of phase A in the MMC, where both ESRs R_{au1}~R_{aun} and capacitances C_{au1}~C_{aun} are considered.

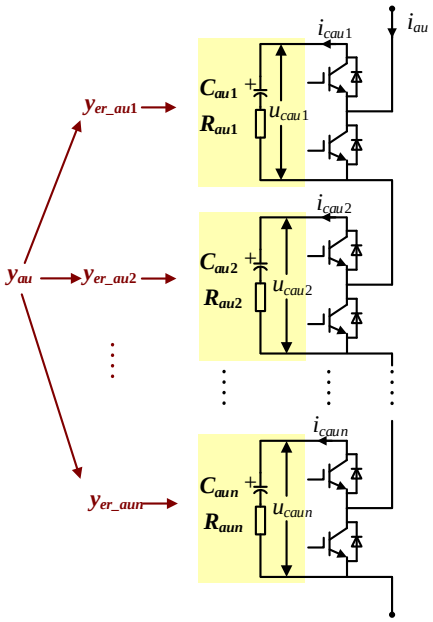

Fig. 4 Upper arm of phase A based on ESR and C.

Suppose the second-order harmonic circulating current is suppressed, the upper arm current i_{au} is

$$i_{au}=\frac{1}{2}I_m\sin\omega_1 t+\frac{i_{dc}}{3}. \tag{3}$$

where I_m is the amplitude of the ac current i_a. ω_1 is the fundamental angular frequency and $\omega_1=2\pi f_1$. f_1 is the fundamental frequency. i_{dc} is the dc-link current of the MMC.

The reference y_{au} for the upper arm of phase A is

$$y_{au}=m\sin(\omega_1 t+\phi). \tag{4}$$

where m is modulation index. ϕ is the phase angle.

Suppose that the capacitor voltages u_{cau1}~u_{caun} shown in Fig. 4 are kept the same with the voltage-balancing control [2], the equivalent reference y_{er_aui} for the i-th SMs in the arm is mainly related to C_{au1}~C_{aun} as shown in (5) [16], because the capacitor's ESR is much smaller than its capacitive reactance at lower frequency [26] and the voltage of the ESR is much smaller than that of the capacitive reactance.

$$y_{er\_aui}=\left(\frac{C_{aui}}{\frac{1}{n}\sum_{i=1}^{n}C_{aui}}-1\right)+\frac{C_{aui}}{\frac{1}{n}\sum_{i=1}^{n}C_{aui}}y_{au} \tag{5}$$

According to (3) ~ (5), the capacitor current i_{caui} of the i-th SM can be obtained as

$$i_{caui}=i_{au}\frac{1+y_{er\_aui}}{2}=\underbrace{\frac{i_{dc}}{6}\left(\frac{nC_{aui}}{\sum_{i=1}^{n}C_{aui}}\right)+\frac{nmC_{aui}I_m}{8\sum_{i=1}^{n}C_{aui}}\cos\phi}_{\text{DC Component}}+I_{1m\_i}\sin(\omega_1 t+\beta_{1\_i})+I_{2m\_i}\sin(2\omega_1 t+\beta_{2\_i}) \tag{6}$$

Fundamental component i_{caui_1f} **2nd-order harmonic component i_{caui_2f}**

with

$$\begin{cases} I_{1m\_i}=\dfrac{nC_{aui}}{2\sum_{i=1}^{n}C_{aui}}\sqrt{\left(\frac{I_m}{2}\right)^2+\left(\frac{mi_{dc}}{3}\right)^2+\frac{mi_{dc}I_m}{3}\cos\phi} \\ \beta_{1\_i}=\arctan\left(\dfrac{2mi_{dc}\sin\phi}{3I_m+2mI_{dc}\cos\phi}\right) \\ I_{2m\_i}=-\dfrac{1}{8}\dfrac{nmI_mC_{aui}}{\sum_{i=1}^{n}C_{aui}} \\ \beta_{2\_i}=\dfrac{\pi}{2}+\phi \end{cases} \tag{7}$$

where I_{1m_i} and β_{1_i} are the amplitude and angle of the fundamental component i_{caui_1f} of the capacitor current in the i-th SM. I_{2m_i} and β_{2_i} are the amplitude and angle of the 2nd-order harmonic component i_{caui_2f} of the capacitor current in the i-th SM. In the steady state, the dc component in the capacitor current is zero and $i_{caui}=i_{caui\_1f}+i_{caui\_2f}$.

Fig. 5 shows the amplitudes I_{1m_1}, I_{2m_1}, I_{3m_1}, I_{4m_1} and I_{5m_1} of the fundamental component, 2nd-, 3rd-, 4th- and 5th-order harmonic component, respectively, in the capacitor current under various power, which is derived from the simulation in Section VI. It can be observed that the I_{1m_1} and I_{2m_1} drop along with the decrease of active power and the I_{3m_1}, I_{4m_1} and I_{5m_1} are quite small and can be neglectable.

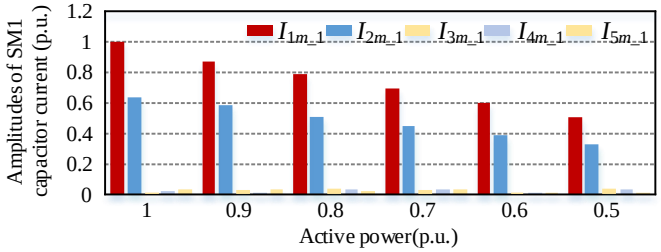

Fig. 5 Amplitudes of fundamental component, 2nd-, 3rd-, 4th- and 5th-order harmonic component in capacitor current under various power.

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B. Capacitor Impedance Characteristics

Since the capacitor current mainly contains the i_{caui_1f} and i_{caui_2f}, the capacitor's ESR mainly considers the fundamental component R_{aui_1f} and the 2nd-order component R_{aui_2f}. Fig. 6 shows the capacitor impedance characteristics in the MMC considering both ESR and C, which can be described as

$$\begin{cases} R_{aui\_1f} = \tan\delta/\omega_1 C_{aui} \\ R_{aui\_2f} = \tan\delta/\omega_2 C_{aui} = R_{aui\_1f}/2 \end{cases} \tag{8}$$

$$\begin{cases} Z_{aui\_1f} = R_{aui\_1f} + 1/j\omega_1 C_{aui} \\ Z_{aui\_2f} = R_{aui\_2f} + 1/j\omega_2 C_{aui} = Z_{aui\_1f}/2 \end{cases}. \tag{9}$$

where Z_{aui_1f} and Z_{aui_2f} are the capacitor impedance corresponding to i_{caui_1f} and i_{caui_2f}. δ is the capacitor loss angle. tanδ is capacitor dissipation factor, which is nearly a constant at low frequency [18, 26] such as fundamental frequency and double-line frequency. $\omega_2=2\omega_1$.

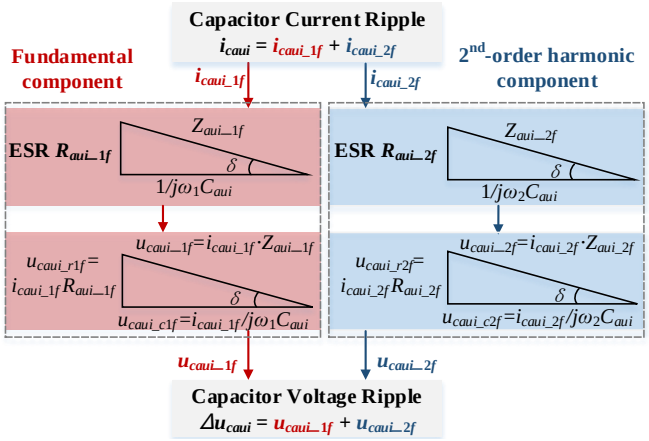

Fig. 6 Capacitor characteristics in the MMC.

C. Capacitor Voltage Characteristics

In Fig. 6, the capacitor voltage ripple u_{caui_1f} and u_{caui_2f} caused by i_{caui_1f} and i_{caui_2f} are

$$\begin{cases} u_{caui\_1f} = i_{caui\_1f} \cdot Z_{aui\_1f} = u_{caui\_c1f} + u_{caui\_r1f} \\ u_{caui\_2f} = i_{caui\_2f} \cdot Z_{aui\_2f} = u_{caui\_c2f} + u_{caui\_r2f} \end{cases} \tag{10}$$

with

$$\begin{cases} u_{caui\_r1f} = i_{caui\_1f} \cdot R_{aui\_1f} \\ u_{caui\_c1f} = i_{caui\_1f} / j\omega_1 C_{aui} \end{cases} \tag{11}$$

$$\begin{cases} u_{caui\_r2f} = i_{caui\_2f} \cdot R_{aui\_2f} \\ u_{caui\_c2f} = i_{caui\_2f} / j\omega_2 C_{aui} \end{cases} \tag{12}$$

where u_{caui_c1f} and u_{caui_r1f} are voltage ripples caused by C_{aui}, i_{caui_1f} and R_{aui_1f}, i_{caui_1f}, respectively. u_{caui_c2f} and u_{caui_r2f} are voltage ripples caused by C_{aui}, i_{caui_2f} and R_{aui_2f}, i_{caui_2f}, respectively.

According to (6) ~ (12), the capacitor voltage ripple Δu_{caui} in the i-th SM can be obtained as

$$\Delta u_{caui} = \underbrace{U_{1m\_i}\sin(\omega_1 t + \alpha_{1\_i})}_{\text{Fundamental component } u_{caui\_1f}} + \underbrace{U_{2m\_i}\sin(2\omega_1 t + \alpha_{2\_i})}_{\text{2nd-order harmonic component } u_{caui\_2f}} \tag{13}$$

with

$$\begin{cases} U_{1m\_i} = I_{1m\_i}\sqrt{R_{aui\_1f}^2 + \left(\dfrac{1}{\omega_1 C_{aui}}\right)^2} \\ \alpha_{1\_i} = \beta_{1\_i} - \arctan\left(\dfrac{1}{\omega_1 C_{aui} R_{aui\_1f}}\right) \\ U_{2m\_i} = \dfrac{1}{2} I_{2m\_i}\sqrt{R_{aui\_1f}^2 + \left(\dfrac{1}{\omega_1 C_{aui}}\right)^2} \\ \alpha_{2\_i} = \beta_{2\_i} - \arctan\left(\dfrac{1}{\omega_1 C_{aui} R_{aui\_1f}}\right) \end{cases} \tag{14}$$

where U_{1m_i}, α_{1_i} are amplitude and angle of the fundamental component u_{caui_1f} in capacitor voltage. U_{2m_i} and α_{2_i} are amplitude and angle of the 2nd-order harmonic component u_{caui_2f} in capacitor voltage.

The capacitor voltage ripple in the i-th SM is composed of u_{caui_1f} and u_{caui_2f}. Owing to that the arm capacitor voltages are kept the same by voltage-balancing control, the U_{1m_1}~U_{1m_n} in arm SM capacitors would be the same as U_{1m}; the U_{2m_1}~U_{2m_n} in arm SM capacitors would be the same as U_{2m}.

Fig. 7 shows the amplitudes of the fundamental component, 2nd-, 3rd-, 4th- and 5th-order harmonic component in the capacitor voltage under various power of the MMC, which is derived from the simulation in Section VI. It can be observed that U_{1m} and U_{2m} decline along with the decrease of power; U_{3m}, U_{4m} and U_{5m} are quite small and can be neglectable.

Fig. 8(a) shows the amplitudes U_{1m_c} and U_{2m_c} of u_{cau1_c1f} and u_{cau1_c2f}, respectively, under various power of the MMC. Fig. 8(b) shows the amplitudes U_{1m_r} and U_{2m_r} of u_{cau1_r1f} and u_{cau1_r2f}, respectively, under various power of the MMC. U_{1m_c}, U_{2m_c}, U_{1m_r} and U_{2m_r} decline along with the decrease of the power of the MMC. Compared with U_{1m_c} and U_{2m_c}, U_{1m_r} and U_{2m_r} are quite small and can be neglectable. In addition, the U_{1m_c} and U_{1m_r} are much bigger than U_{2m_c} and U_{2m_r}, respectively.

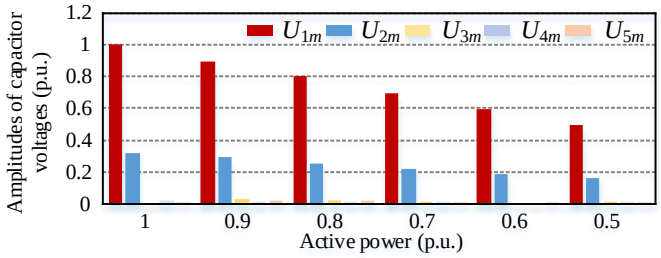

Fig. 7 Amplitudes of fundamental component, 2nd-, 3rd-, 4th- and 5th-order harmonic component in capacitor voltage under various active power.

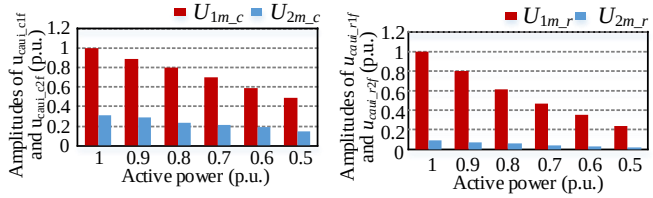

Fig. 8 (a) U_{1m_c} and U_{2m_c}. (b) U_{1m_r} and U_{2m_r}.

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V. Proposed Capacitor ESR and C Monitoring Strategy for MMCs

The ESR is one of the important capacitor parameters. A sorting-based monitoring strategy is proposed in this Section to estimate capacitor's ESR and Capacitance in the MMC.

A. Capacitor Energy Characteristics

According to (6) ~ (9), (13) and [16], the capacitor energy variety W_{aui} of the i-th SM within a fundamental period T_1 (T_1=2π/ω_1) can be obtained as

$$W_{aui}=\int_0^{T_1}(\frac{V_{dc}}{n}+\Delta u_{caui})i_{caui}dt=W_{aui\_r1f}+W_{aui\_r2f}. \quad (15)$$

with

$$\begin{cases} W_{aui\_r1f}=\int_0^{T_1}u_{caui\_1f}i_{caui\_1f}dt=\dfrac{2\pi U_{1m}^2/\omega_1}{R_{aui\_1f}+1/(\omega_1 C_{aui})^2/R_{aui\_1f}} \\ W_{aui\_r2f}=\int_0^{T_1}u_{caui\_2f}i_{caui\_2f}dt=\dfrac{4\pi U_{2m}^2/\omega_2}{R_{aui\_2f}+1/(\omega_2 C_{aui})^2/R_{aui\_2f}} \end{cases} \quad (16)$$

where W_{aui} represents the energy consumption of ESR in the capacitor. W_{aui_r1f} and W_{aui_r2f} are the energy consumption caused by R_{aui_1f} and R_{aui_2f}, respectively.

Fig. 9 shows the capacitor energy variety W_{au1_r1f} and W_{au1_r2f}, respectively, under various power of the MMC, where W_{au1_r1f} and W_{au1_r2f} decline with the decrease of power. In addition, W_{au1_r1f} is much bigger than W_{au1_r2f}, which means that R_{aui_1f} results in the main energy consumption in the capacitor and is the main cause of accelerating the aging process in comparison with R_{aui_2f}.

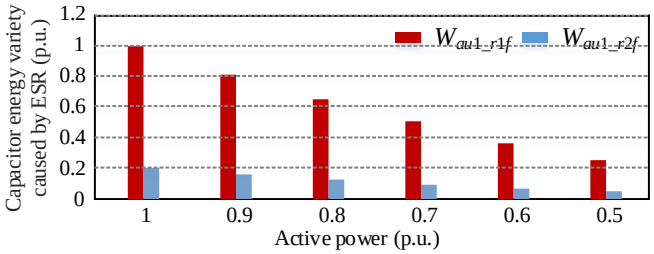

Fig. 9 W_{aui_r1f} and W_{aui_r2f} under various active power.

Substituting (8), (16) into (15), the W_{aui} can be rewritten as

$$W_{aui}=\frac{2\pi}{\omega_1}\left(U_{1m}^2+2U_{2m}^2\right)\frac{1}{R_{aui\_1f}+1/(\omega_1 C_{aui})^2/R_{aui\_1f}}. \quad (17)$$

From (17), it can be observed that the W_{aui} in the SM of the arm is determined by corresponding R_{aui_1f} and C_{aui}, as shown in Fig. 10, as follows.

1) W_{aui} & C_{aui}: W_{aui} increases along with the increase of C_{aui} and vice versa, as shown in Table II.
2) W_{aui} & R_{aui_1f}: the SM capacitance C_{aui} in the MMC is normally on the order of mF [10-12], which results in that R_{aui_1f} <1/(ω_1C$_{aui}$) [18]. Hence, W_{aui} increases along with the increase of R_{aui_1f} and vice versa, as shown in Table III.

TABLE II
Relationship Between W_{aui} and C_{aui}

C_{aui}	W_{aui}
↑	↑
↓	↓

TABLE III
Relationship Between W_{aui} and R_{aui_1f}

R_{aui_1f}	W_{aui}
↑	↑
↓	↓

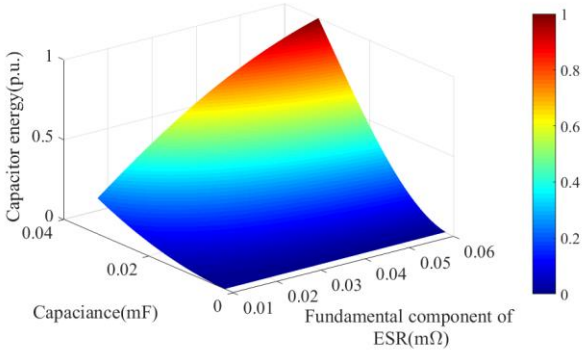

Fig. 10 Relationship between SM W_{aui} and R_{aui_1f}, C_{aui} in the arm of the MMC.

B. ESRs Relationship Among Arm SMs

According to (14) and (17), the variation K_{aui} is defined as

$$K_{aui}=\frac{W_{aui}}{I_{1m\_i}^2}=\frac{2\pi R_{aui\_1f}}{\omega_1}(1+\frac{2U_{2m}^2}{U_{1m}^2}). \quad (18)$$

The K_{aui} of the i-th SM is proportional to R_{aui_1f}, where K_{aui} increases along with the increase of R_{aui_1f} and K_{aui} reduces along with the decrease of R_{aui_1f}, as shown in Table IV.

TABLE IV
ESR Relationship of SMs

K_{aui}	R_{aui_1f}
↑	↑
↓	↓

C. Capacitances Relationship Among Arm SMs

Since R_{aui_1f} is much smaller than 1/$\omega_1 C_{aui}$ [24], (14) can be rewritten as

$$U_{1m}=I_{1m\_i}\Big/\omega_1 C_{aui}. \quad (19)$$

The I_{1m_i} of the i-th SM is proportional to the C_{aui}, where I_{1m_i} increases along with the increase of C_{aui} and I_{1m_i} declines along with the decrease of C_{aui}, as shown in Table V.

TABLE V
Capacitance Relationship of SMs

I_{1m_i}	C_{aui}
↑	↑
↓	↓

D. Proposed Sorting-Based Monitoring Strategy

Based on above analysis, a sorting-based monitoring strategy for capacitor's ESR and capacitance in the MMC is proposed, as shown in Fig. 11(a). Owing to ESR corresponding to fundamental frequency is nearly double ESR corresponding to double-line frequency and is the main energy consumption, only the ESR corresponding to fundamental frequency is estimated here so as to simplify the computation.

In the proposed strategy, the K_{aui} and I_{1m_i} are calculated with the characteristic variables calculation (CVC) block based on the capacitor voltage u_{caui}, switch function S_{aui} and arm current i_{au}, as shown in Fig. 11(b). In the CVC block, the capacitor current can be obtained based on (2). And then, the

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fundamental component of capacitor current i_{caui_1f} can be obtained by a band-pass filter (BPF) tuned at the fundamental frequency, which is used to calculate its amplitude I_{1m_i}. The K_{aui} is obtained based on (15) and (18).

According to the obtained K_{au1}~K_{aun}, the corresponding SM_1~SM_n are sorted in ascending order, so as to find the SM with biggest K_{au} among the n SMs in the arm, because the SM with biggest K_{au} has the biggest ESR. Afterwards, the ESR corresponding to the fundamental frequency in the SM with biggest K_{au} will be calculated based on the ESR estimation method in [22], which utilizes the average capacitor power divided by the square of capacitor current at the fundamental frequency to obtain the ESR. To date, the accuracy of the ESR estimation methods is about 4%~10% [9, 21-24].

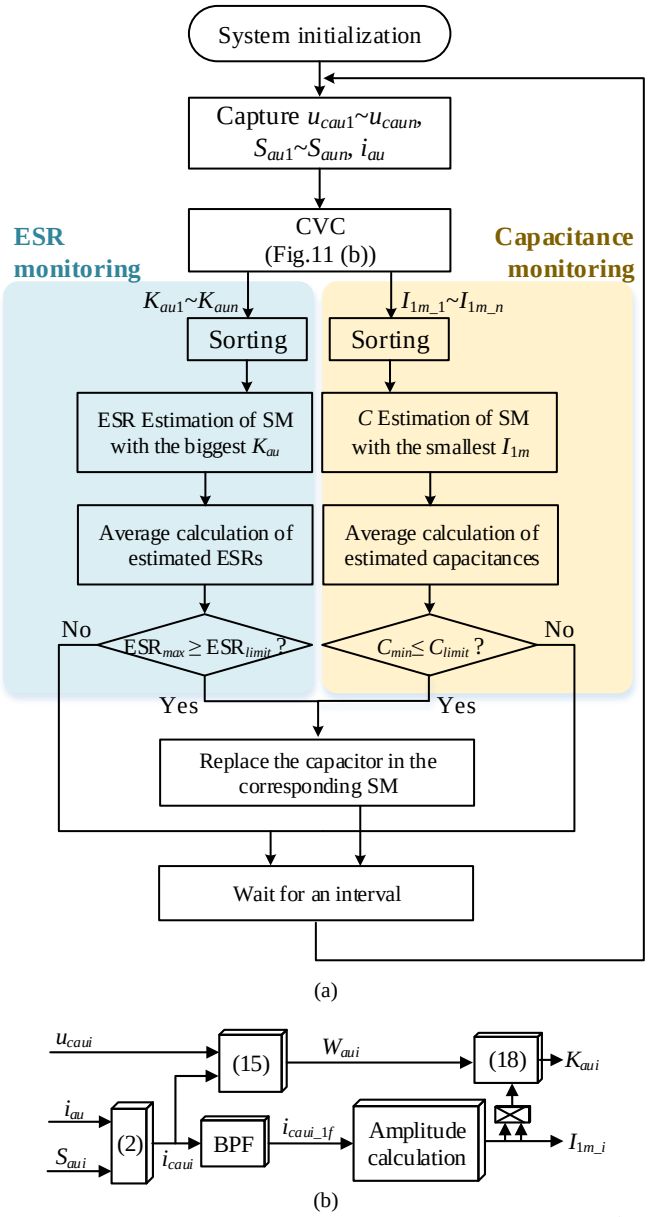

Fig. 11 Proposed capacitor monitoring strategy. (a) Flowchart of the monitoring algorithm. (b) Characteristic variables calculation for K_{au1}~K_{aun} and I_{1m_1}~I_{1m_n}.

On the other hand, based on the obtained I_{1m_1}~I_{1m_n}, the corresponding SM_1~SM_n are sorted in descending order to find the SM with smallest I_{1m} among the n SMs within the arm, because the SM with smallest I_{1m} has the smallest capacitance. Afterwards, the capacitance of the SM with the smallest I_{1m} will be calculated based on the capacitance estimation method in [15], which derives the capacitance based on the relationship between the capacitor voltage variation and capacitor current integration. Normally, the accuracy of the capacitance estimation method is below 1% [15].

In order to reduce the effect of measurement noises in the real MMC system and improve the capacitor monitoring accuracy, several sets of ESRs and capacitances are estimated such as ten sets. Removing the maximum and the minimum among the estimated ESRs and the estimated capacitances, respectively, the average values of the rest ESRs and the rest capacitances are calculated as the ESR and capacitance monitoring results, respectively.

Once the ESR monitoring result, which is the biggest ESR in the SMs of the arm, is over the threshold value ESR_{limit} or the capacitance monitoring result, which is the smallest capacitance in the SMs of the arm, is below the threshold value C_{limit}, the corresponding capacitor would be considered to be replaced with the new one. For electrolytic capacitors, the threshold value ESR_{limit} is normally 2 times of the ESR rated value and C_{limit} is normally 80% of the capacitance rated value [13, 19]. The proposed capacitor monitoring strategy is implemented periodically with some interval, which can effectively monitor capacitor's ESR and capacitance in MMC.

E. Analysis of Proposed Monitoring Strategy

Based on above analysis, the proposed capacitor monitoring strategy indirectly sorts the SMs' ESRs and capacitances in the arm, respectively, and only estimates the biggest ESR and the smallest capacitance in the arm. For the MMC with n SMs per arm, the proposed capacitor monitoring method may require about $(143n+155)/150$ μs to implement the estimation algorithm once based on the digital signal processing (DSP) TMS320F28335, which mainly contains the operation about $(2n+4)$ plus, $8(n+1)$ multiple, $(n+2)$ divide, $(n+1)$ integral and $2(n-1)$ comparison. If the capacitor's ESR and capacitance are estimated with the conventional capacitor monitoring method [22], [15], all SMs' ESRs and capacitances in the arm are required to be estimated, which may require $270n/150$ μs including operation about $7n$ plus, $17n$ multiple, $2n$ divide and n integral to implement the estimation algorithm once. Fig. 12 shows that the operation time of the proposed and conventional estimation algorithm increases along with the increase of SM number in the arm. The operation time of the proposed estimation algorithm is almost half of that of the conventional algorithm.

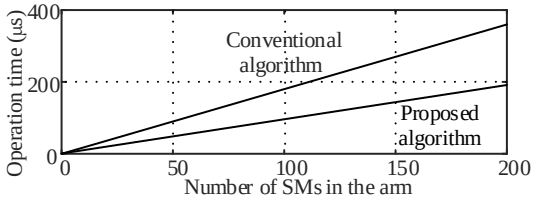

Fig. 12 Operation time of proposed and conventional estimation algorithm.

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VI. Simulation Studies

To verify the proposed ESR and capacitance monitoring strategy for the MMC, a three-phase MMC is built with the professional tool PSCAD/EMTDC, as shown in Fig. 13. The system parameters are shown in the Table VI.

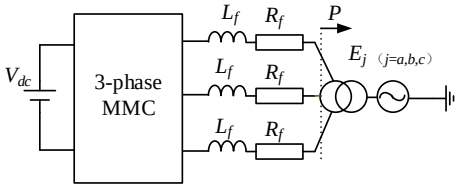


Fig. 13 Schematic diagram of the simulation system.

TABLE VI
Simulation System Parameters

Parameters	Value
Active power (MW)	6
Reactive power (MVar)	0
DC-link voltage V_{dc} (kV)	6
Grid line-to-line voltage (kV)	33
Grid frequency (Hz)	50
Transformer rating voltage	3 kV/33 kV
Transformer leakage reactance	10%
Number of SMs per arm n	6
Nominal SM capacitance C (mF)	13.2
Nominal SM ESR (mΩ)	25.2
Inductance L_s (mH)	1.5
Inductance L_f (mH)	1

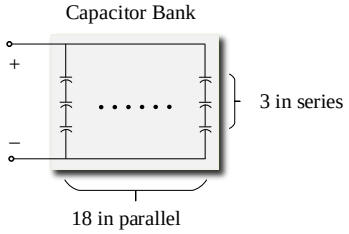


Fig. 14 Capacitor bank in the simulation system.

TABLE VII
Capacitor Parameters in The Upper Arm of Phase A

SM	1	2	3	4	5	6
C_{aui} (p.u.)	1	0.96	0.92	0.88	0.84	0.8
R_{aui_1f} (p.u.)	1	1.2	1.4	1.6	1.8	2

The aluminum electrolytic capacitor (JiangHaiCD293), whose rated capacitance and rated voltage is 2.2 mF and 400 V, respectively, is considered to construct the capacitor bank in each SM. Referring to its datasheet, the nominal ESR of the capacitor under 120 Hz is typically 63 mΩ. Hence, the nominal ESR of the capacitor under 50 Hz can be calculated as 63×120÷50=151.2 mΩ according to (8). In each SM, the capacitance of the capacitor bank is 13.2 mF and the nominal voltage of the capacitor bank is 1 kV. Hence, the capacitor bank in each SM is constructed with 3 capacitors connected in series and 18 capacitors connected in parallel, as shown in Fig. 14. Hence, the R_{aui_1f} of the capacitor bank is 25.2 mΩ. The R_{aui_2f} of the capacitor bank is half R_{aui_1f} according to (8).

To verify the proposed strategy, various ESRs and capacitances are considered in the upper arm SMs of phase A, as shown in Table VII, where the capacitance drops along with the rise of ESR.

Fig. 15 shows the performance of the MMC. Fig. 15(a) and (b) show the output voltages u_{ab}, u_{bc}, u_{ca} and currents i_a, i_b, i_c of the MMC. Fig. 15(c) shows the upper arm current i_{au} and the lower arm current i_{al} in phase A. Fig. 15(d) shows the upper arm capacitor voltages u_{cau1}~u_{cau6} in phase A.

Fig. 16 shows the performance of the proposed capacitor monitoring strategy for the MMC. Fig. 16(a) shows that $K_{au1}<K_{au2}<K_{au3}<K_{au4}<K_{au5}<K_{au6}$, which is consistent with the relationship among R_{au1_1f} ~R_{au6_1f}, as shown in Table VII. Owing to K_{au6} is the biggest one among them, the ESR in the SM6 is decided to be monitored. At 1.04 s, R_{au6_1f} in the SM6 is estimated as 52.15 mΩ and the error is approximately 3.47%, as shown in Fig. 16(b). Fig. 16(c) shows that $I_{1m\_1}>I_{1m\_2}>I_{1m\_3}>I_{1m\_4}>I_{1m\_5}>I_{1m\_6}$, which is also consistent with the relationship among C_{au1}~C_{au6}, as shown in Table VII. Owing to I_{1m_6} is the smallest one among them, the C_{au6} in the SM6 is decided to be monitored. At 1.04 s, the C_{au6} is estimated as 10.49 mF and the error is approximately 0.66%, as shown in Fig. 16(d).

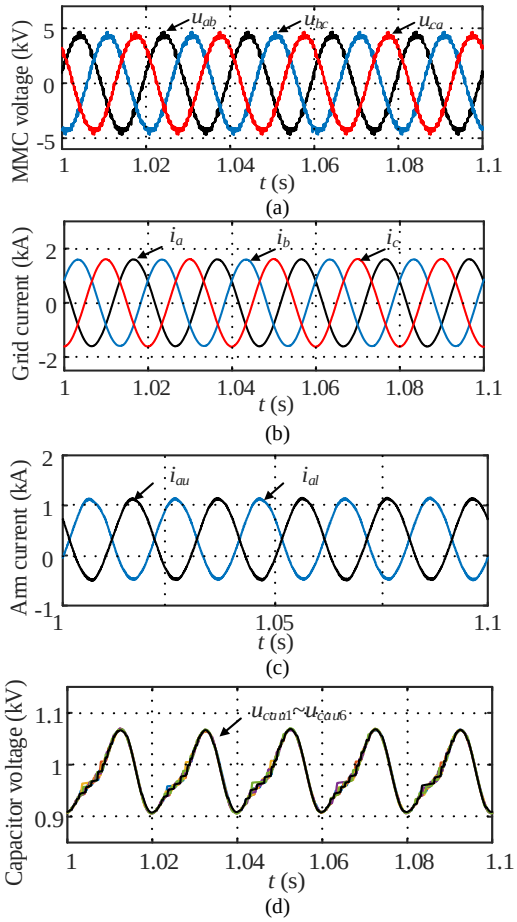
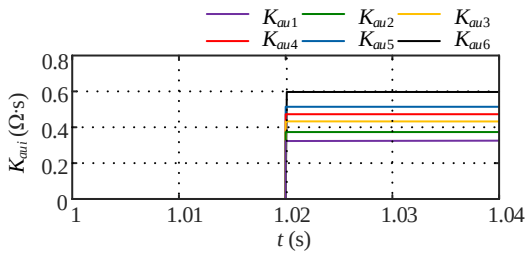


Fig. 15 (a) u_{ab}, u_{bc} and u_{ca}. (b) i_a, i_b and i_c. (c) i_{au} and i_{al}. (d) u_{cau1}~u_{cau6}.



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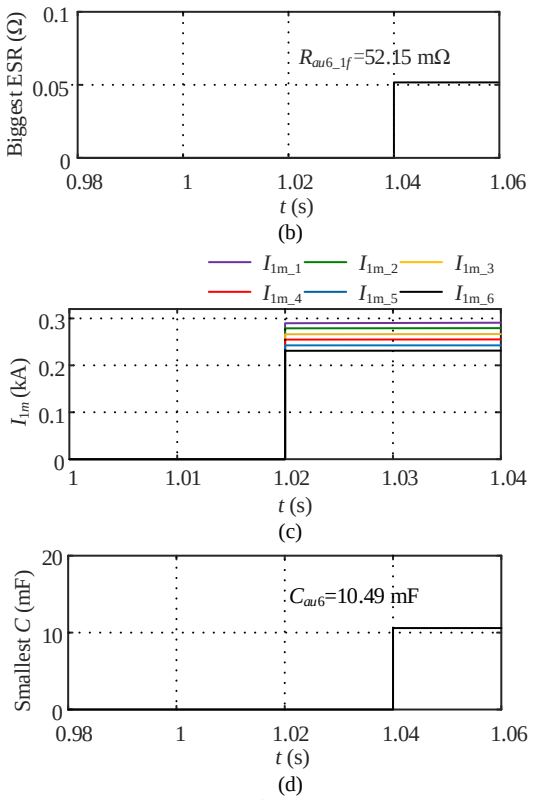


Fig. 16 (a) K_{au1}~K_{au6}. (b) Estimation of R_{au6_1f}. (c) I_{1m_1}~I_{1m_6}. (d) Estimation of C_{au6}.

VII. Experimental Studies

To confirm the proposed strategy, a three-phase MMC prototype with 4 SMs per arm is built in the laboratory, as shown in Fig. 17. A dc power supply (LAB/SMS6600) constitutes the dc bus voltage. The IXFK48N60P is used as the switch/diode and the JiangHai CD293 is used to construct the capacitor bank in each SM. The system control algorithm is implemented in the DSP controller and the pulse signals from the controller are transmitted to the driving panel of each SM by optical fibers. The specifications of the prototype are shown in Table VIII.

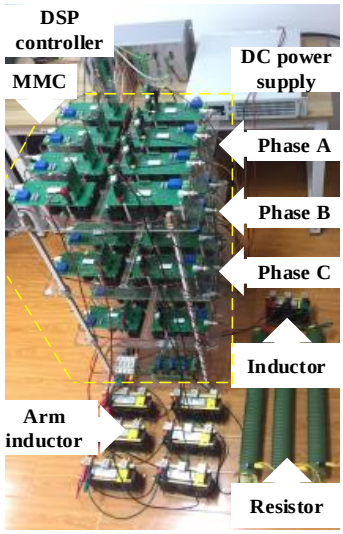


Fig. 17 Photo of the three-phase MMC prototype.

TABLE VIII
Experimental System Parameters

Parameters	Value
DC-link voltage V_{dc} (V)	200
Rated frequency (Hz)	50
Inductor L_s (mH)	3
Load inductor L (mH)	5
Load resistor R (Ω)	10
Carrier frequency (kHz)	4

A. Case I

In this case, the reference values of C_{au1}~C_{au4} and R_{au1_1f}~R_{au4_1f} in the capacitors of the upper arm of phase A are listed in Table IX, which are measured by the LCR meter HIOKI 3522-50. Fig. 18 shows the performance of the MMC. Fig. 18(a) shows the output voltage u_{ab}, u_{bc}, u_{ca} of the MMC. Fig. 18(b) shows the output current i_a, i_b, i_c of the MMC. Fig. 18(c) shows the upper arm current i_{au} and the lower arm current i_{al} of phase A.

TABLE IX
Capacitor Parameters in The Upper Arm of Phase A

SM	1	2	3	4
C_{aui} (mF)	2.25	2.27	2.23	2.23
R_{aui_1f} (Ω)	0.049	0.049	0.047	0.049

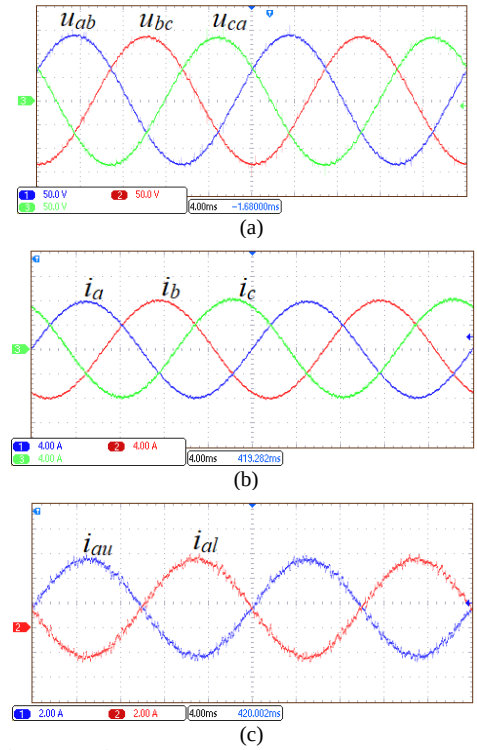
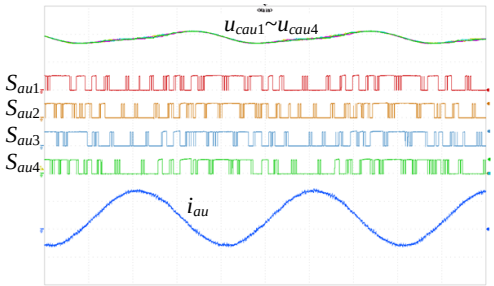


Fig. 18 Performance of the MMC. (a) u_{ab}, u_{bc}, u_{ca}. (b) i_a, i_b, i_c. (c) i_{au} and i_{al}.



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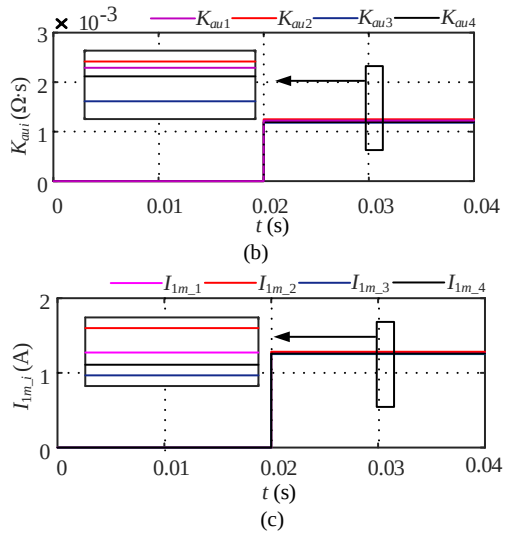

Fig. 19 (a) u_{cau1}, u_{cau2}, u_{cau3}, u_{cau4} (10V/div), S_{au1}, S_{au2}, S_{au3}, S_{au4} (30V/div), i_{au} and i_{al} (4A/div). Time base is 5 ms. (b) K_{au1}~K_{au4}. (c) I_{1m_1}~I_{1m_4}.

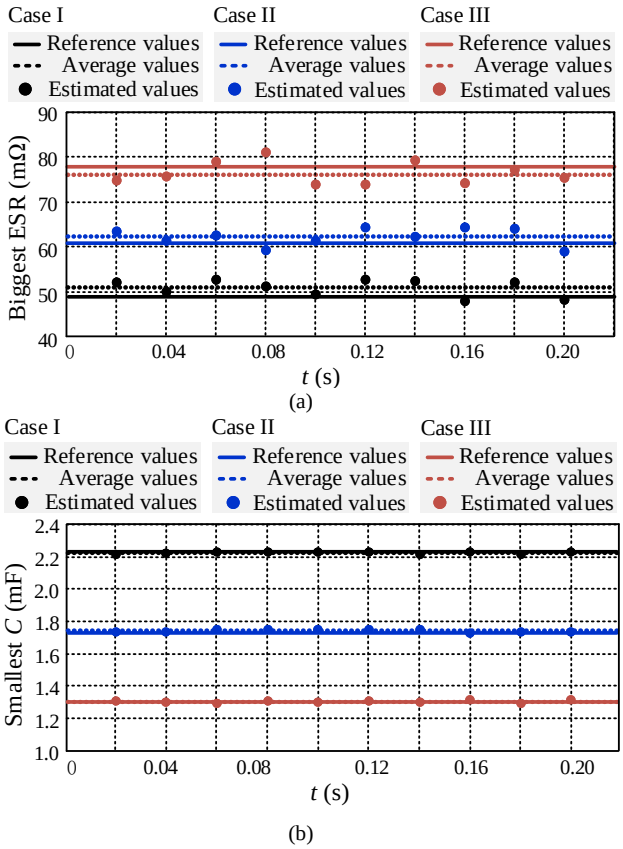

Fig. 20 (a) Distributions of ESRs estimation values in the three cases. (b) Distributions of capacitances estimation values in the three cases.

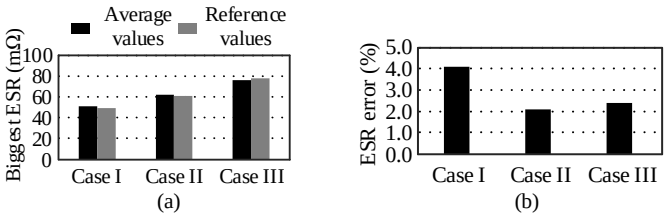

Fig. 21 (a) Estimated value and measured value of biggest ESR in Case I, II and III. (b) Estimation error of ESR.

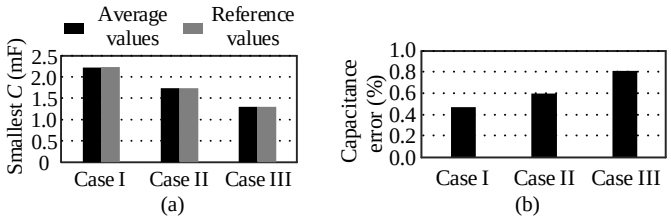

Fig. 22 (a) Estimated value and measured value of smallest capacitance in Case I, II and III. (b) Estimation error of capacitance.

Fig. 19(a) shows the upper arm capacitor voltages u_{cau1}~u_{cau4}, switching functions S_{au1}~S_{au4} and arm current i_{au} in phase A. Fig. 19(b) shows the calculated K_{au1}~K_{au4}, which are close to each other and consistent with the relationship among R_{au1_1f} ~R_{au4_1f} in Table IX. Fig. 19(c) shows the calculated I_{1m_1}~I_{1m_4}, which are also close to each other and consistent with the relationship among C_{au1}~C_{au4} in Table IX.

From Fig. 19(b), the K_{au2} corresponding to SM2 is the biggest one among K_{au1}~K_{au4}, and therefore the R_{au2_1f} of SM2 is selected to be estimated. Fig. 20(a) shows ten sets of estimated ESRs in SM2. Removing the maximum and the minimum, the average value of rest ESRs is 51.0 mΩ shown in Fig. 20(a). The error between the ESR average value and the ESR reference value is about 4.06%, as shown in Fig. 21.

From Fig. 19(c), the I_{1m_3} corresponding to SM3 is the smallest one among I_{1m_1}~I_{1m_4}, and therefore the C_{au3} of SM3 is selected to be estimated. Fig. 20(b) shows ten sets of estimated capacitances in SM3. Removing the maximum and the minimum, the average value of the rest capacitances is 2.22 mF, as shown in Fig. 20(b). The error between the capacitance average value and the capacitance reference value is about 0.45%, as shown in Fig. 22.

B. Case II

In this case, the reference values of C_{au1}~C_{au4} and R_{au1_1f}~R_{au4_1f} in the capacitors of the upper arm of phase A are listed in Table X, which are measured by the LCR meter HIOKI 3522-50. Fig. 23 shows the MMC voltage u_{ab}, u_{bc}, u_{ca}, ac current i_a, i_b, i_c, and arm current i_{au}, i_{al} of phase A.

TABLE X
CAPACITOR PARAMETERS IN THE UPPER ARM OF PHASE A

SM	1	2	3	4
C_{aui} (mF)	2.25	2.27	2.19	1.73
R_{aui_1f} (Ω)	0.049	0.047	0.052	0.061

Fig. 24(a) shows capacitor voltages u_{cau1}~u_{cau4}, switching functions S_{au1}~S_{au4} and arm current i_{au}. Fig. 24(b) shows that K_{au4} corresponding to SM4 is the biggest one among K_{au1}~K_{au4}, which is consistent with the relationship among R_{au1_1f} ~R_{au4_1f} in Table X. Fig. 24(c) shows that I_{1m_4} corresponding to SM4 is the smallest one among I_{1m_1}~I_{1m_4}, which is consistent with the relationship among C_{au1}~C_{au4} shown in Table X. As a result, the capacitor in SM4 is monitored. Ten sets of ESRs and capacitances in SM4 are estimated, as shown in Figs. 20(a) and (b). Removing the maximum and the minimum, the ESR average value is 62.3 mΩ and the capacitance average value is 1.74 mF, as shown in Fig. 20. The error between the ESR average value and the ESR reference value is about 2.06%, as shown in Fig. 21. The error between the capacitance average value and the capacitance reference value is about 0.57%, as shown in Fig. 22.

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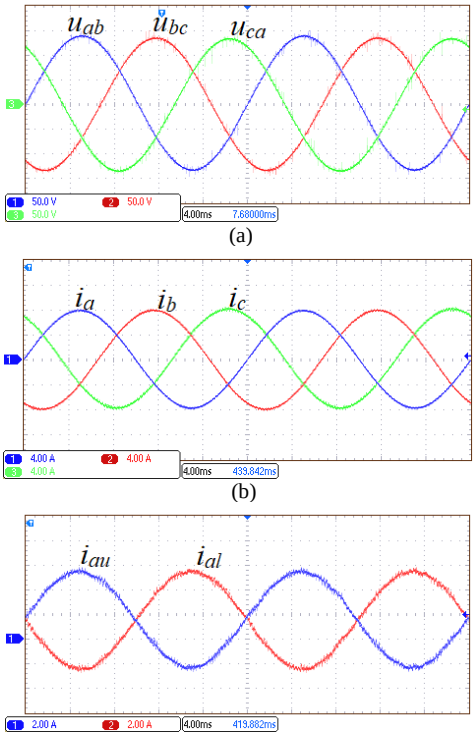


Fig. 23 Performance of the MMC. (a) u_{ab}, u_{bc}, u_{ca}. (b) i_a, i_b, i_c. (c) i_{au} and i_{al}.

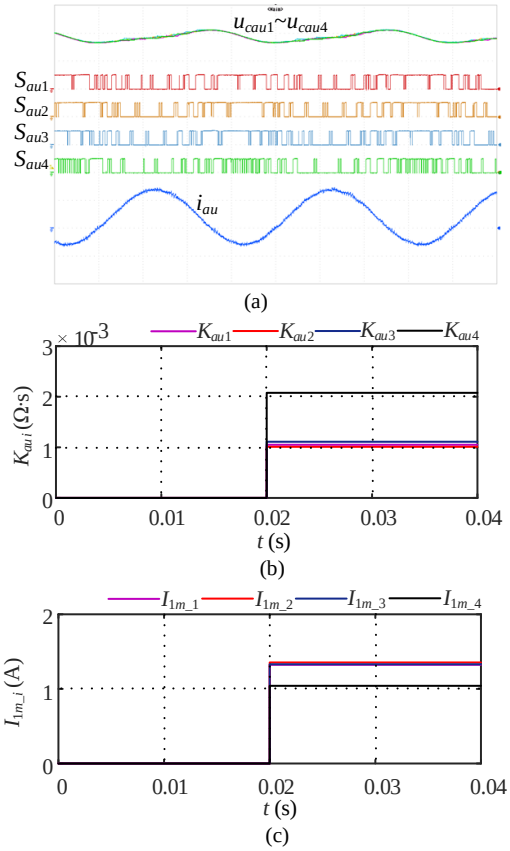


Fig. 24 (a) u_{cau1}, u_{cau2}, u_{cau3}, u_{cau4} (10V/div), S_{au1}, S_{au2}, S_{au3}, S_{au4} (30V/div), i_{au} and i_{al} (4A/div). Time base is 5 ms. (b) K_{au1}~K_{au4}. (c) I_{1m_1}~I_{1m_4}.

C. Case III

In this case, the reference values of the C_{au1}~C_{au4} and R_{au1_1f}~R_{au4_1f} in the capacitors of the upper arm of phase A are measured by the LCR meter HIOKI 3522-50 and listed in Table XI. Fig. 25 shows the MMC voltages u_{ab}, u_{bc}, u_{ca}, ac current i_a, i_b, i_c, and the arm current i_{au}, i_{al} of phase A.

TABLE XI
CAPACITOR PARAMETERS IN THE UPPER ARM OF PHASE A

SM	1	2	3	4
C_{aui} (mF)	2.25	2.27	1.73	1.3
R_{aui_1f} (Ω)	0.049	0.047	0.061	0.078

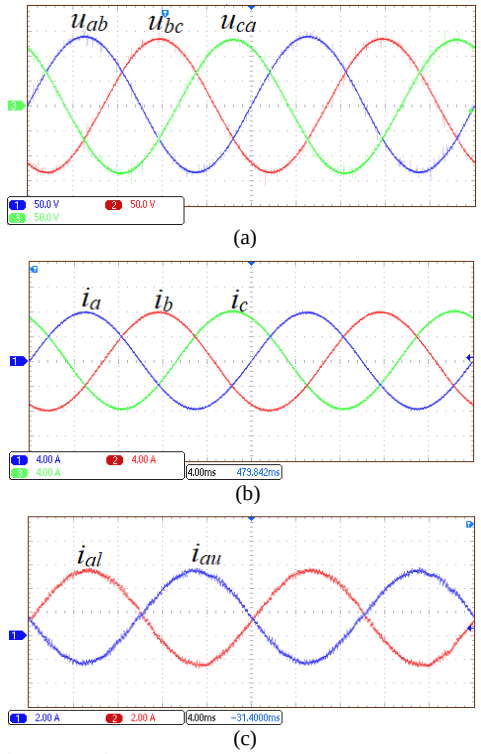
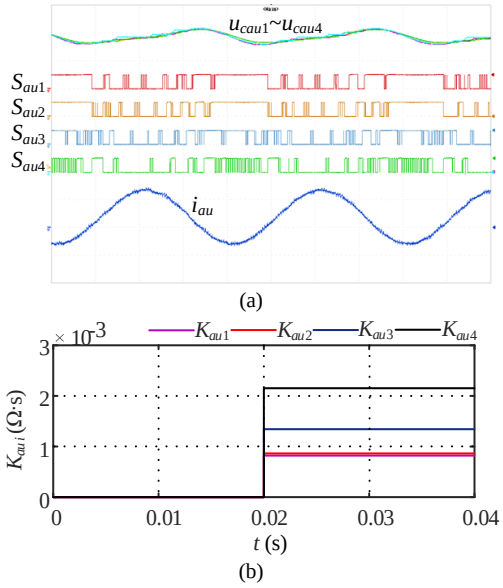


Fig. 25 Performance of the MMC. (a) u_{ab}, u_{bc}, u_{ca}. (b) i_a, i_b, i_c. (c) i_{au} and i_{al}.



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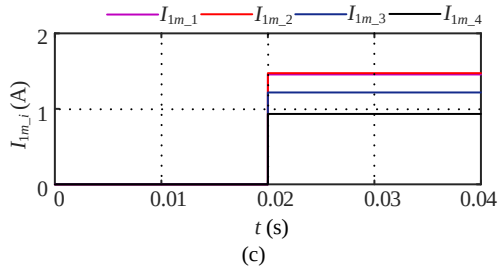

(c)

Fig. 26 (a) u_{cau1}, u_{cau2}, u_{cau3}, u_{cau4} (10V/div), S_{au1}, S_{au2}, S_{au3}, S_{au4} (30V/div), i_{au} and i_{al} (4A/div). Time base is 5 ms. (b) K_{au1}~K_{au4}. (c) I_{1m_1}~I_{1m_4}.

Fig. 26(a) shows the u_{cau1}~u_{cau4}, S_{au1}~S_{au4} and i_{au} in phase A. Fig. 26(b) shows that K_{au4} corresponding to SM4 is the biggest one, which is consistent with the relationship among R_{au1_1f} ~R_{au4_1f} in Table XIII. Fig. 26(c) shows that I_{1m_4} is the smallest one, which is consistent with the relationship among C_{au1}~C_{au4} shown in Table XI. As a result, the capacitor in SM4 is monitored. Figs. 20(a) and (b) shows ten sets of estimated ESRs and capacitances in SM4, respectively. Removing the maximum and the minimum, the ESR average value is 73.9 mΩ and the capacitance average value is 1.29 mF, as shown in Figs. 20(a) and (b). Consequently, the ESR error is about 2.40%, as shown in Fig. 21; the capacitance error is about 0.77%, as shown in Fig. 22.

The three cases show that the proposed capacitor monitoring method can effectively estimate both ESR and capacitance in the capacitors of the MMC to impose system reliability, which has not been considered in the other capacitor monitoring methods [14-17]. To estimate the ESR and capacitance for the MMC with 4 SMs per arm, the proposed monitoring method requires about 4.7 μs to implement the estimation algorithm once while the conventional monitoring method [15], [22] requires about 7.3 μs to implement the estimation algorithm once.

VIII. Conclusion

The existing studies about the MMC capacitor monitoring consider the capacitor as an ideal one, which only consider the capacitance without considering ESR. However, the increase of ESR is normally more pronounced in the deteriorated capacitor in comparison with the reduction of capacitance, which makes the ESR a better characteristic to detect the deteriorated capacitor. In this paper, both capacitor's ESR and capacitance in the MMC are monitored. The ESR of the capacitor in the MMC is mainly composed of the fundamental component and the second-order component. The energy variety of the capacitor in the MMC is analyzed, which increases along with the rise of the ESR and decreases along with the drop of the capacitance. Based on the relationship among the capacitor's ESR, capacitance, energy and current, a sorting-based capacitor monitoring strategy is proposed, where the capacitors' ESRs and capacitances in the arm are indirectly sorted, respectively, and only the capacitor with biggest ESR and the capacitor with smallest capacitance in the arm are monitored. The proposed sorting-based monitoring strategy does not have to monitor the ESRs and capacitances of all capacitors in the arm, which simplifies the monitoring algorithm. The simulation and experiment studies are conducted and the results show the effectiveness of the proposed capacitor ESR and C monitoring in the MMC.

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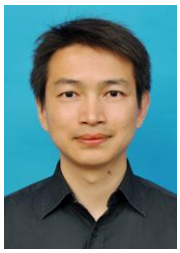

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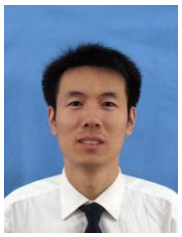

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