March 2021

CASCADE MULTIPLE MOSFET IN CURRENT-MODE LOGIC BUFFER TO REDUCE COMMON MODE NOISE OF SERDES

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ABSTRACT

Addressing the common-mode (CM) noise issue in a Serializer/Deserializer (SerDes) raises a variety of challenges. To address those types of challenges, techniques are presented herein that support cascading multiple metal–oxide–semiconductor field-effect transistors (MOSFETs) in a current-mode logic (CML) output buffer to reduce the CM noise in a SerDes with nearly no impact on, among other things, cost, thermal performance, chip real estate, and power consumption.

DETAILED DESCRIPTION

Addressing common-mode (CM) noise issue in a SerDes raises a variety of challenges. One possible approach to addressing those types of challenges (which for simplicity of exposition will be referred to hereafter generally as a "Parallel Solution" and more particularly as a Parallel Solution in source-series termination (SST)) detects MOSFET status and controls how many MOSFETs are parallelized together to tune the impedance for reducing rise time and fall time (i.e., rise/fall time) mismatch.

Aspects of the Parallel Solution, as described above, are presented in Figure 1, below.

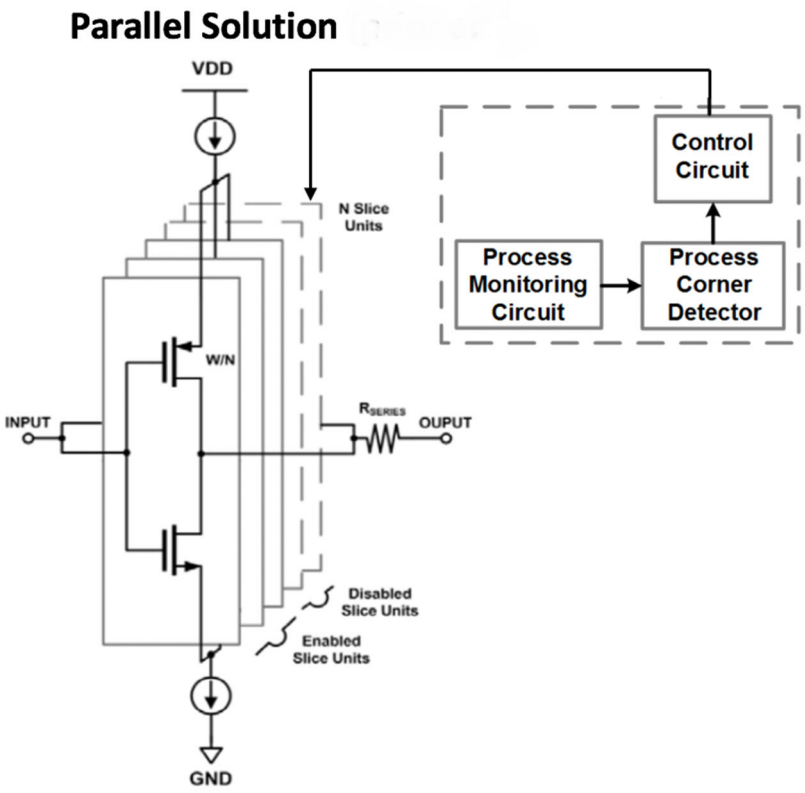

Figure 1: Aspects of Exemplary Parallel Solution

Under the Parallel Solution approach the rise/fall time ratio may be calculated using the equation that is presented in Figure 2, below.

$$\frac{rise\ time}{fall\ time} = R_{series} + \frac{R_p}{N} \Big/ R_{series} + \frac{R_N}{N}$$

Figure 2: Rise/Fall Time Ratio

Techniques are presented herein that support an alternate approach to the Parallel Solution. For simplicity of exposition this alternate approach, which will be described and illustrated in the narrative below, will be referred to hereafter generally as a "Cascade Solution" and more particularly as a Cascade Solution in CML.

Figure 3, below, presents aspects of a Cascade Solution in CML, according to aspects of the techniques presented herein, along with, for convenience, aspects of a Parallel Solution in SST.

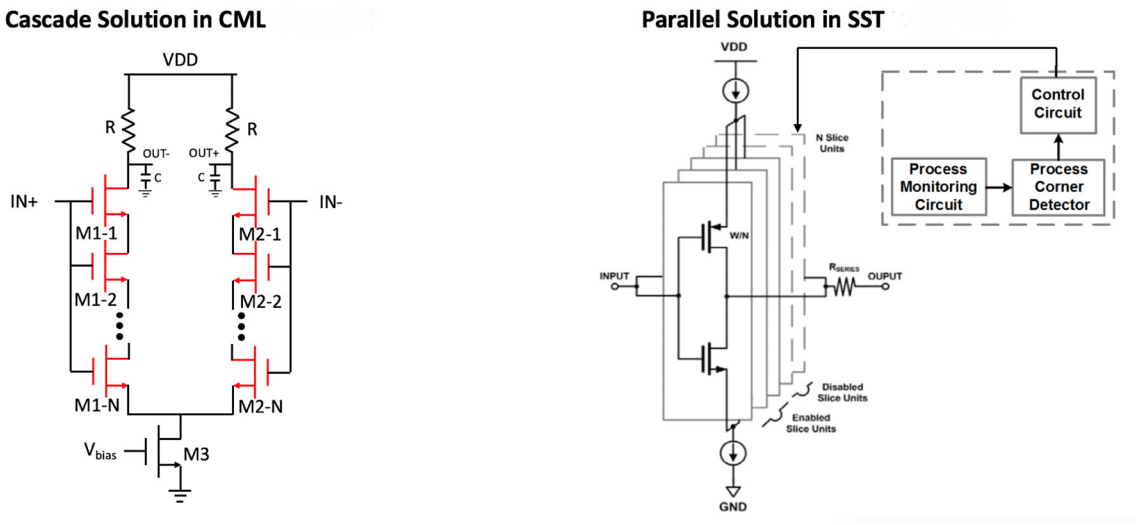

Figure 3: Aspects of the Cascade Solution as Compared to the Parallel Solution

Examining the particulars in more detail, aspects of the equivalent circuitry of both solutions (i.e., a Cascade Solution in CML, according to aspects of the techniques presented herein, and a Parallel Solution in SST) are presented in Figure 4, below.

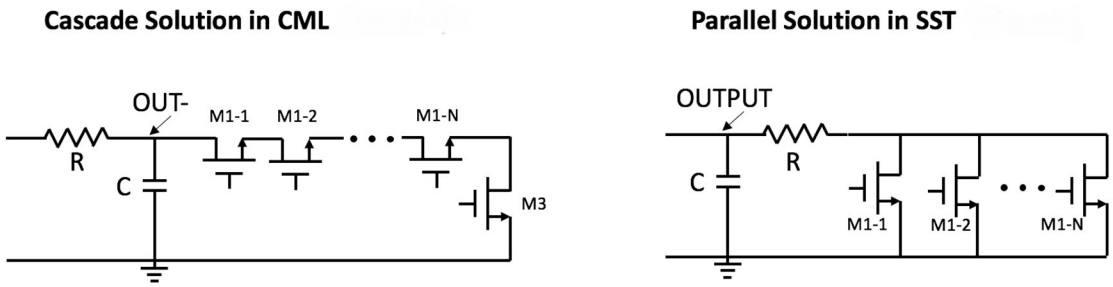

Figure 4: Aspects of Equivalent Circuitry

Based on the equivalent circuity as illustrated in Figure 4, above, and also taking into consideration that the rise/fall time is determined by the output impedance, then the ratio of a rise/fall time may be developed using the equations that are presented in Figure 5, below.

Cascade Solution in CML

$$\frac{rise\ time}{fall\ time} = \frac{R\times(N\times R_{M2}+R_{M3})}{R+(N\times R_{M2}+R_{M3})} \Big/ \frac{R\times(N\times R_{M1}+R_{M3})}{R+(N\times R_{M1}+R_{M3})}$$

Parallel Solution in SST

$$\frac{rise\ time}{fall\ time} = R_{series}+\frac{R_p}{N} \Big/ R_{series}+\frac{R_N}{N}$$

Figure 5: Rise/Fall Time Ratios

Intrinsically, according to the equivalent circuity that was previously presented, under a Cascade Solution, according to aspects of the techniques presented herein, a MOSFET is in parallel with resistor R to form the output impedance in a CML driver. Multiple MOSFETs may be cascaded together, in parallel with resistor R, to make the output impedance closer to R and thus minimize the rise/fall time mismatch. Accordingly, a Cascade Solution is designed for use within a SerDes CML driver.

Under a Parallel Solution a MOSFET is in series with resistor R to form the output impedance in a SST driver and multiple MOSFET may be paralleled together, in series with resistor R, to make the output impedance closer to R and thus minimize the rise/fall time mismatch. Accordingly, a Parallel Solution is designed for use within a SerDes SST driver.

Based on the above intrinsic differences between a CML circuit and an SST circuit, a Parallel Solution cannot be used in a CML driver to reduce CM noise. To further highlight this important point, both a Cascade Solution (according to aspects of the techniques presented herein) and a Parallel Solution may be considered in a CML driver, as depicted in Figure 6, below.

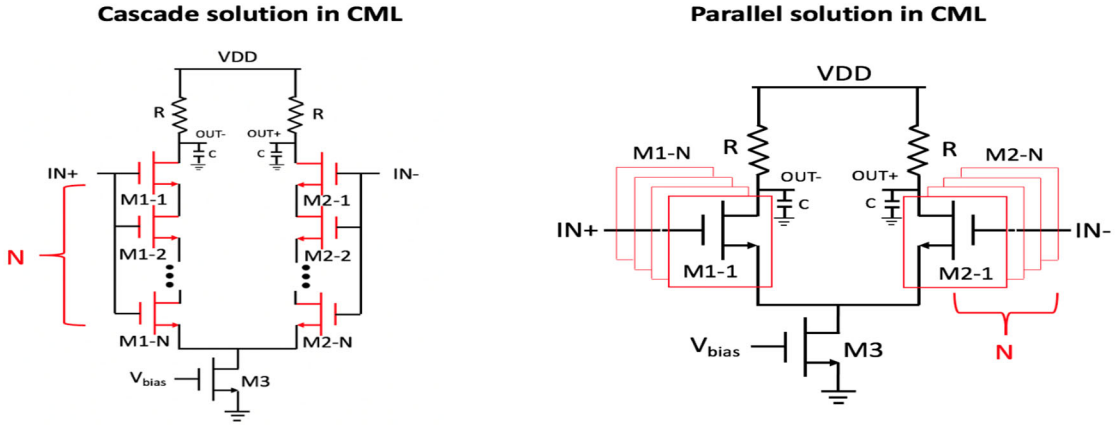

Figure 6: Illustrative Solution Comparison in CML

Within such an arrangement the ratio of the rise/fall time for the two solutions (i.e., a Cascade Solution in CML, according to aspects of the techniques presented herein, and a Parallel Solution in CML) may be calculated using the equations that are presented in Figure 7, below.

Cascade solution

$$\frac{rise\ time}{fall\ time} = \frac{R\times(N\times R_{M2}+R_{M3})}{R+(N\times R_{M2}+R_{M3})} \Big/ \frac{R\times(N\times R_{M1}+R_{M3})}{R+(N\times R_{M1}+R_{M3})}$$

Parallel solution

$$\frac{rise\ time}{fall\ time} = \frac{R\times(\frac{R_{M2}}{N}+R_{M3})}{R+(\frac{R_{M2}}{N}+R_{M3})} \Big/ \frac{R\times(\frac{R_{M1}}{N}+R_{M3})}{R+(\frac{R_{M1}}{N}+R_{M3})}$$

Figure 7: Rise/Fall Time Ratios

When N is set to 1, as has been demonstrated previously, the rise/fall time mismatch is 9.88%.

In the narrative that is presented below, the differences between the two solutions (i.e., a Cascade Solution in CML, according to aspects of the techniques presented herein, and a Parallel Solution in CML) will be considered when N is set to 2.

For a Cascade Solution in CML, according to aspects of the techniques presented herein, the ratio of the rise/fall time may be calculated using the equation that is presented in Figure 8, below.

$$\frac{rise\ time}{fall\ time} = \frac{49.398}{46.667} = 105.85\%$$

Figure 8: Rise/Fall Time Ratio

When N increases from 1 to 2, the mismatch is decreased from 9.88% to 5.85%. Theoretically the mismatch is linear with common mode energy, so a CM noise value of 4.55 decibels (dBs) may be obtained through the calculations that are presented in Figure 9, below.

$$20\times\log\left(\frac{5.85\%}{9.88\%}\right) = 4.55dB$$

Figure 9: Exemplary Noise Calculation

A simulation of the above confirms the different calculations. For example, as illustrated in Figure 10, below, the difference between the two highlighted noise measurements (of -44.127dB and -48.811dB) is 4.68dB, which is indeed similar to the above calculations.

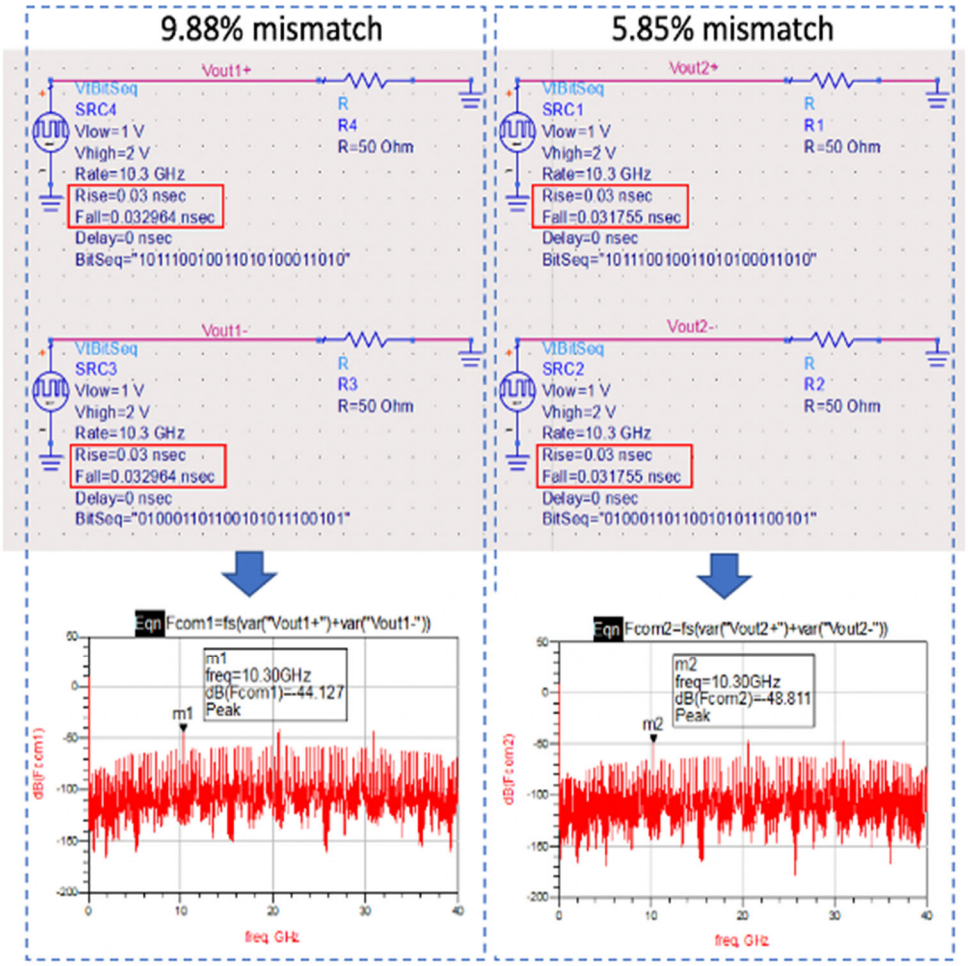

Figure 10: Illustrative Simulation Results

For a Parallel Solution in CML, the ratio of the rise/fall time may be calculated using the equation that is presented in Figure 11, below.

$$\frac{rise\ time}{fall\ time} = \frac{47.826}{41.667} = 114.78\%$$

Figure 11: Rise/Fall Time Ratio

When N increase from 1 to 2, the mismatch is increased from 9.88% to 14.78%, so the CM noise increases by 3.5dB.

For purposes of further comparison, the plot that is presented in Figure 12, below, illustrates the relationship of CM noise change between the two solutions (i.e., Cascade, according to aspects of the techniques presented herein, and Parallel) when they are applied in CML as N varies from 1 to 4.

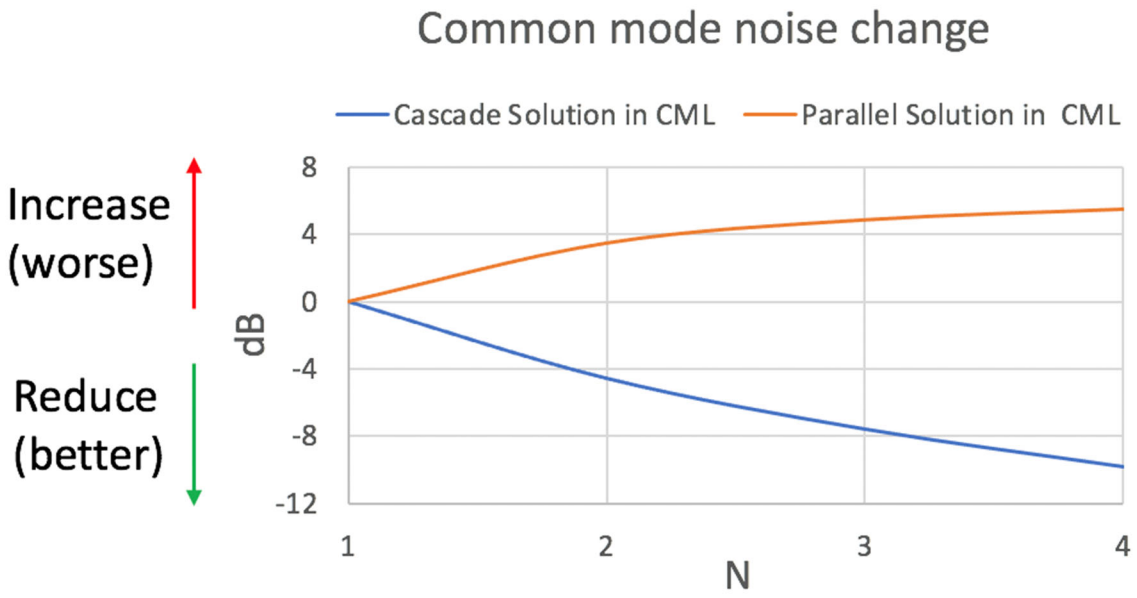

Figure 12: Common Mode Noise Change Comparison as N Varies from 1 to 4

In brief, since a Parallel Solution may be used in a SerDes SST driver (otherwise the CM noise may increase) and a Cascade Solution, according to aspects of the techniques presented herein, may be used in a SerDes CML driver, the two solutions cannot be exchanged between a CML driver and an SST driver. The two solutions have intrinsic differences and can be only used in their corresponding SerDes driver.

Beyond the main difference that was shown above, the table in Figure 13, below, presents some of the other advantages of a Cascade Solution (according to aspects of the techniques presented herein).

	N[1]	Rise/fall mismatch	Real estate increase[2]	Need process monitor circuit/corner detector	Need control circuit
Cascade solution	3	4.14%	120%	No	No
Parallel solution	4	4.27%	230%	Yes	Yes

1: N is the increased number of MOSFET driver pair in cascade solution, N is the enabled slice units in parallel solution.
2: Real estate increase in silicon based on original output driver area(N=1).

Figure 13: Exemplary Cascade Solution Advantages

To achieve a similar rise/fall time mismatch, a Cascade Solution, according to aspects of the techniques presented herein, requires fewer MOSFETs, occupies less silicon real estate, and consumes less power.

Additionally, since a Cascade Solution, according to aspects of the techniques presented herein, does not require a process monitor/corner detector or a control circuit the implementation of such a solution may be much simpler.

In summary, techniques have been presented that support cascading multiple MOSFETs in a CML output buffer to reduce the CM noise in a SerDes with nearly no impact on, for example, cost, thermal performance, chip real estate, and power consumption.