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Original scientific paper

DESIGN OF NOVEL MULTIPLEXER CIRCUITS IN QCA NANOCOMPUTING

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Abstract. *Quantum-dot Cellular Automata (QCA) technology is a promising alternative nano-scale technology for CMOS technology. In digital circuits, a multiplexer is one of the most important components. In this study, an efficient and single layer 2 to 1 QCA multiplexer circuit is proposed using majority gate and inverter gate. In addition, efficient 4 to 1 and 8 to 1 QCA multiplexer circuits are implemented using this 2 to 1 multiplexer circuit. The developed multiplexer circuits are implemented in QCADesigner tool. According to the results, the developed 2 to 1, 4 to 1, and 8 to 1 multiplexer circuits utilize 16 (0.01μm^2), 96 (0.11μm^2), and 286 (0.43μm^2) QCA cell (area). The results demonstrate that the proposed 8 to 1 multiplexer circuit reduces the cost by about 25%-99% compared to the existing multiplexer circuits.*

Key words: *Multiplexer circuit, Quantum-dot cellular automata; coplanar, nanotechnology, nanoelectronics*

1. INTRODUCTION

Quantum-dot Cellular Automata (QCA) is one of the technologies at nano-scale level, which is developed by Lent et al. [1] in 1993. The QCA technology can be used for maintaining the trend predicted by Moore's law [2]. This technology has many advantages such as high device density, high switching speed, and low power consumption in comparison with Complementary Metal-Oxide-Semiconductor (CMOS) technology [3]. Basic devices in this technology consist of QCA cells, wire crossing and QCA logic gates. The fundamental unit in the QCA technology is the QCA cell that is comprised of a square with 4 quantum dots in corners [1, 4]. It should be noted that each QCA cell has only two electrons that can tunnel through neighboring dots. These two electrons are resided in opposite corners. So, there are two possible polarizations. Fig. 1 shows these two kinds of polarization, P= -1 and P=+ of QCA cells [5].

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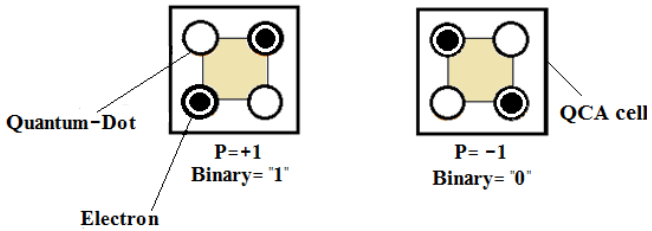

Fig. 1 Two possible polarizations in QCA cells, P= -1 and P=+1[5]

QCA wires consist of a number of QCA cells which can be used for transferring input cell polarization [5]. QCA wires can be categorized in two groups: (a) single layer crossing wire, and (b) multilayer crossing wire.

In addition, A four-phase (four-zone) clock pulse provided synchronization of information flow in the QCA circuits. The QCA clock pulse is employed to reduce power dissipation [3, 6]. The QCA cells behave like a single latch in each clock phase and propagate information in the same direction.

As illustrated in Fig. 2, the QCA clock is composed of four phases and each phase is shifted by 90 degrees [3, 6]. In the clock phase, a signal has four states:

1) Low-to-high state (SWITCH phase),
2) High state (HOLD phase),
3) High-to-low (RELEASE phase),
4) Low state (RELAX phase).

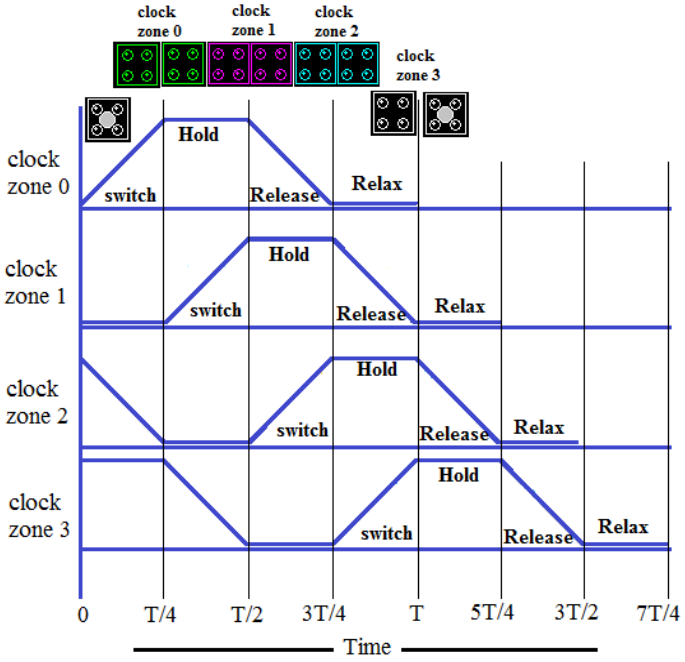

Fig. 2 Four phases of the QCA [3, 6]

When the QCA clock is in the low-to-high state, the potential energy of the QCA cell is low. So, tunneling barriers of the QCA cell start to raise and their polarizations start to actual computation according to the state of their neighboring cells during switch phase. The potential barriers of the QCA cells are in the highest level and they avoid electrons from tunneling in the hold phase. During the release phase, the reduction in the cell polarization is started and the tunneling barriers gradually are reduced. Finally, in the relax phase, the cells stay in an unpolarized state when potential barriers are held in low state and no barrier exists between the dots. The overall delay of the QCA circuits can be specified by the number of critical path clock phase [3].

In QCA circuits basic logic units are Majority Voter Gate (MVG) and inverter gate [1]. The 3-input MVG is considered as the most important gate in the QCA technology. It is because the 2-input OR gate and 2-input AND gate can be constructed using MVG by fixing one of the three inputs to P= +1 or P= -1, respectively [6]. The logic function of the MVG can be defined by the following equation:

$$\mathrm{Maj}\,(A, B, C) = \mathrm{Out} = AB + BC + CA \tag{1}$$

Where A, B, and C are inputs and the output is displayed by Out.

A four-phase clock pulse provides synchronization of information flow in the QCA circuits [7]. In addition, the QCA clock is employed for reducing the power dissipation [8]. The QCA cells behave similarly to a single latch in each clock phase. So, the information is propagated in the same direction.

In recent years, many different logic circuits have been developed in the QCA technology for various applications, such as QCA multiplier [9], QCA full adder [5, 10], QCA multiplexer [3, 6-9, 11-15], QCA counter [16], QCA shift register [17], and QCA comparator [18, 19]. In addition, multiplexer circuits play a significant role in the digital circuit design such as arithmetic logic unit design [6].

In this study, we develop a circuit with the aim of improving the performance of the single-layer 2 to 1 QCA multiplexer. Then, efficient and single-layer 4 to 1 and 8 to 1 multiplexer circuits are implemented based on this 2 to 1 multiplexer.

2. Design of 2 to 1 QCA Multiplexer

The developed 2 to 1 QCA multiplexer is shown in Fig. 3. This circuit consists of one inverter gate, one Rotate Majority Voter Gate (RMVG) and two Original Majority Voter Gates (OMVGs) due to area efficiency and need to have suitable architecture for modular design methodology for constructing efficient 2^n to 1 multiplexer circuits. This circuit consists of two inputs, A and B, one address line, S, and one output, F. The output F is expressed by the following equation:

$$F = A.\bar{S} + B.S \tag{2}$$

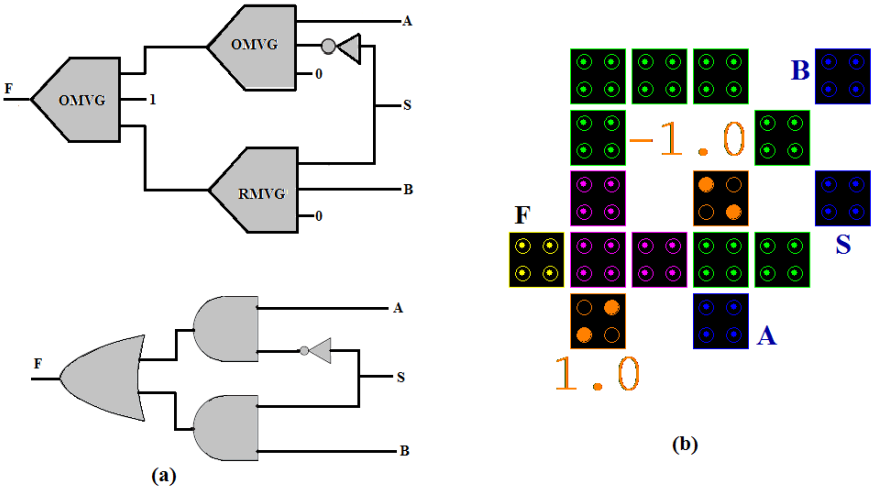

Fig. 3 The developed 2 to 1 QCA multiplexer circuit (a) logical circuit, (b) layout

To verify and justify the layout of the developed single layer 2 to 1 QCA multiplexer, QCADesigner tool version 2.0.3 [20] is utilized as a simulator on the cell level for QCA circuits. Figure 4 shows the simulated waveform of the developed 2 to 1 multiplexer circuit.

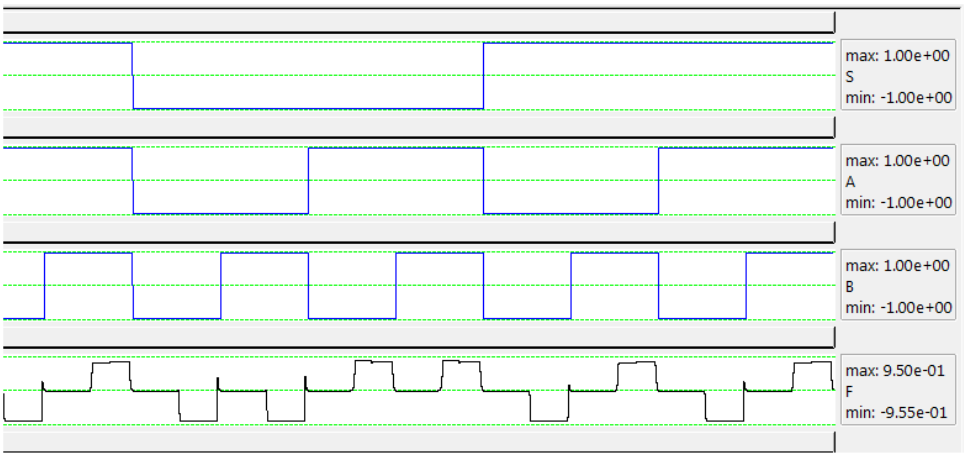

Fig. 4 The waveform of the developed 2 to 1 multiplexer circuit

It should be mentioned that for rapid access to simulation results, bi-stable approximation simulation engine has been chosen. For optimum layout, cellular layout of the developed 2 to 1 multiplexer is designed in one layer using 16 QCA cells and an area of 0.01 μm^2. It also takes 0.5 clock cycles to generate the output.

Table 1 summarizes comprehensive comparison between the developed single layer 2 to 1 QCA multiplexer circuit and other circuits in [3, 6-8, 13, 14] with regard to the latency

(required clock cycles), cell count, circuit area (μm^2), and cost, where the cost is defined by following equation:

$$\text{cost} = \text{Area} \times \text{Latency}^2 \quad (3)$$

Table 1 The simulation results of the single-layer 2 to 1 multiplexer circuits

Reference	Number of cells	Area (μm^2)	Latency	Cost
[14]	27	0.03	0.75	0.0169
[13]	19	0.02	0.75	0.0113
[7]	26	0.02	0.5	0.005
[6]	19	0.02	0.5	0.005
[8]	23	0.02	0.5	0.005
[15]	24	0.02	0.75	0.0113
[3]	15	0.01	0.5	0.0025
This paper	16	0.01	0.5	0.0025

Based on these simulation results, the developed 2 to 1 multiplexer circuit has an improvement with regard to cost, cell count, latency and circuit area compared to other 2 to 1 QCA multiplexer circuits in [13, 14, 15]. Moreover, our developed circuit has advantages with regard to cost, cell count, and circuit area compared to 2 to 1 QCA multiplexer circuits in [6-8]. The results demonstrate that the proposed 2 to 1 multiplexer circuit reduced the cost by about 50%-85% compared to the circuits that are proposed in [6-8, 13-15]. Although the 2 to 1 multiplexer circuit in [3] has advantages compared to our developed 2 to 1 multiplexer, the architecture of the developed 2 to 1 multiplexer is such that it is suitable for modular design methodology for constructing efficient 2^n to 1 multiplexer circuits.

3. Design of 4 to 1 QCA Multiplexer

The developed single-layer 4 to 1 QCA multiplexer circuit is shown in Fig. 5, which utilizes three developed 2 to 1 QCA multiplexer modules.

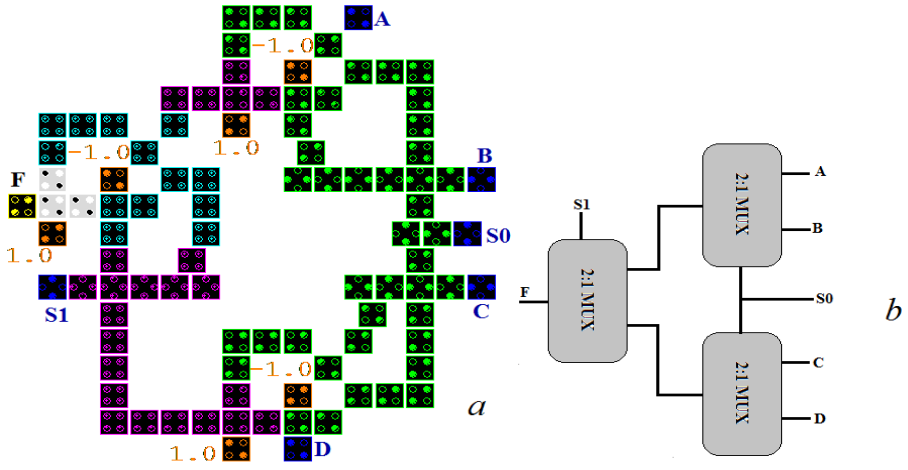

Fig. 5 The developed single-layer 4 to 1 QCA multiplexer circuit (a) layout, (b) logic circuit

The developed circuit consists of two address lines, four inputs, and one output. A, B, C, and D are utilized as input signals, S0 and S1 denote the address lines and output signal is shown by F. The output F is expressed by following equation:

$$F = (S1.S0)D + (S1.\bar{S0})C + (\bar{S1}.S0)B + (\bar{S1}.\bar{S0})A \quad (4)$$

Figure 6 shows the simulated waveform of the developed 4 to 1 multiplexer design.

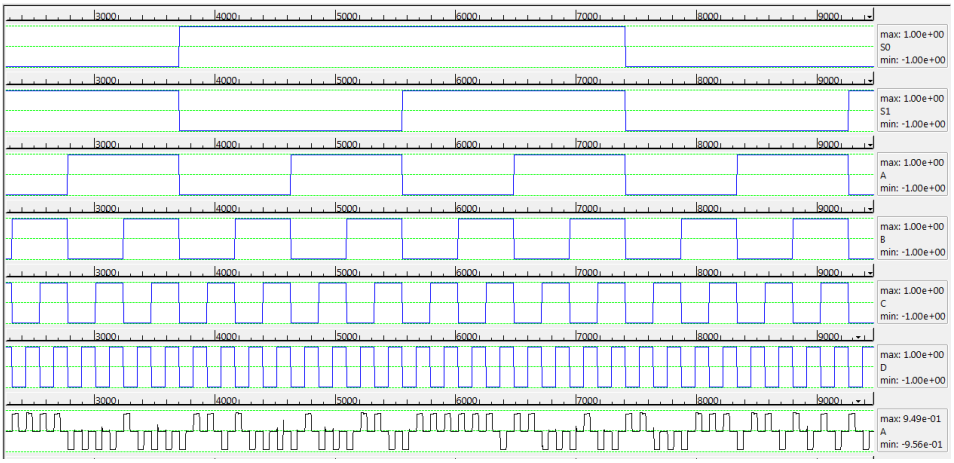

Fig. 6 The waveform of the developed 4 to 1 multiplexer design

For optimum layout, the cellular layout of the developed 4 to 1 multiplexer is designed in one layer using 96 QCA cells and an area of 0.11 μm^2. It also takes 1 clock cycle to generate the output. Table 2 summarizes comprehensive comparison between the developed single-layer 4 to 1 QCA multiplexer circuit and previous 4 to 1 QCA multiplexer circuits in [3, 7, 8, 11, 12].

Table 2 The simulation results for the 4 to 1 QCA multiplexer circuits

Reference	Number of cells	Area (μm^2)	Latency	Cost
[7]	271	0.37	4.75	8.3481
[11]*	251	0.2	1.25	0.3125
[11]	199	0.27	1.50	0.6075
[8]	155	0.24	1.25	0.375
[12]*	103	0.08	1.75	0.245
[3]	107	0.15	1	0.15
This paper	96	0.11	1	0.11

* multilayer

Based on these simulation results, the developed 4 to 1 QCA multiplexer circuit has advantages with regard to cost, cell count, latency, and circuit area compared to other 4 to 1 QCA multiplexer circuits in [7, 8, 11, 12]. Our developed 4 to 1 multiplexer circuit provides an improvement in terms of cost, number of cells, and circuit area compared to 4 to 1 QCA multiplexer circuit in [3]. The developed circuit also provides an improvement in comparison with 4 to 1 QCA multiplexer circuit in [12] with regard to cost, cell count

and latency. The results demonstrate that the proposed 4 to 1 multiplexer circuit reduces the cost by about 26%-98% compared to the circuits that are proposed in [3, 7, 8, 11, 12].

4. Design of 8 to 1 QCA multiplexer

The developed single-layer 8 to 1 QCA multiplexer circuit is displayed in Fig. 7, which utilizes the developed 2 to 1 multiplexer circuit and two developed 4 to 1 QCA multiplexer circuits.

The developed circuit consists of eight inputs, one output, and three address lines. A, B, C, D, E, F, G, and H are utilized as input signals, S0, S1, and S2 denote the address lines and output signal is shown by Out. The output Out, is expressed by the following equation:

$$\begin{aligned}Out=&(S2.S1.S0)H+(S2.S1.\bar{S0})G+(S2.\bar{S1}.S0)F+(S2.\bar{S1}.\bar{S0})E+(\bar{S2}.S1.S0)D\\&+(\bar{S2}.S1.\bar{S0})C+(\bar{S2}.\bar{S1}.S0)B+(\bar{S2}.\bar{S1}.\bar{S0})A\end{aligned} \quad (5)$$

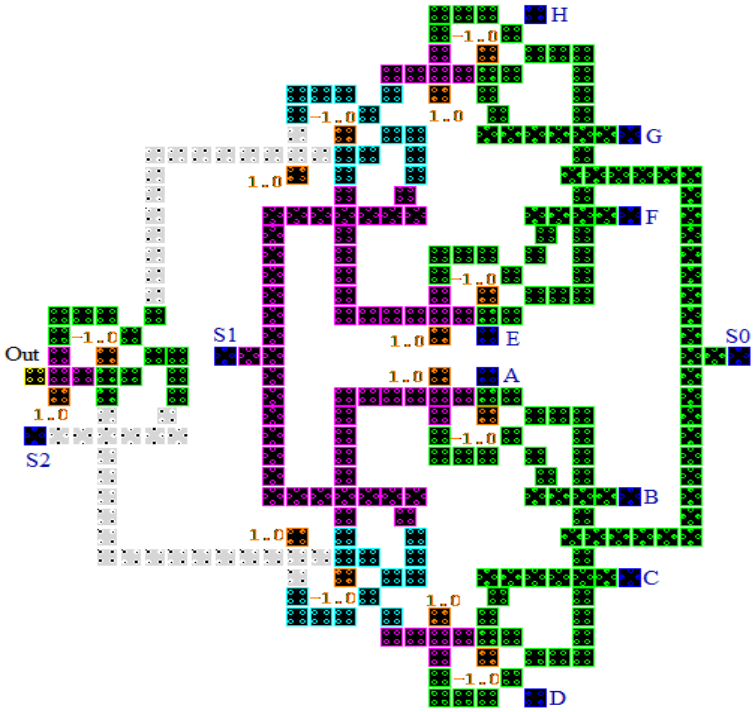

Fig. 7 The developed single-layer 8 to 1 multiplexer circuit

Figure 8 shows the simulated waveform of the developed 8 to 1 multiplexer design.

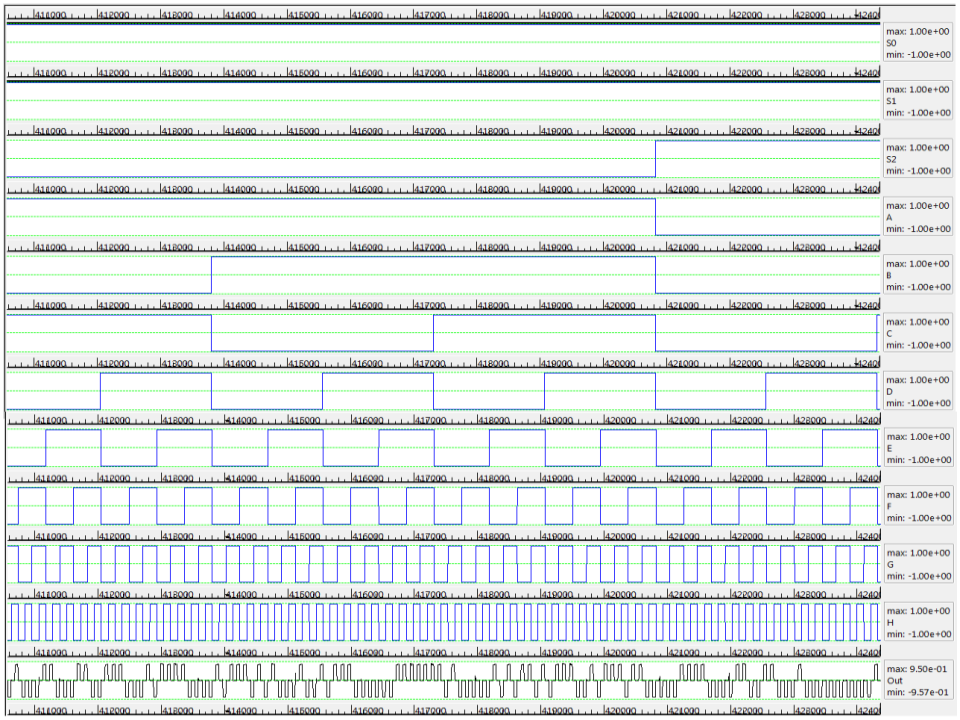

Fig. 8 The waveform of the developed 8 to 1 multiplexer design

For optimum layout, QCA layout of the developed 8 to 1 multiplexer is designed in one layer using 286 QCA cells and an area of 0.43 μm^2. It also takes 1.5 clock cycles to generate the output. Table 3 summarizes comprehensive comparison between the developed single-layer 8 to 1 multiplexer circuit and previous 8 to 1 QCA multiplexer circuits in [3, 7, 8, 11].

Table 3 The simulation results for the 8 to 1 QCA multiplexer circuits

Reference	Number of cells	Area (μm^2)	Latency	Cost
[7]	1312	1.83	10.5	201.76
[8]	462	0.87	1.75	2.67
[11]	494	0.58	2.25	2.94
[3]	293	0.58	1.5	1.31
This paper	286	0.43	1.5	0.97

Based on these simulation results, the developed 8 to 1 QCA multiplexer circuit has advantages with regard to cost, cell count, latency and circuit area compared to other 8 to 1 QCA multiplexer circuits in [7, 8, 11]. Moreover, our developed circuit has advantages with regard to cost, cell count, and circuit area compared to 8 to 1 QCA multiplexer circuit in [3]. The results demonstrate that the proposed 8 to 1 multiplexer circuit reduces the cost by about 25%-99% compared to the circuits that are proposed in [3, 7, 8, 11].

5. CONCLUSIONS

There are several kinds of nanotechnologies that are developed for replacing conventional CMOS technology [21-23]. The QCA technology is one of these nanotechnologies that provide the promising advantages. In this study, we have developed a novel and efficient single-layer circuit for 2 to 1 QCA multiplexer based on majority and inverter gates. Then, using this 2 to 1 QCA multiplexer circuit, the 4 to 1 and 8 to 1 QCA multiplexer circuits are developed. The developed circuits for QCA multiplexers have been simulated using QCADesigner 2.0.3. According to the results, the developed 2 to 1, 4 to 1, and 8 to 1 multiplexer circuits utilized 16 ($0.01\mu m^2$), 96 ($0.11\mu m^2$), and 286 ($0.43\mu m^2$) QCA cell (area). The results demonstrate that the proposed 8 to 1 multiplexer circuit reduces the cost by about 25%-99% compared to the circuits that are proposed in [3, 7, 8, 11].

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