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Low-power and high-detectivity Ge photodiodes by *in-situ* heavy As doping during Ge-on-Si seed layer growth

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Abstract: Germanium (Ge)-based photodetectors have become one of the mainstream components in photonic-integrated circuits (PICs). Many emerging PIC applications require the photodetectors to have high detectivity and low power consumption. Herein, we demonstrate high-detectivity Ge vertical *p-i-n* photodiodes on an *in-situ* heavily arsenic (As)-doped Ge-on-Si platform. The As doping was incorporated during the initial Ge-on-Si seed layer growth. The grown film exhibits an insignificant up-diffusion of the As dopants. The design results in a ~45× reduction on the dark current and consequently a ~5× enhancement on the specific detectivity (D^*) at low reverse bias. The improvements are mainly attributed to the improved epi-Ge crystal quality and the narrowing of the device junction depletion width. Furthermore, a significant deviation on the AsH$_3$ flow finds a negligible effect on the D^* enhancement. This unconventional but low-cost approach provides an alternative solution for future high-detectivity and low-power photodiodes in PICs. This method can be extended to the use of other *n*-type dopants (e.g., phosphorus (P) and antimony (Sb)) as well as to the design of other types of photodiodes (e.g., waveguide-integrated).

1. Introduction

In recent years, germanium (Ge) has been widely adopted into on-chip photonic integration for high-performance photodetectors [1–8] and electro-absorption (EA) modulators [9–15]. As of now, photonic-integrated circuits (PICs) adopting these devices have been demonstrated for diversified applications including sensing [16–18], imaging [19,20], data- and tele-communication [8,21,22], and quantum computing [23], where the photodetectors are generally required to exhibit a high sensitivity (i.e. detectivity) to weak optical inputs. Hence, a low dark current and high shunt resistance are desired for a low shot and thermal noise, respectively, of the Ge photodetectors to maintain the integrity of input signals. Additionally, a lower dark current suppresses the power consumption of both the EA modulators and the photodetectors, and therefore the total power consumption of the PIC. To realize the low dark current and high shunt resistance, a high-quality Ge layer is essential for the photodetectors, which is commonly integrated on silicon (Si) via direct epitaxial growth. The ~4% lattice mismatch between Ge and Si induces misfit and threading dislocations to the epi-grown Ge film, which adversely affects its crystal quality and the corresponding device performance. It has been reported that the dark current in Ge photodetectors is closely correlated to the threading dislocation density (TDD) in Ge [24]. The dislocations act as generation sites for excess carriers contributing to the dark

current. With years of development, Ge-on-Si films with TDDs $\sim 5\times 10^7$ cm^{-2} and lower have been achieved, using two- [25] and three-step [26] growth approaches without SiGe buffers. Dark current densities of the corresponding *p-i-n* photodiodes generally range from ~ 1 to 100 mA/cm^2 at a reverse bias of -1 V [1,2,5–7,27–31]. However, this range is significantly higher than that of In$_{0.53}$Ga$_{0.47}$As counterparts [32] operating at a similar wavelength span and would thus deteriorate the detectivity performance of the photodetectors. Therefore, it is imperative to develop low-cost methods to further improve the Ge crystal quality and suppress the dark current for photodetectors in future high-detectivity and low-power PIC applications.

On the other hand, vertical *p-i-n* structure stands out among the common Ge photodetector designs, exhibiting both a low dark current and high quantum efficiency, and is consequently expected to exhibit superior detectivity. Compared to metal-semiconductor-metal (MSM) configuration, photodetectors with a *p-i-n* structure offer both a broader extension and more uniform distribution of the electric field across the device, resulting in a more efficient collection of photon-generated carriers. Meanwhile, vertical *p-i-n* structure, compared to lateral *p-i-n*, exhibits a lower dark current [33,34] mainly due to the narrower depletion region that covers a smaller number of dislocations. In addition, for thicker (>1 μm) Ge films, the lateral *p-i-n* design faces the challenge of inefficient photon-generated carrier collection due to its limited electric field coverage, since the ion implantation for both the *p-* and *n-* wells is difficult to form deep dopant profiles. Therefore, although there have been numerous reports on reducing Ge TDD to $\sim 10^6$ cm^{-2}, including the incorporation of thick graded SiGe buffers [35], and the use of rapid melting growth [36] and selective epitaxy [37,38], these platforms are either complicated to realize, or impractical for a vertical *p-i-n* structure compatible with monolithic integration. Recently, direct wafer bonding provides a feasible route for high-quality Ge-on-insulator integration [39,40] and is easy to establish a vertical *p-i-n* structure along the process [41]. It would, however, also bring additional process complexity and cost.

Current designs of Ge vertical *p-i-n* photodiodes commonly place the *p*-doped layer at the bottom (in the epi-Ge seed layer or Si substrate) to alleviate the excess dopant diffusion during the subsequent high-temperature growth and annealing processes. This is because *p*-type dopants in Ge [e.g., boron (B)] are slower diffuser compared to *n*-type dopants (e.g. phosphorus (P), arsenic (As)) [42]. However, recently, Lee *et al.* [43] performed *in-situ* heavy As doping into the bottom of Ge during the seed layer growth and discovered an order of magnitude TDD reduction to $\sim 5\times 10^6$ cm^{-2} in the grown film. The As dopants are believed to accelerate the movement of threading dislocations and thus benefit their annihilation and the TDD reduction. A subsequent research utilized the As-doped Ge as a buffer layer for III-V integration, and developed InGaP-based LEDs with superior performances [44]. It is therefore worthwhile to study the performance of vertical *p-i-n* photodiodes on this As-doped Ge platform, due to its superior crystal quality and ease to form a vertical *p-i-n* structure by merely ion-implanting *p*-dopants at the top of the grown film. Hence, as a proof of concept, we herein break the common design rules for Ge photodetectors and investigate the performance of normal-incidence vertical *p-i-n* photodiodes on this bottom heavily As-doped Ge-on-Si platform. A $\sim 45\times$ reduction on the dark current and $\sim 5\times$ enhancement on the specific detectivity (*D**) are demonstrated at low reverse bias ($\in$[-1,0] V), compared to control devices without the *in-situ* As doping. The up-diffusion of As dopants is meanwhile found insignificant, exhibiting a reasonable background doping concentration $\sim 10^{17}$ cm^{-3}. This work provides a novel and low-cost approach to the design of high-performance Ge photodiodes for low-power PIC applications. The concept can also be extended to the design of waveguide-integrated Ge photodiodes, as well as to the use of other *n*-type dopants [45].

2.   Experimental: material growth, device fabrication and characterization

Ge was epitaxial grown on 200-mm Si (100) wafers (*p*-type, resistivity = 1-100 Ω-cm and with 6° off-cut) by metal-organic chemical vapor deposition (MOCVD). The detailed wafer cleaning, surface treatment and growth procedures were described elsewhere [43]. For the heavy As doping, Arsine (AsH$_3$) gas flow (100 and 200 sccm) was introduced during the initial seed layer growth at 400 °C. The flow rates have been verified to result in an active doping concentration of $\sim 10^{19}$ cm^{-3} in Ge [43]. The AsH$_3$ flow was then gradually reduced to zero at the subsequent high-temperature growth step (650 °C), where the growth continued afterwards up to the intended Ge thickness (~ 1.5 µm). After the growth, cyclic annealing was carried out from 650 to 850 °C for 5 cycles, with a 10-min holding time at 850 °C between adjacent cycles. A detailed characterization of the grown films has been discussed in prior work [43]. To study the TDD, the Ge films were dipped in iodine solution (a mixture of HF/HNO$_3$/CH$_3$COOH = 5:10:11 with iodine) for 1 s. As the solution penetrates dislocations to form pits, TDD can thus be determined by counting the etched-pit density.

The grown wafers were then fabricated for vertical *p-i-n* photodiodes. The fabrication started with an ion implantation of boron (B) for the top *p*-layer with a dosage of 4×10^{15} cm^{-2} at 40 keV. Dopant activation was performed via a rapid thermal annealing (RTA) at 650 °C for 15 s. The resulting doping profiles were studied using techniques of secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP). Subsequently, *p*- and *n*-mesas were formed via optical lithography followed by reactive-ion etching (RIE) using chlorine (Cl$_2$) gas. After the photoresist removal and a surface cleaning by a short dip in buffered oxide etchant (BOE, 6:1), a ~ 400 nm silicon dioxide (SiO$_2$) was deposited by plasma-enhanced chemical vapor deposition (PECVD) as a passivation layer. Contact areas were then defined by a third optical lithography followed by carbon tetrafluoride (CF$_4$)-based RIE. The RIE stopped where ~ 50 nm SiO$_2$ remains, followed by a BOE dip to fully remove the SiO$_2$ and expose the *p*-Ge. A stack of Ti/TiN/Al was sputtered and lifted-off for the device metal contacts. The fabrication ended with an RTA at 400 °C for 1 min to facilitate an ohmic characteristic of the contacts. Figures 1(a) and 1(b) show a cross-sectional schematic of the As-doped Ge vertical *p-i-n* photodiode and a microscope image of the fabricated device, respectively. In subsequent sections, devices fabricated on the As-doped Ge with AsH$_3$ flow of 200 sccm, denoted as "As-200", are analyzed and discussed.

For comparison, control devices of vertical *p-i-n* photodiodes on a germanium-on-insulator (GOI) platform, denoted as "Control GOI" in subsequent sections, were also fabricated. A cross-sectional schematic is shown in the right inset in Fig. 2(b). The reason not using bottom *p*-doped Ge-on-Si vertical photodiodes as the control is due to the inferior Ge quality grown on heavily boron-doped Ge by MOCVD [46]. This design uses ion implantation to form both the top and bottom doped regions, which leads to a wide depletion width with abrupt doping profiles [41] to compare with that of As-200, meanwhile maintaining a heavy As doping at the bottom part of the original epi-Ge (before its transfer to form GOI) as that of As-200 but without the dislocation annihilation mechanism. The junction depletion coverage is also comparable with that of conventional Ge-on-Si photodiodes. The GOI fabrication is discussed as follows. First, an identical MOCVD growth (without the use of AsH$_3$) was performed for an un-intentionally doped Ge layer on an identical 200-mm Si substrate. After B implantation at the top of the epi-film, the layer was transferred to another Si handle wafer via a SiO$_2$-intermediated direct wafer bonding. The epitaxy Si substrate was then removed by grinding, tetramethylammonium hydroxide (TMAH) etching and chemical-mechanical polishing (CMP). After the Ge layer was exposed, an As implantation was implemented to realize the vertical *p-i-n* structure. The final Ge thickness is ~ 1.4 µm, close to that of As-200. The fabrication of the GOI photodiodes shares an identical process to that of the As-doped photodiodes as discussed above. A detailed information on the GOI formation as well as its photodiode fabrication can also be found in our earlier
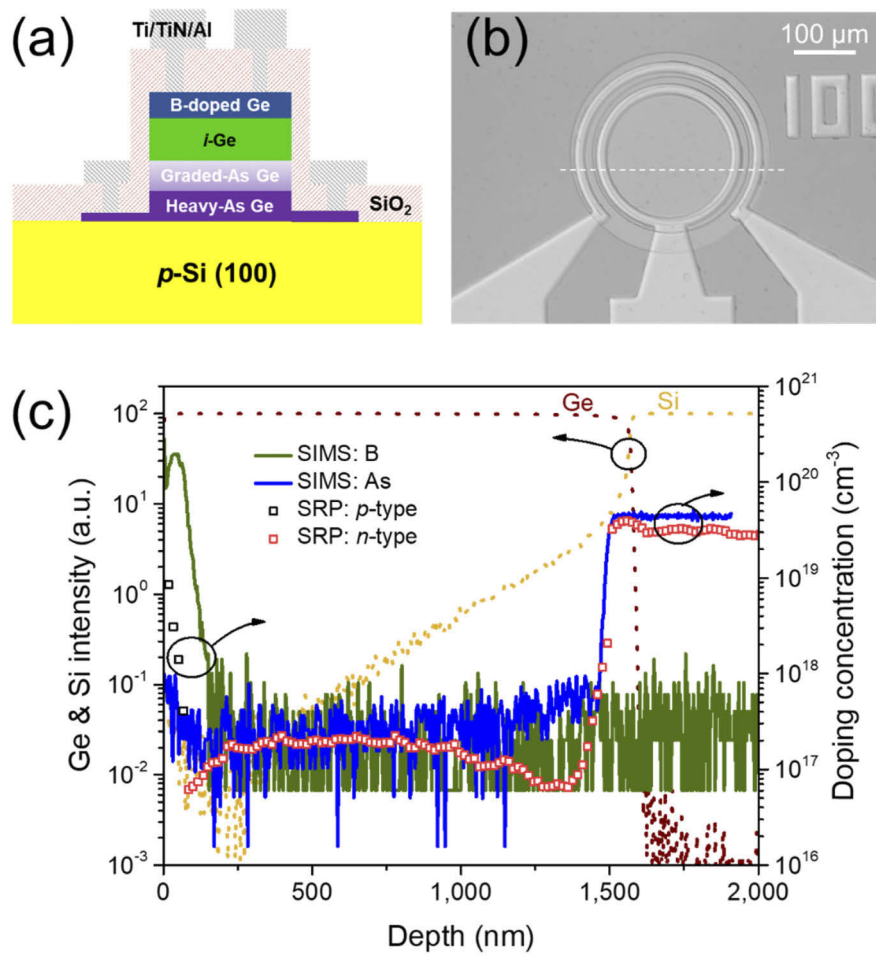
Fig. 1. (a) Cross-sectional schematic of a bottom heavily As-doped Ge-on-Si *p-i-n* photodiode. (b) Optical microscope image of a fabricated photodiode (from top view) with a mesa diameter of 250 μm. Cutting along the white dashed line obtains the schematic in (a). (c) SIMS and SRP doping profiles in the As-doped Ge-on-Si. Elemental intensity counts of Ge and Si are also included as layer reference.

works [39,41], where the photodiode performance has been demonstrated comparable to that of Ge-on-Si photodiodes.
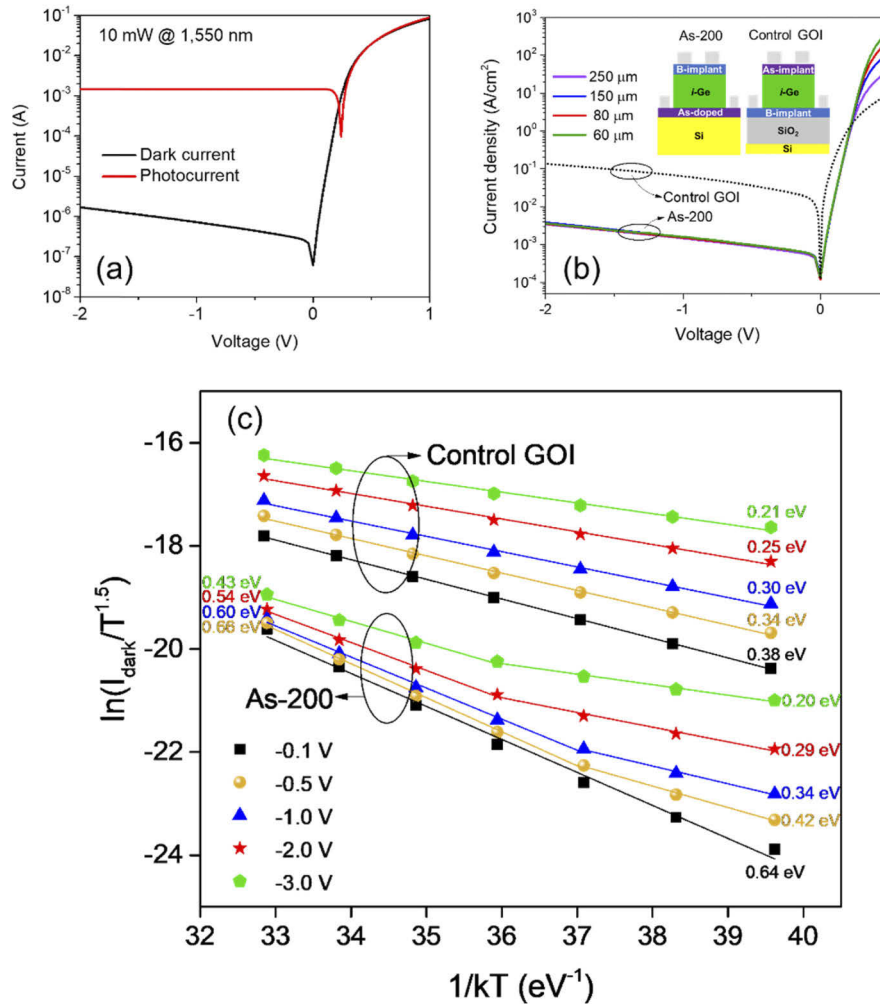
Fig. 2. (a) *I-V* characteristics of an As-200 photodiode with and without an illumination of 10 mW at 1,550 nm (mesa diameter = 250 μm). (b) J_{dark}-*V* characteristics of As-200 photodiodes with different mesa diameters, with that of a control GOI photodiode as a reference. Insets show cross-sectional schematics of respective devices (passivation layers not shown). (c) E_a extraction from the dark currents as a function of applied bias.

Current-voltage (*I-V*) characteristics were both measured at room temperature and from 293 to 353 K, on the fabricated devices using a Keithley 2400 source meter unit (SMU). To measure the optical responsivity, a TUNICS T100S-HP/CL tunable laser covering 1,500 to 1,630 nm was utilized. The output light was coupled into a Corning SMF-28 single-mode silica glass fiber to illuminate on the devices. The corresponding *I-V* characteristics were collected by the SMU via two electrical probes placed on the *n*- and *p*-metal contacts.

3. Results and discussion

3.1. SIMS and SRP analysis

Figure 1(c) displays the dopant profiles of As, B, and their net activated doping via the SIMS and SRP analysis. Elemental intensity counts of Ge and Si, acquired along with the SIMS analysis, are also included as a reference for layer identification. From the plot, abrupt *n*- and *p*-doping profiles are observed with peak carrier concentrations $\sim 10^{19}$ cm^{-3}. It is noteworthy that, different from the initial thinking to have the heavy As doping mainly in Ge, the resulting As profile started very close to the Ge/Si interface and extended deep into the Si substrate. The finding matches with the *n*-doping profile from SRP ($\sim 3 \times 10^{19}$ cm^{-3}) in Si, where it was originally *p*-doped before growth. This reveals the diffusion of As dopants towards the defective Ge/Si interface as well as the Si substrate, which agrees well with earlier reports [45]. The up-diffusion of the As dopants into Ge is thus insignificant, resulting in a mild *n*-type (As) concentration of $\sim 2 \times 10^{17}$ cm^{-3} acceptable for device applications. In addition, the plot reveals a Si out-diffusion into Ge, which also agrees with earlier studies [43,47], indicating an enhanced Si-Ge inter-diffusion induced by the heavy *n*-doping.

3.2. Dark current analysis

Figure 2(a) shows the *I-V* characteristics of a fabricated As-200 vertical *p-i-n* photodetector with and without an illumination of 10 mW at 1,550 nm. The dark current (I_{dark}) is 0.72 µA at -1 V, corresponding to a dark current density (J_{dark}) of 1.47 mA/cm^2 [Fig. 2(b)]. The photocurrent is constant (1.47 mA) throughout the reverse bias. The photocurrent saturation at 0 V indicates a good Ge crystal quality and collection efficiency of photon-generated carriers using only the built-in field of the *p-i-n* junction. Figure 2(b) shows the J_{dark}-V characteristics of the As-200 devices with different mesa diameters. The J_{dark} maintains at ~ 1.5 mA/cm^2 at -1 V independent of the mesa diameters. This indicates that the dark current is dominated by bulk leakage instead of surface leakage, which implies a good device passivation. The J_{dark}-V of a photodiode on the Control GOI was also appended in the same plot for comparison, where the J_{dark} (63.82 mA/cm^2 at -1 V) has also been shown independent of mesa diameters [41]. It can be found that the J_{dark} is reduced by $\sim 45\times$ for the As-200 devices, which is among the lowest compared to that of reported Ge photodiodes [2,28,29]. To find out the root cause for the dark current suppression, the temperature-dependent I_{dark}-V measurement was carried out on both the As-200 and Control GOI devices with mesa diameter of 250 µm. The corresponding plot of $ln(I_{dark}/T^{1.5})$ as a function of $1/kT$ is shown in Fig. 2(c) at different reverse biases to extract the activation energies (E_a) of the dark currents, where T is temperature in kelvin and k is the Boltzmann constant. From the plot, the E_a decreases with an increasing reverse bias, for both the As-200 and GOI devices. This might be due to an enhanced trap-assisted tunneling caused by the increased electric field in the *p-i-n* junction [48]. However, a clear contrast can be seen by comparing the E_a between the two types of devices. The GOI shows an $E_a \sim 0.34$ eV at -0.5 V, indicating a dark current dominated by carrier generation from deep-level traps near the mid-bandgap of Ge via Schottky-Reed-Hall (SRH) process; while the As-200 reveals higher values of ~ 0.42 and ~ 0.66 eV, respectively, at lower (293 to 313 K) and higher (323 to 353 K) range of temperatures. The higher E_a suggests a dark current contributed more prominently from the diffusion process by intrinsic minority carriers generated via inter-band transition. This is especially dominant for the As-200 at low bias, with $E_a \sim 0.66$ eV matching with the Ge bandgap energy. Therefore, it can be inferred that the SRH-generated contribution is significantly reduced in the dark current of As-200 device, considering its diffusion-dominant nature after its $\sim 45\times$ reduction with respect to the GOI device.

The study is continued to demystify the reason for the decrease in the SRH-generated current. As the devices under investigation are with large junction areas (mesa diameter of 250 µm), J_{dark} mainly consists of the bulk carrier generation (J_{gen}) and diffusion (J_{diff}) components as mentioned

in the previous paragraph, with negligible contribution from surface generation [49]. To separate J_{gen} and J_{diff} from J_{dark}, the method described in Ref. [49] was used, where linear interpolation of J_{dark} is performed with respect to the junction depletion width W_d, as J_{gen} linearly scales with W_d for a *p-i-n* junction at a reverse bias larger than ~0.025 V [Eq. (1)].

$$J_{gen} = q\frac{n_i}{\tau_g}W_d\left[\exp\left(\frac{qV}{2kT}\right) - 1\right]$$ (1)

where n_i and τ_g denote the intrinsic carrier concentration and carrier generation lifetime, respectively, in Ge; and V is the applied voltage bias. J_{diff} can thus be extracted as the *y*-intercept of the fitting at $W_d = 0$, and its subtraction from J_{dark} results in J_{gen}. W_d was obtained from a capacitance-voltage (*C-V*) measurement (Keithley 4200SCS probe station, 100 kHz) on the devices with different mesa diameters. The detailed procedure is described in our prior work [41]. The J_{gen} and W_d leads to τ_g using Eq. (1), which is a key parameter related to Ge crystal quality. Here, J_{dark}-*V* characteristics at 353 K were utilized for a more prominent diffusion current for the separation.

Figure 3(a) shows the corresponding J_{dark}-W_d plots as well as their linear interpolation at reverse biases with a step size of 0.1 V. J_{diff} were extracted as 5.80×10^{-2} and 2.64×10^{-2} A/cm², respectively, for Control GOI and As-200 devices. The corresponding J_{gen} were thus calculated as 1.31×10^{-4} and 9.06×10^{-6} A at -0.3 V, respectively, revealing a ~15× reduction on J_{gen} for the As-200 device. This leads to extracted τ_g of 3.14×10^{-8} and 7.80×10^{-9} s, respectively, for As-200 and GOI. The longer carrier lifetime indicates a lower TDD and consequently an improved Ge crystal quality. This also agrees well with the improved crystal quality in the prior work [43] and the decreased etched-pit densities obtained from the SEM images shown in Figs. 3(c) and 3(d), where the TDD is reduced by ~6× (from ~6.1×10^7 to 9.7×10^6 cm⁻²) with the incorporation of the heavy As doping.

Apart from the improved crystal quality, the less overlap of threading dislocations with the depletion region also accounts for the lower J_{gen}. As observed in Fig. 3(a), W_d is much wider for GOI devices (~795 nm at -0.3 V) than that of As-200 (~160 nm). This is simply because the average Ge background doping concentration is approximately an order of magnitude lower for GOI (~10^{16} cm⁻³) than that of As-200 (~2×10^{17} cm⁻³), as shown in Fig. 3(b). Therefore, the depletion coverage for the As-200 is narrower and further away from the heavily dislocated Ge/Si interface, suggesting a less overlap of threading dislocations with the depletion region and consequently a lower SRH-related generation current. For a better illustration of the mechanisms causing the J_{gen} reduction, cross-sectional schematics of the As-200 and GOI devices are drawn, including W_d and the distribution of dislocations, in the insets of Fig. 3(e). To further verify our experimental results, the respective Ge TDDs obtained from the etched-pit densities [Figs. 3(c) and 3(d)] are plotted in terms of their τ_g from the J_{dark}-W_d plots [Fig. 3(a)], as shown in Fig. 3(e). The data points exhibit a good match with theoretical calculation, indicating the validity of the proposed mechanisms for the J_{gen} decrease.

3.3. Specific detectivity (D*) analysis

Figure 4(a) shows the responsivity ($\mathcal{R}$) of the As-200 and Control GOI devices with respect to the reverse bias. Surface reflections have been excluded from the $\mathcal{R}$ calculation. The As-200 exhibits a slightly lower $\mathcal{R}$ ~0.19 A/W independent of bias, due to its narrower W_d resulting in an inferior collection efficiency of photon-generated carriers. On the other hand, the narrower W_d provides a stronger electric field at low biases to maintain the carrier collection efficiency as that at high biases. This explains the $\mathcal{R}$ drop for the GOI device at V> -0.3 V, where the electric field is insufficient to collect all photon-generated carriers due to its wider W_d. The $D*$ is
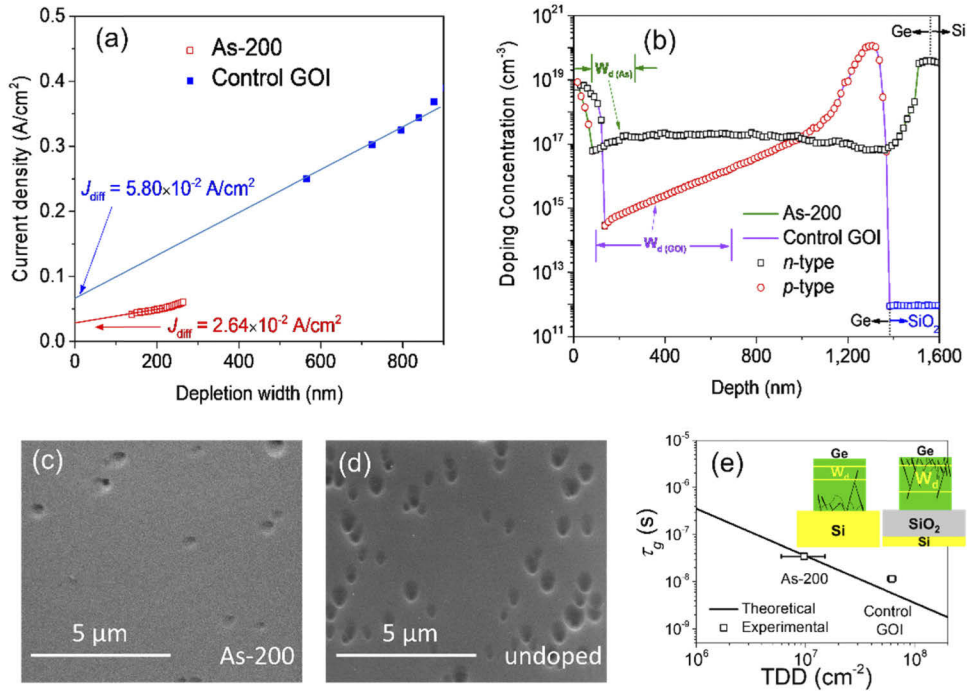
Fig. 3. Analysis for the decrease of J_{gen}. (a) J_{dark}-W_d plots measured at 353 K for the separation of diffusion (J_{diff}) and generation (J_{gen}) leakage components for the extraction of carrier generation lifetime (τ_g). The y-intercept of the linear fitting gives J_{diff}. (b) SRP doping profiles of As-200 and GOI in Ge, labelled with the estimated depletion widths (W_d) at -0.3 V. (c), (d) Top-view SEM images of etched-pit densities (i.e. TDD) of (c) As-200 ($\sim 9.7 \times 10^6$ cm^{-2}) and (d) undoped ($\sim 6.1 \times 10^7$ cm^{-2}, before GOI formation) Ge films on Si, respectively, after the iodine solution dip. (e) τ_g as a function of TDD in Ge. The experimentally determined τ_g and TDD values (from (a), (c) and (d)) show good agreement with theoretical calculation. The error bars indicate the TDD obtained from three distinct locations. Insets show simplified schematics of the devices illustrating the mechanism for the J_{gen} decrease.

calculated using the following relation [50]:

$$D^* = \frac{\Re\sqrt{A\Delta f}}{\sqrt{I_{shot}^2 + I_{ther}^2}} \quad (2)$$

where Δf is the bandwidth (1 Hz), I_{shot} is the shot noise due to the dark current and I_{ther} is the thermal noise. I_{shot} and I_{ther} can be expressed as follows:

$$I_{shot} = \sqrt{2qI_{dark}\Delta f} \quad (3)$$

$$I_{ther} = \sqrt{\frac{4kT \cdot \Delta f}{R_{shunt}}} \quad (4)$$

where R_{shunt} is the shunt resistance, which is extracted by taking dI/dV at V = 0. The R_{shunt} of As-200 and GOI are thus obtained as 1.55×10^5 and 4.50×10^3 Ω, respectively. The I_{shot} was determined as 1.06×10^{-13} and 8.84×10^{-13} A·Hz$^{-1/2}$ for the As-200 at 0 and -2 V, respectively,

compared to 1.39×10^{-13} and 4.63×10^{-12} A·Hz$^{-1/2}$ for the Control GOI; while the I_{ther} was determined as 3.26×10^{-13} and 1.92×10^{-12} A·Hz$^{-1/2}$ for the As-200 and Control GOI, respectively. Both I_{shot} and I_{ther} are reduced for the As-200 device due to the lower I_{dark} and higher R_{shunt}, resulting in a lower device noise equivalent power and consequently an improved D^*. The D^* for As-200 at 300 K (1.24×10^{10} cm·Hz$^{1/2}$W^{-1}) is therefore enhanced by ~5× compared to that of Control GOI (2.45×10^{9} cm·Hz$^{1/2}$W^{-1}) at 0 V, as shown in Fig. 4(b). The improved D^* is comparable to that of commercial Ge photodiodes [51] developed on defect-free bulk Ge. This significant enhancement facilitates a Ge photodiode design for both high D^* and low power consumption. The D^* enhancement remains prominent (~3.6×) at -2 V. The D^* can be further improved using a waveguide-integrated design [6]. In addition, the As-doped Ge photodiodes using the AsH$_3$ flow of 100 sccm were also analyzed for D^*. It can be observed from Fig. 4(c) that AsH$_3$ flows of 100 and 200 sccm both lead to commensurate D^*. This provides a broad design window for the As-doped Ge photodiodes in controlling the actual AsH$_3$ flow and the up-diffusion of As dopants in various epitaxy systems.
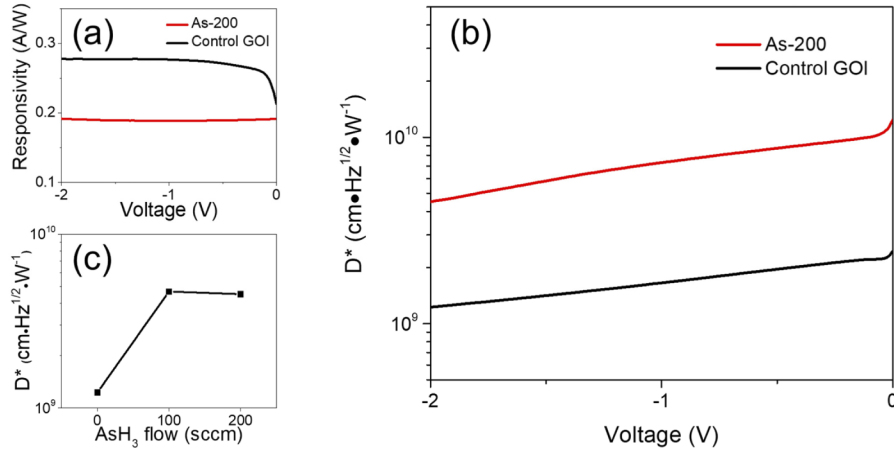
Fig. 4. (a) Responsivity ($\mathcal{R}$) and (b) specific detectivity (D^*) of As-200 and control GOI devices as a function of applied reverse bias. (c) D^* of the photodetectors at -2 V as a function of AsH$_3$ flow used for the heavy As doping.

3.4. Discussion on frequency response

The narrower W_d [~200 nm, Fig. 3(b)] of the As-200 detector accounts for a higher junction capacitance and consequently a slower RC-limited time response. The 3-dB bandwidth of the frequency response can be determined using the following equation:

$$f_{3-\text{dB}}=\sqrt{\left(\frac{1}{f_{\text{trans}}^{-2}+f_{\text{RC}}^{-2}}\right)} \tag{5}$$

where $f_{\text{trans}} = 0.45\cdot v_{\text{sat}}/W_d$ and $f_{\text{RC}} = 1/(2\cdot\pi\cdot RC_j)$ are the carrier transit-limited and RC delay-limited 3-dB frequencies, respectively. The v_{sat} denotes the carrier saturation drift velocity (6×10^{6} cm/s) in Ge and R the load resistance (50 Ω) commonly used in network analyzers; C_j is the junction capacitance $\varepsilon A_j/W_d$ of the device, where ε is the permittivity of Ge and A_j the area of the device mesa. Figure 5 shows the calculated 3-dB bandwidth of the As-doped Ge photodiode as a function of its mesa diameter. The device is expected to own a 3-dB bandwidth >14 GHz at a mesa diameter <20 μm, which can be a useful guideline for normal-incidence PIC applications since the core diameter is ~9 μm for common single-mode fibers at tele-communication wavelengths.

Hence, the narrowing of W_d would not prominently affect the high-frequency performance of the photodiodes, if small mesa diameters are adopted in the design. This conclusion can be similarly applied to the design of heavily As-doped waveguide-integrated Ge photodiodes, by minimizing the detector junction capacitance (e.g., tailoring the detector thickness, width, or length) without compromising the quantum efficiency.

4. Conclusion

In this work, heavy As doping was incorporated into the design of normal-incidence Ge-on-Si vertical *p-i-n* photodiodes at the bottom of the Ge epi-layer during its seed layer growth. The fabricated device (As-200) exhibits a ~45× reduction on the dark current compared to that of control devices without the *in-situ* As doping. The dark current is dominated by the carrier diffusion process, suggesting a prominent suppression of the carrier generation originated from the threading dislocations in Ge. This agrees well with both the ~6× TDD reduction in the epi-film and the W_d narrowing in the device. Further support on this argument lies in the reasonable matching of the extracted τ_g with that from theoretical calculation as a function of TDD. Despite a slight drop in $\Re$, the As-200 device shows a ~5× enhancement on D^* due to the lower dark current and higher shunt resistance. The enhancement maximized at 0 V, facilitating low-power applications. In addition, commensurate D^* enhancement was observed for devices from 100-sccm AsH_3 flow, indicating a broad design window for the As-doped Ge epitaxy. Calculation shows that the W_d narrowing has a minimal influence on the device 3-dB bandwidth, if a small mesa diameter is adopted. This work provides an unconventional but low-cost design of Ge-on-Si vertical *p-i-n* photodiodes for low-power and high-detectivity applications such as sensing, imaging, and communication.
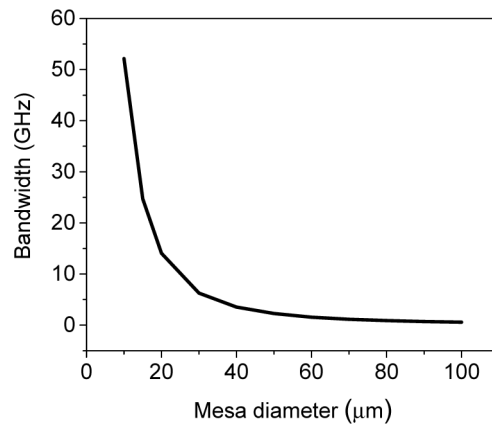
Fig. 5. Calculation of 3-dB bandwidth for the As-200 Ge photodiode as a function of its mesa diameter.

Disclosures. The authors declare no conflict of interests related to this article.

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