A 250-ps Integrated Ultra-Wideband Timed Array Beamforming Receiver in 0.18 μm CMOS

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***Abstract*—This paper presents a 4-channel ultra-wideband (UWB) timed array beamforming receiver designed in a standard 0.18-μm CMOS technology. The proposed timed array receiver achieves a maximum delay of 250 ps at the maximum beam steering angle of $\pm 42^o$ with 10.5^o (8 steps) steering resolution and 2-cm antenna spacing. Each receiver channel provides gains ranging from 3.6 to -35 dB and less than 8% delay variation for all delay settings over a 3.1$-$10.6-GHz frequency range, while consuming a maximum of 58 mW power from a 1.8-V supply. The average -1-dB compression point P_{1dB} is -9.9 dBm. The proposed architecture is modeled and simulated by using Virtuoso Cadence.**

***Index Terms*—Ultra-wideband (UWB), beamforming, true-time delay (TTD), delay cell, timed array receiver.**

I. Introduction

Pulse-based ultra-wideband (UWB) radio technology has attracted lots of attentions over recent decades due to the wideband nature of its signals, and has been mainly investigated for communications, radar, and positioning applications [1]–[3]. This unique feature of the UWB technology provides therefore enhanced specifications in terms of data rate, precision, low system complexity and cost, and low power as compared to the conventional narrowband systems. A large number of narrowband and wideband or UWB systems in communications are based on beamforming technique, in which various beam patterns can be electronically scanned. Fig. 1 illustrates a beamforming antenna receiver realized by two widely used methods, namely, phase shifters (phased array) [4] and true-time delay (TTD) elements (timed array) [5]. The phase shifters cause beam squinting (i.e., frequency-dependent beam angle problem) and thus are limited to narrow frequency bands [6]. As an attractive alternative, the TTD elements with variable gain and delay are a good solution for large bandwidths due to the fact that the beam direction of a TTD-based beamforming system remains independent to the frequency.

The TTD elements can be realized by both passive and active delay sections. The passive delay circuits, such as LC transmission lines [7] and internal-switched delay circuits [8], suffer from large areas for CMOS implementations in order to produce a large amount of delay and are therefore not area-efficient. Two state-of-the-art active g_m-C all-pass delay cells reported in [5] and [9] are largely compact$-$however, their bandwidth is limited to low-GHz frequency ranges (up to 2.5 GHz).

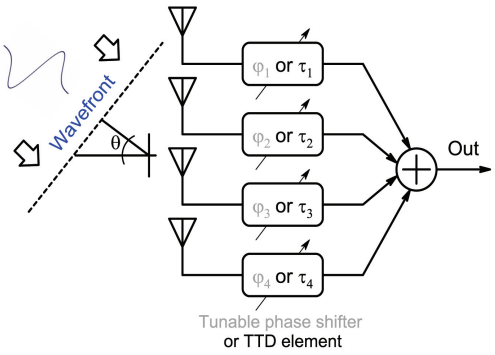

Fig. 1: Architecture of a linear 4-element antenna array receiver realized by phase shifters or TTD elements.

In this paper, we aim to alleviate the problems associated with the prior art by proposing a topology which consists in CMOS integrated timed array receivers and can be suitable for UWB communications, e.g., radar and imaging applications. The proposed architecture is realized by tunable active all-pass filter (APF)-based TTDs, resulting in reduced on-chip area as against the beamforming systems based on passive circuits. Moreover, the proposed architecture is intended for a moderate power dissipation. This will be achievable via effectively designing and optimizing the sub-blocks of the receiver. The proposed timed array receiver is designed in a standard UMC 180-nm CMOS process.

II. UWB Beamforming Systems

This section discusses briefly the functionality and specifications of UWB antenna array systems. In these antenna arrays (see Fig. 1), a received UWB pulse with a direction of arrival θ reaches each one of N antennas at different intervals or, in fact, with different relative delays. The tunable TTD cells are therefore exploited to compensate these relative delays with different amounts of delay in each antenna channels as given by

$$\tau_n = (N-n)\frac{d}{c}\sin\theta; \quad n = 1, 2, ..., N \tag{1}$$

where n denotes the index of antenna element, d is the interelement spacing, and c represents the velocity of light. The maximum required delay, $\tau_{\max}$, is equal to τ_1 with the maximum angle of beam direction, $\theta_{\max}$. The required delay resolution for such a beamforming system can be determined by $\tau_{\text{res}} = \frac{d}{c}\sin\theta_{\min}$, where $\theta_{\min}$ represents the beam steering resolution. The aligned pulses are then added to each other coherently to form the output signal as given by

$$S_{\text{UWB}}(t) = \sum_{n=1}^{N} p_n(t - \tau_n) \tag{2}$$

where $p_n(t)$ is the received pulse (e.g., a Gaussian monocycle) in each antenna element and τ_n denotes the corresponding time delay given in (1). The range resolution of a UWB impulse system can be presented in the form of $\Delta R_{\text{UWB}} = c/2BW$, where BW is the impulse bandwidth. The beamwidth of a UWB antenna array system depends on the signal pulse width (T_{p}) and the interelement spacing (d) as given by $\Delta B_{\text{UWB}} \propto c \cdot T_{\text{p}}/d$.

When compared to a single antenna element, a UWB array system with N antennas improves the output signal-to-noise ratio (SNR) with $10\log_{10}(N)$ [dB] [5].

III. UWB Timed Array Receiver: Proposed Architecture

The topology of the proposed 4-element UWB timed array beamforming receiver is depicted in Fig. 2. In this topology, variable-gain low noise amplifiers (LNAs) exploited at the front of each channel fulfill four tasks: 1) noise reduction, 2) signal amplification, 3) gain adjustment, and 4) impedance matching. Each channel applies TTD elements to control and adjust the gain and delay. Tunable delay of 144 ps, with delay steps of 12 ps (12 steps), will be achieved by a cascade of six TTD cells (maximum 24 ps for each TTD). However, the maximum delay of the timed array receiver is 250 ps (144 ps plus the delay of LNA and switch). The voltage-to-current (V-I) conversion switches $S_1 - S_6$ are used per channel for signal-path selection and signal amplification. Thus, the amount of required delay can be selected by activating the appropriate tap switch. Since only one V-I conversion amplifier will be activated in each channel, the delay stemmed from these switches is similar for all the channels and therefore it does not affect the beam shape. It is noteworthy that the proposed architecture does not use any adder or combiner, since the current signals of all channels can be easily added together to complete the beamforming function. Finally, the load resistor R_L converts back the output signal into voltage. The buffer is used for output impedance matching (50 Ω).

The timed array receiver is intended for a frequency range of $3.1 - 10.6$ GHz, antenna spacing $d = 2$ cm, beam steering resolution $\theta_{\min} = 10.5^o$, and the maximum angle of beam direction $\theta_{\max} = \pm 42^o$.

A. UWB Variable-Gain LNA

The detailed schematic of the UWB LNA is illustrated in Fig. 3 [10]. It consists in a common-gate (CG) input structure

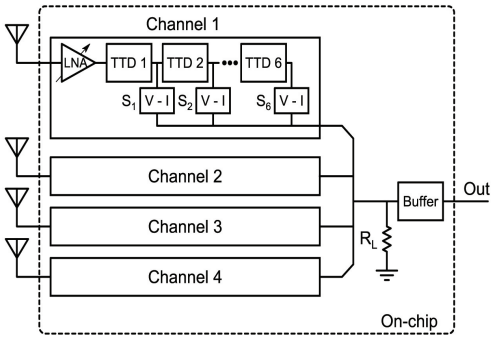

Fig. 2: Architecture of the proposed 4-element UWB timed array receiver.

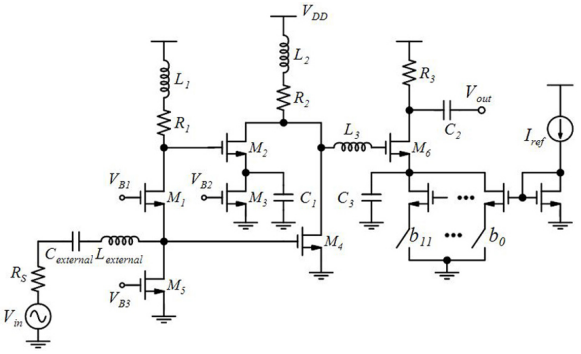

Fig. 3: Schematic of the UWB variable-gain LNA.

which employs a wideband noise-canceling technique. The CG transistor M_1 provides wideband input impedance matching such that the input matching is primarily determined by $1/g_{m1} = R_S$, where g_{m1} and R_S are the transconductance of M_1 and the source resistance, respectively. The noise cancelation is accomplished by the common-source (CS) transistors M_2 and M_4 under the condition of $g_{m2}R_1 = g_{m4}R_S$. The inductors L_1 and L_2 are shunt-peaking elements for bandwidth extension purposes, and L_3 is a series-peaking inductor which further extends the bandwidth and provides some residual peaking on the frequency response. The last stage consisting of M_6 and R_3 is used to boost the power gain of the LNA across the desired band, as well as matching the output impedance to 50 Ω. Unlike [10], we have used a switchable bias current generator at the last stage for the gain-trimming purpose.

B. Tunable UWB TTD Element

Fig. 4 shows the block diagram and schematic of the TTD cell based on first-order APF [11]. The TTD cell applies a CS−CG structure which is composed of two parts: a low-pass part and a unity-gain section. Ignoring parasitic poles and zeros resulting from the parasitic capacitances (C_{gs} and C_{gd}) of M_1 and M_2 and assuming $g_{m1,2} \gg g_{ds1,2}$, the transfer function of this TTD cell becomes

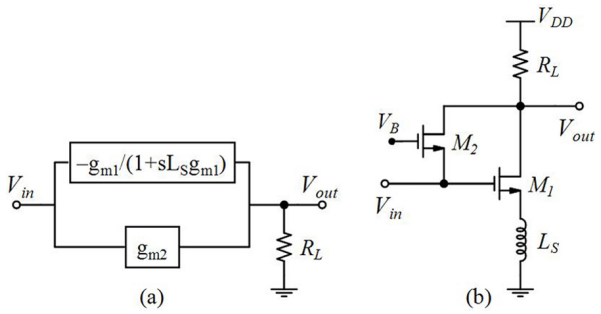

Fig. 4: (a) Block diagram and (b) schematic of the first-order APF-based TTD cell.

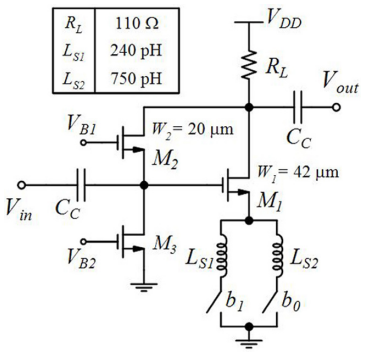

Fig. 5: Schematic of the UWB TTD cell with 2 bit binary tuning.

$$H_{\text{ttd}}(s) = \frac{V_{\text{out}}}{V_{\text{in}}}(s) = -R_L(g_{m1} - g_{m2}) \cdot \frac{1 - sL_S\frac{g_{m1}g_{m2}}{g_{m1}-g_{m2}}}{1 + sL_Sg_{m1}} \tag{3}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively, inductor L_S is a source degeneration element, and R_L is a load resistor to convert back the current signal to voltage. By setting $g_{m2}R_L = 1$ and $g_{m1} = 2g_{m2}$ which result in the unity DC gain and the same absolute values of pole and zero, respectively, an all-pass structure will be achieved. Therefore, the transfer function in (3) can be simplified as

$$H_{\text{ttd}}(s) = -\frac{1 - sL_Sg_{m1}}{1 + sL_Sg_{m1}}. \tag{4}$$

The pole/zero frequency and group delay response are $|\omega_{\text{p1,z1}}| = (L_Sg_{m1})^{-1}$ and $D(\omega) = 2L_Sg_{m1}/(1 + (\omega L_Sg_{m1})^2)$, respectively, where ω is the angular frequency related to the frequency f through $\omega = 2\pi f$. The low-frequency group delay is approximately equal to $2L_Sg_{m1}$. Small-signal analysis conducted on the TTD cell along with the parasitic elements of MOSFETs, led to the existence of extra high-frequency poles and zero. The additional parasitic poles are located at $\omega_{\text{p2}} = -(C_{gd1}R_L)^{-1}$, $\omega_{\text{p3}} = -(C_{gd2}R_L)^{-1}$, and $\omega_{\text{p4}} \approx -g_{m1}/C_{gs1}$. The high-frequency parasitic zero is located at $\omega_{z2} = g_{m1}/(L_Sg_{m1}g_{ds1} + C_{gd1})$. To push the parasitic poles and zero to very high frequencies, the R_L is kept small and the channel length of M_1 and M_2 is selected to be minimum.

Aiming for cascadability and tunability in a delay line, the TTD cell shown in Fig. 5 is introduced. Selectable delays of 12 ps and 24 ps will be achieved by the binary-switchable source degeneration inductors L_{S1} and L_{S2}, respectively. To minimize the delay interval errors due to the cascade of the TTDs, each TTD will be implemented by various inductor values. Transistor M_3 is used for the DC bias and calibration purposes through V_{B2}. To ensure that we have a unity gain in each signal path and channel of the timed array receiver, the value of R_L is selected to be different for each individual TTD cell to control the DC gain [refer to (3)]. This will slightly affect the system performance, but compensate the gain attenuation due to the cascade of the delay cells. The switchable current generator of the LNA will further contribute to the gain tuning of the timed array.

IV. Simulation Results

The proposed UWB timed array receiver is designed to work efficiently over the frequency range of 3.1−10.6 GHz. The simulation results of this work are performed by using Virtuoso Cadence. Fig. 6 illustrates single-channel power gain (S21) and group delay responses for all delay settings. As shown, depending on the delay setting, the gain ranges from a maximum of 3.6 dB to a minimum of −35 dB at 10.6 GHz, while the delays are almost constant within $<$ 20 ps over the whole frequency band. The simulated single-channel input matching (S11), output matching (S22), reverse isolation (S12), and NF are shown in Fig. 7. The S11 and S22 are better than 11.5 dB and the S12 is larger than 150 dB across the frequency band of interest. The worst case NF of the 4-element timed array at the maximum steering angle $\theta_{\max}$ (once the average delay of the single channel is set) [5] is 10.9−25.7 dB versus frequency. Fig. 8 shows time-domain simulation results when the individual receiver channel is fed by a UWB Gaussian monocycle with $T_{\text{p}} = 35$ ps using Verilog-A in Cadence. As illustrated, the maximum delay difference, corresponding to the maximum steering angle of the channel, is approximately 248 ps which is very close to the delay value in Fig. 6. The average −1-dB compression point (P_{1dB}) consisting in the average delay setting and center frequency (f_c) is found to be −9.9 dBm. The maximum power dissipation of the single receiver channel (without buffer) is 58 mW from a 1.8-V supply.

V. Conclusion

A 3.1−10.6-GHz, 250-ps 4-channel CMOS timed array beamforming receiver realized by all-pass sections has been introduced. With 12-ps delay resolution which corresponds to a beam steering resolution of 10.5^o, a total of 9 beams will be generated by the proposed timed array. Table I compares this work with recently reported delay line architectures.

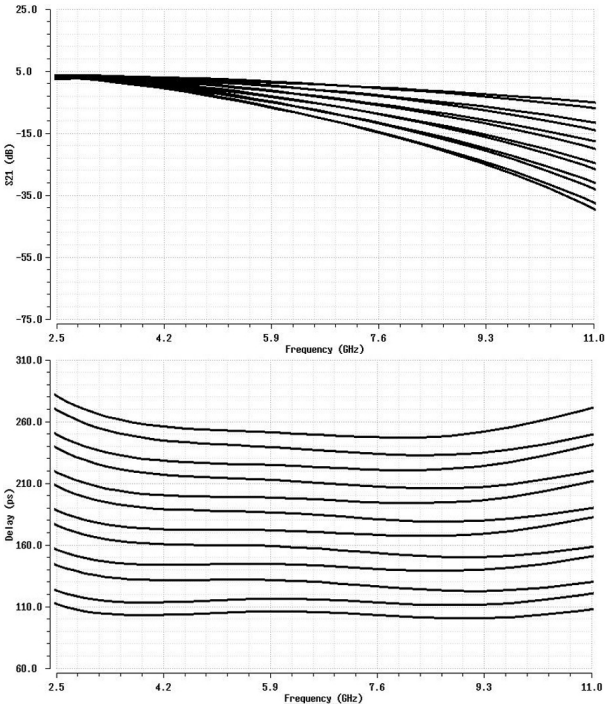

Fig. 6: Simulated single-channel power gain and group delay results for all delay settings.

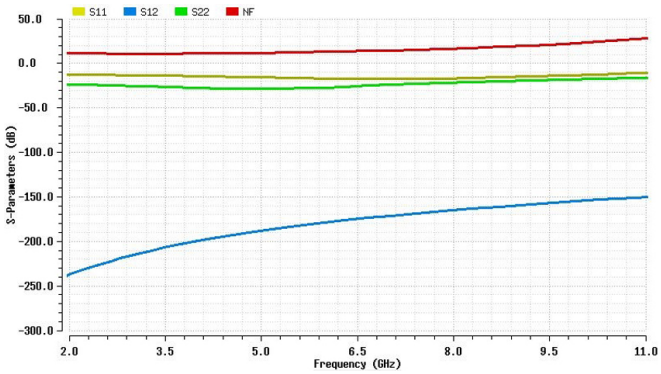

Fig. 7: Simulated single-channel input/output matching, reverse isolation and noise figure when the delay of the single channel is 175 ps.

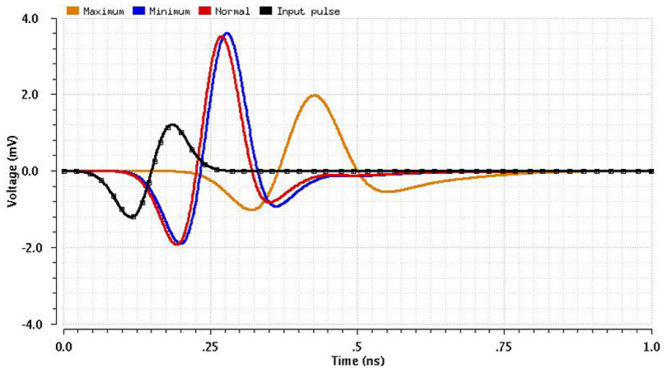

Fig. 8: Simulated single-channel response to a UWB monocycle for the normal ($\theta = 0^o$), minimum ($\theta = 10.5^o$) and maximum ($\theta = 42^o$) steering angles.

TABLE I: Performance summary of reported delay lines.

	[5]	[8]	[9]	This Work
Technology	0.14 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS
Architecture	Active	Passive	Active	Active
Frequency (GHz)	1−2.5	8−18	0.1−2	3.1−10.6
Maximum Delay (ps)	550	125	1700	250
Delay Range (ps)	0−550	0−125	250−1700	100−250
Delay Resolution (ps)	13	3.9	10	12
Delay Variation	1.8%	21%	16%	8%
Gain (dB)	15−12	−15.2 to −23.3	0.6	3.6 to −35
Average NF @f_c (dB)	9	19.25	21	14.3
Average P_{1dB} @f_c (dBm)	−24.5	N/A	−13	−9.9
Supply (V)	1.5	3.3	1.4	1.8
Power (mW)	90	≈ 0	364	58

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