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ABSTRACT Synchronous reference frame proportional-integral (PI) current controller (CC) is considered the most well-established solution for the current regulation in electrical drives. However, the gain selection of the PI CC is still regarded to be poorly reported, particularly in relation to the effect of the inevitable execution time taken by the controller and inverter. Mostly, tuning process of PI CC is done by trial and error or using simple rules based on pole zero cancelation and pole placement methods which ignore time delays through the controller and inverter. Hence, PI CC delivers significantly different performance compared to the expected one during the digital implementation, especially if high bandwidth or low ratio between the switching and operational frequency are required. Therefore, this paper firstly addresses and analyses the common tuning rules of PI CC which ignore the existence of time delays followed by a rigorous analysis for PI CCs' robustness to the influence of computational and modulation delays. Based on this analysis, generic recommendations have been proposed to select the PI CCs' gains as a function of the electrical drive switching frequency considering the delay effect. A set of simple, generic, and fast tuning rules were derived that guarantee fast dynamic performance with reasonable stability margins. Moreover, the effects of model uncertainties on these developed rules have been analyzed and reported. Comprehensive experimental results are provided to prove the key analytical results of this study and to validate the proposed design recommendations.

INDEX TERMS Current Control, Delay effect, Synchronous reference frame, AC drive system

I. INTRODUCTION

AC synchronous machines have been widely used in many industrial applications, particularly the automotive applications which require high steady-state and dynamic performance. So, developing a control system for the synchronous machines in such applications has a great interest in the last few decades. Field oriented control (FOC) is considered as the most established strategy in the electric drive systems. It consists of cascaded control loops, typically with an inner loop for current regulation and outer loop for speed control. It can be argued that the current control loop has a major effect on the overall system performance [1]. Therefore, many studies that investigate various current control schemes are reported in [2-5]. The hysteresis controller, for instance, can achieve instantaneous tracking of the reference. However, the wide variation of the switching frequency during the fundamental period in the hysteresis control may lead to irregular inverter operation [2]. Model Predictive current controllers also provide a very fast dynamic response, but they are very sensitive to the model parameter variations [4]. In general, it can be said that the field of current controller (CC) is dominated by synchronous reference frame (SRF) proportional-integral (PI) CCs. Their success is mainly due to the inherent simplicity in their design and implementation [6-8]. Besides, the fundamental excitation signal in SRF is transformed into dc quantity which easy to be regulated and to achieve zero steady state error using PI controller. However,

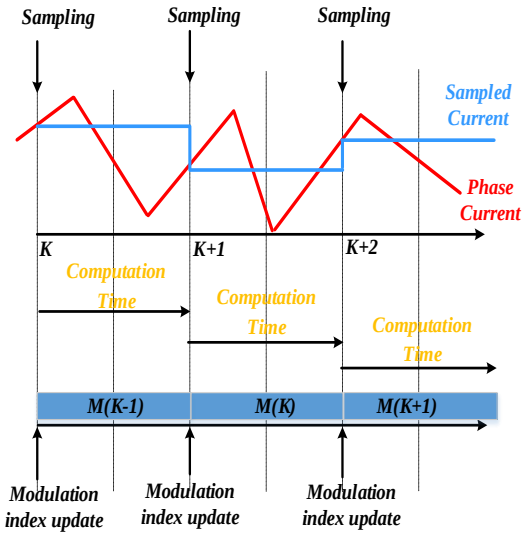


FIGURE 1. **Schematic for current measurement sampling compared with the PWM and control signal updates**

transformation of the electrical signals to the SRF creates cross -coupling between the orthogonal current components that is proportional to the fundamental operating frequency. So, the performance of the current controller is degraded during the increase of operating speed. So that, great efforts have been applied to enhance further their performance hence generating various configurations of this CC technique. Some researchers introduce the added feedforward terms to compensate the cross-coupling components and mitigate operating frequency effects [8]. Others propose the complex vector SRF PI CC to provide better cross-coupling compensation [7, 9, 10]. The design of the CC has also been presented in [11, 12] as a multi-input multi output controller which known by dynamic decoupling CC to improve the cross-coupling compensation. The advanced angle delay has been introduced in [13] to improve the control performance by compensating the delay in the angle due to the rotating d-q frame.

However, despite the widespread usage and development of SRF PI CCs, the gains' selection are mostly based on trial and error or common methods, which set rules for the PI gains in order to achieve a targeted performance, such as pole-placement [14, 15] , pole/zero cancelation [10, 12, 16] ,Ziegler-Nichols and Cohen-Coon methods [17, 18]. These rules are based on assumption of no time delay through the current control loop. This time delay refers to the inevitable execution time taken by controller and inverter [13].

In current control loop, the control action is generated based on the difference between reference and measured current (error signal). The generated control signal is responsible for generating the PWM signals to generate ac voltage applied to the machine such that the machine's currents follow the reference values. Ideally, this process should be instant (i.e., synchronized), but in practice the existence of time delays in controller (discrete-time implementation using DSP) and the inverter prevents this synchronization as illustrated by Fig.1. It shows that the control signal is updated at instant *k* which corresponds to the measured current at previous instant *k-1*. This phenomenon degrades the system performance, including stable operation regions [13, 19]. For many practical applications time delays can be ignored, however in some cases, for example when high bandwidth response or lower switching to operational frequency are required, the performance of digitally implemented CC can be significantly different compared to the expected one due to ignoring the existing time delays [20]. Moreover, high bandwidth operation with negligible overshoot for current controller is desirable for high dynamic performance. Since there are cases where the delay must be taken into account during the CC design, these tuning methods need to be thoroughly analyzed and evaluated. Therefore, this paper presents

1- Comprehensive analysis for various possible structures of PI controllers and their common tuning methods which ignore the time delay in their rules.
2- Comparative stability analysis for their robustness to the influence of computational and modulation delays.
3- Proposed simple tuning rules of PI CCs that guarantee fast and robust dynamics with reasonable stability margins considering effects of the time delay.
4- Experimental results to validate the proposed tuning rules and to prove the analytical outcome in this paper.

II. SRF PI Current Controller Design Schemes

The general structure of the current control system of AC machine with SRF PI CC overall can be shown in Fig. 2 where the machine model is represented by the complex vector notation in SRF as shown by (1), where r and L are the machine resistance and inductance respectively, and ω_e is the electrical angular velocity [21].

The complex vector notation represents the machine as asymmetric three phase R-L load. The imaginary term in the denominator $j\omega_e L$ refers to the cross-coupling terms between orthogonal components of the currents. Their effect can be mitigated by introducing the decoupling current elements ($j\omega_e L'$) as shown in Fig. 2.

$$G_p(s) = \frac{I_{dq}}{U_{dq}} = \frac{1}{Ls + r + j\omega_e L} \qquad (1)$$

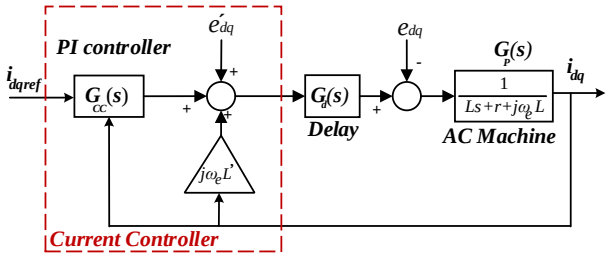


FIGURE 2. **Overall block diagram of current control loop in ac machine represented by the complex vector notation.**

The execution time delay through the inverter and the controller is shown by the block $G_d(s)$ which can be represented in the control system [21] as given in (2), where T_d represents the time delay which is typically evaluated in AC drive systems as 1.5 times of the sampling time T_s [9, 22] and considering the one step advanced angle [13]. Note that Ts coincides with the period of the pulse width modulation (PWM) carrier (T_{sw}) in case of single update mode.

$$G_d(s) = e^{-s\,T_d} \tag{2}$$

The back EMF of the ac machine e_{dq} and its compensation term e'_{dq} are also shown in the block diagram. The difference between them is considered as a disturbance. The PI controller in Fig. 2 can be structured by one or two degree of freedom PI controller which has been discussed in the following subsections. During the CC tuning, operating speed is assumed to be zero as a rule of thumb [23]. Hence, the cross coupling and their compensation elements have been removed during the study of controller's gains selection. The analysis cases in this paper assume controlling the permanent magnet machine with the parameters given in Table 1.

A. Conventional PI CC with Pole/Zero Cancelation Method (1st Design)

The classical PI controller in the current control loop has been considered in this approach as seen in Fig. 3. The open loop transfer function of Fig. 3 can be shown as follows:

$$G_{o.l}(s) = \frac{K_p s + K_i}{s}\frac{G_d(s)}{Ls + r} \tag{3}$$

The controller gains in (3) are tuned based on the pole zero cancelation method where they are selected according to (4) and (5) [7, 8], where L' and r' represent the machine nominal parameters in Table 1. Note that their values might be different from the actual machine parameters L and r.

$$K_i = K_o r' \tag{4}$$

$$K_p = K_o L' \tag{5}$$

If it is assumed that the machine parameters used in the tuning process match the actual values, the corresponding open loop and closed loop transfer functions of Fig. 3 can be expressed by (6) and (7) respectively.

$$G_{o.l1d}(s) = \frac{K_o}{s} G_d(s) \tag{6}$$

$$G_{c.l1d}(s) = \frac{K_o\, G_d(s)}{s + K_o\, G_d(s)} \tag{7}$$

When the time delay is ignored, the closed loop transfer function can be deduced as given by equation (8) where the current control loop is simplified to a first order system and K_o refers to the closed loop system bandwidth.

$$G_{c.l1}(s) = \frac{G_{o.l}(s)}{1 + G_{o.l}(s)} = \frac{K_o}{s + K_o} \tag{8}$$

TABLE 1. MACHINE PARAMETERS

Parameter	Symbol	Value
Phase Resistance	r	1.058 mΩ
Phase Inductance	L_d=L_q=L	99 µH
Poles pairs	p	3
Magnet flux linkage	Φ_m	0.03644 wb
Rated Power	P_{rated}	45 kw

Consequently, the controller gains can be designed easily based on the targeted bandwidth K_o.

B. Conventional PI CC with Pole Placement Method (2nd Design)

The classical PI controller shown in Fig. 3 can also be tuned using pole placement method which has been addressed in this section. Based on (3), a general closed loop transfer from Fig. 3 can be expressed by (9).

$$G_{c.l2d}(s) = \frac{(K_i + K_p s)\, G_d(s)}{Ls^2 + r\, s + K_p\, G_d(s)\, s + G_d(s)\, K_i} \tag{9}$$

When the time delay and also the machine parameters errors are ignored, equation (9) can be simplified to a second order system shown by (10).

$$G_{c.l2}(s) = \frac{K_i + K_p\, s}{L\, s^2 + (r + K_p)\, s + K_i} \tag{10}$$

For pole placement method, the PI gains are set to allocate the closed loop system poles according to desired location to achieve targeted dynamic performance. In this tuning criteria, the PI gains are determined by comparing the denominator of equation (10) and the general form of characteristics polynomial of the second order system ($s_2 + 2\eta\omega_n s + \omega_n = 0$) where ω_n and η are the natural frequency and the damping ratio respectively [24]. Finally, the controller gains can be derived as follows:

$$\left.\begin{aligned} K_p &= (2\eta\omega_n\, L') - r' \\ K_i &= \omega_n^2\, L' \end{aligned}\right\} \tag{11}$$

As shown from (11), the PI gains can be determined based on damping ratio, which is always assumed by 0.707 [23, 25], and natural frequency which can be determined from the targeted bandwidth (BW) as follows [18]:

$$\omega_n = \frac{BW}{\sqrt{1 - 2\eta^2 + \sqrt{4\eta^4 - 4\eta^2 + 2}}} \tag{12}$$

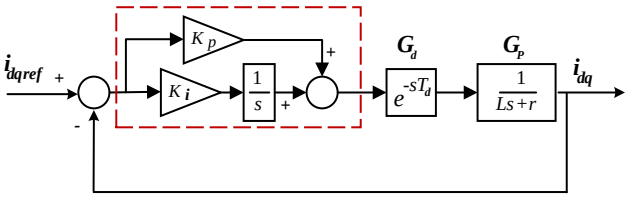


FIGURE 3. Block diagram of the Current control loop using the conventional PI CC.

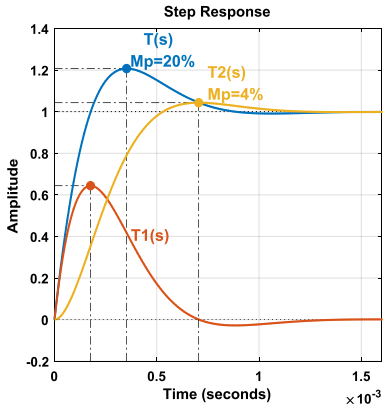


FIGURE 4. **Step response of $T_1(s)$, $T_2(s)$ and $T(s)$**

Despite the simplicity of this method, it has a drawback due to the zero in the closed loop transfer function. This can deprive the controller of obtaining the design requirements in full, even before considering the time delays. Although, this drawback is not related to the delay effect, its impact on the dynamic performance has been analyzed in this section in order to cover the overall change of its dynamic performance during the digital implementation.

This effect can be explained from the analysis of equation (10) as follows:

$$G_{c.l2}(s) = T(s) = \frac{\frac{K_i}{L}\left(\frac{K_p}{K_i}s+1\right)}{s^2+\frac{r+K_p}{L}s+\frac{K_i}{L}} = \underbrace{\frac{K_p}{K_i}\, s\, T_{des}(s)}_{T_1(s)} + \underbrace{T_{des}(s)}_{T_2(s)} \tag{13}$$

where $$T_{des}(s) = \frac{\frac{K_i}{L}}{s^2+\frac{r+K_p}{L}s+\frac{K_i}{L}}$$

In (13), it can be observed that the system response has two components, $T_2(s)$ which represents the desired response, and $T_1(s)$ that refers to the component added by the zero which degrade the performance.

To illustrate the effect of this zero on the loop performance, the step response of $T_1(s)$, $T_2(s)$ and $T(s)$ are simulated as shown in Fig. 4, using PI gains calculated from (11) to achieve bandwidth BW =1 kHz and damping ratio = 0.707. It shows that the additional component $T_1(s)$ rises the system overshoot (MP) by 5 times from the desired value which should be around 4% for 0.707 damping ratio. It can also be observed that the system has a faster response than expected. This refers to higher bandwidth which can be determined from the magnitude of the frequency response of equation (10) as shown in Fig. 5a. It shows that the system bandwidth equals 2.05 kHz which is larger than the desired value (1 kHz) by 105 %. The deviation between the desired and actual performance is considered a drawback because it refers to lower stability margins.

To avoid this drawback, a modification for this PI structure with the pole placement is presented in the following section [26].

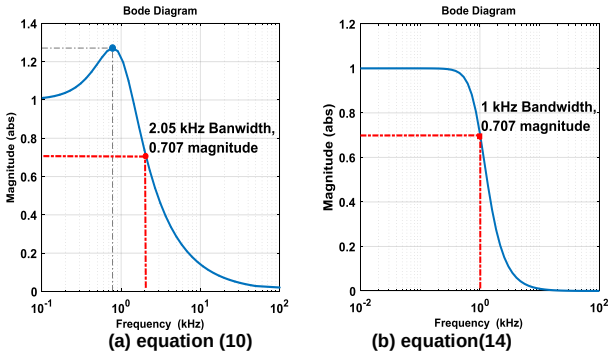


FIGURE 5. **Frequency response of closed loop transfer function**

C. Modified Conventional PI CC with Pole Placement Method (3rd Design)

To achieve the desired performance, whilst considering the issue described in Section II-B above, the resultant closed loop transfer function should be as given in (14).

$$G_{c.l3}(s) = T_{des}(s) = \frac{\frac{K_i}{L}}{s^2+\frac{r+K_p}{L}s+\frac{K_i}{L}} \tag{14}$$

where $$\omega_n^2 = \frac{K_i}{L}\ ,\ \ 2\eta\omega_n = \frac{r+K_p}{L}$$

As described in [26], the conventional PI CC scheme can be rearranged to that shown in Fig. 6 where the open loop transfer function (when the delay block is neglected) is expressed by (15).

$$\therefore G_{o.l3}(s) = \frac{T_{des}(s)}{1-T_{des}(s)} = \frac{\frac{K_i}{s}}{Ls+r+K_p} \tag{15}$$

It can be observed from Fig. 6 that the modified conventional PI CC is structured by using an integral part as the main controller and the proportional gain K_p is set as an additional element in the feedback of the current. The additional element can be considered as a virtual resistance added to the machine resistance as shown from (15). So, it represents a damping element that enhances the disturbance rejection capability of the current control loop.

The modified PI scheme achieves the targeted performance as seen from Fig. 5b. It shows the magnitude of frequency response of equation (14) when the PI gains are tuned to achieve 1 kHz bandwidth and 0.707 damping ratio.

Considering the delay block in Fig.6, the open and closed loop transfer functions for the current control loop can be expressed

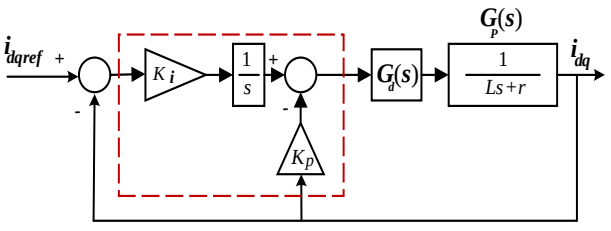


FIGURE 6. **Block diagram of the Current control loop using the modified conventional PI CC**

by (16) and (17) respectively. They have been used in Section III to analyze the delay effect on this CC scheme.

$$G_{o.l3d}(s) = \frac{K_i\, G_d(s)}{Ls^2 + \left(r + K_p G_d(s)\right)s} \tag{16}$$

$$G_{c.l3d}(s) = \frac{K_i G_d(s)}{Ls^2 + \left(r + K_p G_d(s)\right)s + K_i G_d(s)} \tag{17}$$

D. Two Degree of Freedom PI CC with Pole/Zero Cancelation Method (4th Design)

Another method, known as the two degree of freedom (2DOF) control is proposed to optimize the setpoint response and the disturbance response independently [27]. It provides fast disturbance rejection without a significant increase of overshoot in the step point tracking. So, it can be considered as a good option for the current control loop [14]. The 2DOF PI CC can be shown in Fig. 7. It consists of a main compensator (integral part) and two parameters (K_1 and K_2) to represent feedforward and feedback terms, respectively. The control law for 2DOF PI current controller can be represented using the complex vector notation as shown by (18).

$$u_{dqref} = K_1 i_{dqref} + \frac{K_i}{s}\left[i_{dqref} - i_{dq}\right] - K_2 i_{dq} \tag{18}$$

Based on (18), the closed loop transfer function of the system in Fig. 7 can be expressed by (19).

$$G_{c.l4d}(s) = \frac{(K_1 s + K_i)G_d(s)}{Ls^2 + (r + K_2\, G_d(s))s + K_i G_d(s)} \tag{19}$$

For the open loop transfer function, due to existence of feedforward term (K_1), it cannot be derived directly from Fig. 7. So, it is assumed that the open loop transfer function considering an augmented plant with feedback terms can be expressed as shown by (20).

$$G_{o.l4d} = \frac{G_{c.l4d}(s)}{1 - G_{c.l4d}(s)} \tag{20}$$

To tune this CC scheme when the delay is ignored, the corresponding closed loop transfer function should be derived firstly that can be shown by (21).

$$G_{c.l4}(s) = \frac{\frac{K_1}{L}s + \frac{K_i}{L}}{s^2 + \frac{r+K_2}{L}s + \frac{K_i}{L}} = \frac{as+b}{s^2+cs+b} \tag{21}$$

A common approach to tune 2DOF PI CC is by pole-placement to achieve pole/zero cancelation by selecting the coefficients of (21) as follows, where α refers to the closed loop system bandwidth (targeted bandwidth).

$$a = \alpha\ ,\ b = \alpha^2,\ c = 2\alpha \tag{22}$$

Accordingly, the closed loop transfer function is simplified to be a first order system as shown by (23).

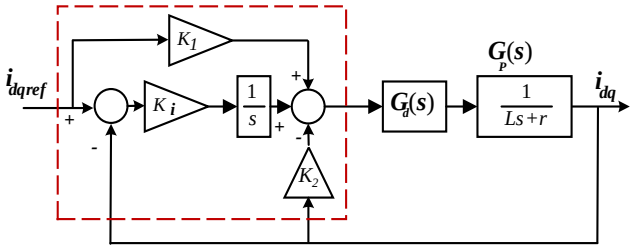


FIGURE 7. Block diagram of the Current control loop using two degree of freedom PI CC

$$T(s) = \frac{\alpha}{s+\alpha} \tag{23}$$

Based on (21) and (22), the controller gains can be derived as seen in (24).

$$\left.\begin{aligned} K_1 &= \alpha\, L' \\ K_i &= \alpha^2 L' \\ K_2 &= 2\alpha\, L' - r' \end{aligned}\right\} \tag{24}$$

III. Robustness of SRF PI CC Schemes to Modulation and Computational Delay

Different schemes of PI CC have been presented in Section II showing that their tuning criteria are based on one parameter, which is the targeted bandwidth (*BW*). Hence, for same drive system and same setting of these schemes, the current response should be the same in the ideal system when the time delay is ignored.

As explained in section I, ignorance of the time delay during the PI CC design deteriorates its dynamic performance during the digital implementation. Therefore, the delay effect on the dynamic performance of the addressed PI CC schemes in Section II is studied and evaluated in this section. The robustness of each one with respect to the delay effects is analyzed to determine which CC type can achieve bandwidth close to the targeted value with less deviation in its stability margins. These margins are evaluated in frequency domain by using two performance factors, namely - phase margin (*PM*), gain margin (*GM*). They measure the stability degree of the stable system. For this analysis, the delay function is approximated by a second order pade expansion as shown by (25) to achieve good accuracy [28].

$$G_d(s) = \frac{1 - \frac{T_d}{2}s + \frac{T_d^2}{12}s^2}{1 + \frac{T_d}{2}s + \frac{T_d^2}{12}s^2} \tag{25}$$

The analysis of the current control system is conducted in frequency domain based on the transfer functions derived in section II. The procedure of calculating the performance factors is explained using an example of the conventional PI CC with pole zero cancelation method (1st Design).

For the 1st design, open and closed loop transfer functions represented in frequency domain including the delay are given by (26) and (27), respectively.

$$G_{o.l1d}(j\omega) = \frac{K_0}{\omega} \angle -90 - 2tan^{-1}\frac{0.5\,T_d\,\omega}{1-0.0833\,T_d^2\omega^2} \quad (26)$$

$$|\,G_{c.l1d}(j\omega)| = \frac{\sqrt{\left(1-0.0833\,T_d^2\omega^2\right)^2+(0.5\,T_d\,\omega)^2}}{\sqrt{\left(-0.5T_d\omega^2+K_o-0.0833\,T_d^2\omega^2K_o\right)^2+\omega\left(1-0.0833T_d^2\omega^2-0.5T_dK_o\right)^2}} \quad (27)$$

Equations (26) and (27) are used to determine the performance factors. The phase margin is the difference between system phase angle and the verge of instability -180 at crossover frequency ω_c which can be found from the following condition:

$$|G_{o.l1d}(j\omega_c)| = 1$$
$$\omega_c = K_o \quad (28)$$

From the resultant ω_c, the corresponding open loop phase angle ϕ_{c1} can be calculated as (29):

$$\phi_{c1} = \angle -90 - 2tan^{-1}\frac{0.5\,T_d\,\omega_c}{1-0.0833\,T_d^2{\omega_c}^2} \quad (29)$$

Then, actual phase margin of the current control loop can be found as follows:

$$P.M_1 = 180 + \phi_{c1}$$
$$= \angle 90 - 2tan^{-1}\frac{0.5\,T_d\,\omega_c}{1-0.0833\,T_d^2{\omega_c}^2} \quad (30)$$

It can be observed that the phase angle shown in (29) is a function of the delay angle which enlarges with the frequency of the input signal. Subsequently, the phase angle of the whole system increases until hits the stability limit (-180̊) and sets a value of the gain margin which is defined by the open loop gain at frequency ω_g, at which the system phase angle hits -180̊. Hence, this factor can be calculated from (29) as follows:

$$-180 = -90 - 2tan^{-1}\frac{0.5\,T_d\,\omega_g}{1-0.0833\,T_d^2{\omega_g}^2}$$
$$\therefore \omega_g = \frac{1.58}{T_d} \quad (31)$$

The frequency ω_g can also be evaluated using the exact delay model represented by (2) as follows:

$$-180 = -90 - \omega T_d$$
$$\therefore \omega_g = \frac{1.571}{T_d} \quad (32)$$

From (31) and (32), it can be concluded that the second order pade expansion (25) provides good approximation for the exact delay model (2) .

From (31), the gain margin can be calculated using the equation for magnitude (27) as follows:

$$G.M = -20\log(\frac{K_o}{\omega_g}) \quad (33)$$

The actual system bandwidth ω_{b1} can be calculated from equation (27) as the point at which the absolute value of the closed loop transfer function equals 0.707.

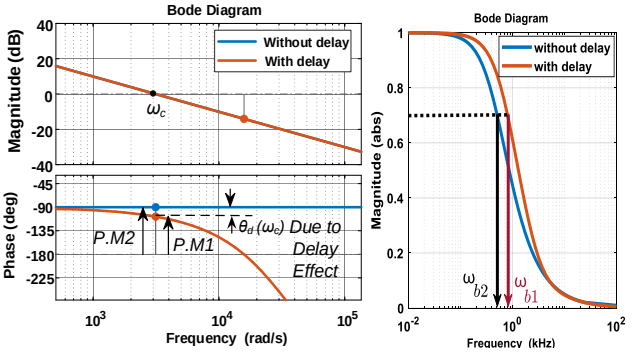
In case of the delay ignorance, it can be seen from (29) that the system's phase angle at $T_d = 0$ has fixed value -90̊. So, the open loop angle does not hit the stability limit -180̊. Consequently, it can be deduced that the system has infinite gain margin.

The aforementioned factors can be explained from Fig. 8 that shows the frequency response obtained by using MATLAB software for open and closed loop functions of 1st design at targeted bandwidth equals 500 Hz and switching frequency equals 15 kHz.

Similar to the analysis above, the performance factors have been calculated for other CCs (2nd, 3rd,and 4th designs). Subsequently, the effect of delay on the system bandwidth is determined using equations (34), where BW refers to the targeted bandwidth and $BW_1 = \omega_{b1}$ for the actual bandwidth (expected after the practical implementation).

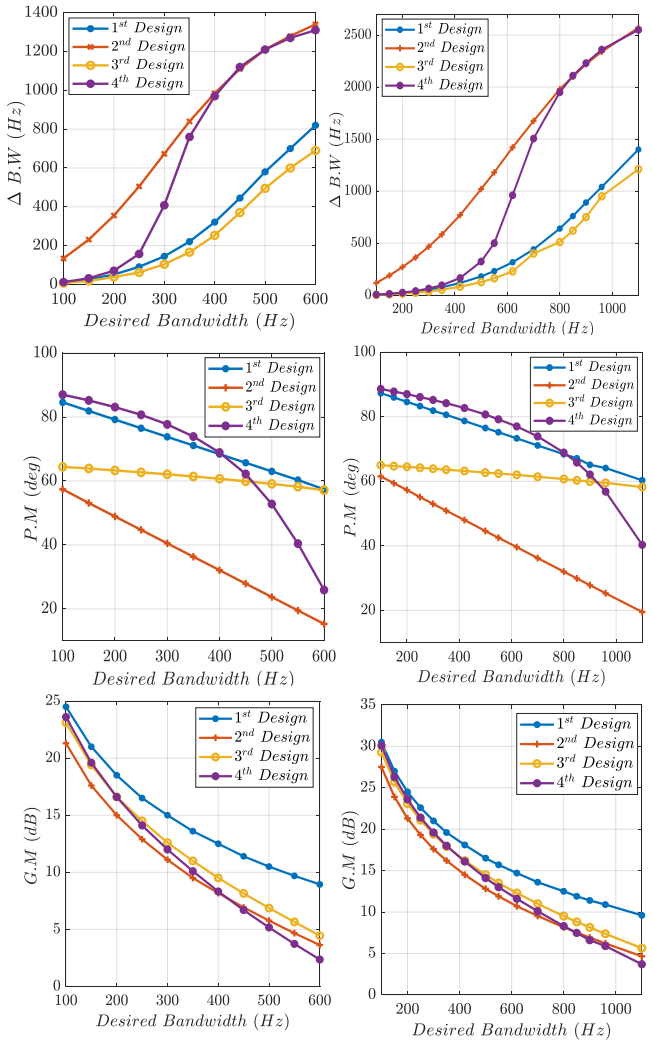
$$\Delta BW = BW_1 - BW \quad (34)$$

The changes in control loop bandwidth and performance factors (*PM* and *GM*) are calculated at different values of the targeted bandwidth. The results are shown in Fig. 9 at two different switching frequencies 10 and 20 kHz (refers to two different delay levels). It can be shown from Fig. 9 that the change of bandwidth has a positive sign and corresponding to (34), it can be deduced that the delay enlarges the system bandwidth. Moreover, it can be observed that phase and gain margins decrease at higher sets of the targeted bandwidth. These effects show the negative impact of the delay on system dynamics especially when high bandwidth is required. Consequently, the desired bandwidth should be chosen in order to achieve reasonable values of the stability margins



(a) Open loop function (b) Closed loop function

FIGURE 8. **Frequency response of the current loop transfer functions**



(a) At fsw=10 kHz (b) At fsw =20 kHz

FIGURE 9. Performance Parameters of current control loop using the frequency response analysis at different switching frequencies

after considering the delay effect, phase margin 40-55^{O} and gain margin 5-6 dB [19, 29].

These margins can be checked by the transfer functions derived in Section II. However, it should be mentioned that, in the current control system of ac machines, there are additional factors that degrade system performance during the operation such as the operating frequency, parameters variation [8, 30, 31]. These factors degrade the system stability during the operation. So, it would be better to tune the CCs to achieve higher stability margins, phase margin 55-65^{o} and gain margins 7-10 dB, to achieve reasonable performance during the machine operation.

For robustness of the CC schemes to the delay effects, from Fig. 9, it can be observed that the minimum change in the current loop system bandwidth happens with the 1st and 3rd designs. For 2nd and 4th designs, the actual system bandwidth is significantly different than its desired value especially for higher bandwidth sets. Consequently, it can be stated that the 1st and 3rd designs have the highest robustness to the delay effect compare to other PI CC schemes.

It can also be noticed that the 1st design has the lowest sensitivity to the targeted bandwidth in terms of the stability effects. It provides better stability margins which refer to better dynamic performance when the bandwidth is set at higher values. On the other hand, the 2nd design is very sensitive to higher bandwidth sets where its stability margins are significantly affected.

As further investigation to differentiate between the dynamic performances of the addressed PI CCs for same electric drive system (same switching frequency which refers to the time delay) and same targeted bandwidth, the concept of delay margin is used to define the maximum time delay that the system can tolerate before going unstable. The formulae to define the delay margin can be derived from Routh stability criterion. The time delay in this derivation is approximated by 1st order Pade approximation (35).

$$G_d(s) = \frac{1 - 0.5T_d\, s}{1 + 0.5\, T_d\, s} \tag{35}$$

It should be noted that the 1st order model for the delay does not provide the same approximation accuracy as 2nd order one which has been used in the previous section. However, the aim of this section to define which CC design can provide a higher delay margin but not to derive an exact delay margin value, i.e., it just represents as an indication factor for the performance comparison, which justifies the acceptance of using simpler 1st order model. The delay margin formula for each CC is derived and summarized in Table 2 where 2nd and 3rd schemes have the same delay margin as they have similar characteristic equations.

The changes of delay margin at different values of the targeted bandwidth *BW* are shown in Fig. 10. It shows that the 1st design has largest delay margin at same targeted bandwidth. Accordingly, for the same targeted bandwidth and same switching frequency, 1st design can provide better stability margins than other CCs. For the other CC schemes, the delay margin of the 3rd design is slightly better than 4th design. These observations from the delay margin study show that the chosen targeted bandwidth for tuning 2nd ,3rd and 4th schemes should

TABLE 2. Delay Margins Formulas

CC SCHEME	Delay Margin (T_{d_margin})
1st Design	$T_{d\_margin} = \frac{2}{K_o}$
2nd Design and 3rd Design	$T_{d\_margin} = \frac{-y + \sqrt{y^2 + 4xz}}{2x}$ $x = 0.25K_i(r - K_p)$, $y = K_iL - 0.5(r^2 - K_p^2)$ $z = -(r+K_p)L$
4th Design	$T_{d\_margin} = \frac{-y + \sqrt{y^2 + 4xz}}{2x}$ $x = 0.25K_i(r - K_2)$, $y = K_iL - 0.5(r^2 - K_2^2)$ $z = -(r+K_2)L$

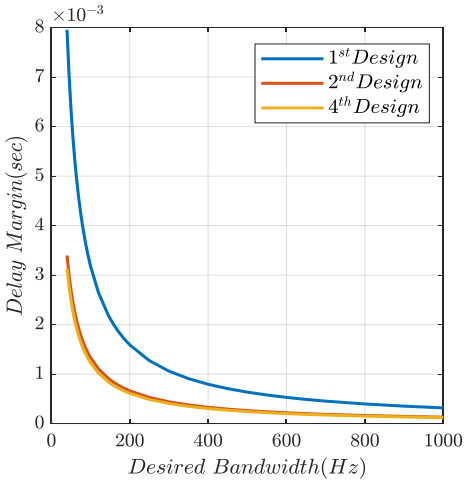


FIGURE 10. Delay Margin change with the desired bandwidth for different types of the CCs

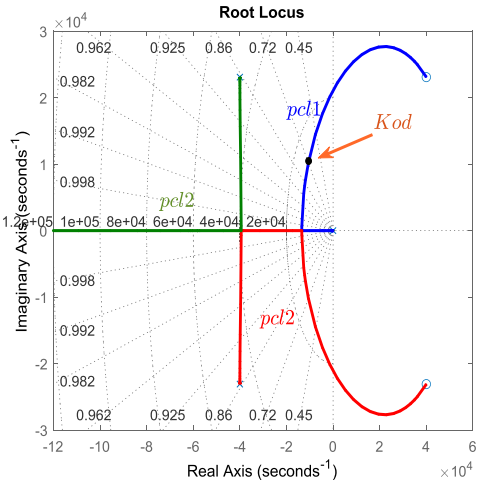


FIGURE 11. Root locus of (36) at 20 kHz switching frequency.

be lower than the value used for the 1st design if same stability margins need to be achieved. Moreover, the targeted bandwidth used for 4th design should be slightly lower than its value for the 3rd design to have same stability margins. These results provide good understanding for tuning these schemes and they have been used to develop a generic recommendation for tuning the PI CCs as presented in Section IV.

IV. Proposed Design Recommendations

The results on Section III show the delay effect on the addressed PI CC schemes and their sensitivity to the targeted bandwidth value used in the tuning process. Accordingly, targeted bandwidth should be carefully chosen to achieve reasonable dynamic performance. To simplify this process, generic formulas have been presented in this section taking the delay effects into account.

For the 1st design, the controller gain K_o (refers to the targeted bandwidth (BW)) in the conventional PI CC with pole zero cancellation can be tuned considering the delay effect based on the root locus of the open loop transfer function represented by (36), where the delay model is represented by (25) in (6) as follows:

$$G_{o.11d}(s) = K_o \frac{1-\frac{T_d}{2}s+\frac{T_d^2}{12}s^2}{s+\frac{T_d}{2}s^2+\frac{T_d^2}{12}s^3} \quad (36)$$

The root locus of (37) can be shown in Fig. 11 at 20 kHz switching frequency. It can be observed that the current control system has three closed loop poles where p_{cl1} and p_{cl2} are considered the dominant poles as the stability margins are determined from their real parts when the value of K_o increases. Subsequently, the controller gain can be tuned using the location of p_{cl1} and p_{cl2} to achieve a certain performance. In order to achieve the strongest disturbance rejection possible with negligible overshoot, the controller should be tuned in order to have an optimal damping ratio (η =0.707) [23]. The proposed setting (K_{od}) can be derived analytically from the symbolic solution for the roots of the characteristic equation (37).

$$T_d^2 s^3 + (6T_d + K_o T_d^2\ )s^2 + (12 - 6K_o T_d)s + 12K_o = 0 \quad (37)$$

The general expressions for the closed loop poles are shown by (38) and (39) [9] as a solution of (37), where f_{sw} is the switching frequency (f_{sw}=1/ T_{sw}).

$$p_{cl1,2} \cong \frac{1}{6}\begin{Bmatrix} \beta[-\beta - 2(K_o + 4f_{sw}) - \beta^2(K_o^2 - 20f_{sw}K_o)] \mp \\ j\left[\sqrt{3}\beta^2 - \beta^3(K_o^2 - 20f_{sw}K_o)\right] \end{Bmatrix} \quad (38)$$

$$p_{cl3} = \frac{1}{3}\left[\beta^2 - \beta(K_o + 4f_{sw}) + \beta^3\left(K_o^2 + 20f_{sw}K_p\right)\right] \quad (39)$$

where

$$\beta = 2f_{sw}\sqrt{\sigma} - K_o^3 - 30f_{sw}K_o^2 - 168f_{sw}^2K_o + 32f_{sw}^3$$

$$\sigma = 9K_o^4 + 504f_{sw}K_o^3 + 6576f_{sw}^2\,K_o^2 - 2688f_{sw}^3\,K_o + 256\,f_{sw}^4$$

At 0.707 damping ratio, the real and imaginary parts of p_{cl1} and p_{cl2} are equal. Therefore, a generic formula for the controller gain K_o can be expressed by (40) from equalizing the real and imaginary parts of (38).

$$K_{od} \cong 0.33\ f_{sw} \quad (40)$$

Considering that f_{sw}=1.5/T_d, the gain and phase margin corresponding to the proposed setting (40) can be evaluated using (30) and (33) from Section II. Accordingly, it can be found that gain and phase margins are 10.1 dB and 61.64^O, respectively. These values guarantee to have acceptable dynamic performance as shown from the step response in Fig.12 at different values of k_o which has been selected as a ratio of the switching frequency.

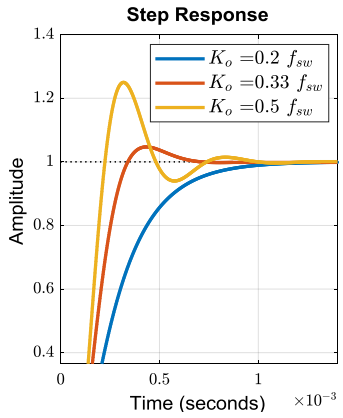
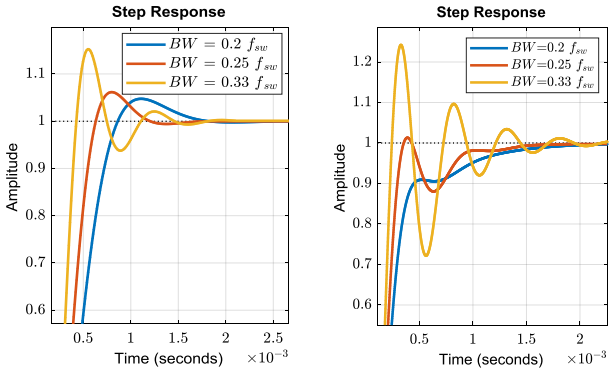


FIGURE 12. Step response using (7) at 16 kHz switching frequency with different controller settings for 1st design CC.



(a) 3rd design (b) 4th design

FIGURE 13. Step response at 16 kHz switching frequency with different controller settings for 3rd and 4th design using (17) and (19) respectively.

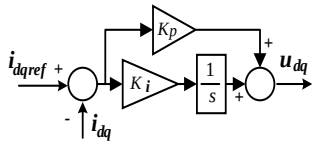
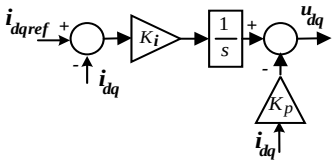
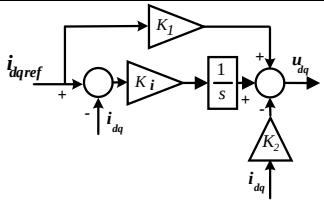
For the other PI CCs (2nd, 3rd and 4th), their targeted bandwidth should be lower than 33% of the switching frequency to provide reasonable performance according to study of their stability margins and delay margins compared to 1st design shown in Section III.

From Fig. 9, the stability margins (GM = 10.1 dB and PM = 61.64^{O}) can be achieved with the 3rd design when its targeted bandwidth set at around 75-85% of the targeted bandwidth of the 1st design. Consequently, the targeted bandwidth of 3rd design can be set at 22-30% of the drive switching frequency to achieve reasonable dynamic performance. For the 2nd design, the chosen targeted bandwidth should be lower than the used in the 3rd design due to the zero effect.

For the 4th design, it can be shown from Fig. 9 that it has a lower gain margin than the 1st and 3rd designs. Moreover, the delay margin of the 4th design is slightly lower than the 3rd design as discussed in Section III. Accordingly, its targeted bandwidth can be around 67% of the proposed ratio for the 1st design. Hence, it can be stated that the 4th design can be tuned for targeted bandwidth (α in rad/s) equals 20-24 % of the drive switching frequency. The step response of the current control loop at 16 kHz switching frequency with 3rd and 4th designs is shown in Fig.13 using the recommended tuning ratios .

The performance factors (overshoot and settling time) for the addressed controllers have been also determined and reported in Fig. 14 at different bandwidth settings. The results show the ability of the 1st design to provide faster dynamics with lower overshoot compared to the other designs. Moreover, it can be noticed that minimum settling time with the 3rd and 4th design occurs within the

TABLE 3. DESIGN GUIDELINES OF SRF PI CC SCHEMES

CC Configuration	PI Controller Structure	Tuning Method	CC Gains	Targeted Bandwidth (BW)
Conventional SRF PI CC (1st Design)		pole/zero cancelation	$K_i = K_o r'$, $K_p = K_o L'$ $K_o = BW$	0.33 f_{sw}
Conventional SRF PI CC (2nd Design)		Pole-placement	$K_p = (2\eta\,\omega_n L') - r'$, $K_i = \omega_n^2 L'$ $\omega_n \cong BW\ (at\ \eta = 0.707)$	(0.17- 0.19) f_{sw}
Modified Conventional SRF PI CC (3rd Design)		Pole-placement	$K_p = (2\eta\,\omega_n L') - r'$, $K_i = \omega_n^2 L'$ $\omega_n \cong BW\ (at\ \eta = 0.707)$	(0.22- 0.3) f_{sw}
2DOF SRF PI CC (4th Design)		pole/zero cancelation based on Pole-placement	$K_i = \alpha^2 L'$, $K_1 = \alpha L'$, $K_2 = (\alpha * 2L') - r'$ $\alpha = BW$	(0.2- 0.24) f_{sw}

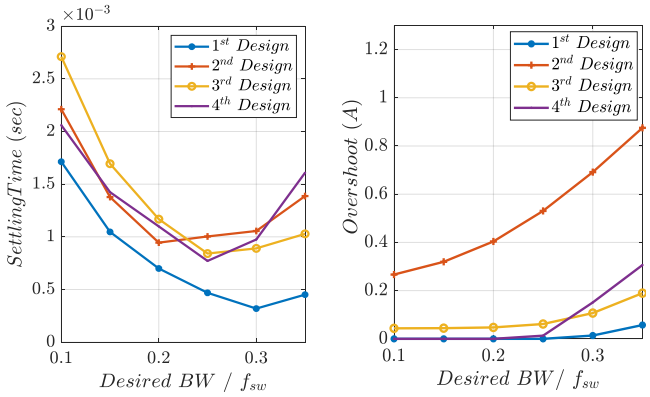


FIGURE 14. Overshoot and settling Time versus the ratio between the desired bandwidth and switching frequency.

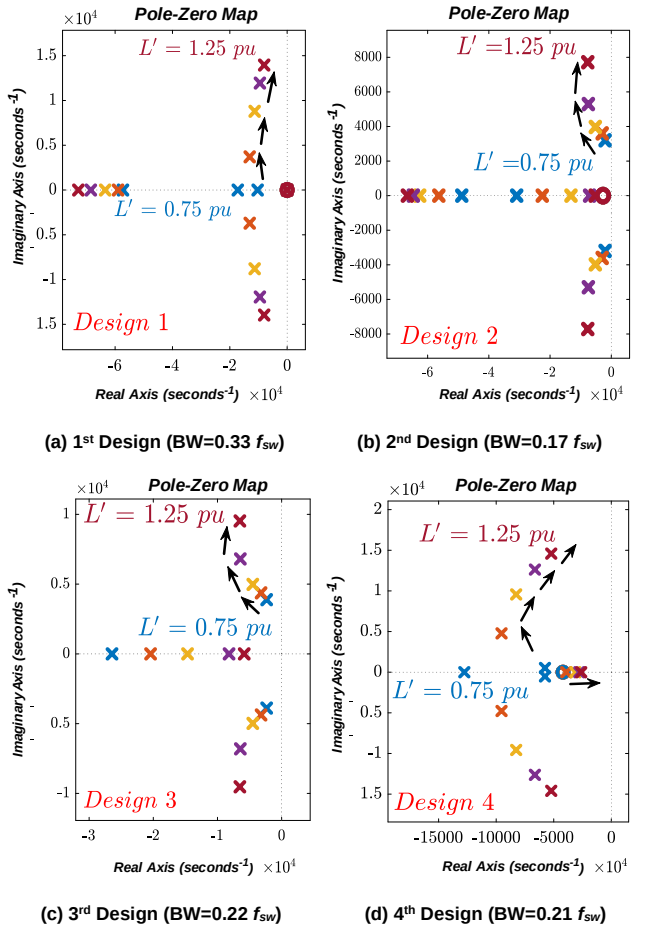
recommended setting which validates the analysis in Section III. To conclude the addressed PI CC schemes and their design recommendations for the gains' selection, they have been summarized in Table 3.

V. Robustness to Model Uncertainties

Tuning guidelines shown in Table 3 depend on the system parameters namely, resistance and inductance values which might be slightly different than their actual values. Therefore, the effects of these uncertainties on the system stability are studied in this section through the analysis of the systems' eigenvalues.

Effects of inductance uncertainties can be shown in Fig. 15. It shows the current control system's eigenvalues when the inductance value used in the controller design has ±25% error. It can be observed from the eigenvalues migration that the proposed design recommendations guarantee system stability even with wide errors in the inductance value . It can also be shown from Fig. 15 that the eigenvalues move away from the real axis at higher inductance sets. Hence, the system bandwidth increases to achieve faster step response.

For the resistance uncertainties, normally the machine resistance increases due to the system heating. As the machine resistance represents a damping element, the system stability margins improve, and the system response becomes slower with lower overshoot. This phenomenon is similar to setting the resistance in the controller to be lower than its actual value [32].



(a) 1st Design (BW=0.33 f_{sw}) (b) 2nd Design (BW=0.17 f_{sw})

(c) 3rd Design (BW=0.22 f_{sw}) (d) 4th Design (BW=0.21 f_{sw})

FIGURE 15. Dominant Eigenvalues migration of current control loop with different inductance sets in the controller's parameters

VI. Experimental Results

The proposed design recommendations and the analytical studies in this paper have been validated using experimental test rig shown in Fig.16. A three phase R-L load (r= 5ohm, L =1 mH) has been used to simulate the three-phase rotating machine and to void the unwanted torque effects [16]. The R-L load is supplied from three level neutral point clamped converter (NPC) at 16 kHz switching frequency. The PI CCs shown in Table 3 have been digitally implemented in a digital signal processor (DSP) (Texas Instrument, TMS320C6713 DSP Starter Kit shown in Fig. 17 using code composer software (CCS). For the digital implementation, discretization of the continuous CCs is required. Various methods can be used to convert the continuous system into an

FIGURE 16. Experimental set up

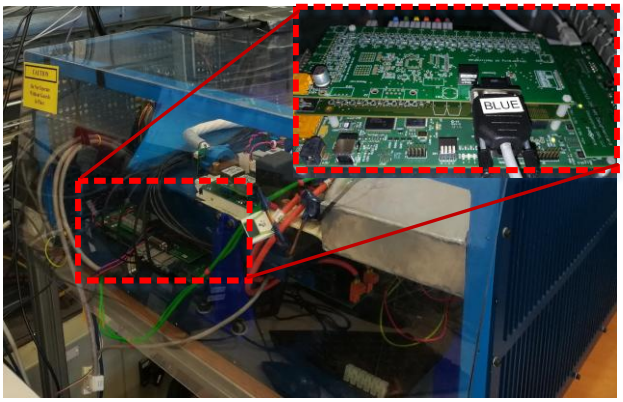


FIGURE 17. **Inverter and Control platform (Texas Instrument, TMS320C6713 DSP Starter Kit)**

equivalent discrete-time system. However, it should be noted, that the continuous system can only be approximated, and the discrete system can never be exactly equivalent. Different methods can result different controller performances. The most important methods are summarized in Table 4 [28, 33]. Among these methods, Tustin transformation is considered the most commonly used method as it allows to maintain same stability properties in both s- and z-domain [28, 34, 35]. Consequently, it has been used to discretize the continuous PI CCs for digital implementation. The dynamic performance of the CCs has been tested by a step response of a 10A as a reference q-current component.

A. Robustness to Delay Effects

The performance dynamics of PI CCs shown in Table 3 have been tested at 350 Hz fundamental frequency as shown in Fig. 18. The desired bandwidth (*BW*) for all PI CCs is selected as a ratio of the drive switching frequency to verify the proposed design recommendations in Section IV and to evaluate the robustness of the PI CC schemes to the time delay effects.

Firstly, it can be seen from Fig. 18 that the 3rd design provides more stable response (less oscillations and lower overshoot) than the 2nd design at same settings which verify the preference of the modified PI structure (3rd design) as discussed in Section II.

It can also be observed that, at high *BW* values, the degradation of the transient response is high with the 2nd and 4th design compared to 1st and 3rd designs. These results refer to higher deterioration in the stability margins of the 2nd and 4th designs compared to the 1st and 3rd designs. The findings from these test results are matching with the analytical results in section III for the frequency response analysis which show the higher robustness of the 1st and 3rd designs for delay effect. Moreover, it can also be observed that the

TABLE 4. **Discretization Methods**

Backword Difference Method	$s = \frac{1}{T_s}(1 - z^{-1})$
Forward Difference Method	$s = \frac{1}{T_s}\left(\frac{1 - z^{-1}}{z^{-1}}\right)$
Tustin (Trapazoidal) Method	$s = \frac{2}{T_s}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)$

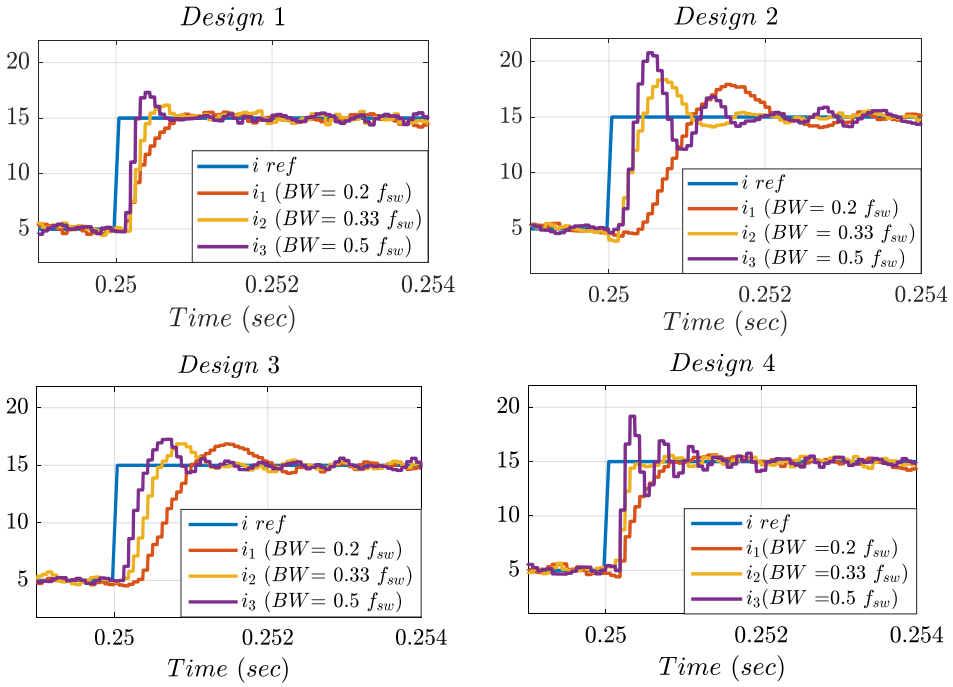


FIGURE 18. **Experimental current responses at different controller's settings**

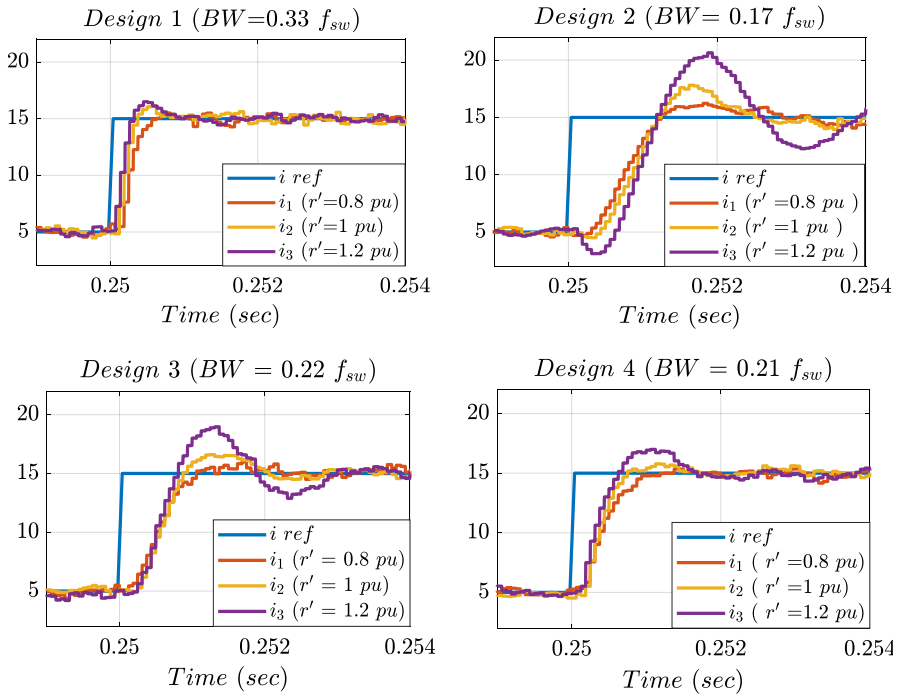


FIGURE 19. **Experimental current responses at different resistance values in controller setting**

1st design provides faster dynamics with better stability margins compared to other CCs at higher bandwidth settings which validates the delay margin study in Section III.

The results also show that the CCs provides reasonable dynamics in terms of negligible overshoot with fast response when the proposed design recommendations in Table 3 are used. These results validate the proposed setting in Section IV which can be used as a fast and simple tuning tool in the industry. The results also show that higher setting for the desired bandwidth degrades the system stability and affects the system performance.

B. Robustness to Model Uncertainties

The robustness of PI CCs to the model uncertainties has been tested when the proposed design recommendations are used. It is assumed that there are errors in the system

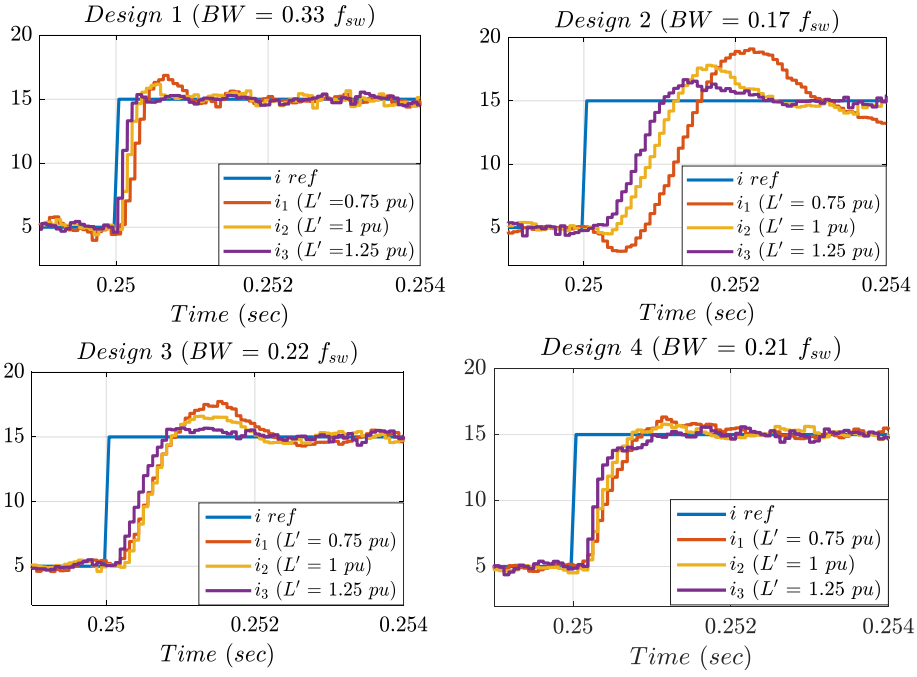


FIGURE 20. **Experimental current responses at different inductance values in controller setting**

parameters (resistance and inductance) used in the controller's setting. The effects of resistance and inductance uncertainties on the system dynamics are tested as shown in Fig. 19 and Fig. 20, respectively. For the resistance effects, it is assumed that there are ±20% error in the resistance value used in the controller setting. The experimental results show that the design recommendations provide reasonable dynamics with large errors in the system resistance. The results also show that lower resistance setting enlarge the damping ratio as it is similar to the case of heating the machine.

For the inductance errors, it is assumed that there are ±25% errors for the inductance value used in the controller setting. The results in Fig. 20 show that the design recommendations guarantee higher stability margins for the addressed CCs during the tuning process with wide errors in the inductance value. It can be also be observed that higher inductance settings provides faster step response which validates the eigenvalues study in Section V. The results also show that the 1st design provides high robustness to the model uncertainties compared to other schemes which can be interpreted by its high stability margins shown in Section III and V.

VII. Conclusion

This paper investigated different tuning configurations of the SRF PI CCs which have not consider the delay effect on their tuning rules. The paper also analyzed and evaluated the effect of computational and modulation delays on their dynamic performance. Generic recommendations for tuning these PI CCs, which are summarized in Table 3, have been proposed as a function of the drive system's switching frequency.

It can be concluded that the classical PI controller tuned by pole zero cancelation method (1st design) provides the highest robustness to the delay effects in terms of achieving the targeted bandwidth with higher stability margins. It is advised to set its gain (targeted bandwidth (*BW*)) at 33% of the drive system's switching frequency. The proposed setting achieves gain and phase margins equal 10.1 dB and 61.64^{O} respectively which provides fast dynamic response with negligible overshoot corresponding to 0.707 damping ratio. For the modified PI controller tuned by pole placement (3rd design), it is advised to set its targeted bandwidth at 22- 30 % of the drive switching frequency whereas this ratio is 20-24 % for the 2DOF PI controller with pole placement method (4th design). These settings guarantee reasonable dynamic performance for the addressed CCs and represent fast and simple tuning rules for the electric drives in the industry. These claims have been validated through experiments.

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