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OPTIMISATION OF THE GATE VOLTAGE IN SiC MOSFETS: EFFICIENCY VS RELIABILITY

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Abstract

This paper presents a comprehensive study of the impact of the gate voltage on the switching and ON-state performance of SiC MOSFETs. It is well known that the gate oxide in SiC MOSFETs is not as reliable as that in silicon MOSFETs due to increased fixed oxide and interface traps. Numerous studies have shown reduced performance on time-dependent dielectric breakdown (TDDB) and oxide robustness in SiC MOSFETs compared to silicon devices. On the one hand, a high ON-state gate-source voltage V_{GS} is required for proper channel inversion, low ON-state loss and fast switching while on the other hand, a lower ON-state V_{GS} reduces the electrical stress on the gate oxide and improves long term reliability. Understanding the implications of the selected gate voltage on the operation of the power device will be fundamental for achieving an optimal balance between electrical performance and gate oxide reliability. This paper shows that reducing the maximum gate driver supply voltage V_{GG} only affects turn-ON losses while turn-OFF losses are independent of V_{GG}. The experimental characterisation is complemented with electrothermal simulations to evaluate the impact of the gate voltage on the operation of a converter. The paper shows that reducing V_{GG} by 10% causes an increase of 7.6 % in the device losses and 1.4 °C in junction temperature in simulated converter operation. Furthermore, if the switching speed is increased by means of reducing the gate resistance, the impact of the conduction losses can be compensated. These results are fundamental for balancing system efficiency and reliability in SiC MOSFETs.

1 Introduction

The reliability of the gate oxide of SiC MOSFETs remains a challenge, compared with their silicon counterparts. The presence of carbon atoms results in a higher interface trap density at the gate dielectric interface. This increased trap density, together with the lower band offsets in the SiC/SiO_2 interface have reliability implications in the case of SiC MOSFETs [1-4]. Due to negative charge trapping, a positive gate voltage stress will cause a positive threshold voltage (V_{TH}) drift (Positive Bias Temperature Instability -PBTI). A negative gate voltage stress will cause a positive charge trapping, hence a negative threshold voltage shift (Negative Bias Temperature Instability - NBTI). These shifts of V_{TH} will have an impact on the operation (PBTI will cause an increase of the on-state resistance [1, 5] whereas NBTI can have catastrophic implications in the case of uneven V_{TH} shift among parallel devices [6]), hence, it is important to select the appropriate gate driver voltage, balancing the gate voltage stress, together with the power device losses and converter efficiency.

Analysing the latest datasheet of different SiC MOSFETs, the manufacturers make a clear distinction between the maximum gate voltage, recommended and operational gate voltage, recommending turning-OFF the MOSFETs with a gate voltage of 0 V or a very low negative gate voltage. This highlights the importance of analysing the most suitable gate driver voltage, balancing the trade-off between gate oxide reliability and converter efficiency. Accelerated stress tests are a suitable tool for evaluating the impact of V_{GS} stress on threshold voltage in MOS gate devices, like MOSFETs and IGBTs. The evaluated Si IGBT is a device with datasheet reference RGTH40TS65 from Rohm, whereas the evaluated SiC MOSFET is a 900V device with datasheet reference C3M006590 from Wolfspeed. The transfer characteristics in Fig. 1, show that BTI is present in the SiC MOSFET, and increases with gate voltage value, whereas the IGBT transfer characteristics in Fig. 2 show no shift in V_{TH}, even in the case of a higher gate voltage stress. The gate stress for the Si IGBT was +40 V at 150 °C during 1 hour, with characterisation before stress and after 5 hours relaxation at V_{GS}=0 [7]. For the SiC MOSFET, the stress was cumulative, increasing the gate voltage in different stages, as indicated in Fig. 2. The stress time was 30 minutes and the transfer characteristics were measured after each stress step, following a relaxation time of 16 hours [8]. More details about the stress circuit and measurements are available in [7, 8].

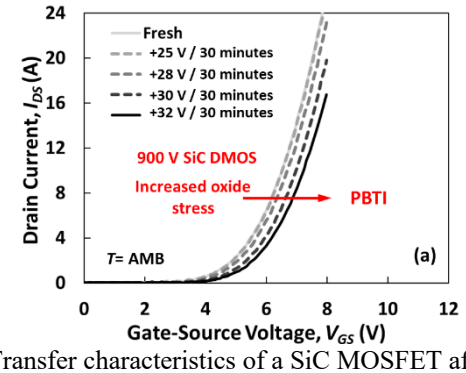

Fig. 1. Transfer characteristics of a SiC MOSFET after positive gate voltage stress [7]

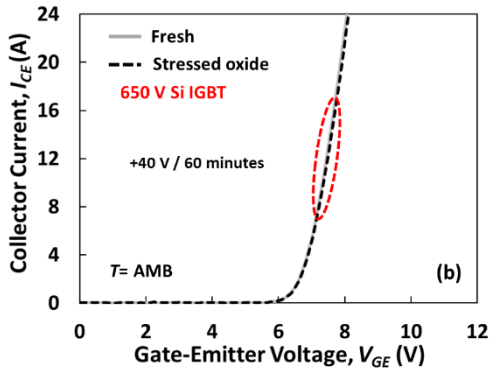

Fig. 2. Transfer characteristics of a silicon IGBT after positive gate voltage stress [8]

Reducing the maximum gate driver voltage reduces the electric field across the gate oxide, assuming the gate oxide thickness is constant. The Fowler-Nordheim tunnelling current density (J_{FN}) is related to the electric field across the oxide (E_{OX}) according to (1) [4].

$$J_{FN} = AE_{OX}^2 e^{-\frac{B}{E_{OX}}} \quad (1)$$

Hence, a reduction of E_{OX} will not only reduce tunnelling currents but also improve oxide reliability [9-11]. This is particularly relevant for SiC given the poorer oxide interface compared to silicon. However, there is a trade-off as reducing the maximum gate drive voltage has a negative impact of increasing ON-state resistance.

In the case of SiC MOSFETs, the channel resistance R_{CH} plays a fundamental role in the total ON-state resistance of the SiC MOSFET [11]. In SiC MOSFETs, due to high critical electric field, the drift resistance R_{DRIFT} is lower, hence, the channel resistance is a greater proportion of the total resistance. For the MOSFET to operate with low losses, the channel must be properly inverted and a high V_{GS} is required to do this [12], as (2) indicates.

$$R_{CH} = \frac{L_{ch}}{W\mu C_{OX}(V_{GS} - V_{TH})} \quad (2)$$

This is not the case of silicon devices where majority of the resistance is the drift resistance. Hence, in SiC MOSFETs, the impact of V_{GS} on the ON-state resistance is more pronounced compared to silicon devices. The balance between the reliability of the gate oxide and the device performance can be fundamental for SiC-based power electronics, hence the special attention must be paid to the selection of the gate voltage.

In this paper, the impact of reducing the drive voltage by 10% on the ON-state and dynamic performance of the SiC MOSFET C3M0065090 has been investigated. Section 2 evaluates the impact of the gate driver voltage on the ON-state losses, the switching performance and switching losses. Section 3 presents the case study of a grid-connected converter, where a simulation model is used for evaluating the impact of reducing the gate voltage on the efficiency and junction temperature. Section 4 presents some reliability remarks, based on the results of the studies presented in this paper and section 5 concludes the paper.

2. Impact of gate driver voltage on the performance of SiC MOSFETs

2.1 ON-state performance and gate driver voltage

The total ON state resistance $R_{DS\text{-}ON}$ of a MOSFET is defined by the sum of the different parasitic resistances of the elements of the MOSFET. In the case of a planar SiC MOSFET, the total $R_{DS\text{-}ON}$ can be approximated by (3), where the different elements are the channel resistance R_{CH}, the JFET region resistance R_{JFET} and the resistance of the drift region R_{DRIFT}.

$$R_{DS-ON} = R_{CH} + R_{JFET} + R_{DRIFT} \quad (3)$$

As mentioned in Section 1, in the case of a planar SiC MOSFET the channel resistance R_{CH} plays a fundamental role in the total ON-state resistance, especially for devices rated below 3300 V [13] and it is dependent on the gate driver voltage used for turning-ON the MOSFET. The impact of the gate voltage on the ON-state performance of the device can be studied using the circuit shown in Fig. 3. It consists of a constant DC current pulse I, with a test duration controlled by an auxiliary switch while the device under test (DUT) is ON at a defined gate voltage $V_{GS\text{-}ON}$. This test can also show the temperature coefficient of the ON-state resistance since if the pulse is long enough for self-heating of the DUT, thereby changing the ON-state resistance. A large aluminium block was used as a heatsink to reduce the total thermal resistance and keep the self-heating at acceptable levels for this study. The results for DC heating pulses of 10 and 20 A, at gate voltages of 13.5 and 15 V are shown in Fig. 4.

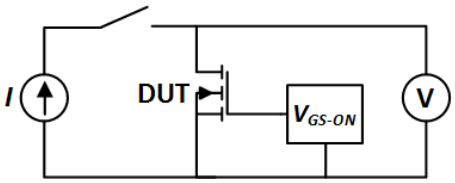

Fig. 3. DC current heating test circuit [14]

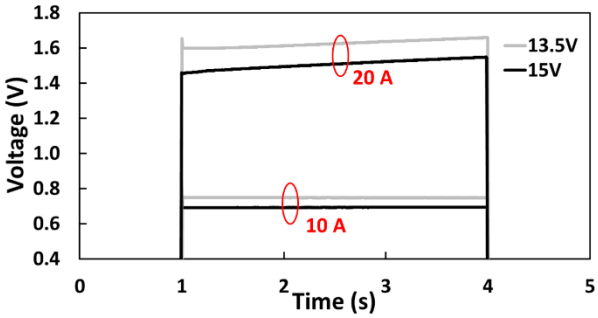

Fig. 4 Impact of gate voltage on the ON-state voltage during a DC current pulse

Fig. 4 shows how reducing the gate voltage has a clear impact on the ON-state performance of the SiC MOSFET. For a current of 10 A, a reduction of 10% on the gate source voltage

is reflected in approximately an increase of 8.6%, whereas for a current of 20 A, before the self-heating affects the ON-state resistance, the increase of resistance is around 10.3%.

2.1 Switching performance and gate driver voltage

The switching performance of a SiC MOSFET can be evaluated using a conventional double pulse test setup, as shown in Fig. 5. The switching characteristics can be measured for different DC link voltages, load currents and junction temperatures. The design allows to characterise the impact of varying the gate driver voltage and the gate resistance R_G. This can be fundamental for assessing the impact of reducing the gate driver voltage on the switching performance.

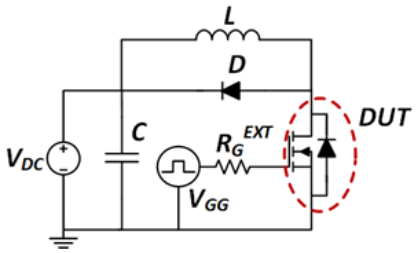

Fig. 5. Double pulse test circuit [14]

Fig. 6 shows the impact of reducing the gate voltage on the turn ON and turn-OFF switching transients of the evaluated SiC MOSFET. The gate driver voltages were 13.5 V and 15 V and the gate resistance was 100 Ω in both cases. The DC link voltage of 400 V, the load current of 20 A and a Schottky barrier diode was the selected freewheeling diode *D*.

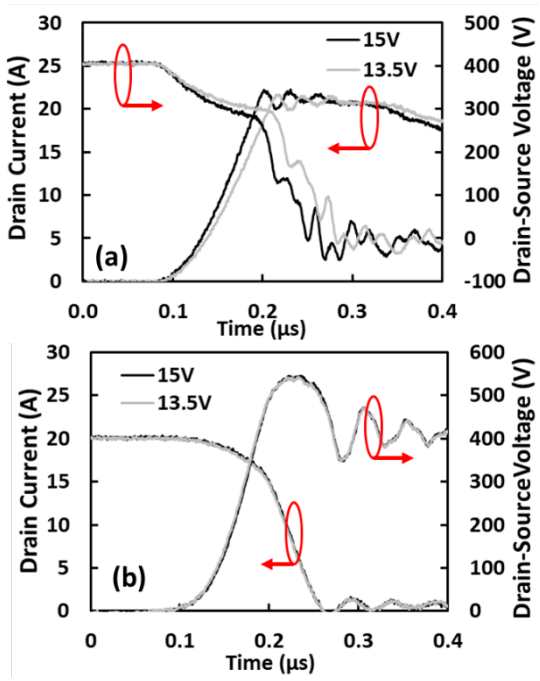

Fig. 6. Impact of gate voltage on the switching transients. (a) Turn-ON, (b) Turn-OFF

The main observation from the switching measurements was that then turn-ON transients are affected by the gate driver voltage, whereas the turn-OFF transients are gate driver voltage invariant. Voltage transitions in power MOSFETs from high to low (during turn-ON) and low to high (during turn-OFF) occur during the charging and discharging of the Miller capacitance (C_{GD} capacitance between the gate and the drain of the MOSFET), which occurs at the Miller plateau voltage V_{GP} [15] During turn-ON, the switching rate of the voltage is determined (4).

$$\frac{dV_{DS}}{dt} = -\frac{V_{GG} - V_{GP}}{R_G C_{GD}} \tag{4}$$

During turn-OFF, the gate drive output voltage is 0 V and the switching rate of the voltage is determined by (5)

$$\frac{dV_{DS}}{dt} = \frac{V_{GP}}{R_G C_{GD}} \tag{5}$$

Analysing (4) and (5) it is clearly observed how the gate driver voltage V_{GG} will have an impact on the turn-ON transient but not on the turn-OFF transient of the drain-source voltage.

The drain current I_D transient during turn-ON and turn-OFF is given by (6) [15], where g_m is the transconductance.

$$I_D = g_m[V_{GS}(t) - V_{TH}] \tag{6}$$

The switching rate of the current is thereby controlled by the gate voltage. During turn-ON, the current transient occurs when the gate voltage rises from V_{TH} to V_{GP} and its transient is given by (7). The turn-OFF transient of the current occurs when the gate voltage reduces from V_{GP} to V_{TH} and its transient is given by (8).

$$V_{GS}(t) = V_{GG}\left(1 - e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}\right) \tag{7}$$

$$V_{GS}(t) = V_{GP}\left(1 - e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}\right) \tag{8}$$

Similarly to the drain-source voltage analysis, evaluating (7) and (8) it can be concluded that the gate driver voltage does not affect the turn-OFF transient of the drain current. This is clearly shown in the turn-OFF gate transients shown in Fig. 7, where the V_{GP} during turn-OFF is identified.

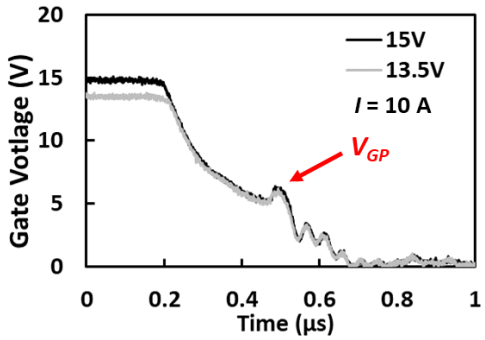

Fig. 7.Impact of V_{GG} on gate voltage turn-OFF transients

The measured turn-ON *dI/dt* and turn-OFF *dV/dt* of the SiC MOSFET driven at its rated V_{GG} voltage and 90% of its rated value are shown in Fig.8 and Fig. 9 respectively.

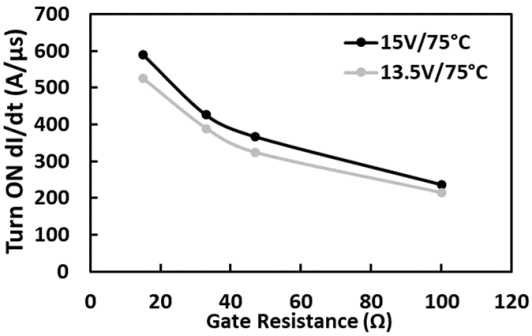

Fig. 8 Impact of V_{GG} on the drain current switching rate during turn-ON. Load current: 20 A

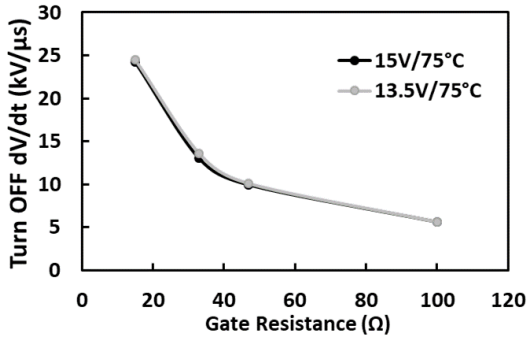

Fig. 9 Impact of V_{GG} on the drain-source voltage switching rate during turn-OFF. Load current: 20 A

The measurements in Fig. 8 and Fig. 9 were done at 75°C, for a load current of 20 A, with different gate resistances R_G ranging from 15 Ω to 100 Ω. From the double pulse test waveforms, the switching energies can be calculated and the penalisation of reducing the gate voltage on the switching efficiency can be quantified. Fig. 10 shows the measured switching energies for a temperature of 75 °C and load current of 20 A.

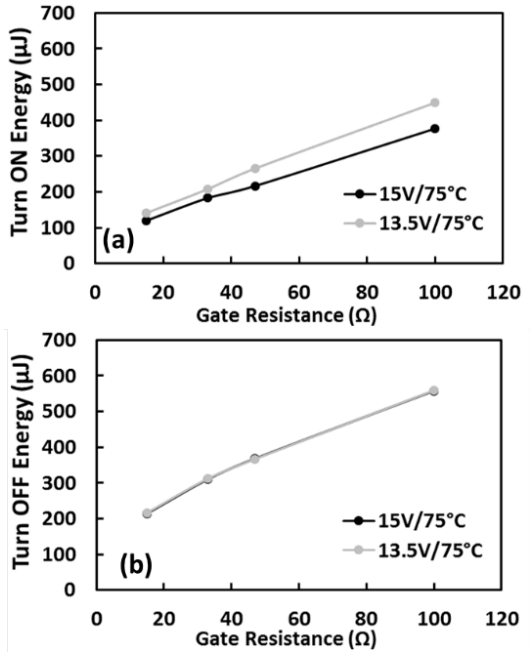

Fig. 10 Impact of V_{GG} on the switching losses. Load current: 20 A. Temperature: 75 °C

Fig. 10(a) shows the turn-ON switching increases by an average of 18 % as V_{GG} is reduced by 10%. During turn-OFF, as shown in Fig. 10(b), the switching energy is independent of the gate driver voltage. Hence, the switching energy penalty for reduced V_{GG} is only during turn-ON. The switching energies were measured at different temperatures and the results in Fig. 11, measured at 150 °C show that the trends are similar at high temperature.

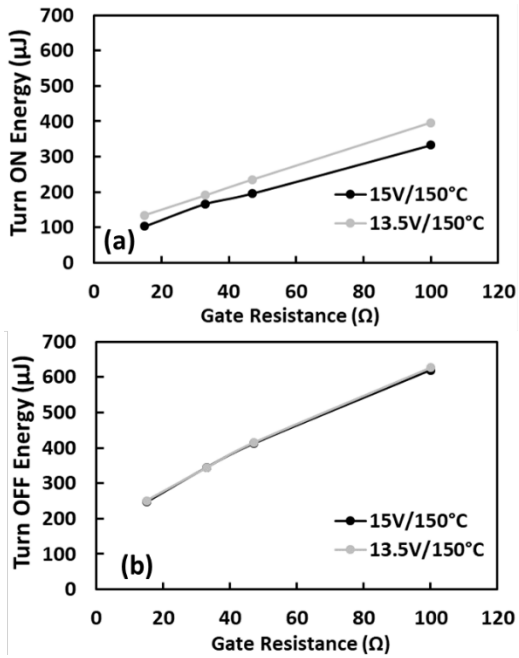

Fig. 11 Impact of V_{GG} on the switching losses. Load current: 20 A. Temperature: 150 °C

3 Case study: Grid-connected converter

The electrical performance of the power MOSFET at different gate driver voltages has been evaluated using the simulation of a grid-connected converter. The model is shown in Fig. 12. The converter is connected to the grid using an inductive filter and the operating conditions are DC link voltage 400 V, switching frequency 20 kHz and mains frequency 50 Hz. The peak output current is 20 A and the power of the converter is 4.8 kW, purely active power. The schematic of the simulated circuit is shown in Fig. 11

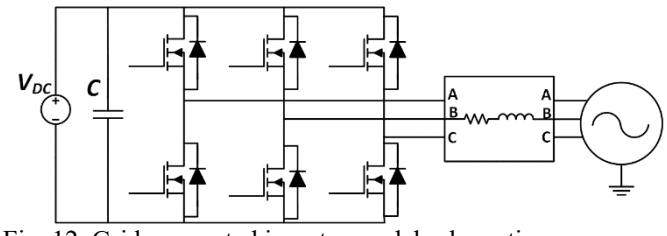

Fig. 12. Grid-connected inverter model schematic

The simulation model was implemented in Matlab/Simulink and it is fully electro-thermal [16]. To account for the conduction losses and its temperature and gate voltage dependency, the $R_{DS\text{-}ON}$ values have been extracted from the SiC MOSFET datasheet, whereas the switching losses have been characterised for a set of temperatures (25, 75 and

150 °C), load currents (10 and 20 A) and gate resistances (15, 33, 47 and 100 Ω), using the double pulse test setup defined in section 2. The measurements were performed using gate voltages of 15 V and 13.5 V and the temperature was adjusted using a small DC heater attached to the device. The thermal model of the device was developed using the Cauer network parameters provided by the manufacturer. The ON-resistance and switching energy values were populated into a look-up table and allow the evaluation of the varying the gate voltage in the converter operation. The model uses the sequence shown in Fig. 13 for updating the dependency of the conduction and switching losses on the current and temperature [16]. The output current of the converter is shown in Fig. 14

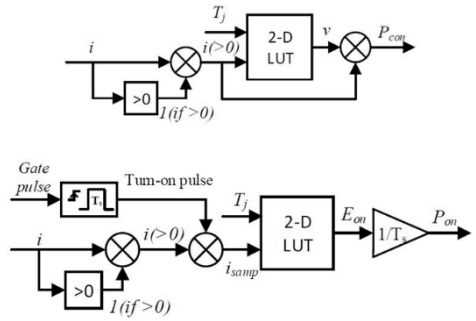

Fig. 13. Temperature dependent loss calculation [16]

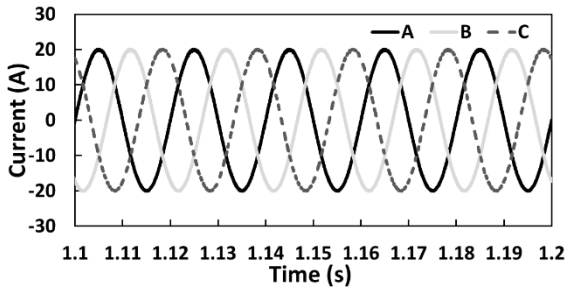

Fig. 14. Output currents of the modelled grid connected converter

Using the model defined previously, the average conduction and switching losses, together with the resulting junction temperature excursion during operation, have been calculated for a combination of gate driver voltages (namely 13. 5 V and 15 V) and gate resistances (namely 15 Ω and 33 Ω). The objective is assessing the impact of reducing the gate driver voltage on the converter performance and the results of the simulations are summarised in Table I. The junction temperature during operation is shown in Fig. 15 and Fig. 16.

Table I: Impact of reducing the gate driver voltage V_{GG} and gate resistance R_G on converter operation.

	V_{GG} = 15 V R_G=33 Ω	V_{GG} = 13.5 V R_G=33 Ω	V_{GG} = 13.5 V R_G=15 Ω
Conduction losses (W)	35.84	39.05	38.94
Switching losses (W)	17.15	17.97	12.46
Delta T_J (°C)	14.2	15.3	13.9
Peak T_J (°C)	78.2	79.6	77.8

First, it is important to compare the performance of the converter if only V_{GG} is reduced, keeping R_G constant. According to the results in Table I reducing V_{GG} a 10% translates into an increase of 7.6 % on the total losses and a peak junction temperature increase of 1.4 °C, assuming a fixed case temperature T_{CASE} of 60 °C. This is clearly observed in the junction temperature transients during operation in Fig. 15.

An option for improving the performance of the converter and minimise the impact of reducing the gate voltage on switching loses can be reducing both the V_{GG} and R_G. Table I shows the result of reducing the gate voltage to 13.5 V and the gate resistance to 15 Ω. Comparing with the original combination of 15 V/33 Ω, the penalisation in conduction losses (8.6%) is compensated with an improvement in the switching losses (-27.3%) and the overall losses reduce a 3%. This is reflected in the junction temperature excursion and peak junction temperature, which have reduced 0.3 °C and 0.4 °C respectively, as can be observed in Fig. 16.

Another option can be using an auxiliary capacitor for boosting the switching transients like in [17], respecting the maximum peak transient gate voltage of the device and keeping the reduced gate voltage during the ON-state.

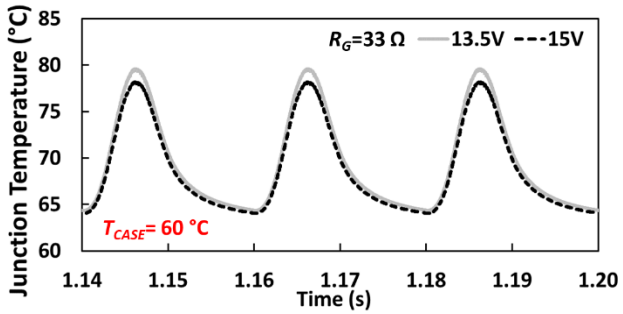

Fig. 15. Simulated junction temperature excursion for V_{GG} 13.5 and 15 V. Gate resistance R_G = 33 Ω

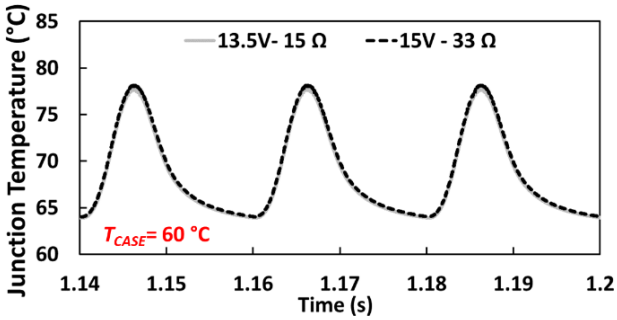

Fig. 16. Simulated junction temperature excursion for V_{GG} =13.5 V/R_G=15 Ω and V_{GG} =15 V/R_G = 33 Ω

4 Reliability remarks

The results in the previous section quantify the impact of reducing the gate driver voltage on the performance of the converter. It is important to remark that while reducing the gate oxide stress by means of reducing the gate voltage will have a positive impact on the oxide reliability and lifetime [9], the higher operating temperatures and junction temperature excursions will have a negative impact on lifetime.

Regarding the higher temperature of operation, in [18] it is shown that higher average junction temperatures and larger junction temperature excursions have a negative impact on the lifetime during power cycling. Most of the lifetime models have been developed for silicon and not for SiC power devices. Models specifically developed for SiC will be fundamental for obtaining more accurate lifetime predictions, especially for new packaging alternatives. Moreover, lifetime predictions have to be analysed carefully, as they are always based on accelerated stress tests.

Considering the oxide reliability, using the data for the C3M006590 presented in [9], reducing the gate voltage shows an improvement on the oxide lifetime. However, the impact of the threshold voltage shift caused by PBTI [1-3] should also be considered as part of the final reliability analysis, as it will affect the losses and resulting junction temperature [5, 7, 19]. The impact of small differences in stresses may be difficult to quantify, especially considering the statistical dispersion in the gate oxide reliability shown in [1]. The role of the gate voltage on the temperature coefficient of the ON-state resistance [12] will have to be evaluated in the case of parallel-connected MOSFETs, to ensure the operation in a positive temperature coefficient region.

5 Conclusion

This paper has investigated the impact of the gate driver voltage V_{GG} in the performance of SiC MOSFETs and its reliability implications. This will be fundamental for achieving an optimal balance between electrical performance and gate oxide reliability. It is shown that reducing the stress on the gate oxide by means of decreasing V_{GG} only affects turn-ON losses while turn-OFF losses are independent of V_{GG}. Simulation models show that the increase of conduction losses can be balanced if the switching losses are reduced, hence the SiC MOSFETs are subjected to similar junction temperature excursions. This should translate in an improved lifetime and reliability of the power device. Further studies should assess the impact of PBTI on the conduction and switching losses, as reducing the gate driver voltage can have a positive impact on the device performance.

6 Acknowledgements

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