Role of Interface in Ferroelectric Polymer based Memory Diodes

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Abstract

Organic electronic devices have the potential to alter our everyday lives with their unique characteristics, such as flexibility, stretchability and low-cost. Among the envisioned devices are non-volatile memories for applications in contactless identification transponders and smart labels. This thesis investigates the operation of such a memory device that uses phase-separated blends of a ferroelectric and semiconducting polymer in a diode configuration. The blend film is composed of columns of semiconductor domains that run continuously through the ferroelectric polymer matrix from the bottom to the top electrode. Polarization of the ferroelectric polymer upon application of appropriate electric fields (greater than coercive field), leads to the modulation of the injection barrier at the metal-semiconductor contact.[28] The diode exhibits a bistable rectifying current-voltage characteristic. Numerical models have been proposed to describe the device physics of the memory diodes.

This thesis provides a potential solution for ambient processing and operation of the memory diodes along with providing the experimental proof of the proposed operation mechanism of the memory diodes. Moreover, current driven memory devices have been demonstrated.

Based on tuneable injection barrier, MEMOLED, a light emitting diode with an inherent ferroelectric switch, has been demonstrated. The advantage of a built-in rectifying switch in the construction of the MEMOLED is to present a non-emissive OFF state and an emissive non-volatile ON state. However, the current efficiency is low as compared to that of pristine semiconductor polymer based OLEDs, and the retention time of the emissive state is short. Here, it is shown that charge trapping in the ferroelectric phase could be a possible reason for the lower performance of the MEMOLEDs. Finally, organic ferroelectric tunnel junctions, based on ultra-thin film of P(VDF-TrFE), with colossal tunneling electroresistance are demonstrated.

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Chapter 1

Introduction

An electronic world is what we live in today. The electronic technology positively impacts health, economy and national security. The manufacturing, usage and the disposal of the resources and methodologies needed for these electronic devices, however, negatively impacts the environment. Therefore, an eco-friendlier and cost-effective solution can be offered by the use of organic materials. Moreover, organic materials like polymers and small molecules with unique structures and properties can also offer great potential of novel functionality, competing well with silicon-based devices in flexible applications.[1]

1.1 Motivation

Organic materials offer unique characteristics such as flexibility, softness and stretchability, in sharp contrast to inorganic materials such as silicon.[2] Field of applications of organic materials range from flexible displays[3], artificial skin[4], information and communication[5], wearable electronics[6], to medicine and biomedical research[7]. For example, a major share of the global market of smartphones is occupied by OLED based displays. The new age OLED TVs introduced by Samsung and LG Electronics not only exhibit very high resolution and sharper colour contrast but are also thinner, lighter and much more energy efficient. Organic photovoltaics (OPVs) offer another exciting application of organic electronics.

The most advantageous characteristics of organic materials is solution processing and compatibility with printing and coating techniques, which enables cheap and large-area manufacturing.[8, 9] For example, roll-to-roll manufacturing of solar cell panels would lead to an increase in the throughput at reduced costs. Thus, printed flexible electronics are a part of key future technologies which have the potential to alter our everyday lives.[10, 11]

Memory is a prerequisite for many of the envisioned applications of organic (flexible) electronics such as contactless identification transponders[12, 13] and smart labels[14]. Operation of memory devices make use of the physical property of 'hysteresis' as a result of an applied electric field. The simplest device structures make use of the charging and discharging of capacitors to store information. However, the disadvantage of capacitor technology is leakage of charge, which necessitates restoration of information at regular time intervals.[15] In addition, implementation of such capacitive structures in integrated circuits leads to destructive read-out of the information.[16] This volatility of memory is, in particular, unsuitable for technologies such as RFID (Radio Frequency Identification) tags which use radio frequency for transmission of stored information and, thus, do not have a constant power supply to perform a memory refresh every time.[17]

Finding a non-volatile rewritable memory device is the focus of the active research in the field of memory technology. Some of the many memory technologies being investigated are metal-organic semiconductor-metal junctions[18, 19], ferroelectricity[15], charge-trapping effects in field-effect transistors[20-22], and electro-mechanical switches[23]. Phase-separated blends of ferroelectric and semiconductor polymers have emerged as a potential candidate for realizing memory devices. Poly(vinylidene fluoride co-trifluoroethylene) (P(VDF-TrFE)) is the most common organic material used as the ferroelectric polymer, whereas, various organic

semiconductors ranging from polymers to small molecules have been used as the semiconductor.[24-26] The blend film is sandwiched between two electrodes. The phase-separated morphology is because of spinodal decomposition, wherein columns of semiconductor domains run continuously through the ferroelectric polymer matrix from the bottom to the top electrode.[28] Polarization of the ferroelectric polymer upon application of appropriate electric fields (greater than coercive field), leads to the modulation of the injection barrier at the metal-semiconductor contact.[28] Current densities corresponding to different polarization states ("up" or "down") can be assigned to individual Boolean logic values ("1" or "0"). This information can be then non-destructively read-out at lower voltages (less than coercive field).

1.2 P(VDF-TrFE) based memory devices

Many solution-processed organic memory devices have been demonstrated so far. The first non-volatile resistive memory with a bistable rectifying current-voltage characteristics was demonstrated by Asadi *et al.* using phase separated blend films of ferroelectric polymer, P(VDF-TrFE) and semiconductor polymer, rir-P3HT [regio-irregular poly(3-hexylthiophene)]. Polymer blends phase separate due to the low enthalpy of mixing and small entropy gain.[27] The P(VDF-TrFE):rir-P3HT film sandwiched between Ag and LiF/Al electrodes forms the diode device layout. The Ag electrode forms an injection barrier of 0.6-0.7 eV with rir-P3HT HOMO (highest occupied molecular orbital) creating a hole injection limited contact. The LiF/Al contact is a blocking contact for both hole and electron injection. The injection barrier at Ag/rir-P3HT is modulated as the ferroelectric polarizes on application of voltage.[28] Schematic of a typical device structure is shown in Figure 1.1a, along with the *I-V* characteristic illustrating the switching effect shown in the Figure 1.1b. On application of positive bias on the bottom electrode, the ferroelectric is polarized and the charges induced from the metal-semiconductor junction compensates the polarization charges lowering the injection barrier via band bending. This leads to space charge limited charge conduction in the device.[15] On the other hand, in the negative bias, the top contact, being blocking in nature, remains injection limited as the polarization charges are not sufficient to decrease the injection barrier. This results in a rectifying diode. The current remains low (OFF state) at low positive voltages but increases significantly when the coercive voltage of the ferroelectric is reached and the dipoles switch, putting the device in the ON state. This low resistance ON state can be read-out at low voltages (green curve). On applying negative bias, the polarization is switched in the opposite direction and the current remains low because of the injection-limited contact. This is high resistance

OFF state and the current remains low when reading at low bias (red curve). These two memory states can be assigned Boolean "1" and "0" and thus, can be read non-destructively.

These memory diodes can be integrated in crossbar array structures. The rectifying nature of the diodes help in reduction of cross-talk between them.[29, 30] Switching time, memory retention and cycle endurance measurements have also been done on these blend devices. The devices have shown a retention time of approximately 10^6 seconds. This long retention time results from the stable polarization of the ferroelectric polymer.[31] The switching time of the blend devices is also comparable to that of pristine P(VDF-TrFE) capacitors, $\approx 10^{-9}$ seconds.[32, 33] In 2011, Asadi *et al.* introduced a concept of MEMOLED as a solution to signage applications with passive addressing.[34] MEMOLED is a light emitting diode with an inherent ferroelectric switch. The study successfully showed MEMOLED as a means of combining active addressing in a passive-matrix crossbar geometry.

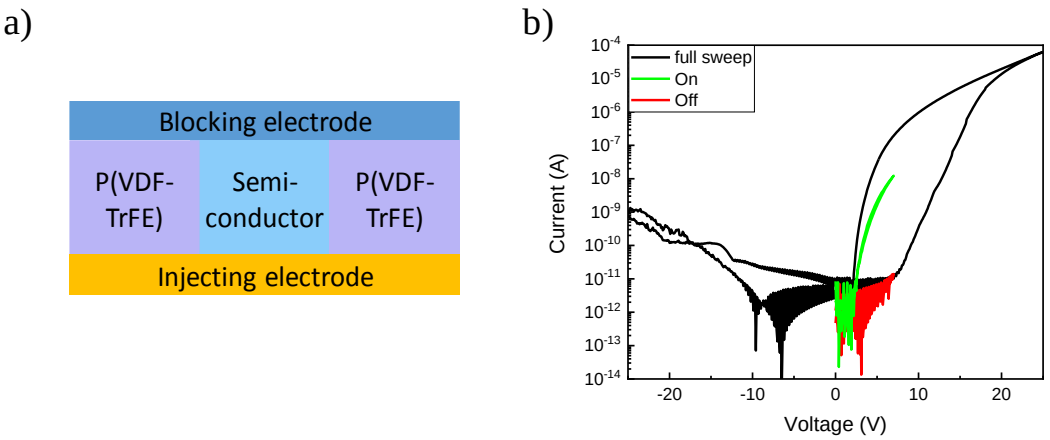


Figure 1. 1. a) Schematic showing cross-sectional view of the polymer blend memory diodes. Charge is injected into the semiconductor from the injecting electrode. b) Current-voltage (*I-V*) characteristics of the memory diode. By polarizing the ferroelectric in opposite directions, ON and OFF states can be programmed which can be read at low bias.

Charge transport has also been extensively studied in such organic resistive switches. The proposed charge transport mechanisms include band bending at the semiconductor-metal contact due to polarization[28, 35] and bulk-limited and injection limited conduction in the ON and OFF states respectively.[25] There have been works based on numerical simulations to study the charge transport through the memory diodes, which have shown that interfacial conduction takes place through the devices. Polarization of the ferroelectric leads to stray electric field between the polarization charges and the compensating image charges which lowers the metal-

semiconductor barrier.[36, 37] Thus, these ferroelectric polymer based memory diodes have been characterized as interfacial devices, which will be the focus of study in this thesis.

Morphology of the P(VDF-TrFE) blends has also been a subject of extensive research.[38-40] The blend tends to phase separate due to spinodal decomposition and the domains of the semiconductor polymer distribute randomly inside the matrix of the P(VDF-TrFE) after annealing. Several attempts have been made to control this randomness in distribution, namely temperature controlled spin coating[26], side-chain modification of semiconductor polymer[41] and use of self-assembled monolayer (SAM) to modify the surface energy of the substrate[41]. Patterning and nano-lithography has also been extensively studied to control the interface of the polymer domain structures.[42-45] However, the memory diodes failed to show much improvement apart from a slight increase in the ON state current density. Thus, to this day, random morphology remains the norm of the device fabrication of these memory diodes.

1.3 Outline of the thesis

This thesis focusses on studying the role of interface in the device physics of the memory diodes and novel functionality of the present-day ferroelectric memory diodes. The thesis puts emphasis on the improvement of the memory diodes. *Chapter 2* elaborates the basic theoretical background needed to understand the operation of the ferroelectric polymer based memory diodes. The concept of ferroelectricity, polymer ferroelectrics and semiconductor polymers, as well as charge injection barrier, and transport in the semiconducting polymers are discussed.

Chapter 3 presents the first experimental proof for the interfacial conduction mechanism in the resistive bistable diodes.[36] *Chapter 4* investigates P(VDF-TrFE)-PFO MEMOLEDs and the effect of electron trap on MEMOLED's operation. *Chapter 5* provides details as how to process and operate the memory diodes in normal ambient conditions and address the issue of air-sensitivity for both fabrication and memory operation.[180]

Chapter 6 demonstrates ferroelectric tunnel junctions (FTJs) based on a planar electrode configuration, and unambiguously shows that the current transport through a FTJ is dominated by tunneling that is modulated by ferroelectric polarization. Finally, *Chapter 7* discusses current driven ferroelectric memory devices, and shows that the ferroelectric polymer based resistive switches have the potential to be programmed by current pulses as well. The chapter discusses the retention time measurements and switching dynamics of the memory devices by applying

current signals. Furthermore, the potential application of such current driven memory devices in neuromorphic computing has been discussed.[274]

Chapter 2

Theory of Ferroelectric Memory Diodes

This chapter elaborates the theoretical background and functioning of ferroelectric polymer based memory diodes. The chapter begins with introducing the basic concepts of ferroelectricity, organic ferroelectric and semiconductor polymer. The concept of injection barrier is discussed in order to understand the charge conduction in the memory devices. Finally, the concept of ferroelectric tunneling is discussed briefly.

2.1 Ferroelectricity

The phenomenon of ferroelectricity was first discovered in 1920 by Valasek in Rochelle salt ($KNa(C_4H_4O_6)\cdot 4H_2O$), while observing the reversal of polarization upon application of an external electric field.[46, 47] It is analogous to ferromagnetism in iron, showing the property of spontaneous polarization upon cooling below a certain temperature (Curie temperature). In addition, ferroelectric materials (ferroelectrics) exhibit the property of hysteresis between electric polarization and electric field. Therefore, just as the magnetic field B and magnetization M vary with applied magnetizing field H in ferromagnets, dielectric displacement D and polarization P vary with applied electric field E in ferroelectrics. Ferroelectrics also exhibit other phenomena like pyroelectricity (temperature dependent electric polarization of material) and piezoelectricity (electrical polarization due to mechanical stress).[48]

Ferroelectricity remained an interesting, theoretical, phenomenon until 1944, when $BaTiO_3$ was discovered, which opened the path to ferroelectric memory applications.[48, 49] Soon after the PZT ($Pb(Zr,Ti)O_3$) family of materials became the material of choice for FeRAMs (Ferroelectric Random Access Memories). Ferroelectrics have crystalline structures that consist of local polar regions known as domains. Orientation of spontaneous polarization can be different in each domain. At zero electric field these domains are randomly orientated, cancelling each other's polarization and thus, giving zero net polarization at zero electric field. Domain walls are the transition regions between domains of different polarization directions.[50, 51] The characteristic feature of ferroelectric materials is reversal of spontaneous polarization, P upon application of an electric field, E, forcing the dipoles to orient along the direction of the electric field. This leads to a ferroelectric hysteresis loop between P and E (Figure 2.1). The

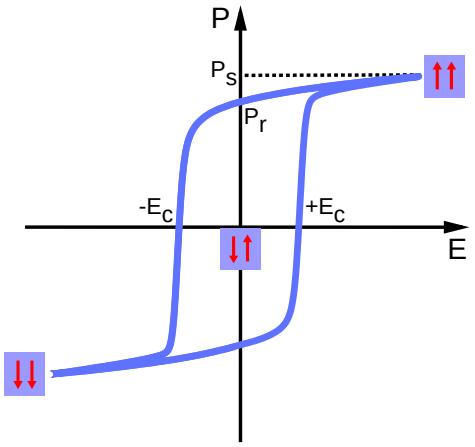


Figure 2. 1. Schematic of a polarization versus electric field loop for a ferroelectric material.

key features of a ferroelectric are a coercive field, E_c and remnant polarization P_r. The $+E_c$ or $-E_c$ is the minimum electric field strength required to orient the electric dipoles in either of the "up" or "down" directions, respectively.

P_s is the saturation polarization reached while applying the electric field, i.e., all the dipoles have oriented themselves in the electric field direction. On the other hand, P_r is the remaining polarization in the material when the electric field is removed. In addition, ferroelectric materials also portray a distinctive feature of phase transition above a certain temperature know as Curie temperature (T_c). Above this temperature, ferroelectric phase changes to unpolarized paraelectric phase that is accompanied with structural phase transition.

The *P-E* hysteresis loop is a necessary but not a sufficient condition to characterize a material as ferroelectric.[52, 53] Phenomenon such as charge trapping-detrapping at Schottky electrodes[54], leakage current[48] and surface polarization[55] can also lead to hysteresis-like behavior. The ferroelectric nature of a material can also be determined by analyzing its *C-V* characteristics. A butterfly-shaped plot of voltage dependence of small signal capacitance is characteristics of a ferroelectric, as shown in the Figure 2.2.[56, 57] The measured response depends upon domain wall motion near the local energy minima along with ionic and electronic displacements. The capacitance peaks at coercive field because of the high concentration of the domain wall at that point.[56]

Reliability of a ferroelectric material in memory applications is judged based on three properties, namely, polarization loss, fatigue, and imprint. Retention loss is characterized by the amount of polarization decrease with time as compared to their original state. Depolarization field, along with charge injection and internal built-in voltage, are considered the main causes

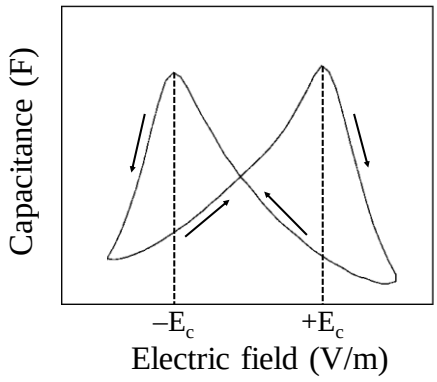


Figure 2. 2. Characteristic form of the *C-E* curve of a ferroelectric material (adapted from reference [93]).

for polarization loss.[58, 59] Depolarization is an inherent phenomenon that arises due to spontaneous polarization. Polarization charges remain uncompensated at the electrode interfaces, giving rise to a depolarization field opposite to the polarization direction, as shown in Figure 2.3a.[60, 61] It is an important issue in ferroelectric devices that can lead to loss of remnant polarization, which increases as the thickness of the ferroelectric material decreases.[62] On the other hand, fatigue is a result of repetitive polarization reversal cycles, leading to reduction in the switchable polarization and shrinking of the *P-E* loop (Figure 2.3b). Thus, fatigue is the measure of loss of polarization charge upon repetitive switching. The cause of fatigue has been attributed to both bulk- and interface-related phenomena. Or more precisely to domain wall pinning by charged defects in both bulk ferroelectric films and at the interface of ferroelectric and electrode.[63-65] Even oxygen vacancies at the interface, which later redistribute themselves within the ferroelectric layer under electrical stress, can lead to reduction in polarization.[66-68]

Lastly, imprint is characterized by the shift of the *P-E* hysteresis loop along the electric field axis and thus, loss of remnant polarization, as shown in Figure 2.3c.[69] Imprint causes, one polarization state to obtain a higher value than the other does. Interpretation of this effect has been based on buildup of an internal bias due to defect in dipole alignment, which again originates from oxygen vacancies.[70, 71] Furthermore, presence of interfacial layer between the ferroelectric and the electrode has also been cited as a cause for imprint.[72, 73]

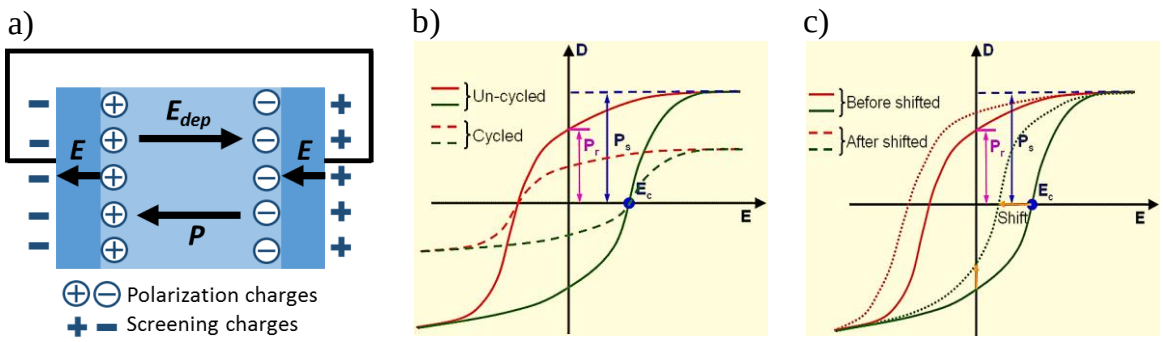


Figure 2. 3. a) Schematic showing the development of screening charges on the metal electrodes on application of electric field, *E* and polarization, *P* in the ferroelectric. Depolarization field, E_{dep} is formed opposite to polarization direction. Schematics illustrating the phenomenon of b) fatigue and c) imprint. The figures have been adapted from reference [69].

2.2 Organic ferroelectric and semiconductor materials

2.2.1 Organic ferroelectric materials

Current research focusses on many ferroelectric materials, for example, charge transfer complexes, polymers, crystalline organic materials,[74, 75] superamolecular systems, liquid crystallines[76, 77] and hydrogen bonded networks.[78, 79] Although, organic ferroelectrics display inferior performance as compared to their inorganic counterparts, they have shown considerable potential owing to their low temperature processability, substrate flexibility and cost-effectiveness.[80, 81] In this respect, polyvinylidenefluoride (PVDF) and its copolymers with TrFE have been extensively studied. The molecular dipoles along the electropositive hydrogen atoms and electronegative fluorine atoms give rise to polarization which is switchable upon application of an external electric field (Figure 2.4a).[82] Considerable research has been done within the field of PVDF and P(VDF-TrFE) based ferroelectric memory devices[31, 83-87], along with negative capacitance devices[88], organic solar cells[89] and multiferroic devices[90].

Five distinct crystalline forms are exhibited by PVDF polymers, namely, α, β, γ, ε and δ phases. Formations of each phase uniquely depend on the processing conditions. With the help of poling, stretching and annealing approaches, material can even transit between different phases.[91] β phase exhibits the ferroelectric and piezoelectric phase and has an all-trans (TTTT) zig-zag molecular configuration, with a dipole moment of 7×10^{-30} Cm.[92] The all-trans conformation associated with β phase is enhanced even more upon addition of TrFE monomer to PVDF. This is due to larger steric hindrance induced by fluorine atoms in the overall copolymeric monomer.[82] The schematic of the crystal structure of P(VDF-TrFE) is shown in

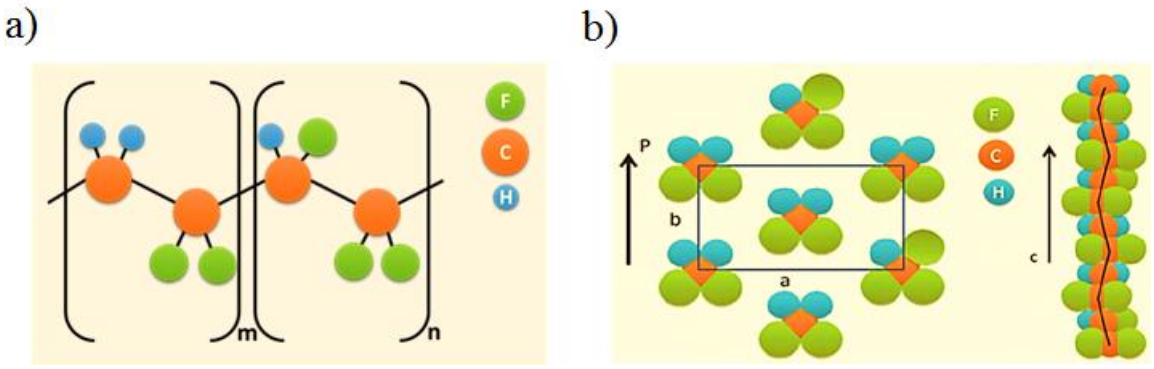


Figure 2. 4. a) Chemical formula of P(VDF-TrFE) random copolymer. b) Schematic of β crystal structure in *ab* plane and c axis is perpendicular to *ab* plane (adapted from reference [93]).

Figure 2.4b.[93] The *c*-axis is along the carbon backbone, polarization direction is along *b*-axis and is perpendicular to the *c*-axis, and *a*-axis is perpendicular to the *b*- and *c*-axes. Annealing is performed in order to achieve higher crystallinity of the β phase in P(VDF-TrFE). The most researched composition of P(VDF-TrFE) is 70/30 with the maximum spontaneous polarization value of 10 μC/cm^2.[94] In addition, introduction of TrFE to VDF reduces the phase transition (ferroelectric to paraelectric) temperature or the Curie temperature, T_c in the copolymer. The greater PVDF content in the copolymer shifts the T_c to higher temperatures. On increasing the PVDF content from 50 mol% to 80 mol%, T_c increases from 70 °C to 140 °C. The phase transition T_c in ferroelectric polymers is of order-disorder type, meaning that the alignment of dipoles becomes randomized and amorphous.[95, 96]

Processing of ferroelectric thin films is relatively easy compared to their inorganic counterparts, due to their simple solution processability. Conventionally, spin coating method has been used to prepare smooth and good quality thin as well as thick films. For PVDF and its copolymers, many solvents are available to choose from, for example, methyethylketone (MEK), dimethylsulphoxide (DMSO), tetrahydrofuran (THF), cyclohexanone, and dimethylformamide (DMF) among others. Film thickness can be controlled by spin parameters like spin speed and acceleration. Homogeneity and roughness depends upon processing conditions like temperature and relative humidity. Favorable conditions for smooth and homogenous thin films are low relative humidity or high substrate temperature.[97] At high relative humidity, the film structure tends to become porous and hence, rough. At high substrate temperatures, however, films are denser and smoother. The morphology of P(VDF-TrFE) thin films, prepared by spin coating, consists of both crystalline and amorphous structures.

Polarization switching in ferroelectric materials has been investigated extensively. The dynamics of ferroelectric switching is quantitatively described by the Kolmogorov, Avrami and Ishibashi (KAI) model.[98-100] The KAI model is based upon an extrinsic switching process of nucleation and domain growth, wherein, the electric dipoles orient themselves in the direction of applied electric field. The process begins with nucleation of domains which grow in longitudinal and transverse directions, and coalesce together resulting in unidirectional dipoles along the electric field.[101]

Time dependent polarization change is given by[102]

$$\frac{\Delta P(t)}{2P_r} = 1 - exp\left(\sum_i \frac{S_i}{S_0}\right) \qquad 2.1$$

where, S_i is the area of growing domains, S_0 is the sample area and P_r is the remnant polarization at zero electric field. In addition, the KAI model assumes that the growth of a domain, after nucleation, takes place with unrestricted expansion and follows

$$S_i = (vt)^n \quad 2.2$$

where, v is the constant domain-wall velocity, t is the time and n is the Avrami index. The normalized change in the polarization can then be written as

$$\frac{\Delta P(t)}{2P_r} = 1 - exp\left(-\left(\frac{t}{t_0}\right)^n\right) \quad 2.3$$

where, t_0 is the characteristic switching time and the Avrami index that depends on the dimensionality of the system of domains. For epitaxial films, n = 2, whereas for single crystals, n = 3.

Merz law defines the relationship between the switching time t_0 and the activation field E_a as follows[103]

$$t_0 = t_\infty \exp\left(\frac{E_a(t)}{E}\right) \quad 2.4$$

where, t_∞ is the switching time at infinite electric field. E_a is proportional to domain-wall energy and is inverse functions of temperature. Thus, ferroelectric switches quickly at higher temperatures, requiring less activation field.

Polarization switching in P(VDF-TrFE) has been studied in-depth.[104-107] In thick films, the switching is extrinsic in nature, characterized by nucleation and domain-wall motion. The switching time in P(VDF-TrFE) has been observed to follow Merz law. On the other hand, change in polarization is well described by Eq. 2.3. Extracted Avrami indices have been reported between 1 and 3.[104] The polarization switching depends highly on the microstructure of the polymer film, which in turn depends on the process conditions such as choice of solvent and annealing temperature.

2.2.2 Organic semiconductors

The discovery of chemically doped polyacetylene in 1977 triggered the application of organic conjugated materials as electrically active materials.[108] Apart from flexibility, easy processability and cost effectiveness, there are a number of other advantages of organic polymers in comparison to their inorganic counterparts. Some of them include fine tuning of material properties by molecular restructuring[109], low temperature processability and large

number of low-cost processing techniques to choose from, for example, spin coating, inkjet coating, bar coating, spray coating, roll-to-roll printing etc.[110-114] Extensive research done in the past two decades, to improve the synthesis and processing of new class of semiconducting polymers, has led to their enhanced performance. This can be seen in applications such as field-effect transistors (OFETs), organic light-emitting diodes (OLEDs) and solar cells.[115, 149, 169]

The charge transport phenomenon in inorganic semiconductors is intrinsic in nature, i.e., the thermal agitation leads to excitation of charges from the valence to the conduction band. Typical intrinsic charge densities are in the range of 10^6 to 10^{16} cm^{-3}, which can be enhanced by doping. Moreover, the atoms are covalently bonded. However, in the case of organic semiconductors, conductivity is extrinsic in nature and is caused by charge injection, from doping or by light induced electron-hole pair generation.[116] Organic semiconductors are class of π-conjugated systems, which are further divided into two categories depending on their weight, namely π-conjugated polymers and small molecules.[117] Molecular structures of both consist of p_z orbitals of sp^2-hybridized C atoms forming the conjugated π-electron system. Delocalization of electrons is increased with the p_z-orbitals participating in the π-bond (Figure 2.5a). The π bonding is significantly weaker as compared to σ bonding, which forms the backbone of the molecules. Thus, π–π* transitions constitute the lowest electronic excitations in conjugated molecules. As shown in Figure 2.5b, the overlapping molecular π-orbitals form the highest occupied molecular orbit (HOMO) in which hole transport takes place. Similarly, electron transport takes place in the overlapping π* orbitals (anti-bonding), constituting the lowest occupied molecular orbit (LUMO). This corresponds to an energy gap of typically 1.5 to 3 eV, leading to light absorption or emission.[118] The optoelectronic properties can be tuned

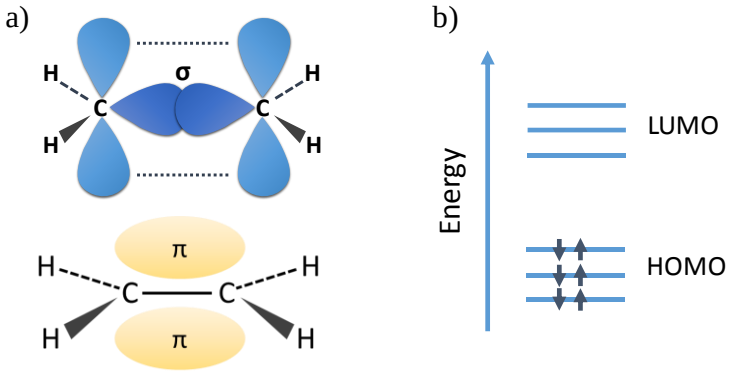


Figure 2. 5. a) An example of conjugated *π* electron system in ethane. b) Energy level diagram of an organic semiconductor demonstrating the highest occupied molecular orbitals (HOMO) and the lowest unoccupied molecular orbitals (LUMO).

by varying the factors such as conjugation length and presence of electron donating/withdrawing groups.

2.3 Charge transport in organic semiconductor

Charge transport in organic semiconductor devices is divided into two categories, namely, bulk transport, where the charge carriers are generated within the bulk of the material (e.g., solar cells) or interface transport in which the charge carriers are injected from the metal or oxide electrode into the organic semiconductor material (e.g., organic light emitting diodes and field effect transistors).[115, 119] On the basis of charge transport, organic semiconductor can show electron-only, hole-only or ambipolarity with the ability to transport both electrons and holes.

Charge carrier mobility is the key factor characterizing the charge transport. Charge mobility, μ is described by the Einstein-Smoluchowski equation: [149, 169]

$$\mu = \frac{eD}{k_B T} \qquad 2.5$$

where, e is the electron charge, D is the diffusion coefficient, k_B is the Boltzmann constant and T is the temperature. Also, D is given by $< x^2 >/nt$. $< x^2 >$ is the mean square displacement of the charges, t is the time and n represents dimension of the system. For 1D, 2D or 3D systems, n equals 2, 4 or 6 respectively. With application of electric field, mobility is alternatively described as

$$\mu = v/E \qquad 2.6$$

where, v is the velocity acquired by the charge carriers in electric field, E.[119, 149, 169]

In a diode configuration, the electrical characteristics are studied by sandwiching an organic film between two electrodes. The electrodes are chosen in a way that only holes or electrons are injected at low voltages. At low voltages the current transport is Ohmic with a slope of 1.[120] The film is thick enough for the charge conduction to be bulk-limited. At higher voltages, the current density, J scales quadratically with the applied voltage, V and the charge conduction is called space-charge limited current (SCLC). When the number of injected charges is maximized, the built-up electrostatic potential prevents additional charges to be injected and the injection charge density reaches a maximum at the semiconductor-electrode interface.[121, 122]

With the assumption of mobility value to be low and constant, J-V characteristics of SCLC type of conduction is given by the following Mott-Gurney equation[123]

$$J = \frac{9}{8}\epsilon_0\epsilon_r\mu\frac{V^2}{L^3} \quad 2.7$$

where, ϵ_r denotes the dielectric constant of the medium and L is the material thickness. However, for organic semiconductors, due to their disordered nature, the mobility scales with the width of Gaussian density of states (DOS) (σ), temperature, electric field and charge carrier density. Disordered nature of the polymers leads to localization of the charge carriers at the molecular bodies like small segments of a polymer chain. Transport of these charge carriers is possible only by hopping to the adjacent sites with variable energies. The hopping sites are often characterized by Gaussian distribution. In addition, the hopping distance statistically varies between adjacent sites. This leads to energetic broadening of the DOS, meaning that the mobility in disordered polymers is several orders lower than in the crystalline counterparts and is temperature and field dependent.[149, 169]

For an electron to hop from (r_i, ξ_i) to (r_i, ξ_j), where r and ξ are the position and energy corresponding to a particular site. In order to hop from site i to j, it has to overcome a distance of $R_{ij} = r_j - r_i$ and energy $\Delta\xi = \xi_j - \xi_i$. The hopping rate κ_{ij} from site i to j is described by Miller-Abrahams formalism as follows

$$\kappa_{ij} = \nu \exp(-2\gamma R_{ij})\, exp\left(-\frac{\xi_j-\xi_i}{k_BT}\right) \text{ for } \xi_j > \xi_i \quad 2.8$$

where, ν denotes the attempt hopping frequency and γ is the overlap factor. It should be noted, that the second exponential becomes 1 for downhill hopping, i.e., for $\xi_j < \xi_i$. This formalism is valid for low temperatures and electron-phonon coupling.[119]

Gaussian distribution is attributed to any site in a disordered system. The charge carriers tend to relax into the tail of the Gaussian distribution and the mean energy of them equal – σ^2/k_BT. Mobility scales exponentially with $1/T^2$ at low carrier densities, and with $1/T$ at higher.[124] Electric field dependence of mobility follows Poole-Frenkel behavior ($E^{1/2}$) at higher fields, whereas at lower fields, mobility is constant.[125] At higher electric fields, energetic disorder increases as does the diffusion constant and temperature dependence of mobility is also low. At low electric fields, temperature dependence is greater. It is also worth noticing that charge carrier density dependence is dominant over temperature dependence.[126] In addition, morphology of the polymer film has an impact on the mobility. If the film is ordered, then σ will decrease and as a result the mobility increases. For example, in thin film field-effect transistors, mobility is many orders higher due to ordered alignment of the polymer chains.[127, 128]

2.4 Charge injection

Schottky contact is the interface between the metal and the semiconductor. Barrier height plays a crucial role in determining the current transport to be either space charge limited or injection limited.[129-131]

An Ohmic contact is formed for electrons when the work function of metal, Φ_M < electron affinity (EA) or lowest unoccupied molecular orbital (LUMO) of the organic semiconductor. When these two materials are brought into contact, Fermi level (ξ_F) aligns with LUMO and flow of electrons takes place. On the other hand, when work function of metal, Φ_M > ionization potential (IP) or highest occupied molecular orbital (HOMO), Ohmic contact is formed between the HOMO and metal contact. This causes ξ_F to align with HOMO, aiding in an uninterrupted flow of holes.[132,133] However, in case the work function lies between IP and EA, such that EA < Φ_M < IP, then neither electrons can be transferred from metal to LUMO nor holes from HOMO to the metal. In this case Fermi level pinning does not occur. Moreover, energy barriers are formed for both electron as well as hole injection.

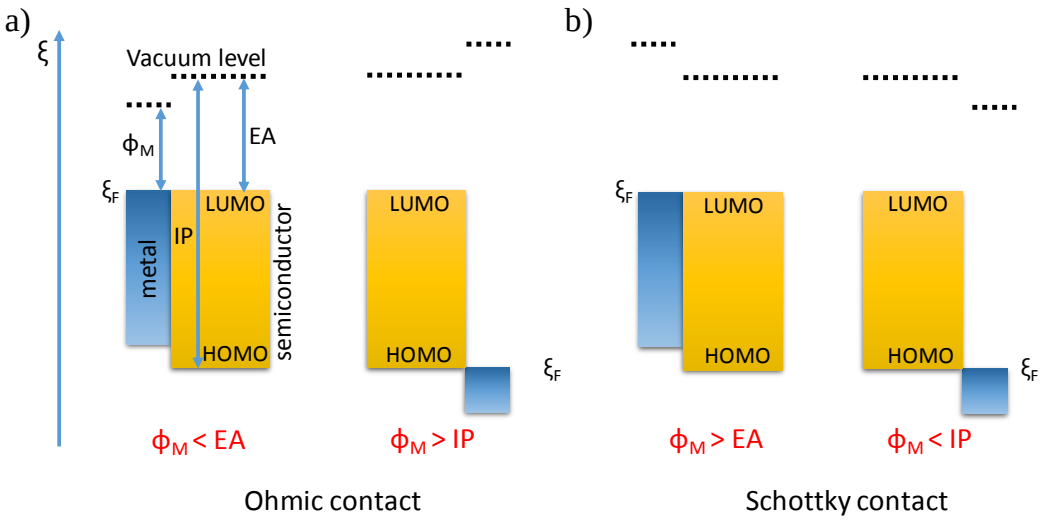


Figure 2. 6. a) Schematic of energy level diagram showing the formation of Ohmic contact between a metal and a semiconductor. The dotted lines represent vacuum level, which shift on alignment of the fermi levels. Electron transfer takes place when $\Phi_M < EA$ (electron affinity of semiconductor), and hole transfer takes place when $\Phi_M > IP$ (ionization potential of semiconductor). b) Formation of Schottky contact is illustrated in the schematic. When $\Phi_M > EA$ and $\Phi_M < IP$, then a Schottky barrier is formed.

Thermionic injection is the classical model that describes charge injection at Schottky contacts. It is based on charge carriers acquiring enough thermal energy that they are able to overcome the contact barrier. The current density is given by the following expression[134, 135]

$$J = A^{*}T^{2}exp\left(-\frac{\Phi_b - \Delta\Phi}{k_B T}\right) \quad 2.9$$

where, A^* is the effective Richardson constant, $A^* = 4\pi q m^* k_B^2/h^3$, m^* is the effective mass of the charge carrier, h is the Planck's constant and q is the electron's charge. Φ_b is the interfacial energy barrier. $\Delta\Phi$ is the decrease in the energy barrier due to electric field, E and image force effect. Image force effect is the decrease in the potential energy of the injected charge due to the Coulomb interaction between the remaining charges in the metal. The effective barrier is given by[136, 243]

$$\Phi_B = \Phi_b - \Delta\Phi = \Phi_b - \sqrt{\frac{q^3 E}{4\pi\epsilon_0\epsilon_r}} \quad 2.10$$

However, this classical injection model differs for semiconductors with low carriers mobilities. A comparatively low bulk mobility leads to back diffusion of charge carriers. The charge carriers are injected at a high rate from the metal electrode, but due to the low mobility in the bulk of the semiconductor material, they accumulate at the interface and often result in backflow into the electrode.[137] This makes the injection at the interface diffusion-limited, expressed as following[138]

$$J = qN_V\mu E\ exp\left(\frac{-\Phi_B}{k_B T}\right) \quad 2.11$$

with N_V being the effective density of states.

Another mechanism describing charge injection is field emission or barrier tunneling. It is based on the theory of charge carrier tunneling through the barrier in the presence of an electric field.[139] Fowler-Nordheim model has been used to characterize the quantum mechanical tunneling of the charge carriers through the interface. The current density across the interface is given by

$$J = BE^2\left(\frac{8\pi(2m^*)^{1/2}\Phi_B^{3/2}}{3hqE}\right) \quad 2.12$$

where, B is a constant. For full derivation of the formalism, the reader is suggested to refer to the references[140-142].

Charge injection by thermionic emission is more relevant to crystalline semiconductors where the energy states are delocalized and charge motion is ballistic in nature. However, in case of organic semiconductors, the energy states are highly localized and charge transport takes place via hopping.[143] In the previous section, the charge transport in an organic semiconductor was described by hopping mechanism between discrete sites by Miller-Abrahams formalism (Eq. 2.8). In order to explain the charge injection through the electrode-semiconductor interface, many models have been demonstrated. Van der Holst came up with a master Pauli equation[144]

$$\Sigma_{j\neq i, j_x\neq 1, m_x}\left[W_{ij}p_i\left(1-p_j\right)-W_{ji}p_j(1-p_i)\right]+\Sigma_{j\neq i, j_x=1, m_x}[W_{ij}p_i-W_{ji}(1-p_i)]=0 \qquad 2.13$$

with the first term describing the hopping between the organic sites. The second term describes the hopping between the electrodes, which are positioned at $i = 1$ and $i = m_x$, where, m_x denotes the size of the 3D lattice (box). The carrier occupation probability on site i is denoted by p_i. It is assumed that the hopping of charge carriers from one site to another is due to thermally assisted tunneling mechanism. The final injection limited charge density is given by

$$J = J_0 h(E) exp\left(-\frac{\Phi_B}{k_B T}+\left(\frac{1}{2}-c_2\right).\frac{\sigma^2}{(k_B T)^2}\right)\frac{eaE}{\sigma} \qquad 2.14$$

where, $J_0 = (ev_0/a^2)exp(-2\alpha a)$ denotes the current density of the system with all the sites fully occupied ($p_i = 1$), $c_2 = 0.42$ and $h(E)$ describes the field dependence of mobility.[144]

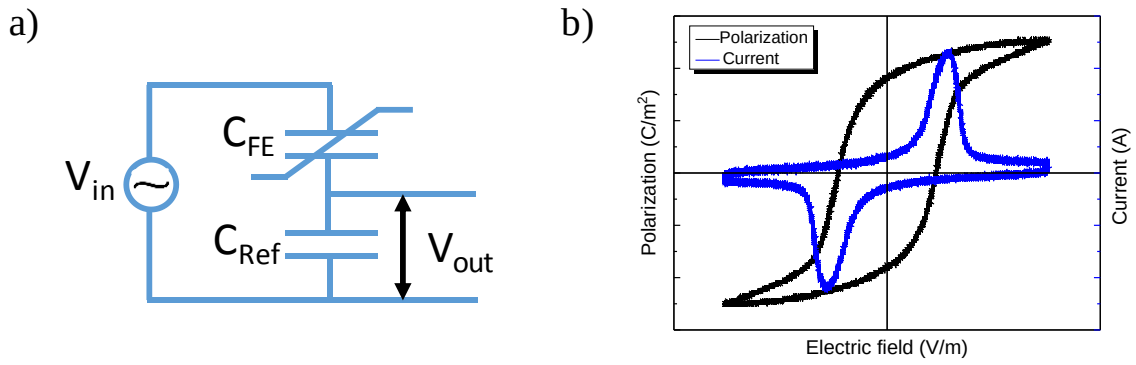


Figure 2. 7. a) Sawyer Tower circuit diagram used for the electrical characterization of ferroelectric capacitor. b) Polarization vs electric field loop of a P(VDF-TrFE) capacitor (black) and corresponding switching current (blue curve), when the reference capacitor is replaced by a resistor in the Sawyer-Tower.

2.5 Ferroelectric memory devices

Extensive amount of research has been done in the field of memory devices to come up with a viable solution for a wide variety of applications. One of the active domains of this has been ferroelectricity based memory applications, which have shown considerable amount of developments over the past two decades. In this part most common approaches relevant to the scope of this thesis will be discussed.

The simplest of device structures is that of a capacitor. *Ferroelectric capacitors* consist of a film of ferroelectric polymer sandwiched between two electrodes. Sawyer-Tower circuit has been used for electrical characterization of the ferroelectric capacitors, as given in Figure 2.7a. A time varying triangular waveform (frequency 100 Hz) is generated from the function generator (here, Tektronix AFG3102), which is amplified and fed to the ferroelectric capacitive, C_{FE} device. The applied bias voltage waveform, V_{in} is fed to channel 1 of the oscilloscope (here, LeCroy Waverunner LT372) as well. The reference capacitor, C_{Ref} is put in series with the ferroelectric capacitor and the voltage across it, V_{out}, as a function of time, is measured by channel 2 of the oscilloscope. Upon application of bias, the ferroelectric polarizes causing charges to appear on the capacitor plates to compensate the polarization charges. The amount of charge across the ferroelectric capacitor is same as that of the reference capacitor. By knowing the capacitance value of the reference capacitor, the polarization value can be determined. The applied electric field, E is determined by dividing the voltage applied by the thickness, t of ferroelectric polymer film. At $E = 0$, $P = D$, where, P is given by remnant polarization. Thus, $P \approx D$, holds as a sufficient approximation and will be used in this thesis.

Memory operation is achieved by applying electric field greater than the coercive field. Correspondingly, the electric dipoles will align in either up or down directions with respect to the field. The *I-V* plot gives characteristic switching peaks at the coercive fields as shown in the Figure 2.7b. A second voltage signal is applied in order to read the programmed state. If the direction of the applied field is the same as the polarization direction then no switching peak will be seen in the *I-V*, as it does not alter the polarization.[15] Thus, the read out of the memory state in a ferroelectric capacitor is destructive in nature, which makes it necessary to reprogram the device after every read operation to its initial memory state after readout. In addition, it costs more power dissipation due to the continuous write-read operations and fatigues the device faster.

Another feature of capacitive structures is that they can be employed in cross-bar arrays, allowing an increase of the memory density on a substrate.[145] Inorganic materials when used in these embedded memory arrays, tend to suffer from "half-select" problem.[67] In brief, to target one memory element, the entire row is supplied with (+1/2 V_t) and the column with (-1/2 V_t). The target element receives ± V_t and the state is programmed, while the other elements remain unaffected. This, however, practically is not true. Repetitive application of (±1/2 V_t) polarizes the neighboring states and results in corruption of data. This problem was rectified by use of active matrix of transistors with "1T 1C" configuration (one transistor for one capacitor). Despite that, it led to cost increase due to additional fabrication steps and larger surface area per element.[146] However, it has been proven experimentally that it is possible to use organic ferroelectric materials (especially P(VDF-TrFE)) in passive geometry without suffering from the "half-select" problem and destructive read out of memory state.[147, 148] This is due to longer switching time of P(VDF-TrFE). This is also optimum enough in order not to disturb the neighboring states and read the desired programmed state at the same time. In addition, the switching time is long enough to read the programmed state and short enough that it does not harm the original polarization of the state, thus, increasing the number of read operations before the need of reprogramming arises.

Another class of memory devices is *ferroelectric field-effect transistors* (FeFET) with a ferroelectric material constituting the gate dielectric. The FeFETs operate based on the resistive switching induced by polarization of the ferroelectric gate dielectric. Structural layout of FeFET comprises of a stack of metal-semiconductor-ferroelectric materials, with the ferroelectric layer

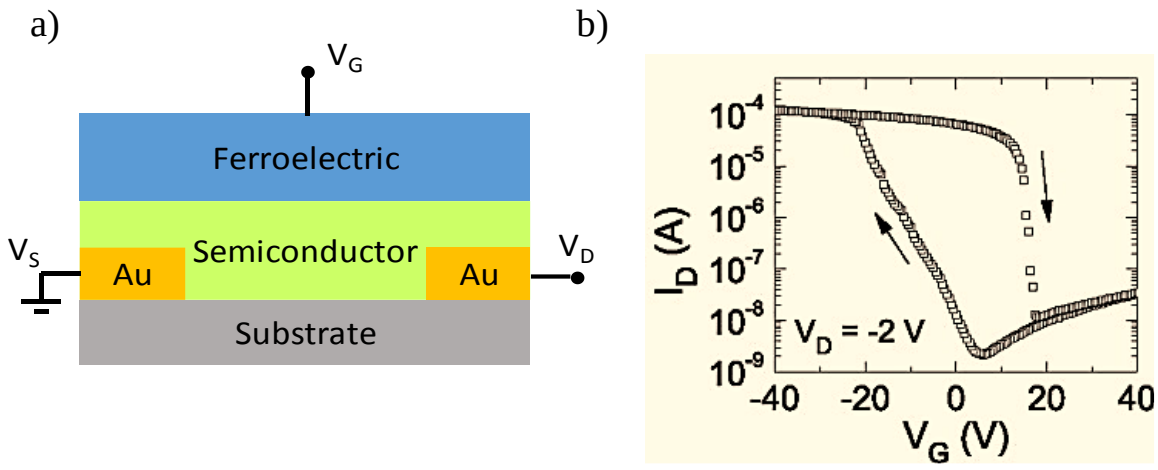


Figure 2. 8. a) Schematic layout of a FeFET with Au as source drain electrodes. b) *I-V* transfer curve of a *p*-type FeFET, with arrows indicating the sweep direction (adapted from reference [149]).

serving as the gate dielectric. Depending on the polarization orientation of the ferroelectric, charges are induced through the ferroelectric-semiconductor interface into the semiconductor channel. The ferroelectric polarization changes depending on the gate bias, which shifts the injected charge density in the semiconductor, which further defines the drain current levels. The high and low drain current levels can be correspondingly defined as Boolean "1" and "0".[15, 149] The high and low semiconductor channel conductance is maintained even after the gate voltage is removed, making the read-out non-destructive.[15] It has been seen that the ON state of the FeFET is stable due to the polarized state of the ferroelectric gate; however, the OFF state is not thermodynamically stable. The lack of compensation charges from the semiconductor leads to an increased depolarization field in the device.[15, 150] As an example, *I*-*V* characteristic of a typical *p*-type unipolar FeFET is demonstrated in Figure 2.8b. The current remains low at the beginning of the curve, as the ferroelectric remains unpolarized. At switch-on voltage, the current starts to increase with increase in the negative bias and saturates when the negative coercive voltage (~ -20 V) is reached, as the ferroelectric becomes fully polarized. This is the ON state. Upon back scanning, the ferroelectric remains polarized and the current remains high. At around +20 V, the ferroelectric polarization switches and the current decreases as the electrons cannot be injected into the *p*-type semiconductor. This puts the device in OFF state.[149] The main figure of merit of an organic FET (OFET) device is the field-effect mobility, whose value has changed drastically from ~ 10^{-6} cm^2 V^{-1} s^{-1} to nearly 10 cm^2 V^{-1} s^{-1}.[151-155] Temperature independent charge transport with high mobility has been observed in highly ordered semiconductor materials like pentacene and heteroacene derivatives.[155-157] Semi-crystalline materials such as conjugated polymers P3HT and PBTT have also been the focus of research.[151, 158-160]

The destructive nature of information read out can also be avoided by the use of a diode structure, which was discussed in detail in the previous chapter. The current rectifying property of the ferroelectric diodes also help in minimizing the "cross-talk" phenomenon, which can occur in integrated memory arrays.

2.6 Charge conduction mechanism in memory diodes

2D numerical models have been proposed explaining the device physics behind the operation of ferroelectric diodes. In this section, the operation mechanism will be discussed. The development of a stray electric field between the compensating image charges and the polarization charges inside the polarized ferroelectric leads to barrier lowering.[161] Along with

the stray electric field inside the device, tunneling of charge carriers through the metal-semiconductor interface and accumulation at the semiconductor side also takes place.[37] 2D polarization of the ferroelectric phase leads to the bending of electric field lines near the semiconductor phase. This results in charge conduction along the interface of the P(VDF-TrFE) and the semiconductor phase.[36] The numerical model also considered variable range hopping theory for charge conduction in the organic semiconductor,[162] along with disorder[163-165]. Physical equations solved in the numerical simulator included continuity, Poisson and drift-diffusion transport equations.[166-169] The charge flow at the ferroelectric-semiconductor interface was defined together with thermionic emission, energy disorder, drift-diffusion, tunneling and barrier lowering by image force.[37, 138, 144, 170-172]

However, most importantly ferroelectric polarization was considered as a function of electric field.[168, 173, 174] The ferroelectric polarization was modelled following the approach of Miller *et al.*[174] The model is described as following

$$P_s(E) = P_{sat}.\tanh\left(\frac{E-E_c}{2.E.\left(ln\left(\frac{1+P_r/P_{sat}}{1-P_r/P_{sat}}\right)\right)}\right) \quad 2.15$$

where, P_s is spontaneous polarization, P_{sat} is saturation polarization, and E_c is coercive field.

To model the charge transport in semiconductor, hole only device with PFO as semiconductor was fabricated with electrodes that form Ohmic contact with PFO. Polymer semiconductors like PFO are typically disordered, thus, they are characterized by localized states. The charge conduction in disordered semiconductors is via thermally activated hopping as described in section 2.3. The hopping rate between donor and acceptor sites is given by Eq. 2.8. The macroscopic conductivity, Γ is given by the following equation[37, 162, 163, 175]

$$\Gamma = \Gamma_0\ exp\left(\frac{\xi_F}{k_BT}\right) \quad 2.16$$

where, Γ_0 is proportional to T, σ, v_0 and inter-site distance. The drift-diffusion equation for hole transport inside the semiconductor is given by the following

$$\vec{J}_p = \Gamma\nabla\varphi + qD_p\nabla_p \quad 2.17$$

where, $J_p$represents hole current density, φ is the electric potential and D_p is the hole diffusion constant. The continuity equation is described by

$$\frac{dp}{dt} = -\frac{1}{q}\ \nabla.\vec{J}_p \quad 2.18$$

and the Poisson equation by

$$\rho = \epsilon_0 \epsilon_r \nabla . \vec{E} \qquad 2.19$$

where, ρ is the net charge carrier concentration and $\vec{E}$ is the electric field.

The charge injection mechanism is described by thermionic emission and barrier tunneling for crystalline inorganic materials. However, for disordered semiconductors, charge hopping mechanism has been proposed for charge injection as shown in the section 2.3. The barrier lowering due to image forces has been previously discussed and is given by Eq. 2.10. The effective hole charge carrier density at the interface of electrode and the semiconductor, due to effective energy barrier, Φ_b is approximated to [37]

$$p_0 = N_t exp\left(\frac{-1}{k_B T} \times (\Phi_b - \sigma^2 / 2k_B T)\right) \qquad 2.20$$

Other charge injection mechanisms include thermionic emission given by the following equation

$$J_p = \frac{AT^2}{N_t}(p - p_0) \qquad 2.11$$

with *A* as the Richardson constant. Barrier tunneling describes the hole carrier density flowing through the metal-semiconductor interface as

$$J_{tun} = \frac{AT}{k_B T} \int_{-\infty}^{+\infty} \kappa_p(r, \xi) \times \psi(r, \xi)\, \partial\xi \qquad 2.12$$

Here, $\kappa_p(r, \xi)$ is the tunneling probability given by Wentzel-Kramers-Brillouin (WKB) approximation[176] and $\psi(r, \xi)$ is a logarithmic function of position-dependent Fermi energy, $\xi_F(r,)$. The reader is suggested to refer to the reference[37] for details of the model and parameters used.

Thermionic emission and charge tunneling mechanisms explain the charge transport in crystalline (ordered) semiconductors where the charge conduction is governed by band-like transport. However, organic semiconductors have amorphous structures, which make charge hopping the major charge transport mechanism in them. So far, basic components of charge transport in semiconductor, P(VDF-TrFE) and at the interface of the metal-semiconductor have been described in brief.

Chapter 3

Interfacial Conduction in Organic Ferroelectric Memory Diodes

*This chapter presents the experimental proof of interfacial charge conduction in memory diodes based on phase-separated blends of ferroelectric and semiconducting polymers. To do so, in the diode structure the electrode contacting the semiconductor phase has been intentionally modified.**

*The results presented in this chapter have been published in H. Sharifi Dehsari, M. Kumar, M. Ghittorelli, G. Glasser, T. Lenz, D. M. de Leeuw, F. Torricelli and K. Asadi, *Applied Physics Letters* 113, 093302 (2018).[36]

3.1 Theoretical predictions by numerical models

Solution processed blend of a ferroelectric and a semiconductor polymer undergoes spinodal decomposition phase separation yielding a thin-film with bicontinuous columnar semiconducting domains that are randomly distributed in the P(VDF-TrFE) matrix.[38, 40, 177, 178] To realize a bistable rectifying diode, the injecting electrode is chosen such that it forms a Schottky contact with a large barrier height with the semiconductor. The ferroelectric polarization modulates the injection barrier, enabling reversible switching of the diode resistance between a high-resistance OFF-state and a low-resistance ON-state.[25, 37]

Charge conduction in these memory devices has been extensively investigated. Two-dimensional (2D) numerical models have been presented describing the *I-V* characteristics on the basis of ferroelectric polarization and charge injection through metal-semiconductor interface.[25, 37, 168, 174] The model predicts bending of the electric field lines near the semiconductor phase, due to the emergence of an in-plane component for the ferroelectric polarization, as shown in Figure 3.1a. As a result, a large stray electric field exists at the semiconductor-P(VDF-TrFE) interface. The bottom contact facilitates tunneling of the charge carriers and effectively lowers the barrier for charge injection. Appearance of the *x*-component of the electric field leads to confining of the injected charge carriers in the semiconductor to the interface with P(VDF-TrFE) phase, as illustrated by the red arrows in Figure 3.1a. The 2D simulations thus predict that the memory diode is an interface device, wherein the charge injection occurs only through the fraction of the contact just underneath the

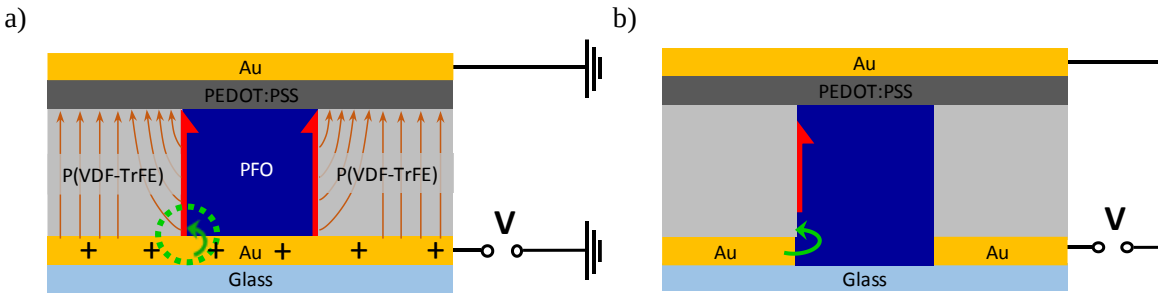


Figure 3. 1. Schematic illustrating a) Structure of conventional memory diode. Electric field distribution in the P(VDF-TrFE) phase is shown by orange arrows. The thick red-arrows show confinement of the current to the PFO phase boundaries. b) Bottom-contact-etched memory device structures. The green-arrows show that charge injection takes place at the corner of the ternary interface (between the injecting contact with the PFO|P(VDF-TrFE)). Both diode structures should give the same switching behavior.

semiconductor|P(VDF-TrFE) interface , as shown in Figure 3.1a. Therefore, only the corner point of contact is needed for the memory operation and the charge conduction inside the device takes place along the semiconductor|P(VDF-TrFE) interface. However, to back these key theoretical findings, no experimental proof has been given so far.

Thus, in this chapter, we unambiguously demonstrate charge injection from the contact point just beneath the semiconductor|P(VDF-TrFE) interface in the memory diodes. To this aim, a new memory device structure, shown in Figure 3.1b, was realized. The part of the injecting bottom electrode in contact with the semiconductor is removed, leaving only the contact point under the semiconductor|P(VDF-TrFE) interface for charge injection to take place. Poly(9,9-dioctylfluorene) (PFO) was used as the semiconductor polymer. It is experimentally demonstrated that the memory diode shows a similar on-current upon switching of the ferroelectric polymer, while the off-current shows subtle but relevant differences. Furthermore, 2D numerical simulations were performed taking the specific diode geometry into account. It was seen that the model successfully reproduced the experimentally measured *I-V* characteristics with an identical set of parameters for both diode geometries and further explained the origin of the observed OFF-state current. Moreover, the findings of this work can be employed for further optimization of the memory devices, and light-emitting diodes with built-in ferroelectric memory functionality e.g. the MEMOLEDs.[34, 179]

3.2 The modified memory device structure

Poly(vinylidene fluoride-trifluoroethylene) (PVDF-TrFE) with the composition of 65%–35% was used as the ferroelectric polymer in this work. It was purchased from Solvay, Belgium. Poly(9,9-dioctylfluorene) (PFO) was used as the semiconductor polymer and was purchased from TNO, The Netherlands. All polymers were used as received. Cyclohexanone, was used as the common solvent and was purchased from Sigma Aldrich. Top polymer electrode, PEDOT:PSS (CLEVIOS P VP AI 4083) was purchased from Heraeus. All chemicals and polymers were used as received without further purification.

Conventional memory diodes, as shown in Figure 3.1a with Au (50 nm)/PFO:P(VDF-TrFE) (270 ± 10 nm)/PEDOT:PSS (70 nm)/Au (70 nm), were prepared from a solution of 4 wt. % PFO:P(VDF-TrFE) in cyclohexanone with a polymer weight ratio of 1:9. Both polymers were dissolved in a common solvent and the solution temperature was kept at 80 °C for about 1 hour.[180] The blend solution was filtrated using 1 μm polytetrafluoroethylene (PTFE) filters prior to film deposition. Next, the substrates were annealed in a vacuum oven (10^{-1} mbar) at 140 °C

for 2 hours to enhance the crystallinity of the P(VDF-TrFE) phase. Wire-bar coating technique was used for preparing polymer blend thin films for organic ferroelectric memory diodes. The instrument used was K202 control coater (RK PrintCoat Instruments Ltd, UK). The desired phase-separated morphology of the polymer blend films P(VDF-TrFE)/PFO was realized by controlling the glass substrate temperature. By the precise control of the substrate temperature, high quality thin films with low roughness were obtained. Polymer blend films of ~250 nm thickness were prepared. Devices were finished by deposition of top electrodes.[36] The final

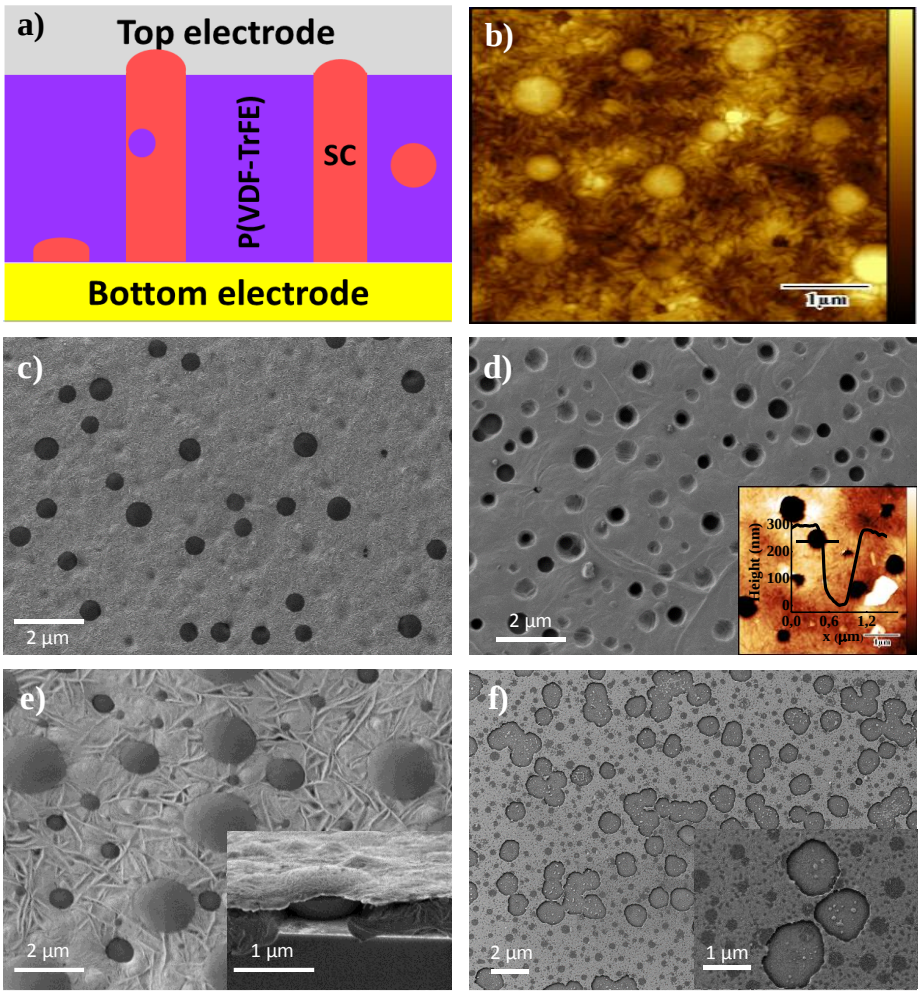


Figure 3. 2. a) Schematic illustrating the final device structure of the conventional memory diodes based on ferroelectric-semiconductor polymer blend. b) AFM and c) SEM images showing the phase separated morphology of PFO:P(VDF-TrFE) polymer blend. d) SEM and AFM topography images of the films after PFO removal. The height profile of the AFM image is from 0 to 300 nm (excluding the bright area which corresponds to dust). The line profile shows PFO domains are fully etched away. e) Top view SEM images of a PFO back-filled film after annealing (inset showing cross-sectional SEM image). f) SEM image of an etched Au electrode.

device layout is given in Figure 3.2a. Cr/Au was used as the bottom electrode in the fabrication of polymer blend memory diodes, with Cr acting as an adhesive between the glass substrate and the Au bottom electrode. Atmospheric thin-film processing of P(VDF-TrFE) leads to very rough films, due to vapor induced phase separation (VIPS).[38, 181] Increasing the substrate temperature suppresses VIPS and thereby allows for realization of ultra-smooth P(VDF-TrFE) thin-films suitable for microelectronic applications. Hence, to prevent VIPS and roughening of the surface, the substrate temperature is set at 70 °C. Formation of a phase separated microstructure, wherein the semiconductor polymer domains are continuous through the film thickness, is crucial for the operation of the diode. The bright circular domains are in the amorphous semiconductor phase. The surrounding matrix is P(VDF-TrFE) with a distinct needle-like microstructure.

For obtaining the device structure of diodes in Figure 3.1b, the following was done: after deposition of the PFO:P(VDF-TrFE) blend film, in order to realize a self-aligned etching mask for the gold bottom electrode, PFO domains were selectively etched away using an orthogonal solvent, e.g. hot toluene (60 °C) overnight.[177] Afterwards, the substrates were blow dried with nitrogen, following which, they were immersed in a diluted solution of $KI:I_2:H_2O$ (0.1:0.016 M or 0.05:0.008:27 mol ratio). To prevent severe gold under etching, the etching time was optimized to about 3 minutes. After the etching process, the substrates were thoroughly washed with DI-water and dried in vacuum oven at 80 °C for 2 hours. Subsequently, the holes in the P(VDF-TrFE) layer were back filled with pure PFO using spin coating. Pure PFO was prepared from a 0.5 wt% solution in toluene. After the PFO back-filling the films were annealed at 140 °C for 2 hours. There was no apparent formation of a PFO ad-layer.[37, 168] It should be noted that the memory diodes also operate if an ad-layer is present provided that its thickness is below 70 nm.[35] The devices were finished with deposition of the top electrodes.

For morphological analysis, SEM (using Zeiss 1530 Gemini) and AFM (using Nanoscope Dimension 3100) scanning was done at every step of device fabrication. Figures 3.2b and,-c show the top view AFM and SEM micrograph of the blend thin-film. The micrographs show typical morphology of the phase-separated PFO:P(VDF-TrFE). The average diameter size of the PFO domains amounted to 300-500 nm. The selective removal of the PFO domains is captured in the SEM image shown in Figure 3.2d. The inset shows the AFM height profile of the film. It can be seen that holes extend through the whole film thickness reaching the bottom contact.

The next steps of the bottom Au electrode etching, back-filling with PFO, and subsequent annealing at 140 °C is showing in Figure 3.2e. The inset provides the cross-sectional SEM image, showing a complete back-filling of the holes. It can be seen that the backfilled PFO domains in Figure 3.2e are larger than the PFO domains in Figure 3.2c because an excess amount of PFO was used for the backfilled case, resulting in overfilled domains. Besides, this overfill has no influence on the switching of the injection barrier since the experiments were done at the bottom contact. To evaluate the morphology of the Au bottom electrode, P(VDF-TrFE) masking layer was removed after the Au etching process by immersing the substrate in cyclohexanone overnight. The result is shown in Figure 3.2f, showing the SEM image of the etched Au bottom contact. Round holes are formed in the Au bottom electrode, exposing the glass substrate underneath. However, the size of the etched regions are slightly larger than the size of the removed PFO columns, which could be because of slight over etching of gold.

3.3 Electrical characterization

To investigate the working of the modified memory diodes, electrical measurements were carried out. For *I-V* measurements, Keithley 4200 SCS and 4155B Semiconductor Parameter Analyzer from Hewlett Packard was used. The device under test was kept in a probe station and bias was applied on the bottom electrode in all the measurements. The devices were kept under vacuum ~ 10^{-5} mbar. A voltage sweep from 0 V to +20 V and back from +20 V to 0 V was

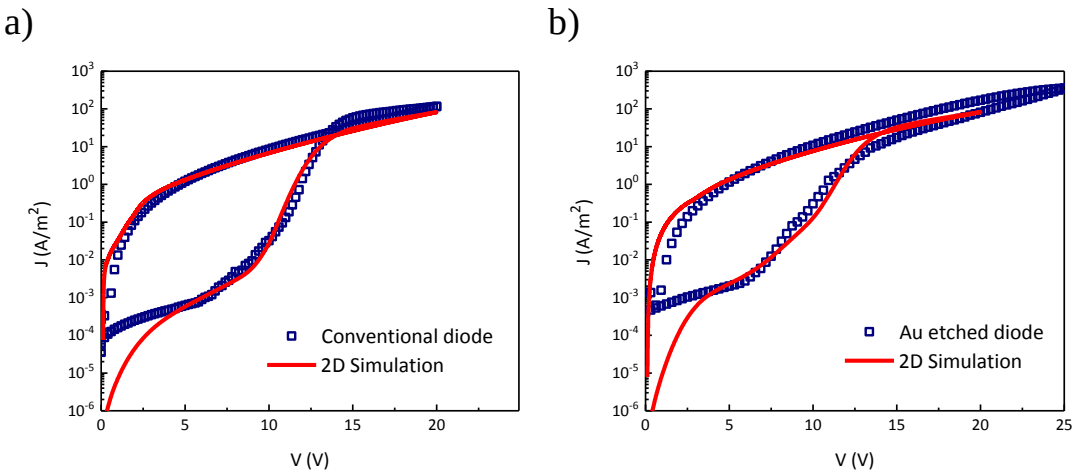


Figure 3. 3. Current-voltage characteristics of a a) conventional diode with device layout as shown in Figure 3.1a, and b) of a diode with etched gold bottom electrode, with a device layout as shown in Figure 3.1b. The solid lines are the results of the numerical 2D simulations.

applied to the bottom Au electrode, while keeping the top electrode grounded. For reference, *I-V* sweep characteristics of a conventional diode are shown in Figure 3.3a. In brief, the current density is low at low bias, since Au-PFO contact is injection limited. The device remains in the high resistance OFF-state. With increase in bias, P(VDF-TrFE) polarizes, increasing the current through the device, and the resistance is lowered by several orders of magnitude, putting the device in the ON-state. Upon sweeping back, the ferroelectric polarization is maintained, and the diode remains in the ON-state. The diode is put back into the OFF-state on application of a bias larger than the negative coercive voltage.

Interestingly, the Au-etched device demonstrated similar hysteretic *I-V* characteristics, as shown in Figure 3.3b. The ON-state current is almost the same as that of the conventional diode. However, the OFF current is marginally higher. Origin of this divergence will be discussed later in this chapter. Presentation of hysteretic *I-V* characteristics for the diode with modified contact is a conclusive proof of the ferroelectric memory diodes being interface devices, exhibiting charge injection through ferroelectric|semiconductor interface.

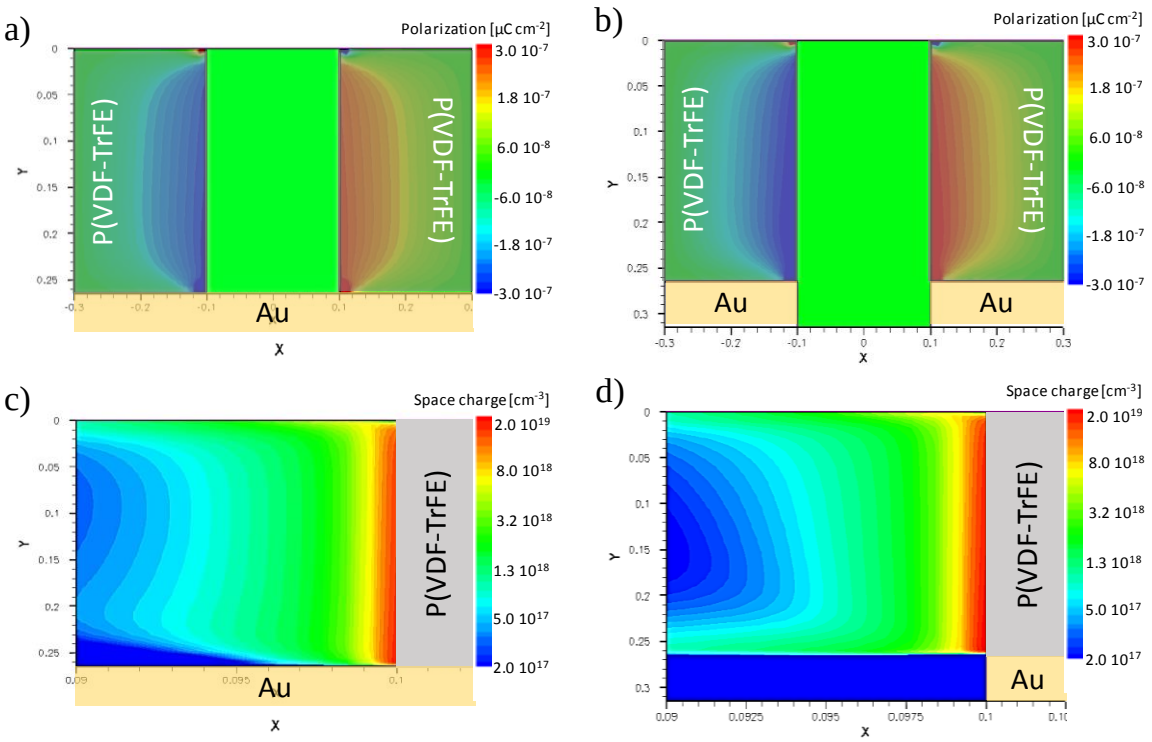


Figure 3. 4 *x*-component of the polarization vector in the ON-state for the device in a) conventional memory diode and b) Au-etched diode geometry. Hole density distribution in the PFO pillar in the ON-state for the device with c) conventional geometry and d) Au-etched diode geometry.

3.4 Numerical simulations

2D simulations were performed in order to support the above-mentioned experiment, focusing particularly on the point of contact between the injecting electrode and ferroelectric|semiconductor interface. In the model developed by M. Ghittorelli *et al.*, behavior of ferroelectric polarization with applied bias and charge conduction through the semiconductor phase is considered.[37, 138, 144, 162-165, 170, 172, 182, 183] The details of the model has been previously discussed in Chapter 2. Solid lines in the Figures 3.3a and, -b represent the simulation using the model, for conventional and Au-etched memory diodes, respectively. Parameters such as mobility and hopping distance were kept identical for both devices. For PFO, the average inter-site distance, d_a = 1.5 nm and the energy disorder parameter, σ = 0.16 eV. The HOMO level of PFO was taken to be 5.8 eV and the work function of Au, measured by Kelvin probe, amounted to 4.5 eV - 4.6 eV, resulting in an injection barrier of ~1.3 eV. The simulations reproduce the full hysteretic *I*-*V* characteristics.

Figures 3.4a and, -b shows the *x*-component of polarization of the P(VDF-TrFE) phase for both diode geometries at 20 V. It can be seen that same magnitude of polarization is formed in both cases. It can be recalled that the formation of this *x*-component of polarization is due to the large stray electric field between the polarization charges and the compensating image charges in the Au electrode. A zoomed-in image of charge accumulation profile for both diode geometries is shown in Figure 3.4c and, -d. It can be seen that the accumulated charge density at the PFO|P(VDF-TrFE) interface is 2 × 10^{19} cm^{-3} and is nearly 100 times lower at a distance of 10 nm away from the interface. Thus, both charge concentration profiles can be considered as similar.

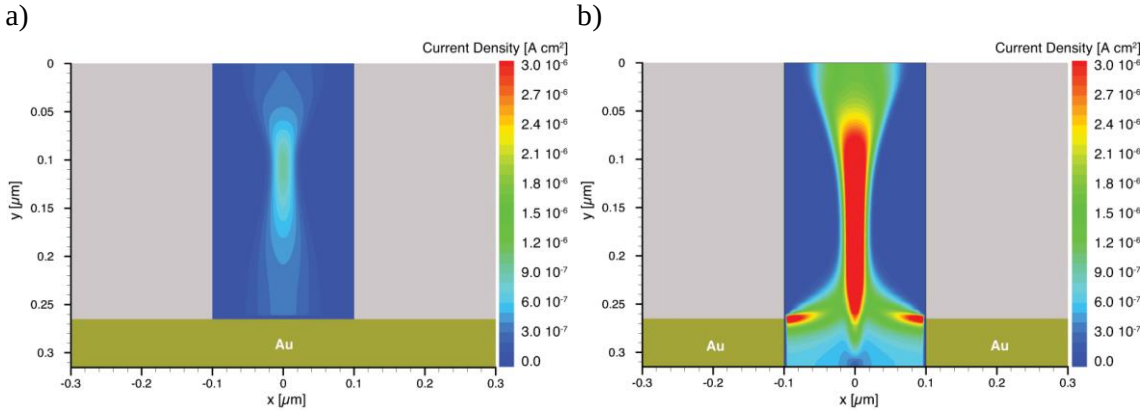


Figure 3. 5. OFF-state current density calculated with 2D numerical simulations at the bias level of 5 V for a) conventional diode structure and b) a diode with etched Au contact.

3.5 Origin of increase in OFF-state current

The model indicated that the OFF-state current in the Au-etched device is larger due to improved charge injection through the corner point of the etched contact electrode and ferroelectric|semiconductor interface. In conventional diodes, the OFF-state current is low because the electric field is facing the opposite direction. This impedes the charge carrier tunneling and hence, the contact remains injection limited. Furthermore, the electric field is maximum in the center of the bottom Au electrode, as shown in Figure 3.5a. On the other hand, in the diode with etched contact, the stray electric field is centered around the interface of Au|P(VDF-TrFE) with PFO. This leads to better charge injection and therefore, a better charge conduction through the center of the PFO phase, as can be inferred from Figure 3.5b.[36]

3.6 Conclusion

In summary, this chapter presented experimental demonstration of interfacial conduction in ferroelectric memory diodes. It was unambiguously shown, that the charge injection at the interface of the bottom Au contact and semiconductor|ferroelectric interface is dominated by the stray electric field there. For this purpose, a modified diode structure was realized, where, the Au contact beneath the PFO domains was etched away and then back filled with PFO. Thus, only the corner point of contact between Au and semiconductor|ferroelectric interface remained for the charge injection into the PFO. It was seen that the conventional and the modified structured diodes showed similar electrical behavior, which was also confirmed by performing 2D numerical simulations. A potential application of the modified diode structure could be in improving the performance of the MEMOLED device, which is a light emitting diode with an in-built ferroelectric switch. The semi-transparent Au electrodes in conventional MEMOLEDs lead to at least 50% loss in light output.[34, 184] Thus, etched Au bottom electrode can be employed in MEMOLED device structures to enhance light output. However, a crucial issue with conventional MEMOLEDs is their low electrical efficiency as compared to their OLED counterparts. The next chapter addresses this issue while following a comparative study of the charge trapping in conventional MEMOLED and pure semiconductor based OLED devices.

Chapter 4

Charge Trapping in MEMOLEDs

*MEMOLED concept has emerged based on tunable injection barriers. The MEMOLED is a light emitting diode with an inherent ferroelectric switch. However, the MEMOLED suffers from low light efficiency as compared to conventional LEDs. This chapter provides a quantitative analysis of capacitance-voltage characteristics of a PFO-P(VDF-TrFE) MEMOLED, and ascribes the low light efficiency to electron trapping by the P(VDF-TrFE) layer.**

*M. Kumar, and K. Asadi *Charge trapping in MEMOLEDs*. Under Preparation.

4.1 The MEMOLED: Memory + OLED

Polymer based light emitting diodes (PLEDs) have received considerable attention due to their potential for application as printed large-area full-color displays and lighting.[183, 185-187] The PLED displays are envisioned for signage applications. The challenge is simplifying the driving scheme and reduction in the processing steps.[188, 189] To address this issue, a new light-emitting device concept, i.e., the MEMOLED was introduced.[190] The MEMOLED is an organic light emitting diode with an integrated resistive bistable memory, based on a phase-separated blend of a light emitting semiconductor polymer (PFO) and a ferroelectric polymer (P(VDF-TrFE)). A semitransparent gold bottom electrode was chosen as the anode and Ba/Al as the cathode. The energy level difference between the highest occupied molecular orbital (HOMO) of the *p*-type semiconductor phase and the poorly injecting electrode leads to the formation of an injection barrier. The conduction mechanism is again based on ferroelectric polarization induced modulation of injection barrier at the semiconductor and the metal interface leading to resistive switching between two non-volatile states for light emission.[28, 38, 40, 191] Figure 4.1a shows current voltage characteristics of a PFO:P(VDF-TrFE) polymer blend which shows bistability in the forward bias. On reaching the coercive voltage (~11 V) of P(VDF-TrFE), the diode switches from a high resistance OFF state to a low resistance ON state. The corresponding electroluminescence plot is shown in Figure 4.1b, which illustrates the bistability of the light output in the forward bias. The OFF state of the diode is dominated by trap limited electron current which leads to leakage causing no light output to be seen. Light emission begins with the onset of the ON state, i.e., with injection of holes into the semiconductor at coercive voltage.

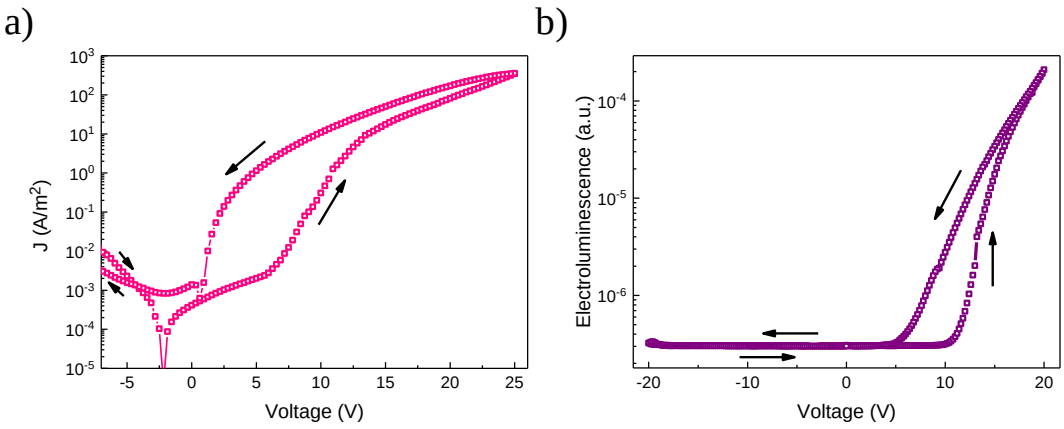


Figure 4. 1. a) Current voltage (*I-V*) characteristics of a MEMOLED with PFO:P(VDF-TrFE) blend, showing electrical bistability. b) Electroluminescence of the MEMOLED showing hysteresis corresponding to the hysteretic *I-V* curve.

This kind of device structure is ideal for passive matrix geometry, wherein, the integrated memory can be programmed to allow active addressing of the polymer LEDs.[34]

The current efficiency (ratio of photocurrent and electrical current) of these MEMOLEDs, however, when compared with that of PFO-only based PLED, is much lower. The reason behind this is still unclear.[191-194] In this chapter we demonstrates that trapping of electrons at the interfacial boundaries could be the origin of this lower efficiency. As stated in the previous chapter, Ghittorelli *et al.* quantitatively analyzed the device physics of the ferroelectric memory diodes based on phase separated PFO and P(VDF-TrFE) polymer blends.[37] They concluded that the charges from the electrodes are efficiently injected into the semiconductor and the injected charge carriers are located at the ferroelectric-semiconductor interface. Due to the LUMO levels of the two polymers being relatively close to each other, many electrons tend to fall into these interfacial traps leading to non-radiative electron-hole recombination, thus, leading to decrease in the light output from the devices.[191] Electron trapping can lead to changes in the relaxation time of the charge carriers and in the capacitance of the devices. It has been previously reported, that organic LEDs that inject both electrons and holes can result in negative differential capacitance at low frequencies.[191, 193, 195, 196] This negative capacitance can arise due to several factors, including charge accumulation at organic interfaces[196], bimolecular recombination[195], charge injection through interfacial states[193], and self-heating.[191] The comparative changes in the relaxation time of the MEMOLEDs and the PFO LEDs are in correspondence with trap-assisted recombination.

4.2 Current efficiency comparison of MEMOLED and PFO based LED

MEMOLED devices with the structure Au (20 nm)/ PFO:P(VDF-TrFE) (250 nm)/ Ba(5 nm)/ Al (100 nm), were prepared from a solution of 4 wt. % PFO:P(VDF-TrFE) in THF, with a weight ratio of 1:9 using wire-bar coating.[197, 198] The substrates were annealed in a vacuum oven (10^{-1} mbar) at 140 °C for 2 hours to enhance the crystallinity of the P(VDF-TrFE) phase. Only PFO based LEDs were also fabricated with the device structure Au (20 nm)/ PFO (210 nm)/ Ba(5 nm)/ Al (100 nm) from a solution of 1 wt. % PFO in THF. Electrical characterization was carried out under N_2 atmosphere with a Keithley 2400 source meter and, light output was recorded with a calibrated Si photodiode. The impedance data was taken using Agilent 4284a LCR meter with a DC bias swept from -15 V to 15 V, superimposed by an AC bias of 100 mV at various frequencies, *f*. In this measurement, the time varying current is measured across the

device. The ratio of voltage and current is given by a complex number known as impedance, *Z*. The measurement gives the phase difference between current and voltage curves, θ and impedance. The capacitance, *C* and resistance, *R* values can be calculated according to the following:

$$C = \frac{1}{2\pi f Z sin\theta} \quad 4.1$$

$$R = \frac{-1}{2\pi f C tan\theta} \quad 4.2$$

As a first step, an electroluminescence measurement was conducted for the MEMOLED fabricated with the blend of PFO:P(VDF-TrFE) as shown in Figure 4.2a. At approximately 12 V, which corresponds to the coercive field of the P(VDF-TrFE), the diode switches from the high resistance (OFF) state to the low resistance (ON) state. Hole dominated current flows through the semiconductor PFO and light emission sets in. During the backward sweep, the current remains high because the dipoles of the ferroelectric remain switched. However, the light emission continues down to +5 V below which the current is trap limited.[190] The diode remains in the OFF state in the reverse bias until -15 V with no light emitting out of the device as the semiconductor-metal junction remains injection limited. Thus, the hysteresis in the curve indicates switching of the ferroelectric above the coercive field, which also correspondingly makes the light output bistable. PFO LEDs were similarly characterized for electroluminescence. The current efficiency of MEMOLED compared with that of a PFO LED

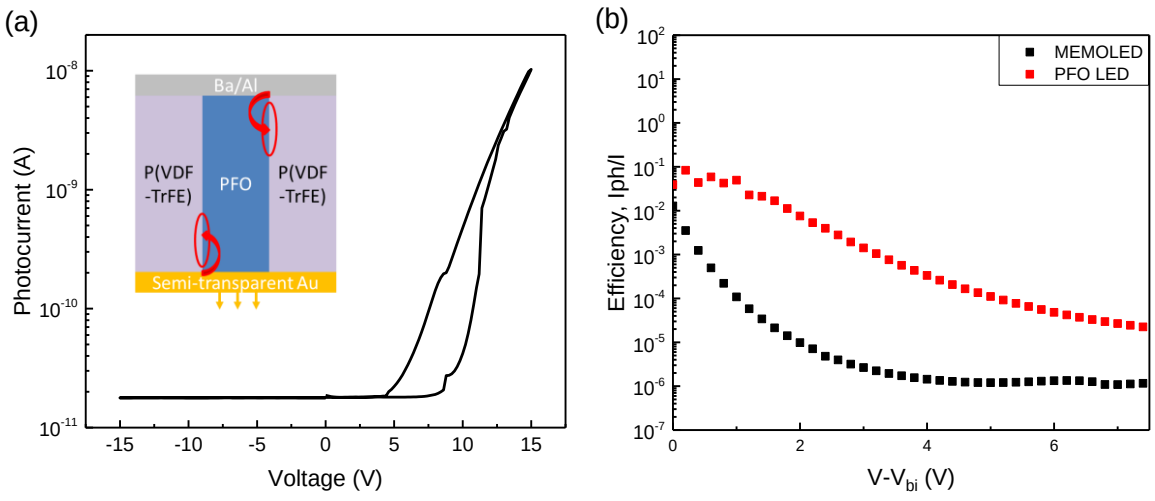


Figure 4. 2. a) Electroluminescence showing switching of the light output above coercive field of the ferroelectric. b) Current efficiency comparison for PFO-P(VDF-TrFE) based MEMOLED and PFO based LED (*x*-axis: voltage is corrected by built-in voltage of both the devices).

is shown in Figure 4.2b. It can be clearly seen from the plots that the current efficiency of the PFO LED is higher than the former by almost two orders of magnitude.

4.3 Impedance spectroscopy

In order to study the capacitance-voltage (*CV*) characteristics, impedance spectroscopy measurements of the MEMOLED devices were carried out. Figure 4.3a shows the capacitance of a PFO-P(VDF-TrFE) device as a function of frequency. At the positive bias, when the MEMOLED is in the ON state and the metal-semiconductor junction is Ohmic, the capacitance equals geometric capacitance, C_0 of the device given by Eq. 4.3. As the voltage is decreased down to -20 V, the capacitance starts to decrease as the device enters the OFF state. The capacitance becomes negative as the charge conduction becomes electron-trap limited. At a low frequency of 20 Hz, the minimum value of capacitance that is reached is -40 μF at 20 V. This decrement in the capacitance becomes weaker as the frequency is increased.

For comparative analysis, impedance spectroscopy of the only PFO LEDs was also carried out in a similar manner. Figure 4.3b shows the *CV* plot at different frequencies for a PFO LED. It should be noted that the minimum capacitance reached at 20 Hz is almost -0.2 μF which is almost two orders less than that for MEMOLEDs. It can be inferred from both the data sets that the increased negative capacitance for the PFO-P(VDF-TrFE) based devices can be due to an increment in the electron traps on blending P(VDF-TrFE) with PFO polymer. This leads to an enhanced electron trap density at the interface of the polymers. To validate this

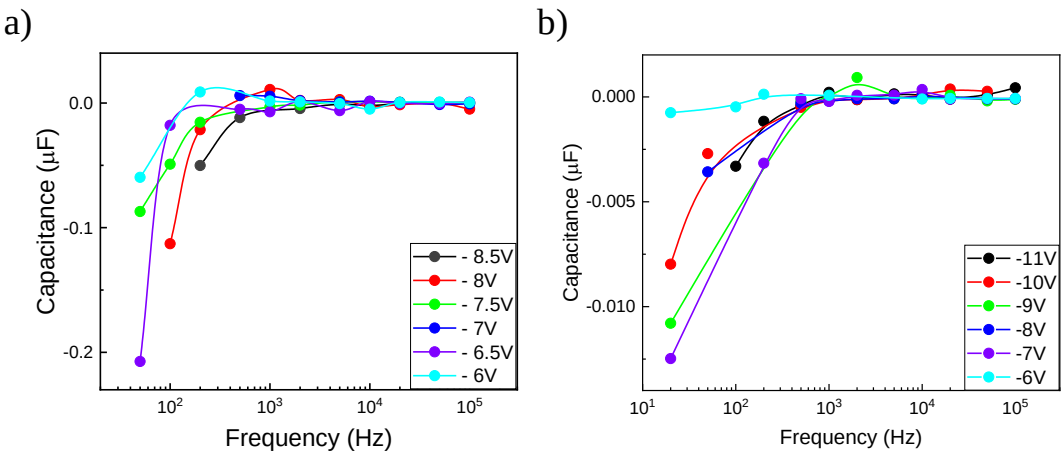


Figure 4. 3. Differential capacitance versus frequency plot with varying voltages for a a) MEMOLED device and b) PFO based OLED.

theory, a detailed analysis of the trap densities and relaxation time of the electrons is demonstrated in this work.

4.4 Electron trap density analysis

Electron trap density can be quantified by studying the electron-hole transport for trap-assisted recombination. According to Niu *et al.*,[191] the origin of the negative capacitance is related to the positive derivative of the transient current (here, recombination current, j_r), which is in response to a voltage step, ΔV.[197, 198] The capacitance related to this transient current is given by

$$C(\omega) = C_0 - \frac{\alpha\tau_r}{1+\omega^2\tau_r^2} \qquad 4.3$$

where C_0 is the geometrical capacitance of the device given by $\varepsilon_0\varepsilon_r A/d$, A being the area of cross-section and d being the thickness, ω is the angular frequency, α is a proportionality factor (that scales with recombination current at t = 0), and τ_r is the relaxation time.[197, 199]

In addition, the rate for trap-assisted electron-hole recombination, R is given by

$$R = C_n C_p N_t(np - n_1 p_1)/[C_n(n+n_1) + C_p(p+p_1)] \qquad 4.4$$

where C_n and C_p are the electron and hole capture coefficient, respectively, proportional to electron-hole mobility, N_t is the trap density, n and p are the density of electrons and holes in

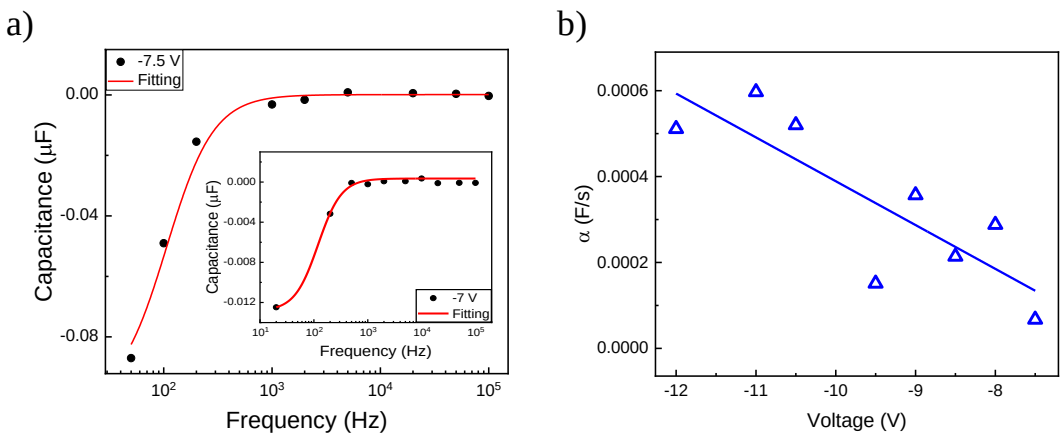


Figure 4. 4. a) Capacitance versus frequency plot for MEMOLED with black circles donating experimental data and red line represents fit using Eq. 4.3. The inset depicts the data and fitting for a PFO LED. b) α(V) as function of voltage calculated via fitting Eq. 4.3 at different frequencies.

their respective bands, and n_1 and p_1 satisfy the equation: $n_1 p_1 = N_{cv} \exp(-E_g/kT) = n_i^2$ with n_i being the intrinsic charge concentration.[191, 199]

The expression for R can further be simplified, using the approximations, $C_n = C_p$, $np \gg n_1 p_1$ and $n \approx p$ for polymer based LEDs, to

$$R = C_p N_t p/2 \quad (4.5)$$

which gives the relaxation time as the following[191]

$$\tau_r = 2/C_p N_t \quad (4.6)$$

Eq. 4.3 is used to fit the experimental data of capacitance vs frequency at different voltages for MEMOLED (as shown in Figure 4.4a), with τ_r and α as the fitting parameters. A voltage independent value of relaxation time, τ_r of 0.5 ms is obtained. It should be noted that the negative capacitance is seen only in a limited voltage regime, which in our case, is the OFF state of the device, when the charge injection is limited due to injection-limited barrier between the metal-semiconductor. Moreover, a steep increase of α with "negative" voltage is also observed (Figure 4.4b), consistent with previous reports on electron traps in PLEDs. It has been shown that α(V) has voltage dependence similar to that of current. However, the dependence of carrier mobility on field and charge density makes α(V) behavior near exponential, as can be seen from Figure 4.4b.[191, 200] The hole capture coefficient given by $C_p = q\mu_p/\varepsilon_r\varepsilon_0$ amounts to 3.0 x 10^{-18} m^3s where, ε_r = 8.0 is obtained from the *C vs f* curve and previously reported value of hole mobility, μ_p = 1.3 x 10^{-9} m^2/Vs is used.[194] The estimated electron trap density N_t then equals 1.3 x 10^{21} m^{-3}, using the Eq. 4.6.

To further investigate whether non-radiative trap-assisted recombinations are indeed due to negative capacitance, only PFO devices were similarly characterized. The data from impedance spectroscopy measurement carried out for PFO LEDs was fitted using Eq. 4.3 and τ_r was determined from the frequency response, corresponding to a value 2.0 ms. Following the discussion above, the C_p was estimated to be 10.6 × 10^{-18} m^3s with ε_r = 2.2, which further results in the electron trap density, N_t of 9.5 × 10^{19} m^{-3}. It should be noted that for the analysis of these PLEDs, the value of hole mobility remained the same for both cases. This is due to the fact that only the number of electron traps increase and the PLED current is hole dominated.[201] It can be clearly seen that the relaxation time increases for MEMOLED as well as the electron trap density on blending PFO with P(VDF-TrFE). Charge transport in PFO based light emitting diodes has been extensively studied and it has been pointed out that the electron current is

strongly reduced as compared to the hole current. This has been attributed to trap-limited charge conduction.[121, 183, 202, 203] These electron traps are present near the anode interface which leads to unbalanced charge conduction at higher electric fields, which further leads to non-radiative recombinations of these trapped electrons with the holes.[194, 202, 204] The electron trap distribution is identical for most of the conjugated polymers lying at an energy level of about 3.6 eV and having concentration of about 10^{23} m^{-3}.[183, 205] In addition to this, the LUMO of P(VDF-TrFE) also lies at about the same level as that of the electron traps.[206, 207] Due to this reason, the injected electrons can be trapped in the P(VDF-TrFE) film. The trapped charges provide the required compensation charge to stabilize the ferroelectric. However, as soon as the field is removed, the trapped charges undergo slow detrapping and return to the electrode. As a result, the polarization cannot be stabilized anymore and the P(VDF-TrFE) slowly depolarizes in time. In the diode, this depolarization manifests itself in reduced ON-current density, as shown in Figure 4.5. The diode with both Au top and bottom electrodes show an stable ON-state current whereas the diode with Au bottom and Ba/Al top electrode shows unstable ON-state current, hence proving the assumption of charge trapping at the interfaces.

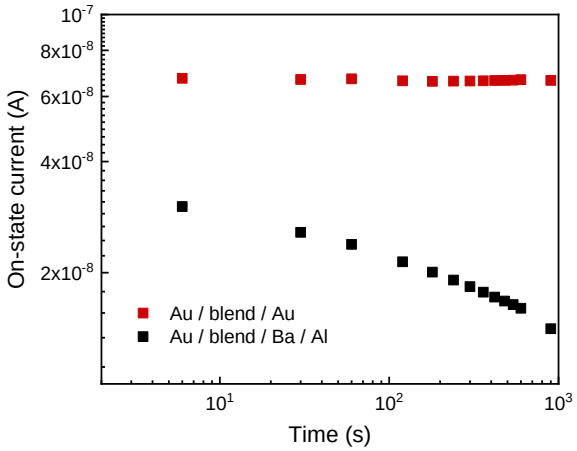


Figure 4. 5. Illustration of depolarization of P(VDF-TrFE) in diodes with different top electrode configuration.

4.5 Conclusion

To summarize this chapter, it was demonstrated that impedance spectroscopy can be used to quantitatively determine the trap densities in organic bipolar MEMOLEDs. The negative capacitance observed in the *CV* characteristics of MEMOLEDs was characterized by relaxation time for trap-assisted recombination and was found to be larger than that of only PFO based

light emitting diodes. Enhancement of the negative capacitance in P(VDF-TrFE) based MEMOLEDs can be explained by an increase in the number of electron traps in MEMOLEDs, which was determined to be 2.0×10^{22} m^{-3}. The results demonstrate the use of impedance spectroscopy in quantifying the electron trap density in organic bipolar devices and gives insight into understanding the charge transport in MEMOLEDs.

Chapter 5

Air-Stable Memory Array of Bistable Rectifying Diodes based on Ferroelectric-Semiconductor Polymer Blends

*Stability and reliable operation of memory arrays in air, are still the bottlenecks impeding upscaling of memories. In this chapter, fabrication and air-stable operation of the memory diodes in normal lab ambient (25 °C and 45% humidity) conditions are demonstrated. A 4-bit memory array that is free from cross-talk and with a shelf-life of several months, is presented.**

*The results of this chapter are published in M. Kumar, H. Sharifi Dehsari, S. Anwar and K. Asadi, *Applied Physics Letters* 112, 123302 (2018).[180]

5.1 Processing issues with organic memory diodes

Poly(vinylidene fluoride co-trifluoroethylene) (P(VDF-TrFE)) has been typically used as the ferroelectric polymer, in combination with a wide variety of organic semiconductors ranging from polymers to small molecules.[24-26] The diodes are processed from the ferroelectric:semiconductor mixture from a common organic solvent. The wet blend film goes through spinodal decomposition phase separation leading to a microstructure, wherein, round semiconductor domains are randomly distributed in the ferroelectric matrix.[39] The semiconductor domains are continuous through the film from the bottom to the top electrode.[28, 40] Furthermore, imprinted patterned microstructures have also been employed for realization of the memory diodes.[42, 168] Resistance switching has been realized by deliberately choosing an electrode that forms an injection limiting contact to the semiconductor phase. Upon switching of the ferroelectric, the stray field of the ferroelectric polarization facilitates charge tunneling over the barrier leading to essentially removal of the injection barrier at the electrode.[208] The robust performance of discrete diodes has been employed in realization of a 9-bit[29] and later a 1 kbit crossbar array of resistive switches, that were free from cross-talk.[30]

The fabrication processes of memory diodes have so far been conducted in clean rooms or inside N_2-filled gloveboxes with water and oxygen levels typically below 1 ppm. Ba/Al or LiF/Al have been used for the realization of rectifying diodes. As a result, the memory arrays can only operate in vacuum or inside a N_2-filled glovebox. The processing and device geometry are both prohibitive for large-scale production as well as for array operation under normal atmospheric conditions, such as 23 °C in air with 45% humidity. The phase separation of the blend is a complex three-phase (solvent : ferroelectric : semiconductor) process. Processing of the blend in atmospheric conditions further complicates the phase separation due the presence of water in the atmosphere. Most solvents used for the blend processing are miscible with water. Due to the ingress of water in the drying film, vapor-induced phase separation takes place, which eventually leads to very rough films. A high roughness leads to a large distribution of switching voltages and on/off ratios for discrete diodes, which further leads to reliability issues, thus impeding the realization of a functional array.[38, 209] Therefore, a rectifying diode design is required that eliminates air sensitive contacts, thereby enabling long shelf life. In this chapter, realization of air-stable bistable memory arrays with P(VDF-TrFE) as the ferroelectric and poly(triaryl amine) (PTAA) as the air-stable semiconductor, has been demonstrated.[210, 211] PTAA is a highly stable amorphous p-type semiconductor polymer, and is particularly used to study electrical transport in organic field effect transistors (OFETs). PTAA can be easily

handled in air which makes them ideal candidates for realizing stable devices that can operate in ambient conditions with mobilities greater than 10^{-3} cm^2 V^{-1} s^{-1}.[266-270] Thin-films were reproducibly fabricated using an optimized process for atmospheric conditions. Reactive electrodes were replaced by robust air insensitive contacts in the device stack. The yield of functional diodes was nearly 100%. It should be noted that the memory arrays were prepared, kept, and characterized under atmospheric conditions. The memory diodes showed air stability and robust performance, with an information retention time of more than two months and a shelf-life beyond several months. Moreover, a protocol was developed to boost the endurance of the memory array beyond 10^6 cycles. The findings bring the concept of the ferroelectric phase separated blends one step closer to the market.

5.2 Characterization of P(VDF-TrFE):PTAA memory diodes

Bistable memory diodes based on P(VDF-TrFE):PTAA polymer blend were fabricated via wire-bar coating. The mixing ratio of P(VDF-TrFE):PTAA was kept at 95:5 in weight. The polymers were dissolved in a common solvent, cyclohexanone, with a total solution concentration of 5wt. %. Cr/Au (1 nm/50 nm) served as the bottom electrodes and 100 nm of Al as the top. Blend film of 250 nm was bar coated (at a substrate temperature of 70 °C), which was later annealed at 140 °C for 2 hours. The work function of the Au electrode was measured using a Kelvin probe in the atmospheric conditions and amounted to 4.8 eV. The reported HOMO level for PTAA is at 5.1 eV.[212] The Au bottom contact therefore forms an injection barrier of nearly 0.4 eV with PTAA.

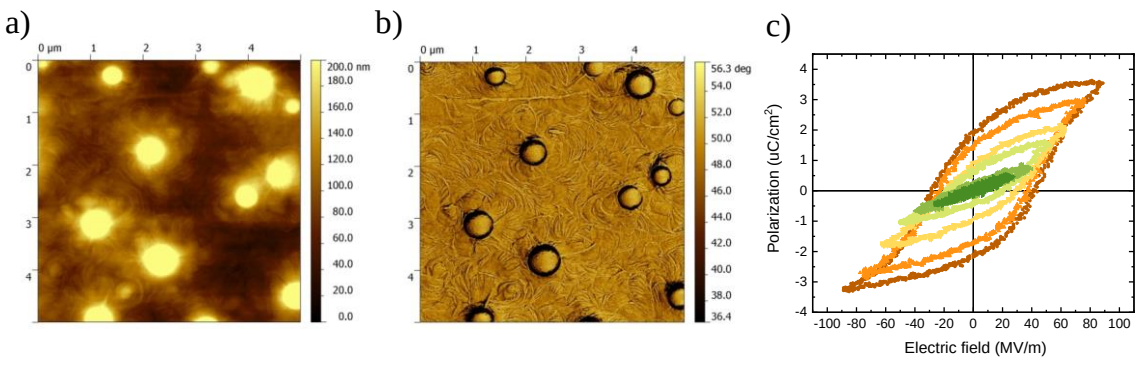


Figure 5. 1. Surface morphology of the blend, with 5 wt. % PTAA in the P(VDF-TrFE) matrix after annealing, shown in AFM a) height and b) phase images c) Hysteretic *P-E* loop of a ferroelectric memory diode.

Figure 5.1a and b shows the AFM height and phase images of the polymer blend film, illustrating the morphology. The bright circular domains are the amorphous PTAA phase. The surrounding matrix is P(VDF-TrFE) with distinct needle-like microstructure. In order to confirm ferroelectricity of the blend, Sawyer-Tower measurements were performed. Figure 5.1c shows the typical ferroelectric hysteresis loops of the diode. The coercive field and remnant polarization amounted to 30-40 MV/m and 2-2.5 μC/cm^2, respectively.

5.3 Programming of diodes

The *I-V* measurements were performed by applying the bias on the Au bottom contact while keeping the top Al contact grounded. Current increased upon increasing the bias from 0 V toward higher positive values and at approximately 15-17 V, a sudden rise in the current was observed. Upon sweeping the voltage back, the current showed the typical hysteretic response of the phase separated diodes and remained high. In reverse bias, sweeping from 0 V towards -40 V and back, the current remained low. However, at around -17 V, the current showed a peak which corresponded to the switching peak of the P(VDF-TrFE). Thus, the PTAA:P(VDF-TrFE) blend sandwiched between Au as injecting and Al as blocking contacts, forms a switchable rectifying diode. A typical *I-V* sweep is shown in Figure 5.2a. Digital information was coded by programming the device using voltage pulses of ± 40V (larger than the coercive bias). In order to read the programmed state, *I-V* was swept only for low voltages well below the coercive voltage, e.g. ± 5 V, as shown in the inset of Figure 5.2b. Depending on the polarity of the applied

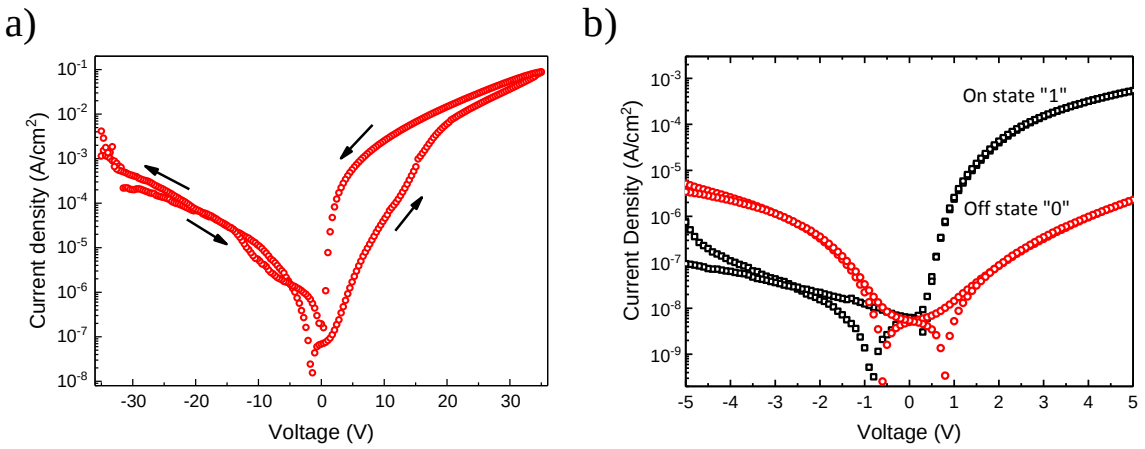


Figure 5. 2. a) Full *I-V* sweep demonstrating the bistable rectifying behavior. b) *I-V* measurement showing the low-voltage read-out of the programmed states of "1" and "0".

pulse, a high resistance "0" or a low resistance "1" state could be programmed, and then successfully read.

5.4 Data retention analysis

To study the long-term stability of the programmed states, retention time analysis of the ON- and OFF-states was carried out as shown in Figure 5.3. First, the high resistance OFF-state was programmed and measured over a course of two months. No increase in the OFF-state current was observed. Afterwards, the low resistance ON-sate was programmed. The ON-state current was stable for more than a week, and it shows only slight degradation after two months. Memory window of 10 orders is still maintained after degradation.

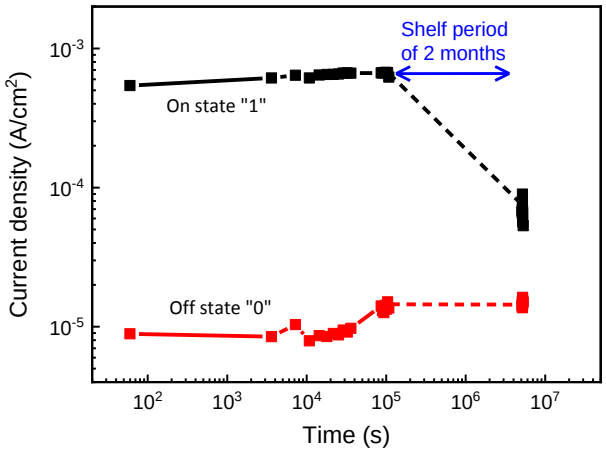


Figure 5. 3. Data retention measurement obtained for a diode after programming it in either the ON state or OFF state.

5.5 Cycle endurance measurement

Cycle endurance tests were carried out using Radiant Precision Multiferroic Test System (Radiant Technologies, Inc.). The fatigue measurements were done in order to study the degradation of the ferroelectric polarization with number of poling cycles. A time varying bipolar triangular waveform with different voltage amplitudes and frequencies was applied to the device under test. After a set of consecutive cycles, the remnant polarization was determined in the device. For the cycle endurance test, consecutive switching pulses of ±20 V were applied and ON- and OFF-state currents were then subsequently read at low bias (+5 V). It was observed that after nearly 1000 cycles, the polarization quickly drops to zero as shown in Figure 5.4a. After the value of number of cycles reached 10^6, the diode could not be polarized anymore and on/off ratio dropped to one.

It has been observed in P(VDF-TrFE) capacitors that, upon continuous cycling, the polymer chains break and lead to formation of HF gas, which accumulates under the top electrode causing its delamination and thus, results in loss of contact.[213, 214] To cope with the problem of delamination of the top contact, and hence enhance cycle endurance, a waiting period of 5 seconds was introduced between two consecutive programming pulses.[215] Using the modified pulsing scheme significantly enhances the endurance of the diodes. As shown in the Figure 5.4a, at 10^6 the normalized polarization is still at 70% of its original value. In spite of a 30% drop in the polarization, the ON-and OFF-state currents remained insensitive to polarization drop and therefore unaltered for the number of cycles approaching 10^6, as shown in Figure 5.4b.

5.6 Array measurement

Integration of discrete PTAA:P(VDF-TrFE) diodes into a functional cross-bar memory arrays has been discussed in this section. A 2 × 2 bit memory array constitutes the simplest crossbar array, consisting of two word lines and two bit lines, which yields 4 bits with 16 different logic states, as schematically shown in the Figure 5.5a. One of the most challenging logic states prone to crosstalk are 1110 states, where “1” and “0” refer to the low resistive ON-, and high resistive OFF-states respectively.

To program the array, initially, all bits were put in the OFF-state. Individual bits were programmed by a half-voltage scheme[29]: one half of the programming voltage +/−10 V was

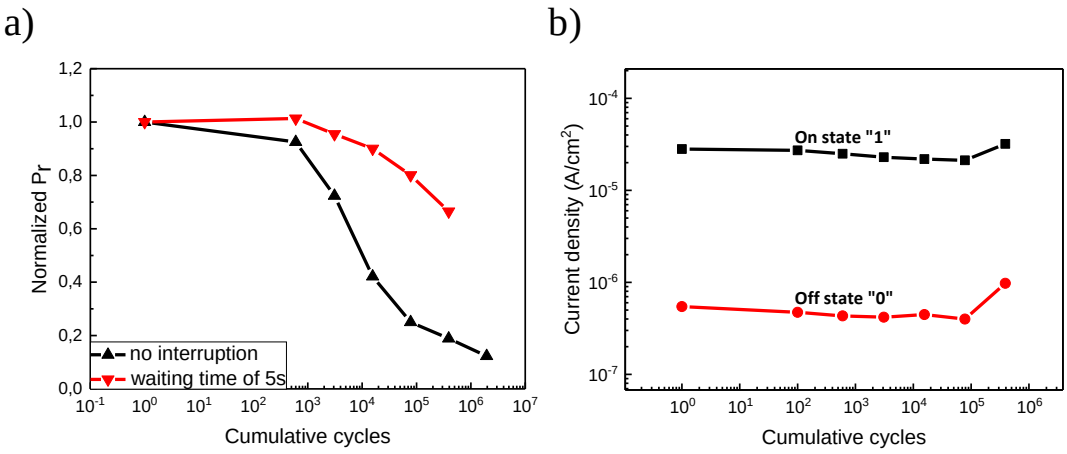


Figure 5. 4. Fatigue measurements a) Polarization measurement after consecutive application of switching pulses of ±20 V. b) Cycle endurance of the diodes tested with interrupted waveforms every second with a waiting time of 5s and measuring on and off current levels at low bias.

applied on the word line and the other half of the voltage −/+10 V on the bit-line, while grounding all other lines. After programming, the logic state of each individual bit was read out by measuring the current at +5 V, using the similar half-voltage scheme. The measured 1110 logic state is demonstrated in Figure 5.5b. Three different current levels are easily distinguishable. When none of the bits are addressed the current level is dominated by background leakage current. It can be seen that the current level of a bit in the OFF-state, state "0", is distinctly lower than the ON-state current, state "1". In addition, different permutations of the logic state 1110, i.e., 1110, 1101, 1011, were easily programmed and read out non-destructively under ambient conditions.

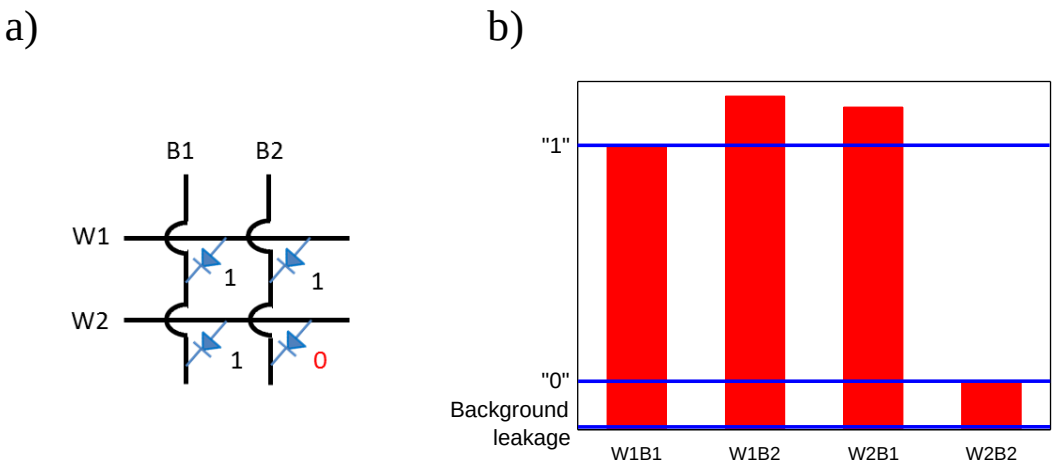


Figure 5. 5. a) Schematic of cross-bar memory array configured. b) Array measurement showing the read-out of "1110" state, which is the most challenging memory state. The current density level for "1"and "0" is 3×10^{-6}A/cm^2 and 3×10^{-7} A/cm^2, respectively.

5.7 Conclusion

In summary, in this chapter, a 4-bit functional cross bar memory array using unpatterned thin-films of P(VDF-TrFE):PTAA blend was demonstrated. The fabrication steps and subsequent array characterizations were carried out in laboratory atmospheric conditions and under conventional laboratory lighting conditions. The most challenging logic state of the array, i.e., 1110 state, could be programmed and unambiguously identified. The shelf life and information retention time of the diodes was observed to be of more than two months. The endurance of the array exceeds 10^6 cycles which shows an improvement, orders of magnitude larger in comparison to what has been previously reported in the literature. Demonstration of the air-stability brings organic ferroelectric diodes arrays one step closer toward upscaling and

commercialization of the cost-effective disposable memories needed for instance in packaging applications.[24, 216]

Chapter 6

Colossal Tunneling Electroresistance in Co-Planar Polymer Ferroelectric Tunnel Junctions

*Ferroelectric tunnel junctions (FTJs) are emerging as promising non-volatile resistance switching devices that operate based on the modulation of the tunnel barrier by the polarization of the ferroelectric layer. Despite the simplicity of the concept, FTJs have remained only as a scientific curiosity due to the lack of an industrially viable lithography based manufacturing technique. In this chapter, we demonstrate resistance switching in poly(vinylidenefluoride-co-trifluoroethylene), P(VDF-TrFE), based FTJs by employing planar nanogap electrodes fabricated with adhesion lithography. Using the nanogap with asymmetric metallic electrodes, we have obtained a giant tunneling electroresistance (TER) that approaches 10^6 % at room temperature. The tunneling nature has been corroborated using Simmons direct tunneling model. Demonstration of TER in co-planar nanogap electrodes fabricated using this, scalable lithography-based nano-patterning technique, could pave the way to low-cost and large-scale manufacturing of FTJ for emerging memory applications.**

*Results from this work have been published in the reference M. Kumar, D. G. Georgiadou, A. Seitkhan, K. Loganathan, E. Yengel, H. Faber, T. D. Anthopoulos, and K. Asadi, *Advanced Electronic Materials* 1901091 (2019).[274]

6.1 Introduction

A polymeric ferroelectric tunnel junction (FTJ), is the last missing resistance switching device based on ferroelectric polymers.[217] In brief, The FTJ, an extension of polar switch proposed by Esaki *et al*.,[218] is a metal/ferroelectric/metal junction with the ferroelectric layer being thin enough to allow for quantum mechanical tunneling of charge carriers. The resistance of the junction, or tunneling electroresistance (TER), switches between two nonvolatile states through the reorientation of polarization of the insulating ferroelectric tunnel barrier.[219-223] Hence, FTJs are ideal for memory and neuromorphic applications.[52, 218, 224, 225] This work focusses on P(VDF-TrFE) based FTJ, which is known to be the last missing resistance switching device. Due to challenges associated with contact formation to soft polymeric ultra-thin films, and the lack of a reproducible and industrially viable fabrication method, reliable P(VDF-TrFE)-based FTJs have not been demonstrated yet.[226]

Out of plane vertical stacks of metal/ferroelectric/metal layers have been the focus of ferroelectric community, for the fabrication of the FTJs.[219-223] The critical step in the fabrication of a FTJ is defining the metal top electrode. Direct vapor deposition of metals such as Au and Pt onto the thin ferroelectric layer can easily create local electrical shorts.[227] Deposition of reactive metals is not desired due to the formation of an interfacial non-ferroelectric dead-layer.[228, 229] Alternatively, FTJs have been realized using scanning probe techniques such as piezoresponse force microscopy (PFM) and conductive atomic force microscopy (C-AFM).[217, 219, 230-233] The probe techniques, however, suffer from poorly defined contacts, device area and scalability.[234] Hence, for viable FTJ memories, there is still much need for a reliable lithography-based technique that allows reproducible fabrication and enables upscaling and integration.

6.2 Planar FTJs

Planar devices such as break junctions with metal electrodes separated by a few nanometers, have been successfully used by the molecular electronics community for the study of charge transport in single molecules.[231, 235] The advantage of in-plane configuration is that the electrodes can be fabricated before deposition of the ferroelectric layer. However, techniques like break junctions have low device throughput and are therefore, ideal only as research.[220, 221, 236] Recently, in an attempt to alleviate the poor scalability issues of the break junctions, a lithography-based method, namely adhesion lithography (a-lith) has been demonstrated for rapid fabrication of nanogap electrodes, with typical gap spacing between 4 - 10 nm,[234-237] and

have successfully been employed to demonstrate memristors based on both inorganic and organic semiconductors.[238, 239] In this work, adhesion lithography has been employed to fabricate a nanogap with asymmetric electrodes. P(VDF-TrFE) is used as the ferroelectric polymer that demonstrate stable and reproducible giant TER approaching 10^6 %. The FTJ is a non-volatile two-terminal resistive memory with rectifying behaviour and shows time-invariance of the tunneling current in the programmed states. It has been unambiguously shown that the current transport through a FTJ is dominated by tunneling which is modulated by ferroelectric polarization.

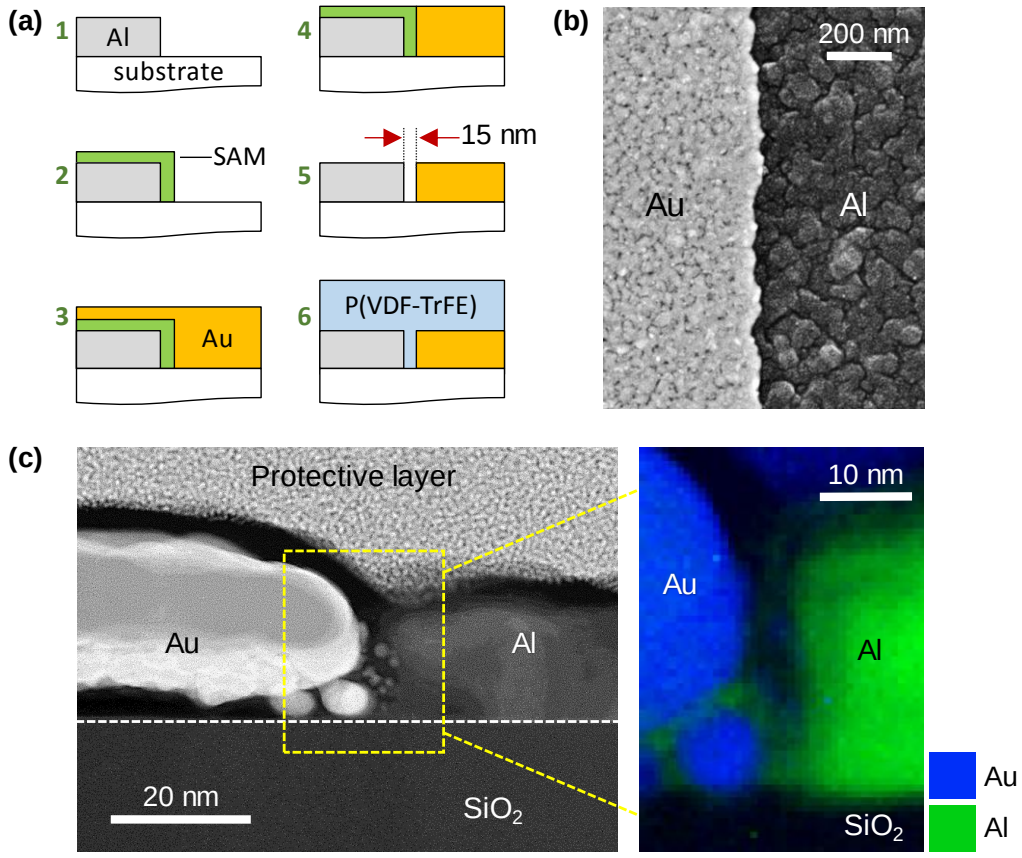


Figure 6. 1. a) Schematic showing the device fabrication using the principle of adhesion lithography for the patterning of nanogap asymmetric Al/Au electrodes (1. Al deposition and photolithography patterning, 2. SAM (self-assembled monolayer) functionalization of Al, 3. Au deposition, 4. Au removal from SAM-functionalised area of Al, 5. SAM burn off and empty nanogap formation) and finished off with P(VDF-TrFE) layer deposition (in 6). b) Top view SEM image depicting the Au/Al interface. c) Cross-sectional TEM image of the Au/Al nanogap area with elemental mapping, showing an inter-electrode separation less than 10 nm.

6.3 In-plane P(VDF-TrFE) based FTJ fabrication

As discussed earlier, the fabrication of nanogap electrodes has been done elsewhere, the details of which can be found in the reference.[234] Nevertheless, we briefly describe the fabrication of the nanogap electrodes in this section. Octadecylphosphonic acid (ODPA) was used as a self-assembled monolayer (SAM). Silicon (Si) wafers with 100 nm-thick silicon dioxide (SiO_2) were used as the substrate. All Si/SiO_2 wafers were first cleaned by ultrasonication in deionized water, acetone and isopropanol for 10 minutes and dried under a stream of dry nitrogen gas. Next, a 40 nm-thick layer of Al was deposited via thermal evaporation in high vacuum (10^{-6} mbar) and subsequently patterned via standard lift-off photolithography and then immersed in an isopropanol solution containing 1 mM ODPA for 20 hours to form a selective and dense SAM atop the native alumina (Al_2O_3) layer. The wafers were removed from the SAM solution, rinsed with isopropanol, dried with dry nitrogen gas and annealed at 75 °C on a hotplate for 10 minutes. The second Au electrode (80 nm) was then deposited via thermal evaporation under high vacuum. A thin coating of the commercial adhesive First Contact™ was applied from solution over the entire sample's surface and left to dry at room temperature for 30 minutes. The adhesive layer was then manually peeled-off to remove regions of the top Au layer

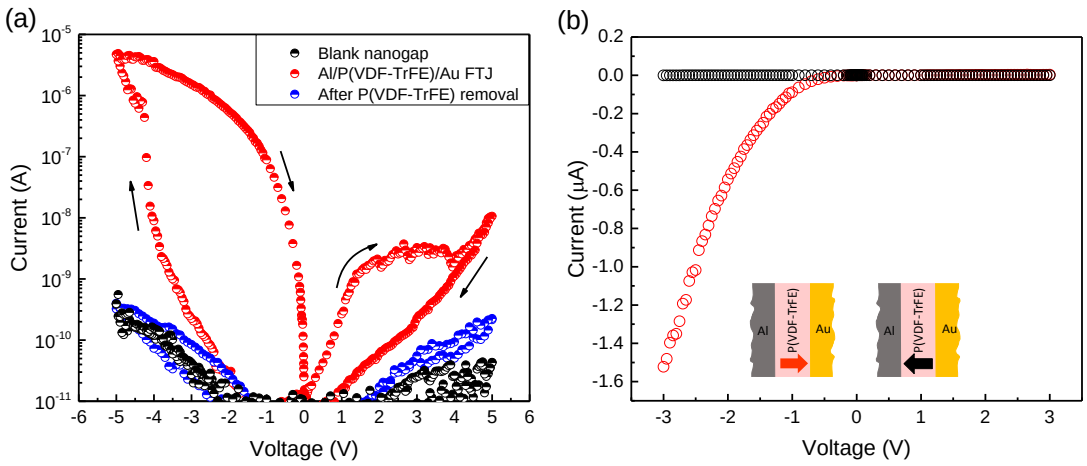


Figure 6. 2. a) *I-V* characteristics of the tunnel junction. Black symbols show the pristine empty nanogap, prior to deposition of P(VDF-TrFE) layer. Red symbols show the bistable switching behavior of the tunnel junction after deposition of P(VDF-TrFE) polymer. Blue symbols show the *I-V* of an empty nanogap device after washing off the P(VDF-TrFE) layer. At -3 V, TER ratio is ~ 10^6 %. b) The red and black symbols show the low-voltage *I-V* curves for the ON- and OFF-states of the Al/P(VDF-TrFE)/Au tunnel junctions for negative and positive polarization of the P(VDF-TrFE) layer, respectively.

overlapping with the bottom SAM-treated Al electrodes. The resulting patterns consisted of co-planar asymmetric Al/Au electrodes with a nominal inter-electrode gap of ~10 nm. Figure 6.1a displays the process steps used for the formation of the co-planar nanogap electrodes. The adjacent Al/Au electrodes are shown in the top view scanning electron microscopy (SEM) image in Figure 6.1b, where the presence of a homogeneous interface with nm-scale gap between the two metal electrodes is clearly visible. The extreme dimensionality of the nanogap can be better visualized in the cross-sectional transmission electron microscope (TEM) image shown in Figure 6.1c, where short inter-electrode distances < 10 nm can be discerned.

Prior to the deposition of the P(VDF-TrFE) layer, the substrates were subjected to 15 minutes UV/O_3 treatment to remove any traces of ODPA from the surface. P(VDF-TrFE) was dissolved in cyclopentanone (5 wt%) and was spin coated at room temperature atop the pre-pattern nanogaps resulting in a 300 nm-thick layer. The devices were annealed at 140 °C in a partial vacuum (1 mbar) for 2 hours to increase the crystallinity of the P(VDF-TrFE) layer. All electrical measurements were performed using a Keithley 4200 SCS in a cryogenic probe-station under high vacuum (10^{-6} mbar).

6.4 Electrical characterization of FTJ devices

To ensure the successful formation of electrically-isolated nanogaps, current-voltage (*I-V*) measurements were performed before deposition of the P(VDF-TrFE) layer. Bias was applied to the Au electrode, while keeping the Al electrode grounded. The bias was swept from 0 V to +5 V, to -5 V and back to 0 V. The current for the as-prepared (empty) nanogaps, shown with black symbols in Figure 6.2a, was in the order of 10 pA, and close to the detection limit of our measurement setup. Hence, it could be concluded that the Au and Al electrodes were electrically isolated- and, thus, reliable nanogaps have been formed. Afterwards, current transport through Au/P(VDF-TrFE)/Al nanogap devices was measured post deposition of P(VDF-TrFE) on top of the Al/Au nanogap electrode, as described in the previous section. The applied bias on Au was varied from 0 V to -5 V, to +5 V and back to 0 V. Figure 6.2a shows the *I-V* sweep. For the sweep direction from 0 to -5 V, the current was initially in the order of 10 pA. At nearly -2 V, the current showed an exponential rise with increasing |voltage|, and then showed a steep jump at -4 V from several nA to nearly 1 µA, eventually reaching 5 µA at -5 V. Upon back sweeping from -5 to 0 V, the current remained high and followed a different path, exhibiting a hysteretic behavior. During the sweep from 0 V to +5 V, in the beginning, the current showed exponential rise with bias up to nearly +2 V. Above +2 V the current saturated, and between

+4 V and +5 V, the current increased slightly. For the scan direction +5 V to 0 V, the current exponentially showed a decrease with the bias. The full *I-V* loop is hysteretic and shows a bistable rectifying behavior. It can be seen that the junction switches to the low-resistance ON- and the high-resistance OFF-state at -4 V and +4 V, respectively. The spacing between the Au and Al electrodes for the FTJs is less than 10 nm (Figure 6.1c). Thus, the electric field at which resistance switching occurs amounts to ~ 400 MV/m. This high value of coercive field coincides with those reported for ultra-thin films of P(VDF-TrFE).[240, 241] The occurrence of the resistance switching at electric fields comparable to the coercive field of P(VDF-TrFE) is a strong indication that the modulation of the resistance is due to polarization switching of the P(VDF-TrFE) ferroelectric layer. To explicitly attribute the measured *I-V* to polarization switching of P(VDF-TrFE), the polymer film was washed away from the junction in the next step. The current, as shown in Figure 6.2a, drops down to a value comparable to that of the as-prepared pristine junction, viz. 10 pA.

Programmability of the Au/P(VDF-TrFE)/Al junction was demonstrated by applying pulses of +/−5 V for 100 ms to set the junction into high/low-resistance states. The programmed state was subsequently probed using a voltage sweep between -3 and 3 V or a voltage pulse at ±3 V. As shown in Figure 6.2b, the Au/P(VDF-TrFE)/Al junction can be programmed into two distinct ON- and OFF-states. In the ON-state, the junction shows rectifying behavior, which is highly desired for memory applications.[36, 37, 180] The coplanar FTJ show a giant TER ratio of

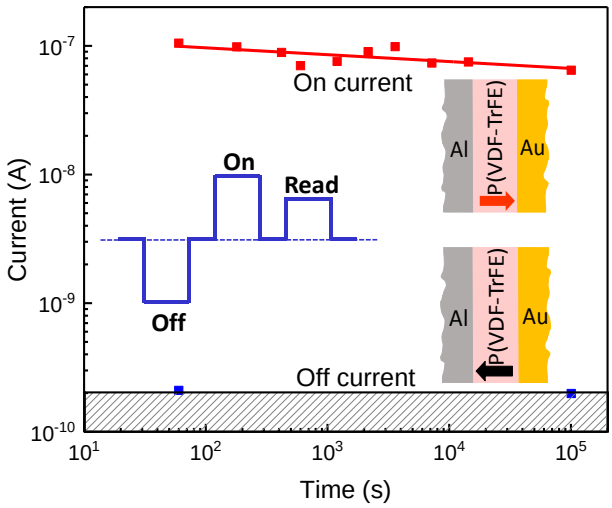


Figure 6. 3. Plot showing the program used for retention measurements of both ON- and OFF-states after polarizing the device by applying a voltage pulse of −/+ 5 V and reading at low voltage bias of −3 V.

8×10^5 %, approaching 10^6 %. The TER ratio has been obtained from the ON- and OFF-state currents at -3 V which amount to 8×10^{-7} A and 1×10^{-10} A, respectively.

For measurement of the retention time of the programmed resistive states, the FTJs were programmed into the ON- and OFF-states by application of ±5 V pulses, and the state at -3 V was read in time. Both the ON- and OFF-states did not show any deterioration for a period longer than 24 hours, as shown in Figure 6.3. The work functions of the Au and Al electrodes amount to 4.9 and 4.2 eV, respectively. Therefore, there is a built-in potential, $\Delta\varphi$, of 0.7 eV in the junction in the absence of the external bias. Considering that the nanogap is ~ 10 nm, the built-in field amounts to 70 MV/m. The coercive field at which P(VDF-TrFE) switches is 400 MV/m, which is nearly six times larger than the built-in field. Therefore, no back switching or depolarization of P(VDF-TrFE) would be expected. Consequently, a long retention time is anticipated and indeed is experimentally measured.

6.5 Mechanism of charge transport in FTJ

By sandwiching an ultra-thin insulator film between two metal electrodes, current can flow between the electrodes by tunneling of charge carriers through the insulating film. A number of theoretical studies have been performed explaining the tunneling phenomena. Sommerfeld

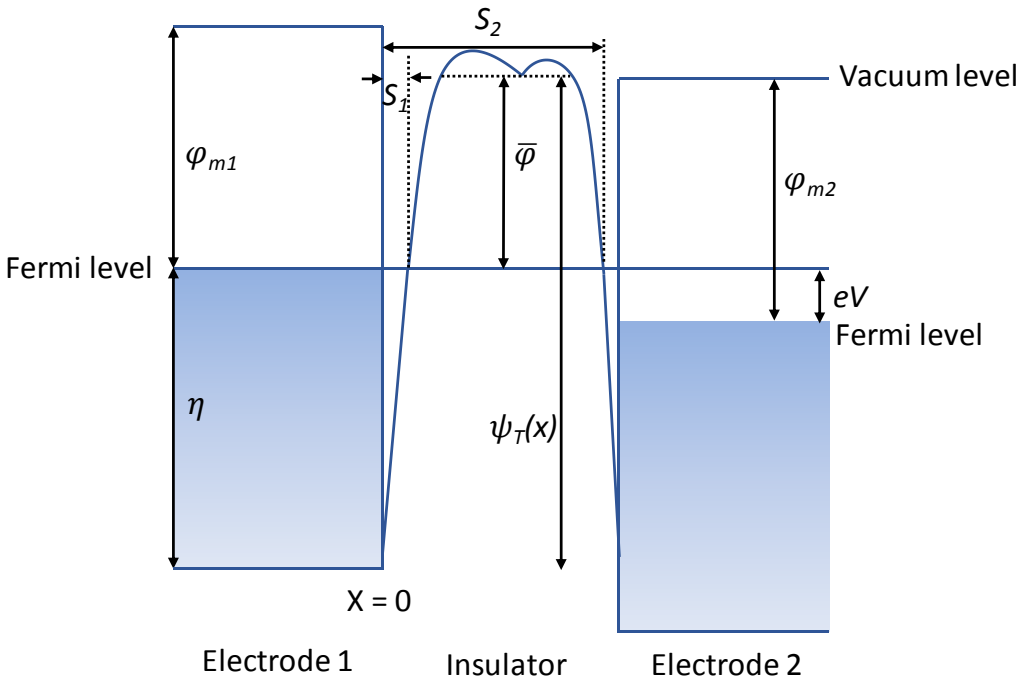


Figure 6. 4. Block diagram illustrating a generalized potential barrier of thin insulating film sandwiched between two metal electrodes.

and Bethe[271] presented the first theoretical study of tunneling at very low voltages and at high voltages using WKB (Wentzel-Kramers-Brillouin) approximation. The theory was later extended to include intermediate voltage regime,[272] or to take into account image potential and a symmetric parabola as approximation to the barrier potential.[273] In 1963 Simmon presented a unified theory based on tunneling current through a generalized barrier,[242] which takes into account low, intermediate and high voltage ranges more accurately and uses hyperbolic form of image potential.[242] If the potential barrier is assumed to extend in *x*-direction, then the probability of electrons tunneling across a potential barrier of height $\psi_T(x)$ and of thickness S_2-S_1 from electrode 1 to electrode 2 per second is given by WKB approximation

$$N_1 = \frac{4\pi m}{h^3}\int_0^{E_m} D_T(E_x)dE_x \int_0^{\infty} f(E)dE_r \qquad 6.1$$

Similarly, the number of electrons tunneling per second from electrode 2 to electrode1 to given by

$$N_2 = \frac{4\pi m}{h^3}\int_0^{E_m} D_T(E_x)dE_x \int_0^{\infty} f(E+qV)dE_r \qquad 6.2$$

where, E_m is the maximum energy of electron in the electrodes and $D_T(E_x)$ is the probability density function of electrons crossing the potential barrier. Detailed derivation of this probability density function is beyond the scope of this work.

The current density due to the net flow of electrons between the two electrodes is given by $J = q(N_1 - N_2)$. Following Simmons model[242, 243] for tunneling through insulating films with a generalized potential barrier, the current flowing through the junction is:

$$J = J_T\left[\bar{\varphi}\, exp\left(-C\bar{\varphi}^{1/2}\right) - (\bar{\varphi}+qV)\, exp\left(-C(\bar{\varphi}+qV)^{1/2}\right)\right] \qquad 6.3$$

where J_T, C and $\bar{\varphi}$ are current pre-factor, tunneling parameter, and the tunnel barrier height at the Fermi level of the electrodes. We note, C is proportional to electron's effective mass.

To investigate charge transport in the Au/P(VDF-TrFE)/Al junction, the device was programmed into the ON-state, and *I-V* sweeps were subsequently measured at different temperatures. Figure 6.5a shows temperature dependence of the ON-state current sampled at -3 V. The current shows very weak quadratic temperature dependence, which is a characteristic of a direct tunneling process as predicted by Simmons.[244] The temperature dependence of the current can be written as:[245]

$$J_{T>0\,K} = J_{0\,K}\left(1 + \frac{1}{6}(\pi\alpha k_B T)^2\right) \qquad 6.4$$

where $J_{0\,K}$ is the current passing through the junction at 0 K, α is a constant, k_B is the Boltzamn constant and T is the temperature. Fitting Eq. 6.4 to experimentally measured current, gives $J_{0\,K}$ and α that amount to 2.0×10^{-7} A, and 4.5×10^{21} N.m., respectively. The Au/P(VDF-TrFE)/Al is, therefore, a ferroelectric tunnel junction. The current in the ON-state depends only on the tunnel barrier heights.[224, 246, 247]

Representative *I-V* characteristics of the FTJ at room- (293 K) and low-temperature of 113 K are shown in Figure 6.5b. The *I-V* characteristics of the FTJ at reverse bias are very well described by Eq. 6.3, as shown in Figure 6.5b. The values for J_0, C and $\bar{\varphi}$ can be determined from the fits. Interestingly, all *I-V* curves could be fitted using similar C and $\bar{\varphi}$ of 1.18 ± 0.005 and 2.89 ±0.02 eV, respectively. The temperature dependence comes from J_T, which is well described by Eq. 6.4. The ON-state current in the forward bias, i.e., injection from the Au electrode can also be described with Eq. 6.3 using the same C value but different J_0 and $\bar{\varphi}$ of ~ 4×10^{-9} A m^{-2} and 4.2 eV, respectively. Using the schematic band diagram, the substantially larger current in the reverse bias as compared to the forward bias, has been later explained in this section. In the OFF state, both forward and reverse bias currents are low and comparable to the leakage current. Therefore, any attempt to analyze the OFF-state current, at this point, is prone to wishful interpretations.

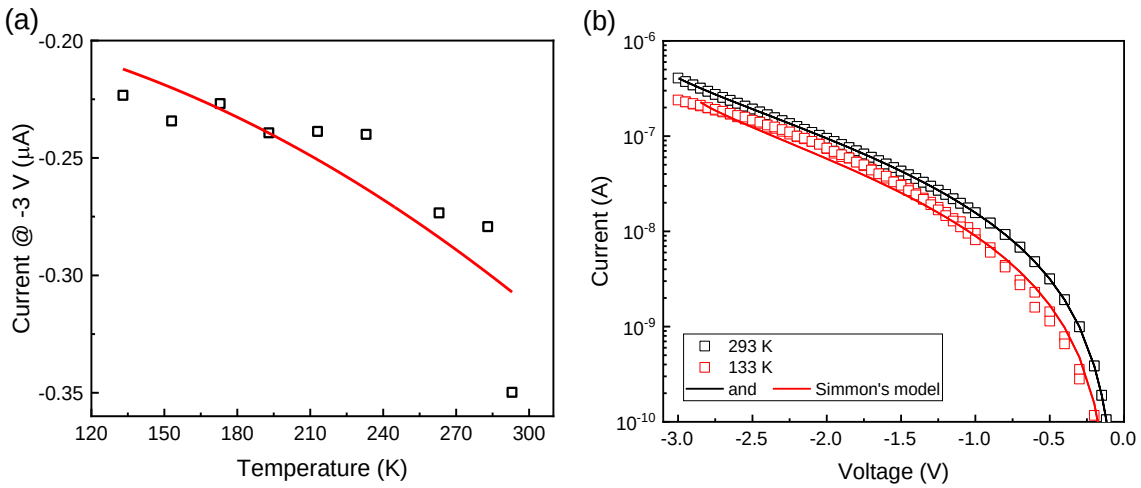


Figure 6. 5. a) Temperature dependence of the ON-state current sampled at -3 V. b) Representative I-V sweeps at the highest (RT) and lowest measured temperatures of 293 K and 133 K. The solid lines in a) and b) are fitted using equations 6.4 and 6.3, respectively.

6.6 Band diagram

Figure 6.6a schematically illustrates the energy band diagram of the Al/P(VDF-TrFE)/Au FTJs in its un-polarized pristine state. To draw the band diagram it is assumed that lowest unoccupied molecular orbital (LUMO) of P(VDF-TrFE) lies at 3.5 eV.[248] The work function of Al and Au electrodes were measured using Kelvin probe and amount to 4.2 eV and 4.9 eV, respectively. To account for the presence of the native Al-oxide layer, which is typically ≈ 1 nm thick, the presence of a thin insulating barrier at the Al electrode is assumed. Figure 6.6b shows the FTJ under negative polarization, at zero bias. Due to the presence of polarization charges, there is a slight distortion in the alignment of the energy levels, particularly at the LUMO of P(VDF-TrFE). It should be noted that the thickness of the skin depth for the metal electrode can be disregarded because of its small magnitude, compared to the thickness of the P(VDF-TrFE) layer.[246] Figure 6.6c, shows the FTJ in the ON-state under the reverse bias of -3 V. The

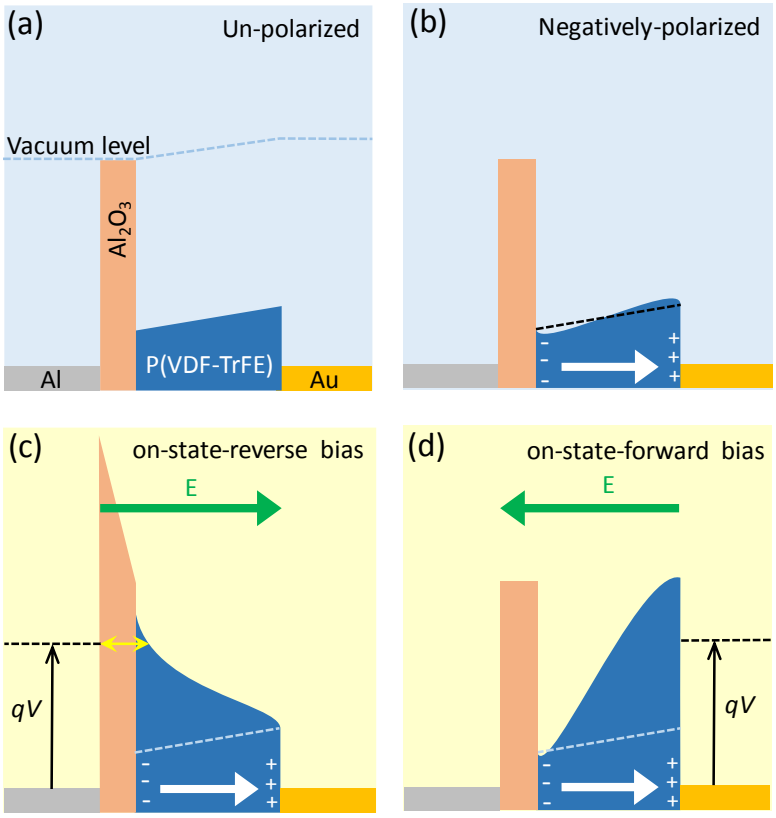


Figure 6. 6. Tentative energy band diagram of Al/P(VDF-TrFE)/Au FTJ at a) pristine unpolarized state, b) negatively polarized ON-state at zero bias, with the white arrow indicating the direction of ferroelectric polarization, c) negatively polarized ON-state at reverse bias of -3 V with the yellow arrow indicating tunnel barrier width, and d) negatively polarized ON-state at forward bias of +3 V. Green arrows indicate direction of electric field.

ferroelectric polarization is pointing toward the Au electrode. The effective tunnel barrier width is shown with the yellow arrow. Because both the external field and ferroelectric polarization are parallel, under the reverse bias condition, the tunneling barrier width is substantially lowered and the current is high. The forward bias situation is shown in Figure 6.6d. Ferroelectric polarization and applied external field are anti-parallel. Moreover, the majority of the applied potential is dropped over the P(VDF-TrFE) layer. Therefore, the Al-oxide barrier acts as an extra barrier which blocks charge transport. As a result, the effective tunnel barrier is large and the current under forward bias is substantially lower. Therefore, the presence of the Al-oxide interfacial layer would lead to a rectifying behavior of the junction. The tentative description based on the band diagram is in agreement with the calculated J_0 and $\bar{\varphi}$ for both reverse and forward bias situations.

6.7 Conclusion

In summary, rectifying FTJs with P(VDF-TrFE) were realized using co-planar nanogap asymmetric electrodes fabricated by adhesion lithography; a simple, scalable and highly cost-effective patterning technique. The FTJs show ferroelectric polarization switching at room temperature and giant TER approaching 10^6 %, along with good data retention above 24 hours. Analysis of the current-voltage characteristics suggests direct tunneling as the operating mechanism of the P(VDF-TrFE) ferroelectric tunnel junctions. Barrier modulation at the Al/P(VDF-TrFE) electrode interface is responsible for the observation of the giant TER effect in P(VDF-TrFE) FTJs that have been realized using adhesion lithography. The fabrication technique of the FTJs bears the potential for up-scaling and large-scale integration, paving the way towards a low-cost industrially viable technology.[238, 249]

Chapter 7

Current Driven Ferroelectric Memory Devices

This chapter focusses on current-driven resistance switching in phase separated polymer blends memory diodes. The unique morphology of the ferroelectric-semiconductor polymer allows storage of memory by application of current signals. Demonstration of current driven ferroelectric memory devices paves way for application of such devices for neuromorphic computational research.

7.1 Current induced ferroelectric polarization

The operation of the memory relies on the polarization of the ferroelectric polymer, P(VDF-TrFE) in our case, which can be switched by the applied voltage. If the voltage is greater than the coercive voltage, P(VDF-TrFE) polarizes in the respective direction of the applied electric field and modulates the injection barrier between the metal contact and the semiconductor.[15, 16, 19] If the top and bottom electrodes are the same, then the device geometry results in a symmetric *I-V* characteristic as shown in the Figure 7.1a.[25]

So far, ferroelectric resistance switching has been demonstrated only by applying an electric field. In this chapter we show that the same polarizing behavior of P(VDF-TrFE) can be obtained by application of current sweeps. This can be seen in the Figure 7.2a, where the current sweeps are applied to the bottom electrode and the corresponding voltage across the memory device is recorded. It can be seen the *V-I* curves open into a hysteretic loop after a certain threshold current value is crossed. This threshold value can be assumed to be the coercive current value, similar to coercive voltage. The jumps seen in the curves are due to internal instrument limitation.

It can be seen form Figure 7.2b that the memory device can be programmed by appropriate current pulses in ON and OFF states which can be read as well at low current values (less than coercive current). However, it is difficult to infer the exact coercive current value from the plot – the opening of the hysteretic *V-I* loop would suggest a coercive value between

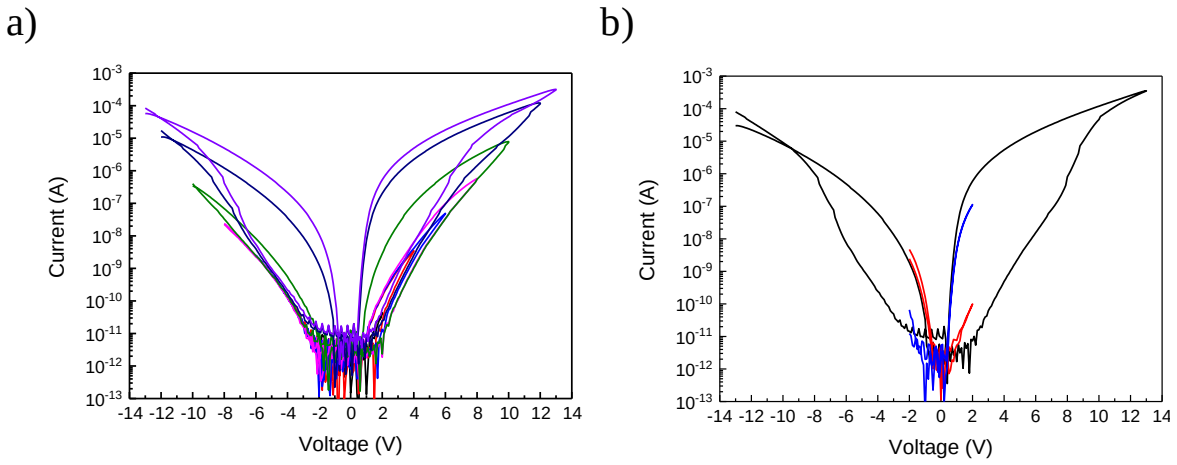


Figure 7. 1. a) Inner *I-V* loops opening up into a hysteretic curve with increasing voltage for a ferroelectric memory device. b) The reading of programmed ON and OFF states at low voltages.

100 nA and 1 µA. The clear distinction between the voltage values of the ON and OFF states indicate the programming capability of the ferroelectric memory devices by current pulses.

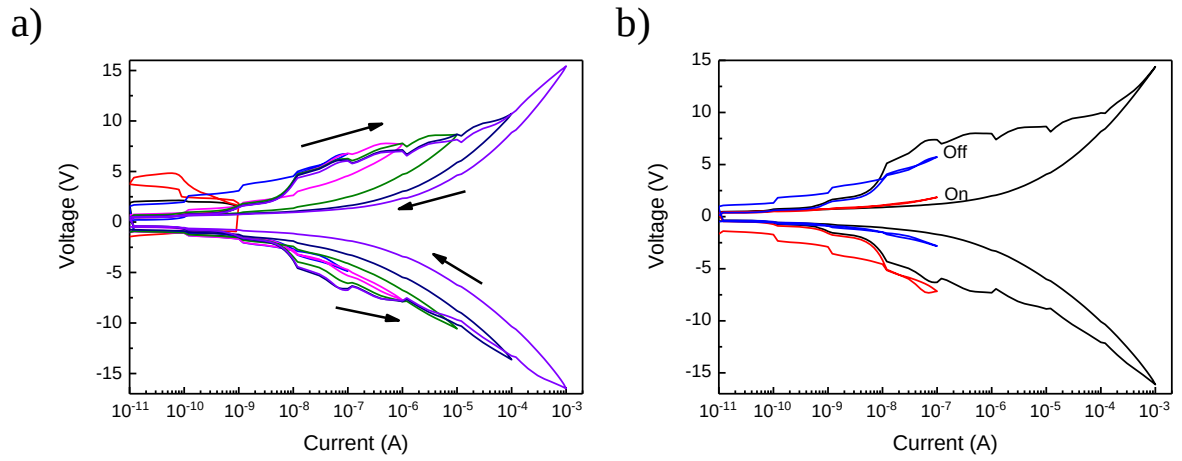


Figure 7. 2. a) *V-I* characteristics of the polymer blend memory device showing the hysteretic behavior above a certain coercive current value. b) Programming of ON and OFF states by programming current pulses and reading at lower current values.

7.2 Retention time measurements

To study long term data retention of memory in our devices, retention time measurements were carried out as shown in the Figure 7.3. The measurements carried out with voltage pulses is shown in Figure 7.3a. The device was programmed in either ON or OFF state and read at a low

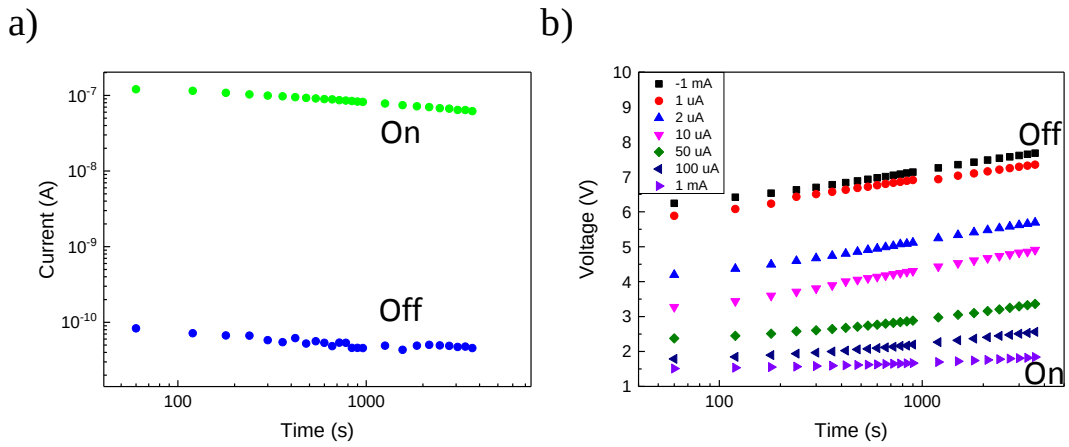


Figure 7. 3. a) Retention time measurement of the ON and OFF states of a polymer blend memory device using a voltage source. b) Retention time measurements of the memory devices using current source. The intermediate states were also programmed which could be also be read distinctly with current pulses.

voltage value for one day. The OFF state remains stable for the time measured, with ON current showing slight degradation after few hours. This could be due to an increased depolarization field. A memory window of the order 1000 is still maintained.

On the other hand, the retention time measurements done with current pulses are shown in the Figure 7.3b. The ON and OFF states were programmed by current pulses (100 ms pulse width) of magnitudes 1 mA and -1 mA respectively. The states were then read at low current values of 100 nA. In addition, intermediate states could also be programmed by current pulses of 1 µA, 2 µA, 10 µA, 50 µA, and 100 µA. These intermediate states could be clearly read with low current pulses.

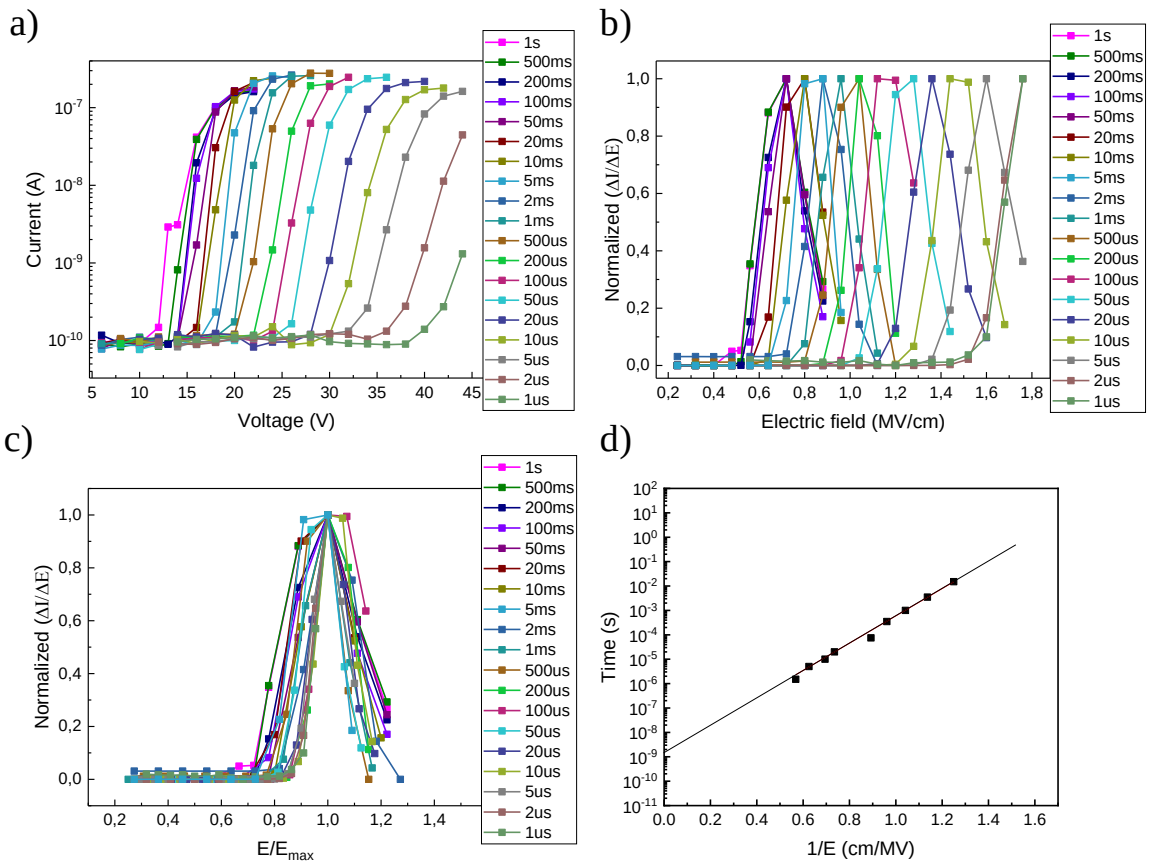


Figure 7. 4. a) Switching dynamics of the device when starting from OFF to ON state, at various pulse widths. b) Normalized curves of $\Delta I/\Delta E$ versus the applied electric field at various pulse widths. c) Normalized curves of $\Delta I/\Delta E$ with respect to scaled electric field axis to a maximum value, E_{max}. d) Calculation of the activation electric field and the switching time using the empirical relation, $\tau(E) = \tau_0 \exp(E_a/E)$.

7.3 Switching time measurements

In order to understand switching dynamics of the polymer blend memory devices, pulsed (voltage) switching measurements were performed. The measurements were carried out by first putting the device in the OFF state by applying a pulse of -25 V (100 ms pulse width). Thereafter, a programming pulse of varying frequency and voltage amplitude is applied and subsequently read at low voltage (7 V). Prior to every programming pulse, the device was put into OFF state. The measured switching transients of the programmed voltage pulses are shown in the Figure 7.4a for OFF to ON state. For large pulses of 1 s pulse width, the switching voltage was recorded to be around 13 V, whereas, for short pulses of 1 µs, the voltage where the switching begins, is around 40 V. With increase in frequency of the applied pulses, polarization switching shifts to higher voltage value as larger force is needed to orient the ferroelectric dipoles along the field. IFM (inhomogeneous field mechanism) model can be used to numerically quantify the switching behavior of the memory devices. It states that disordered

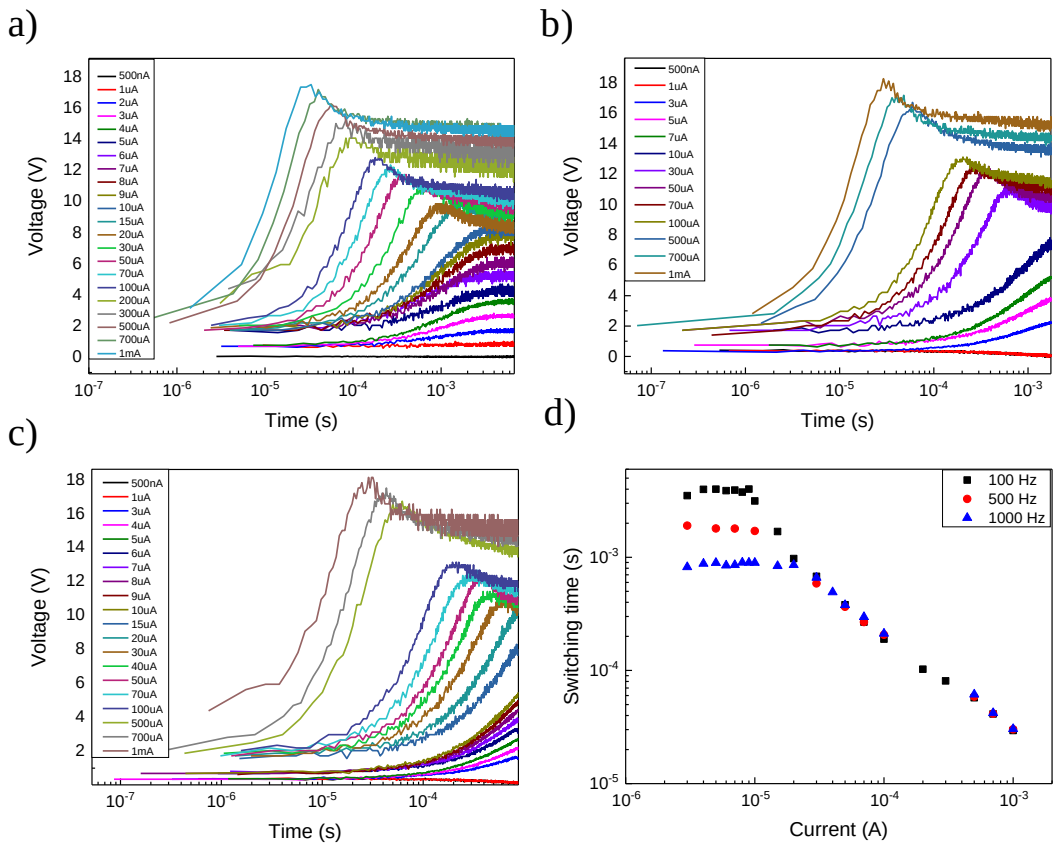


Figure 7. 5. Switching time measurements with current square pulses of frequencies a) 100 Hz, b) 500 Hz and c) 1000 Hz. The corresponding voltage transients have been recorded. d) Switching time versus current pulse amplitudes at various frequency values.

ferroelectrics consist of randomly distributed domains and the polarization kinetics are governed by time dependent local fields, which are switching time dependent (Eq. 71).[32, 33, 250] All the domains switch in a uniform manner and their switching transients follow a universal master curve, with which the characteristics switching time of the ferroelectric can be determined.[33, 251]

$$\Delta P(E_m, t) = \int_0^\infty E_m^{-1} f\left(\frac{E}{E_m}\right).p(t, \tau(\mathrm{E}))\mathrm{dE} \qquad 7.1$$

where E_m is the step electric field applied which switches polarization by ΔP and $p(t, \tau(\mathrm{E}))$ is stretched exponential of the local polarization with τ being some characteristic time. For details, the reader is suggested to refer to the references.[33, 250]

It has been shown by Lee *et al.* that such ferroelectric memory diodes can be well described by the framework of IFM model, which can be used to obtain the characteristic switching time of the diodes .[33] The derivative of the memory current with respect to applied electric field (ΔI/ΔE) can be plotted as a function of electric field, *E* (Figure 7.4b). The master curve showcasing the plot of normalized ΔI/ΔE against appropriately scaled electric-field axis at the maximum position, E_{max}, is shown in Figure 7.4c. If the switching time is defined as the time where ΔI/ΔE peaks, then the characteristic switching time can be found using the empirical Merz's law[24, 101, 146]

$$\tau(E) = \tau_0 \exp(E_a/E) \qquad 7.2$$

where, τ_0 is the characteristic switching time parameter and E_a is the activation electric field. The obtained values for the fit from the plot (shown in Figure 7.4d) are τ_0 = 0.61 ns and E_a = 1.39 GV/m. Both the values conform to the previously reported values of the 1 ns and 1 GV/m for P(VDF-TrFE) capacitors.[101, 251, 252]

The switching measurements of the ferroelectric polymer based memory devices were further studied using current pulses. The current switching time measurements were carried out using the instrument setups Keithley 6221 and Keithley 2182a. Square pulses of different frequencies and current amplitudes were applied as shown in the Figure 7.5. It can be seen that for 100 Hz frequency (Figure 7.5a), the voltage saturation of ~8 V is reached at around 10 µA and the switching time is ~2 ms. A further increase of the current amplitudes leads to shift in the switching time towards lower values. This is due to the fact, that the time taken by the ferroelectric dipoles to orient themselves along the applied electric field decreases with increase in the amplitude of the applied current pulse. Similar measurements were carried out at different

frequencies of 500 Hz and 1000 Hz. The saturation voltage does not seem to vary largely. Additionally, the switching time shifts to lower values for same value of current pulse. When the switching times of the three graphs are compared together (Figure 7.5d), it can be clearly seen that after a certain value of current, ~10 μA, the saturation voltage is reached, i.e., all ferroelectric material becomes fully polarized, irrespective of the frequency. It can thus be inferred that only when a certain amount of charge (~10 nC) is supplied, does the ferroelectric switches polarization.

7.4 Ferroelectric polymer based memory device – a memristor?

A memristor was conceptualized by *Chua* in 1971 as the fourth missing element, other than resistor, inductor, and a capacitor.[253-255] These elements are defined by the relationships among the four parameters: voltage *v*, current *i*, flux *φ*, and charge *q*. *φ* and *q* are the time integrals of voltage *v* and current *i*, respectively. The relationships between these elements are explained in the Figure 7.6 and the missing link between *φ* and *q* is defined by memristor. The Memristance *M(q)*, can be defined as the derivative of the flux *φ* with respect to the charge *q* as following[256]

$$M(q) = \frac{d\varphi(q)}{dq} \qquad 7.3$$

According to Chua, a two terminal non-volatile memory device based on resistance switching is a memristor.[253] A pinched hysteresis loop is the distinctive feature of these memristors, which is confined to the 1st and 3rd quadrant of the *I-V* characteristic. The contour shape of the loop can change with varying amplitude or frequency of the applied current or voltage signal. A number of reports confirming the existence of memristive behavior of ferroelectric memory devices have been given in the past.[257-261] However, apart from reporting the pinched loop

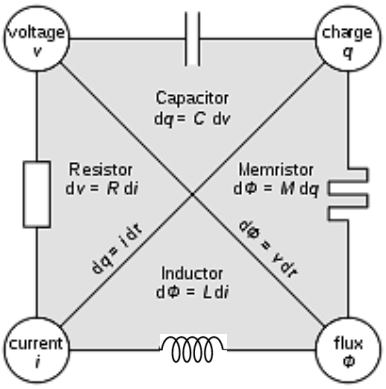
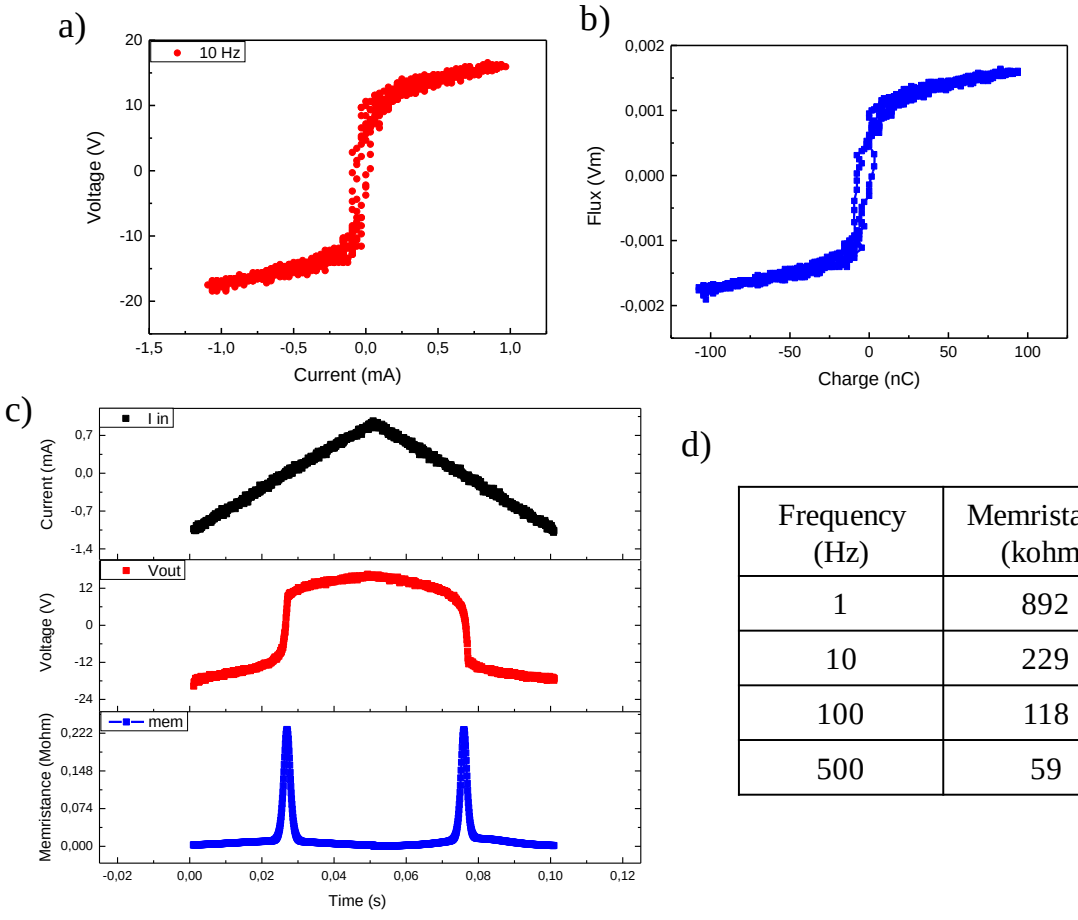


Figure 7. 6. Schematic diagram illustrating the qualitative relationships between the four parameters: *i, v, φ* and *q.*

feature, the reports fail to demonstrate the quantitative analysis proving their ferroelectric memory devices as memristors. In the following section, we take on the task of quantitatively analyzing the hysteretic behavior of the ferroelectric polymer blend memory devices and calculating the memristance according to Eq. 7.3.

The measurement on ferroelectric polymer and semiconductor polymer blend based memory devices was carried out by applying current ramp pulse of amplitude 1 mA and frequency 1 Hz. The voltage response was recorded across the device using a nano-voltmeter. As expected, the plot between the current ramp and voltage gives a hysteretic loop as shown in the Figure 7.7a. The two mathematical variables $\varphi(t)$ and $q(t)$ can be computed from the time integrals of the device's voltage $v(t)$ and current $i(t)$



Frequency (Hz)	Memristance (kohm)
1	892
10	229
100	118
500	59

Figure 7. 7. a) Hysteretic *I-V* loop when a current ramp pulse of 10 Hz frequency is applied across the polymer blend memory device and its voltage response is recorded. b) Flux versus charge curve. The flux and charge time integrals of voltage and current, respectively. c) Voltage and Memristance ($d\varphi/dq$) curves corresponding to the current ramp pulse. d) Memristance value calculated for current ramp pulses with varying frequency but same amplitude of 1 mA.

$$\varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau \quad 7.4$$

$$q(t) = \int_{-\infty}^{t} i(\tau)d\tau \quad 7.5$$

The plot between *φ(t)* and *q(t)* is shown in Figure 7.7b. Memristance can be determined by employing Eq. 7.3, which means by differentiating the *y*-axis *φ* with respect to *x*-axis *q*. The resulting memristance plotted against time is shown in Figure 7.7c. It has been pointed out by *Chua* that even when current and voltage become zero, the memristor holds the value of *φ* and *q*, thus, a passive memristor exhibits non-volatile memory.[253] This behavior can be seen in the memristance curve in Figure 7.7c, with a memristance value of approximately 230 kΩ. Hence, ferroelectric polymer based memory devices can be considered of as "true" memristors. Table given in Figure 7.7d displays the memristance values calculated by employing the same calculations but at different frequencies (and same amplitude) of the applied current ramp pulses. The memristance values are observed to be decreasing with increase in frequency. This behavior conforms with the theoretical predictions of *Chua*, that as the frequency of the input waveform is increased, keeping the amplitude constant, the memristance value diminishes approaching zero.[253] Memristors can be a great platform for advancement in the efficiency of neuromorphic computations.[262-265]

7.5 Conclusion

This chapter discusses the possibility of storing data in ferroelectric polymer based resistive switches by application of current pulses. It has been demonstrated that by applying current pulses, the surge of charge through the device polarizes it. Both ON and OFF states could be successfully programmed by current pulses and read at low current values. Retention time measurements of the intermediate states over a period of one day has also been shown. In order to investigate the switching dynamics of the memory devices under current and voltage influence, switching time measurements for both scenarios were studied. It was observed that the switching time of the devices was much higher (~2 ms) with current pulsing as compared to that with voltage source, which was ~1 ns. Finally, the idea of ferroelectric memory devices being memristors was explored based on *Chua*'s theoretical predictions and the values of memristance were calculated at different frequencies.

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List of Publications

1. **M. Kumar**, D. G. Georgiadou, A. Seitkhan, K. Loganathan, E. Yengel, H. Faber, T. D. Anthopoulos, and K. Asadi. *Colossal Tunneling Electroresistance in Co-Planar Polymer Ferroelectric Tunnel Junctions*. Advanced Electronic Materials 1901091 (2019).

2. **M. Kumar**, H. Sharifi Dehsari, S. Anwar, and K. Asadi. *Air-stable memory array of bistable rectifying diodes based on ferroelectric-semiconductor polymer blends*. Applied Physics Letters 112, 123302 (2018).

3. H. Sharifi Dehsari, **M. Kumar**, M. Ghittorelli, G. Glasser, T. Lenz, D. M. de Leeuw, F. Torricelli, and K. Asadi. *Interfacial conduction in organic ferroelectric memory diodes*. Applied Physics Letters 113, 093302 (2018).

4. **M. Kumar**, and K. Asadi *Charge trapping in MEMOLEDs*. Under Preparation.

5. H. Sharifi Dehsari, **M. Kumar**, A. Saad, M. Hassanpour Amiri, C. Yan, S. Anwar, G. Glasser, and K. Asadi. *Thin-Film Polymer Nanocomposites for Multi-Ferroic Applications*. ACS Applied Nano Materials 1, 6247-6257 (2018).

6. M. Sajedi Alvar, **M. Kumar**, P. W. Blom, G. J. A. Wetzelaer, and K. Asadi, *Absence of ferroelectricity in methylammonium lead iodide perovskite*. AIP Advances 7, 095110 (2017).

Declaration

I hereby declare that I wrote this dissertation submitted without any unauthorized external assistance and used only sources acknowledged in the work. All textual passages which are appropriated verbatim or paraphrased from published and unpublished texts as well as all information obtained from oral sources are duly indicated and listed in accordance with bibliographical rules. In carrying out this research, I complied with the rules of standard scientific practice as formulated in the statutes of the Johannes Gutenberg-University Mainz to insure standard scientific practice.

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