



# Development of a reference signal source to verify electromagnetic emissions test benches

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Bachelor's thesis

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In partial fulfillment
of the requirements for the Bachelor's Degree in
**Telecommunications Technologies and Services Engineering**

Supervised by:
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August, 2020

**Abstract**

Electromagnetic Compatibility (EMC) laboratories must ensure the quality of the tests they perform. In this regard, periodic calibrations and internal verifications should be carried out systematically to provide evidence that the test benches are in compliance with the standard requirements of measurement accuracy and instrumentation uncertainty. In particular, the electromagnetic emissions test consists of measuring the interference produced by the equipment under test (EUT). The failure or misfunctioning of any of the elements in the electromagnetic emissions test benches can lead to significant errors in the measurement results and, ultimately, to an incorrect assessment of the EUT compliance with regards to the standard emissions requirements. Just-before-test verifications are a mean for detecting such problems in the test benches, thus preventing the test laboratory from delivering wrong results to their clients.

The Electromagnetic Compatibility Group from the UPC is aware of the importance of such calibrations and verification activities. Furthermore, GCEM-UPC is also a TECNIO agent, which means that it has been accredited by "Generalitat de Catalunya" as an excellent, experienced, and high-quality technology service provider. In practice, this means that GCEM-UPC must demonstrate it has a quality assurance process and it is periodically audited. Therefore, GCEM-UPC is continuously improving the established EMC testing methods as well as developing new, better ones alongside with their required verification and calibration procedures.

In this regard, this work aims at developing a reference signal source capable of generating specific waveform patterns with useful properties for accelerating the verification of electromagnetic emissions test benches. This implies designing and implementing an easy to use device ready for performing just-before-test verifications with a single apparatus.

**Resum**

Els laboratoris de Compatibilitat Electromagnètica (EMC) han de garantir la qualitat dels assaigs que realitzen. En aquest sentit, s'han de realitzar calibracions periòdiques i verificacions internes de manera sistemàtica per proporcionar evidència que els bancs d'assaig compleixen amb els requisits estàndard de precisió i incertesa de la instrumentació. En particular, l'assaig d'emissions electromagnètiques consisteix a mesurar la interferència produïda per l'equip sotmès a assaig (ESE). La fallada o mal funcionament de qualsevol dels elements dels bancs d'assaigs d'emissions electromagnètiques pot donar lloc a errors importants en els resultats de la mesura i, en última instància, a una avaluació incorrecta de l'acompliment de l'ESE pel que fa als requisits de emissions estàndard. Les verificacions just abans de la prova són un mitjà per detectar aquests problemes en els bancs d'assaig, evitant així que el laboratori lliuri resultats incorrectes als seus clients.

El Grup de Compatibilitat Electromagnètica de la UPC és conscient de la importància d'aquest tipus d'activitats de calibratge i verificació. A més, GCEM-UPC també és un agent TECNIO, el que significa que ha estat acreditat per la Generalitat de Catalunya com a proveïdor de serveis tecnològics d'excel·lència, amb experiència i de qualitat. A la pràctica, això significa que GCEM-UPC ha de demostrar que té un procés de seguiment de la qualitat i que és auditat periòdicament al respecte. Per tant, GCEM-UPC està millorant contínuament els mètodes d'assaig d'EMC establerts, així com desenvolupant mètodes nous i millors juntament amb els procediments de verificació i calibratge requerits.

En aquest sentit, aquest treball té com a objectiu desenvolupar una font de senyal de referència capaç de generar patrons de forma d'ona específics amb propietats útils per accelerar la verificació dels bancs d'assaig d'emissions electromagnètiques. Això implica dissenyar i implementar un dispositiu fàcil d'utilitzar preparat per fer verificacions just abans de l'assaig amb un únic aparell.

**Resumen**

Los laboratorios de Compatibilidad Electromagnética (EMC) deben garantizar la calidad de los ensayos que realizan. En este sentido, se deben realizar calibraciones periódicas y verificaciones internas de manera sistemática para proporcionar evidencia de que los bancos de ensayo cumplen con los requisitos estándar de precisión e incertidumbre de la instrumentación. En particular, el ensayo de emisiones electromagnéticas consiste en medir la interferencia producida por el equipo sometido a ensayo (ESE). El fallo o mal funcionamiento de cualquiera de los elementos de los bancos de ensayos de emisiones electromagnéticas puede dar lugar a errores importantes en los resultados de la medida y, en última instancia, a una evaluación incorrecta del cumplimiento del ESE con respecto a los requisitos de emisiones estándar. Las verificaciones justo antes de la prueba son un medio para detectar tales problemas en los bancos de ensayo, evitando así que el laboratorio entregue resultados incorrectos a sus clientes.

El Grupo de Compatibilidad Electromagnética de la UPC es consciente de la importancia de este tipo de actividades de calibración y verificación. Además, GCEM-UPC también es un agente TECNIO, lo que significa que ha sido acreditado por la Generalitat de Catalunya como proveedor de servicios tecnológicos de excelencia, con experiencia y de calidad. En la práctica, esto significa que GCEM-UPC debe demostrar que tiene un proceso de seguimiento de la calidad y que es auditado periódicamente al respecto. Por lo tanto, GCEM-UPC está mejorando continuamente los métodos de ensayo de EMC establecidos, así como desarrollando métodos nuevos y mejores junto con los procedimientos de verificación y calibración requeridos.

En este sentido, este trabajo tiene como objetivo desarrollar una fuente de señal de referencia capaz de generar patrones de forma de onda específicos con propiedades útiles para acelerar la verificación de los bancos de ensayo de emisiones electromagnéticas. Esto implica diseñar e implementar un dispositivo fácil de usar listo para realizar verificaciones justo antes del ensayo con un único aparato.

**Acknowledgements**

M'agradaria donar les gràcies a tothom que m'ha fet costat durant la realització d'aquest treball. En especial a tot l'equip de GCEM-UPC i al Marco per a guiarme en la direcció correcta.

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# Abbreviations

**AWG** Arbitrary Waveform Generator.

**CDN** Coupling Decoupling Network.

**CF** Crest Factor.

**CM3+** Raspberry Pi Compute Module 3+.

**DAC** Digital to Analog Converter.

**DDR2** Double Data Rate type 2.

**EMC** Electromagnetic Compatibility.

**EMI** Electromagnetic Interference.

**ESD** Electrostatic Discharge.

**EUT** Equipment Under Test.

**FFT** Fast Fourier Transform.

**FPGA** Field Programmable Gate Array.

**FS** Full Scale.

**GCEM-UPC** Grup de Compatibilitat Electromagnètica de la Universitat Politècnica de Catalunya.

**HDMI** High Definition Multimedia Interface.

**JEITA** Japan Electronics and Information Technology Industries Association.

**JTAG** Joint Test Action Group.

**LDO** Low Dropout Regulator.

**LISN** Line Impedance Stabilization Network.

**LVDS** Low-Voltage Differential Signaling.

**MPU** Microprocessor Unit.

**PE** Protective Earth.

**PLL** Phase Locked Loop.

**PSRR** Power Supply Rejection Ratio.

**RAM** Random Access Memory.

**RF** Radio Frequency.

**RMS** Root Mean Square.

**SFDR** Spurious Free Dynamic Range.

**SNR** Signal to Noise Ratio.

**TEMPS** Time-domain EMI Measurement and Processing System.

**VSWR** Voltage Standing Wave Ratio.

# 1 Introduction

This project has been carried out in the framework of GCEM-UPC, the Electromagnetic Compatibility Group from Universitat Politècnica de Catalunya that is part of the Electronic Engineering department of the same university.

Electromagnetic Compatibility (EMC) is an engineering field dedicated to the study of the electromagnetic interaction between different electronic equipment and the environment, including the problems arising from such interaction and the methods to avoid/solve them. Its mission is to ensure that electric equipment and systems are able to perform as intended within the same electromagnetic environment.

To ensure equipment coexistence, countries and regions have mandatory regulations for all electrical and electronic equipment that may cause or be affected by electromagnetic interference. Specifically, in Europe, directive 2014/30/EU [1] is the main regulation regarding EMC, although below this one there are specific directives for different types of products (these are called product directives).

To ensure compliance with these directives, various recognized European normalization bodies (like CEN, CENELEC or ETSI) have created harmonized standards following the requests of the European Union. These harmonised standards can be used by manufacturers to demonstrate compliance of their products with the corresponding directive. However, these harmonised standards are not mandatory, but then the product compliance has to be approved by an European notified body.

In order to comply with the European directives, electromagnetic emissions of the product must be kept below established levels and it also must be able to function properly when perturbed by disturbance levels higher than those that should be found in their operating environment. This evaluation is performed using different tests compiled in various standards defined so that they are reproducible, that is, they are independent of the moment, place of measurement and environmental conditions. The most commonly performed tests are:

- Electromagnetic emissions.
  - EN 55016-2-1 (CISPR16-2-1): Conducted disturbance measurements.
  - EN 55016-2-3 (CISPR16-2-3): Radiated disturbance measurements.
- Immunity to electromagnetic disturbances.
  - EN 61000-4-2: Electrostatic discharge immunity test.
  - EN 61000-4-3: Radiated, radio-frequency, electromagnetic field immunity test.
  - EN 61000-4-4: Electrical fast transient/burst immunity test.
  - EN 61000-4-5: Surge immunity test.
  - EN 61000-4-6: Immunity to conducted disturbances induced by radio-frequency fields.
  - EN 61000-4-8: Power frequency magnetic field immunity test.
  - EN 61000-4-11: Voltage dips, short interruptions and voltage variations immunity test.

In particular, we are interested in conducted emissions defined in CISPR16-2-1. CISPR16 is a series of publications (international standard) specifying equipment and methods for measuring disturbances and immunity at frequencies above 9 kHz. Specifically, CISPR16-1-1 [2] specifies the characteristics and performance requirements of equipment for the measurement of radio disturbance in the frequency range 9 kHz to 18 GHz. This frequency range is divided into various bands, being band A (from 9 kHz to 150 kHz) and band B (from 150 kHz to 30 MHz) the only relevant for our purposes. This standard also defines the three main detectors that a EMC compliant receiver has to incorporate:

- An Average detector that indicates the mean value of the disturbance, particularly to discriminate between broadband and narrowband disturbances.
- A Peak detector that indicates the highest amplitude of the disturbance.
- A Quasi-Peak detector whose reading is a function of the repetition frequency of the disturbance.

In compliance with CISPR16-2-1 [3], the test setup consists mainly of a CISPR16-1-1 measuring receiver, a coupling device such as a CND or a LISN, and one or two ground planes.

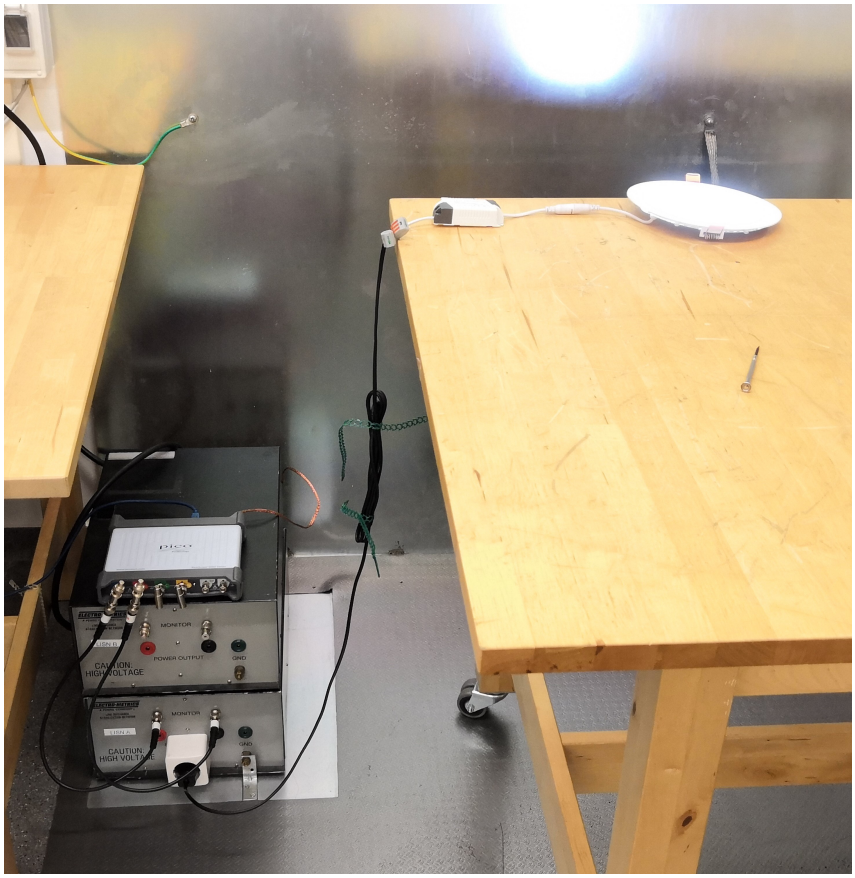



Figure 1: Close look at the GCEM's conducted emissions setup while a test is being performed. The EUT is connected to one of the LISNs inputs (bottom left) and their outputs are connected to the receiver. Note that the EUT is positioned at a predefined distance from both horizontal and vertical ground planes.

Within these frequency bands, the measurements are performed using the Quasi-Peak and Average detectors. According to [3], using a standard EMI receiver or spectrum analyzer to perform these measurements, the minimum scanning time is 47 min for band A and 99.5 min for band B. In GCEM-UPC's Electromagnetic Compatibility laboratory we use an innovative system for measuring electromagnetic emissions in the time domain called TEMPS (Time-domain EMI Measurement and Processing System), which has emerged from many years of group research in the area. The software makes use of the digital processing techniques described in [9] to the samples of an oscilloscope to compute the power spectral density and normative detectors of the signal, allowing to reduce the measurement time down to a few seconds.

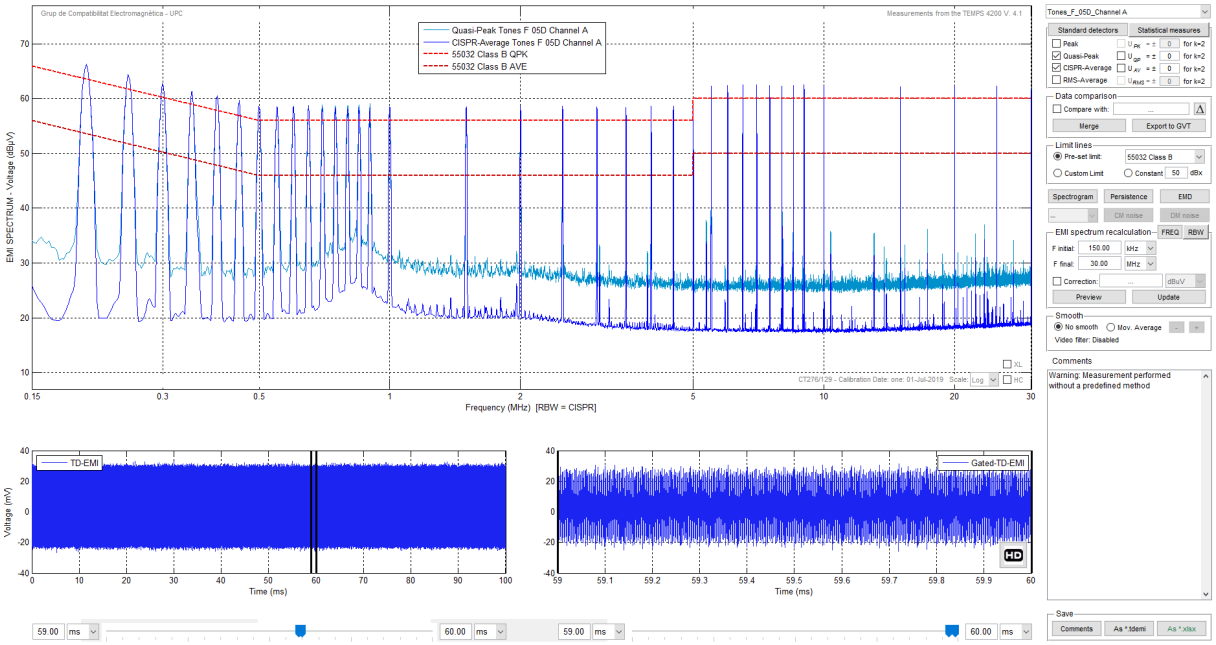



Figure 2: Screenshot of a measurement performed with the TEMPS software.

Electromagnetic Compatibility (EMC) laboratories must ensure the quality of the tests they perform. In this regard, periodic calibrations and internal verifications should be carried out systematically to provide evidence that the test benches are in compliance with the standard requirements of measurement accuracy and instrumentation uncertainty. The failure or malfunctioning of any of the elements in the electromagnetic emissions test benches can lead to significant errors in the measurement results and, ultimately, to an incorrect assessment of the EUT compliance with regards to the standard emissions requirements. Just-before-test verifications are a mean for detecting such problems in the test benches, thus preventing the test laboratory from delivering wrong results to their clients.

The Electromagnetic Compatibility Group from the UPC is aware of the importance of such calibrations and verification activities. Furthermore, GCEM-UPC is also a TECNIO agent, which means that it has been accredited by "Generalitat de Catalunya" as an excellent, experienced and high-quality technology service provider. In practice, this means that GCEM-UPC must demonstrate it has a quality assurance process and it is periodically audited.

This work aims at developing a first prototype of a reference signal source capable of

generating specific waveform patterns with useful properties for accelerating the verification of electromagnetic emissions test benches. This implies designing and implementing an easy to use device ready for performing just-before-test verifications with a single apparatus. To fulfil the GCEM-UPC needs, this device has to comply with some requirements:

- The device should be capable of being connected to the conducted emissions test bench.
- The device should generate the desired spectrums.
- The device should be able to serve as a reference standard for conducted emissions.
- The device should comply with a fixed accuracy and always better than that of the measuring element.
- The device should be capable of working without the need of an external computer.

The design of a device is a complex and time consuming task that usually is carried out by multiple people. This project will be developed mostly by myself, making it a long-term project. Consequently, this document will cover the first steps in the development of the device. Therefore, the main goals of the thesis are:

- To study the electromagnetic emissions test setups and their instrumentation to identify critical parameters that must be verified to ensure the validity of the test results.
- To define reference signals suitable for verifying the electromagnetic emissions test setups and to model them through the mathematical description of their waveforms in the time and frequency domain.
- To design a device capable of generating the required reference signals with output level accuracy and uncertainty in compliance with the electromagnetic compatibility standards.

# 2 Waveform design

With regards to the evaluation of the test setups, the approach followed in previous research consisted in applying the reference waveforms to the measurement system as if it were the actual interference of the EUT, as described in [5]. If the measurements performed by the test receiver are within the specifications of the standard, it means that the waveforms have not been degraded in their propagation through the signal path (cables, connectors, LISN), which necessarily implies that the measurement setup is correct and our test bench is adequately configured.

In particular, our device will verify the sine-wave accuracy and the response to broadband pulses of the setup described in CISPR16-1-1 [2]. This chapter presents the research and simulations carried out in order to define such a suitable set of waveforms for the intended verifications.

The analysis presented in what follows has been performed in Matlab in order to reuse the core functions and algorithms already implemented and validated for the TEMPS software.

## 2.1 Sine-wave accuracy

According to [6], the conventional method for calibrating the sine-wave accuracy of a receiver consists in applying to the receiver a single tone with a well defined frequency and amplitude and verifying that all of the detectors read the same value for all the frequencies. Instead of that, and since the goal is to rapidly verify the equipment and not calibrate it, they purposed synthesizing a multitone waveform whose amplitudes of the tones follow the limit lines of different standards. They demonstrated in [5] that the possible failures in the test setup will exhibit different changes in the measured waveform, resulting in variations of the signal spectrum. Figure 3 shows with a green trace the effect of connecting the LISN to earth with a very thin wire and in red the LISN connected to earth with a very long mesh.

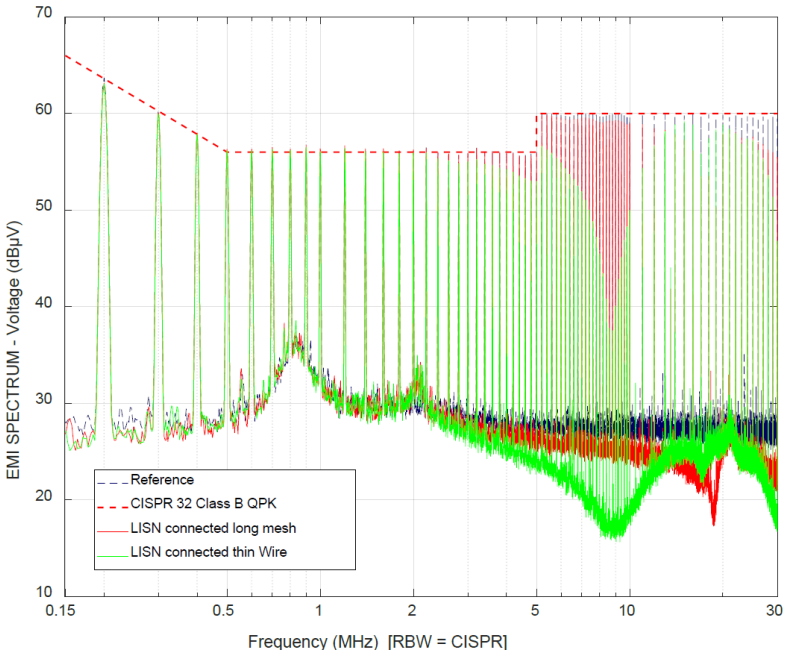


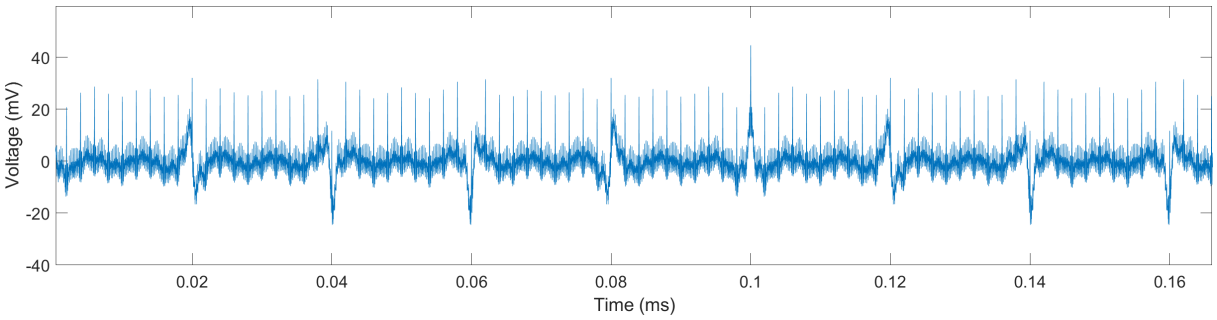

Figure 3: Measurements performed in [5] of the multi-tone signal generated with an AWG and applyed to the EUT entrance of the test setup with various LISN faults

In [6] and [5], the signal was computed with all the tones being in phase but, as [7] shows, this approach tends to create signals with large Crest Factors (which is the ratio between the peak value and the RMS value of a signal). Specifically, the peak of a multitone signal with all the tones in phase (or with the phases varying linearly) and with the same amplitude, as in (1), increases with the square root of the number of tones ($\sqrt{2N}$).

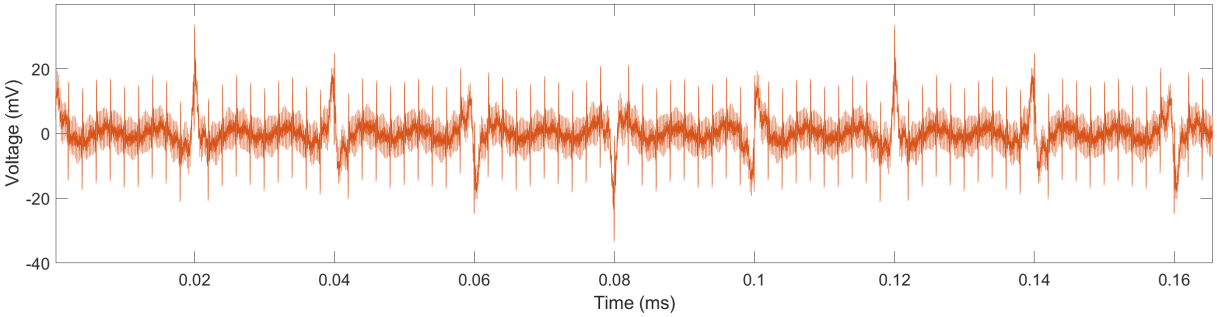
$$x(t) = \sqrt{\frac{2}{N}} \sum_{k=1}^{N} cos(k \cdot t + \delta_k) \tag{1}$$

In this type of EMI measurements, only the magnitude of the spectrum is used for compliance assessments. Therefore, it is possible to optimize the phase of the components of the multitone signal for minimizing the resulting CF of waveform by means of the algorithms defined for this purpose[7]. Minimizing the crest factor helps increase the SNR, reduces the possible nonlinear distortions created by an amplifier and maximizes the dynamic range usage of the measuring device.

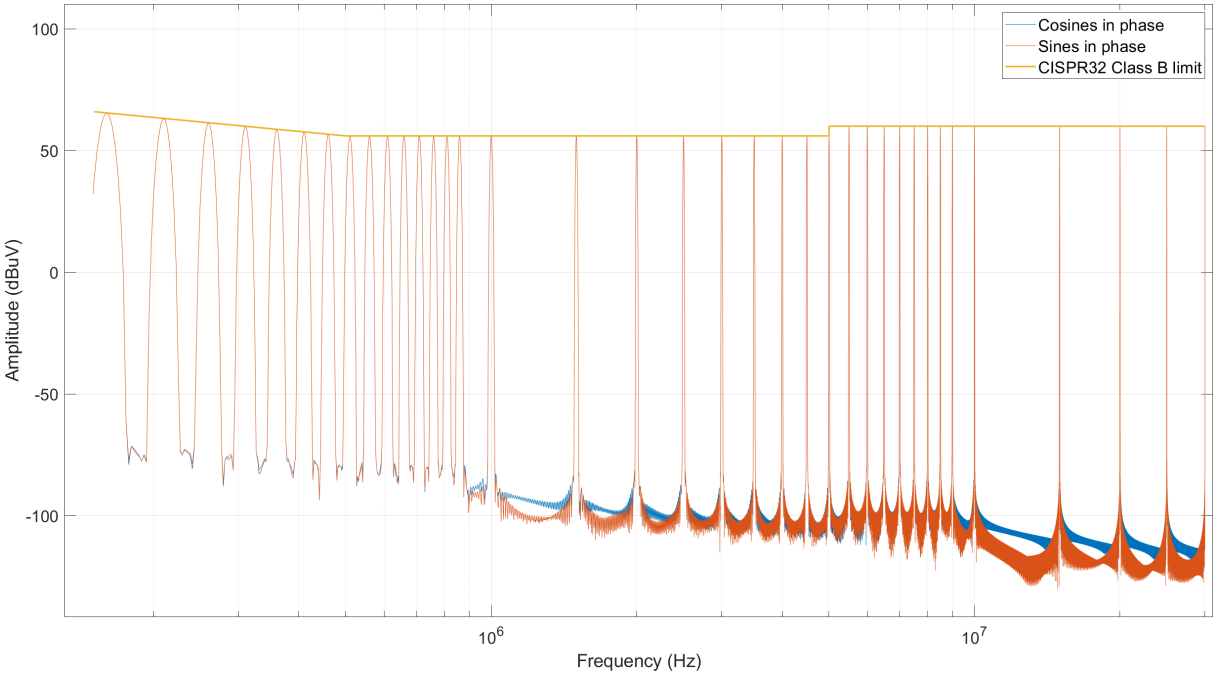
Figure 4 shows the simulation of the signals described before, created by the sum of 40 sines and cosines in phase (produced by a spacing of 50 kHz between 9 kHz and 1 MHz; 500 kHz between 1 MHz and 10 MHz; and 5 MHz between 10 MHz and 30 MHz), with a resulting crest factor of 6.178 for the multi-sine and 8.203 for the multi-cosine. Although this signal is proved to be working for our purposes [6], a reduction of the CF would be beneficial for the performance of the device.




(a) 40 cosines in phase, linear distribution, CF = 8.203




(b) 40 sines in phase, linear distribution, CF = 6.178




(c) Quasi-Peak spectrum of the signals

Figure 4: Simulated multitone signals with 40 tones (from 9 kHz to 30 MHz) in phase with amplitudes following the CISPR32 Class B limit.

To try to reduce the CF of the multitone waveform, I applied the two algorithms from [7]. One is an algorithm that modifies the phases of the tones following the Shapiro-Rudin sequence, and the other varies the phases quadratically as D. J. Newman suggested.

### Shapiro-Rudin phases algorithm

With this algorithm, whenever the number of tones, $N$, is a power of 2, there are phases

which yield a crest factor as low as 2 (the algorithm can still be used even if the samples are not a power of 2 but at the cost of a poorer performance). The algorithm consists in creating a vector ($Ph$) that lately will contain the phases for each tone. This vector starts as $Ph = [1, 1]$ (following the Matlab notation). Then, repeatedly concatenate to $Ph$ a copy of $Ph$ with its second half negated untill the number of elements in the vector equals the number of tones:

$$Ph = [1, 1] \rightarrow Ph = [1, 1, 1, -1] \rightarrow Ph = [1, 1, 1, -1, 1, 1, -1, 1] \rightarrow ... \tag{2}$$

Then, the vector values equal to one are replaced by zeros and the vector values equal to minus one are replaced with $\pi$. Equation (3) shows the resulting phases for a 32 tone signal.

$$Ph = [0, 0, 0, \pi, 0, 0, \pi, 0, 0, 0, 0, \pi, \pi, \pi, 0, \pi, 0, 0, 0, \pi, 0, 0, \pi, 0, \pi, \pi, \pi, 0, 0, 0, \pi, 0] \tag{3}$$

When the vector with the phases is ready to create the resulting signal, then all the sines/cosines are summed up as shown in (4), being $A_n$ the amplitude of each tone and $f_n$ the frequency of each tone.

$$Y(t) = \sum_{n=1}^{N} \sqrt{2} \cdot A_n \cdot sin(2\pi \cdot f_n \cdot t + Ph_n) \tag{4}$$

The Matlab implementation of this algorithm is shown in Code 1.

Code 1: Matlab code for the Shapiro-Rudin phases algorithm

```
%Shapiro-Rudin Phases
vectorSize = 1e6;
toneNumber = 40;
TIME = (0:1:vectorSize-1);
TIME = TIME/Fs;

N = 2^(ceil(log2(toneNumber)));
PHASES = zeros(1,N);
PHASES(1:2) = [1,1];
for i = 2:log2(N)
    PHASES( 2^(i-1)+1 : 2^(i-1) + 2^(i-2) ) = PHASES(1 : (2^(i-2)));
    PHASES( 2^(i-1)+2^(i-2)+1 : 2^i) = -PHASES( (2^(i-2)+1) : (2^(i-1)) );
end
PHASES = pi*(PHASES-1)./2;

WAVE = zeros(1,vectorSize);
for f = 1:toneNumber
   WAVE = WAVE + sqrt(2)*amp(f)*cos(2*pi*FSTEP(f)*TIME + PHASES(f));
end
```

### Newman phases algorithm

The algorithm consists in the quadratic variation of the phase for each tone:

$$Ph_n = \frac{\pi(n-1)^2}{N} \tag{5}$$

Although not proved to always yield very low crest factors, numerical investigations [7] suggest that it can be as low as 1.7, decreasing when N increases.

To create the multitone signal, (4) is applied but now with the Newman phases vector. Below is shown the Matlab code used to create the waveforms for this algorithm.

Code 2: Matlab code for the Newman phases algorithm

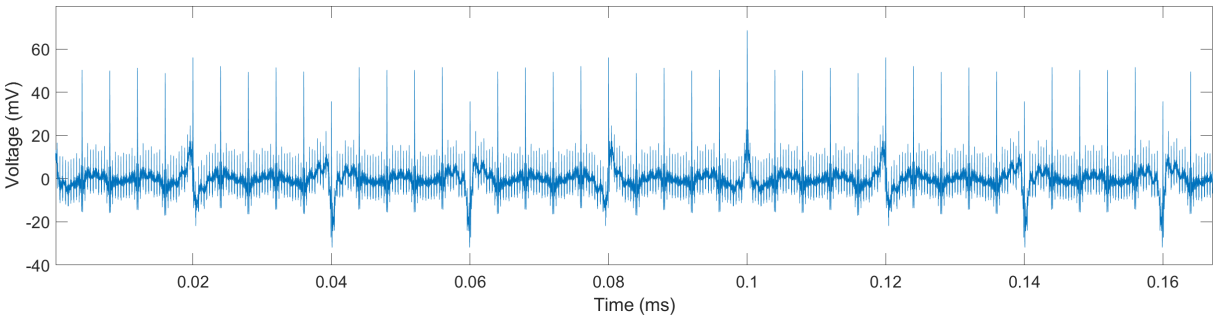
```
%Newman Phases
vectorSize = 1e6;
TIME = (0:1:vectorSize-1);
TIME = TIME/Fs;

WAVE = zeros(1,vectorSize);
for f = 1:N
   WAVE = WAVE + sqrt(2)*amp(f)*cos(2*pi*FSTEP(f)*TIME + pi*((f-1)^2)/length(FSTEP));
end
```

### Comparison

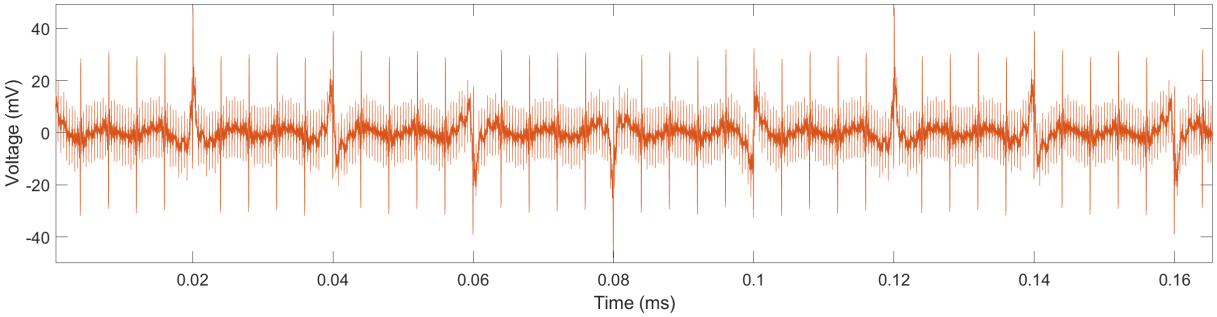
Table 1 shows a comparison of the different crest factors obtained when computing the multitone waveform using 5 different algorithms with 40 or 60 tones (being 60 the result of halving the tone spacing per decade) distributed linearly or logarithmically along the frequency range. The logarithmic distribution tends to create waveforms with lower crest factors as the number of tones increases, which is beneficial, but this approach does not fully fit the device's purposes because the period of the signal is very difficult to identify and the device needs to reproduce the waveforms periodically. The linear distribution by itself does not accomplishes this periodicity but, if some care is taken when choosing the frequencies, it can be easily achieved. In the example from Figure 5 the periodicity of the signals is quite clear and one period only requires a few samples. Taking this into account and although the linear distribution tends to increase the CF as the number of tones increases, the Shapiro-Rudin algorithm using a linear frequency distribution seems to perform the best. Because of its reduced computational complexity compared to Newman phases algorythm, the Shapiro-Rudin algorithm will be used to produce the multitone waveforms.

Table 1: Resulting CF of different algorithms for different distributions of tones.

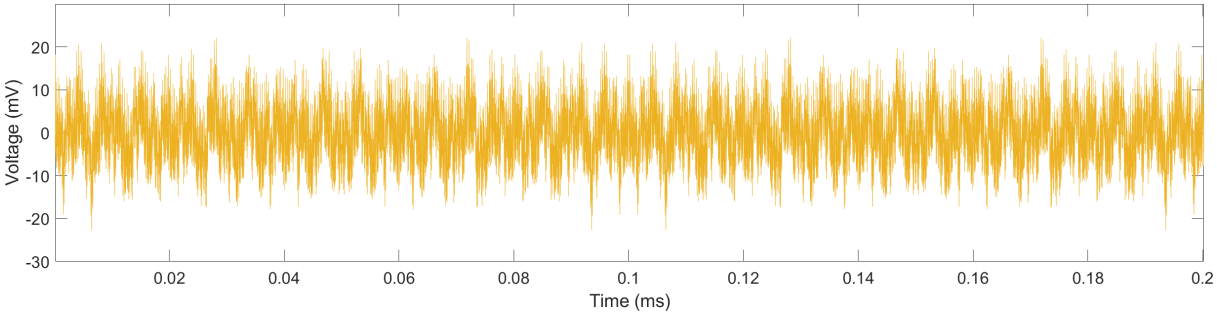
| | **Linear distribution** | | **Logarithmic distribution** | |
|---|---|---|---|---|
| **Algorithm** | **40 Tones** | **60 Tones** | **40 Tones** | **60 Tones** |
| Cosines in phase | 8.203 | 10.271 | 8.451 | 10.407 |
| Sines in phase | 6.178 | 7.188 | 3.593 | 3.682 |
| Cosines with Shapiro-Rudin phases | 3.517 | 3.389 | 4.325 | 3.954 |
| Cosines with Newman phases | 4.402 | 4.456 | 4.609 | 4.025 |
| Cosines with random phases | 3.464 | 3.559 | 4.008 | 4.575 |



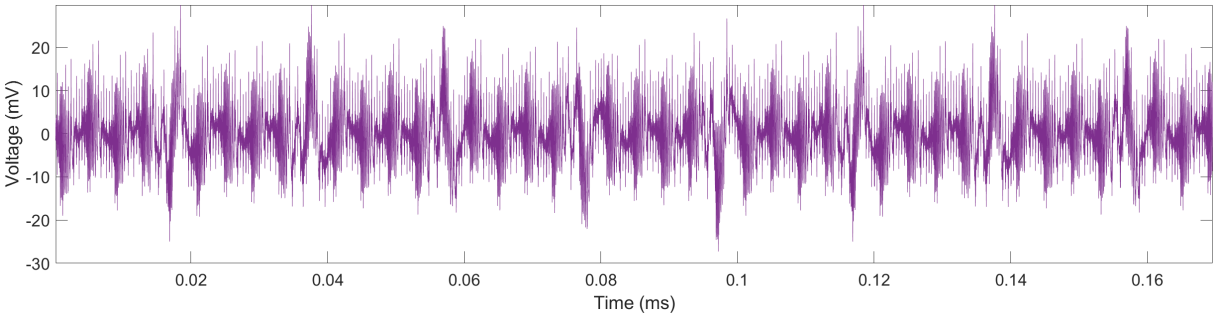

(a) 60 cosines in phase, linear distribution, CF = 10.271



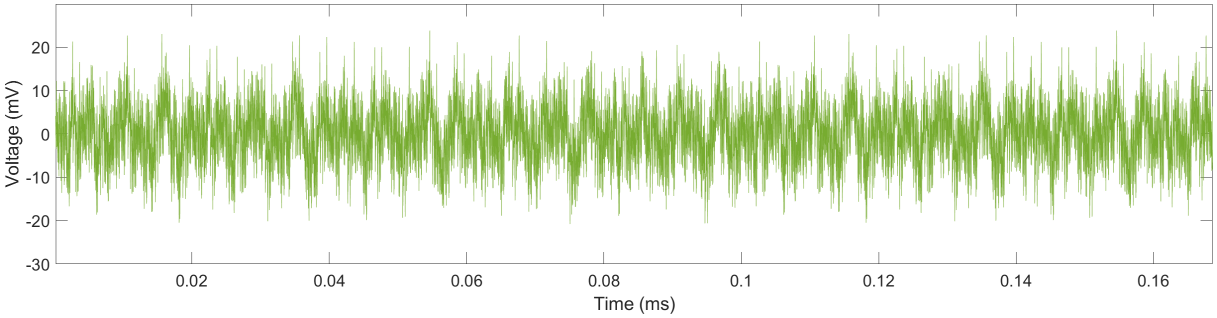

(b) 60 sines in phase, linear distribution, CF = 7.188



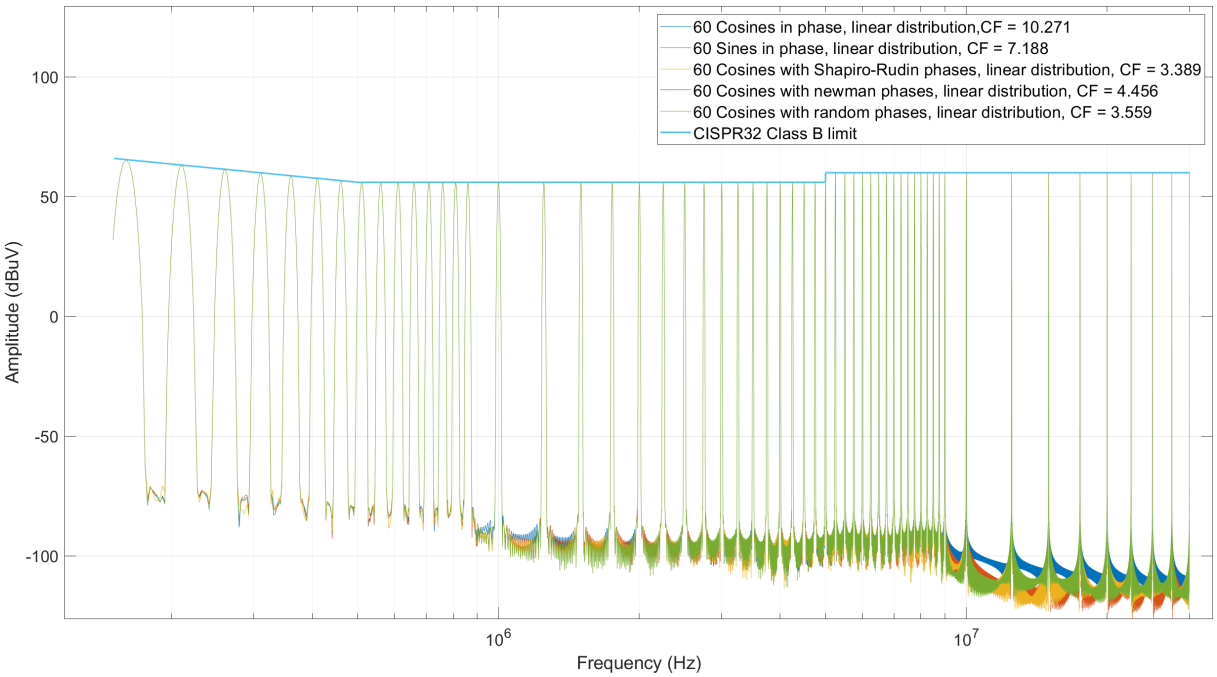

(c) 60 cosines with Shapiro-Rudin phases, linear distribution, CF = 3.289




(d) 60 cosines with Newman phases, linear distribution, CF = 4.456




(e) 60 cosines with random phases, linear distribution, CF = 3.559




(f) Quasi-Peak spectrum of the tones

Figure 5: Simulated multitone signals with 60 tones spaced linearly with amplitudes following the CISPR32 Class B limit and their corresponding Crest Factor

## 2.2 Response to broadband pulses

The receiver's response to pulses of the weighting detectors is the most challenging aspect of a receiver that must be calibrated [4]. CISPR16-1-1 does not stipulate the exact waveforms to be used but requires the pulse to comply with some parameters. In special, the response of the quasi-peak detector to pulses of impulse area a) at 50 Ω having a flat response up to at least b) repeated at a frequency of c) has to be equal to the response to an unmodulated open circuit sine-wave of 66 dBuV (from Table 2) [2]. The pulses also have to exhibit a decay of at least 10 dB at twice the maximum frequency of the band.

Table 2: Test pulse characteristics for quasi-peak measuring receivers

| **Frequency band** | **a) Pulse area (μVs)** | **b) Upper bound (MHz)** | **c) Repetition frequency (Hz)** |
|---|---|---|---|
| A (9 kHz to 150 kHz) | 13.5 | 0.15 | 25 |
| B (150 kHz to 30 MHz) | 0.316 | 30 | 100 |

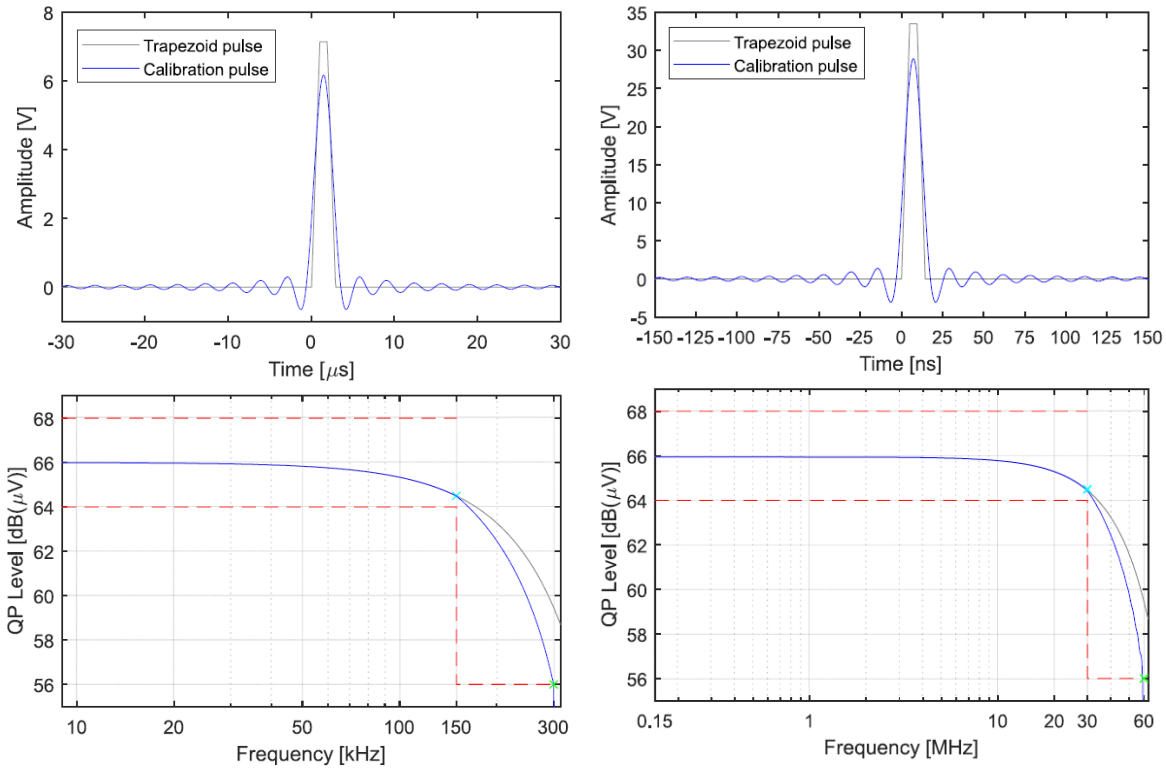
Regarding the peak detector, it must follow the relationship in Table 3 with respect to the quasi-peak detector.

Table 3: Relative pulse response of peak and quasi-peak measuring receivers

| **Frequency band** | **A_imp (µVs)** | **B_imp (kHz)** | **Ratio peak/quasi-peak (dB) for pulse repetition ratio** | |
|---|---|---|---|---|
| | | | **25 Hz** | **100 Hz** |
| A (9 kHz to 150 kHz) | 6.67 | 0.21 | 6.1 | - |
| B (150 kHz to 30 MHz) | 0.148 | 9.45 | - | 6.6 |

On the other hand, average detectors are generally not used for the measurement of impulsive disturbances, reason why they will not be considered for the pulse response verification.

In this context, [4] purposes a parametric model for pulsed waveforms that are compliant with the requirements established by CISPR16-1-1. The model is numerically solved and evaluated to produce a waveform vector that can be transformed into a reference voltage signal using arbitrary function generators.




(a) Band A

(b) Band B

Figure 6: Calibration pulses for CISPR bands A and B and their frequency spectrum synthesized in [4]

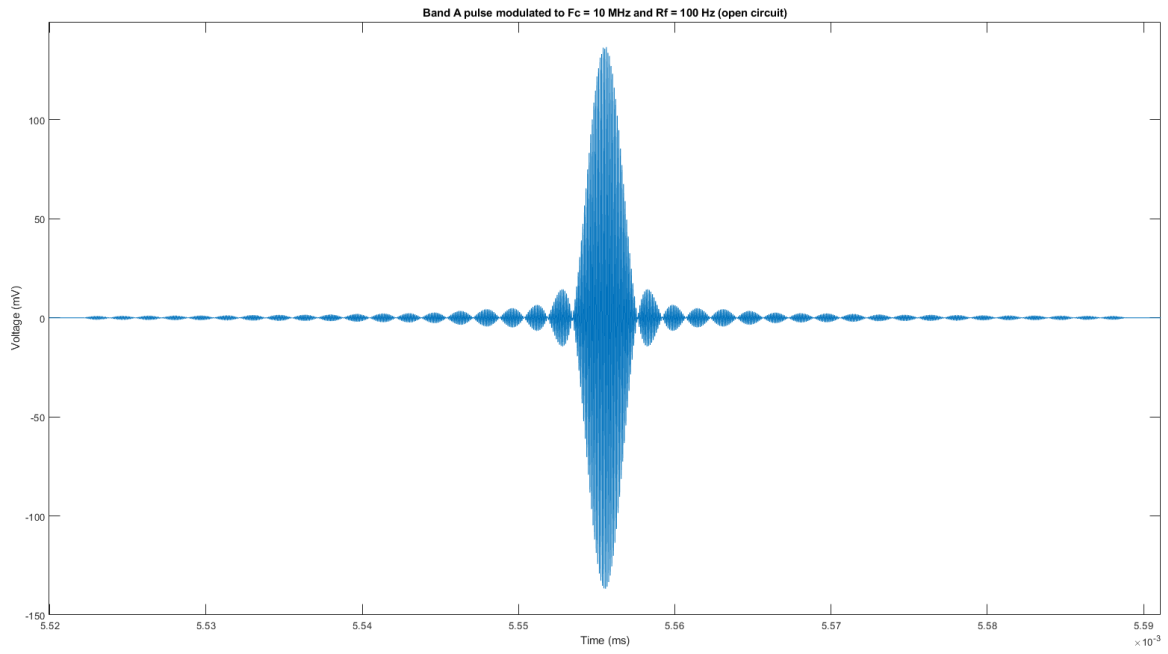
This approach works well for band A but the tremendously fast rising times and high amplitudes needed to create the desired spectrum for higher frequency bands make it very difficult to reproduce without very high end arbitrary waveform generators. Instead of trying to design a sophisticated and dedicated circuit to reproduce this pulse, my approach here is to take advantage of digital signal processing and modulate the synthesized band A pulse to a band B frequency to then generate it with an AWG-like device. To verify

the setup in this band, the ratios between the readings of the detectors have to be within the CISPR16-1-1 specifications shown above.

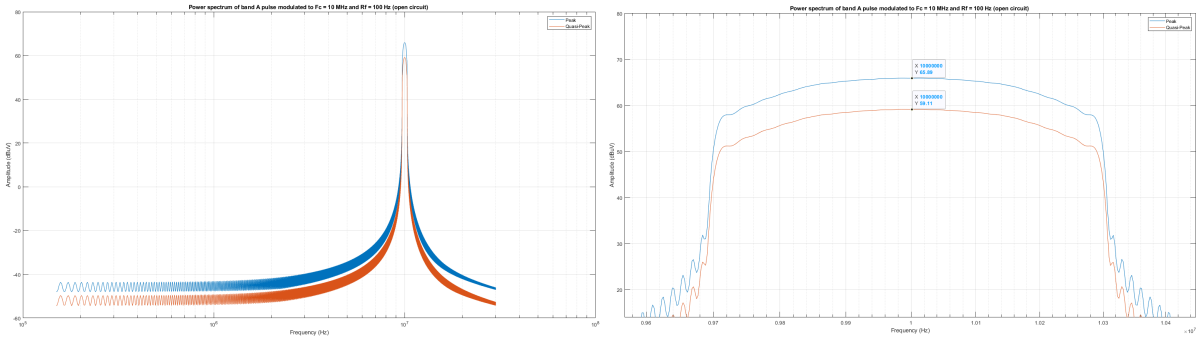
Code 3: Matlab code to modulate the band A pulse to a Fc frequency within band B

```
load Short_A_225MHz;

Fs = 225e6;
RBW = 9E3;
Fc = 10e6;

vectSize = 2.5e6;
pulseLength = length(Pulse_A_225MHz);
WAVE = Pulse_A_225MHz;
WAVE = WAVE./(RBW/200);
TIME = linspace(0,vectSize/Fs,vectSize)';
WAVE = modulate(WAVE,Fc,Fs);
P = zeros(vectSize,1);
P(vectSize/2 - pulseLength/2 : vectSize/2 + pulseLength/2 -1) = WAVE;
```

Code 3 shows the Matlab implementation used to modulate the band A pulse (sampled at 225 MHz with a repetition frequency of 100 Hz) to a carrier frequency of 10 MHz. It is important to note that the band B pulse, by definition, has an impulse area smaller than the pulse in band A to compensate for the increase in resolution bandwidth (200 Hz in band A compared to 9 kHz in band B). This has to be taken into account and the amplitude of the pulse has to be reduced by a factor of $\frac{9\,\text{kHz}}{200\,\text{Hz}} = 45$.




(a) Zoom of the band A pulse




(b) Full spectrum (c) Zoom of the spectrum

Figure 7: Peak and quasi-peak spectrum of band A pulse modulated to a carrier frequency of 10 MHz with a repetition frequency of 100 Hz

Figure 7b and Figure 7c show the peak and quasi-peak detectors applied to the band A pulse modulated to a carrier frequency of 10 MHz. The ratio between them is 6.78 dB, 0.18 dB above 6.6 dB, which is within the ± 1.5 dB tolerance allowed by the standard.

# 3 Device Design

This chapter presents a detailed description of the work undergone for designing the reference signal generating device. The workflow comprised the following steps: definition of hardware performance requirements; high-level design using block diagrams to represent the fundamental modules; identification and selection of main the components of each module; schematic circuit design and simulation including the selection of the appropriate circuit topologies and performing the calculation for all the required component; design of the non-included footprints and 3D models of each component; physical design with regards to the enclosure and printed circuit board layout.

Although it seems to be a straight design path, all the phases listed above are closely tied to each other and a change in one aspect of the device may result in modifications in the rest of the modules, requiring to continually jump in between phases.

## 3.1 Hardware performance requirements

The device is intended to be used to verify standard test setups and measuring instruments in EMC laboratories, therefore, it must comply with the following mandatory requirements:

- According to CISPR 16-1-1, the output frequency range of the device must comprise the CISPR bands A and B, that is, from 9 kHz to 30 MHz.
- The device must be able to generate the previously designed waveforms.
- The device must have enough memory to store the waveform datasets.
- The device must feature an output connector capable of working in the frequency range of the device.
- The device must feature a $50\,\Omega$ output impedance.
- The device must be able to be connected to a V-LISN artificial network described in CISPR16-1-2.
- The accuracy of the device must be better than:
  - $\pm 01\%$ of the desired frequency.
  - $\pm 0.25\,\mathrm{dB}$ of the desired spectrum amplitude.
- The device sample rate must be greater or equal to 100 Msps (in order to be able to generate precisely and reliably the previously designed signals).
- The Spurious Free Dynamic Range must be better than that of the measurement system: SFDR $>$ 60dB.
- The resolution of the output signal must be greater or equal to 14 bits.
- The dynamic range of the output must be capable of producing the previously generated signals.

- The output uncertainty levels must be better than those specified in CISPR16-4-2 for measurement instruments in the range between 9 kHz and 30 MHz (Table F.1), resulting in an expanded uncertainty $< 3.3$dB.

## 3.2 Circuit design

In order to determine how this device is going to reproduce the waveforms designed in section 2 some initial choices have to be taken. These initial decisions are captured in the block diagram from Figure 9.

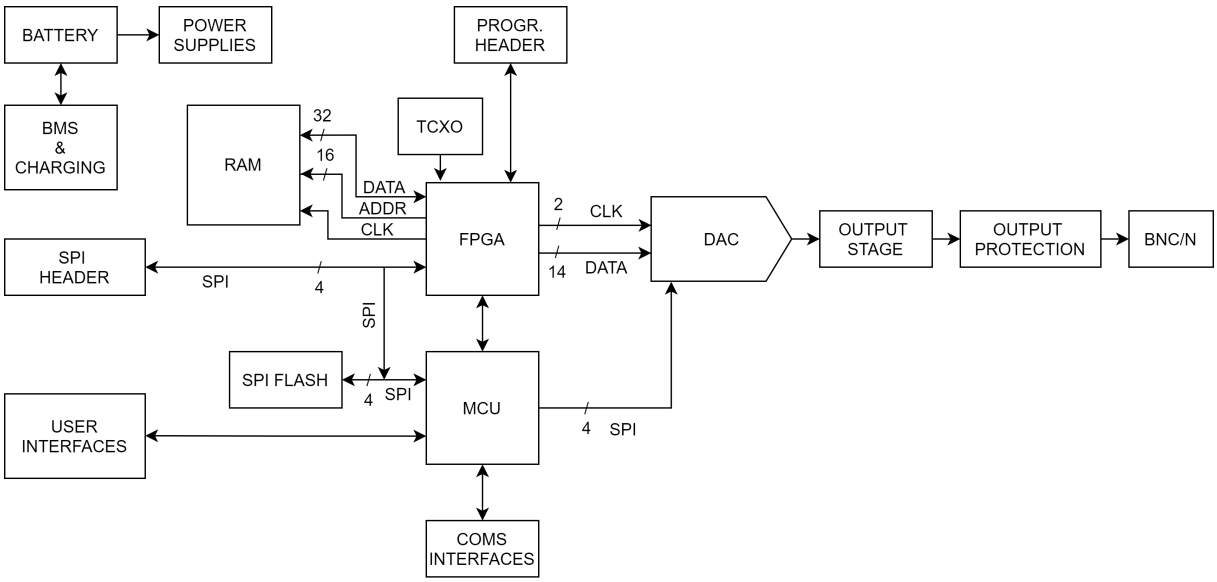



Figure 8: Block diagram of the circuit

Considering the device has to output several different types of complex waveforms, the only feasible option was using a high speed low noise Digital to Analog Converter (DAC). A DAC by itself is not capable of producing as wide range of amplitudes as we need while maintaining the required resolution, so in order to condition the signals to the desired levels, an output stage has to be placed after the DAC.

This device will have two differentiated domains: the digital and the analog domain. The analog portion of the circuit will include precision analog components whereas the digital part will contain lots of noisy circuits. For the purpose of trying to isolate the noise created by the digital elements, both domains will need different ground planes and power supplies.

Data fed to a DAC that works at such high frequencies is usually done by means of a high speed differential serial interface or a parallel interface, both of which require high speed communications but being the serial interface the one that needs higher link speeds. This implies that some sort of high speed memory will have to be present along with some non-volatile memory to store the waveforms when the device is turned off.

In order to be able to connect all these elements, the best solution is an FPGA because of the high complexity and high customization degree this interconnection requires.

The RF output of the device must be protected in case that mains voltages are present. This is possible because the device will be plugged into the power port of a LISN which is

used to power and, at the same time, decouple devices from the power grid, meaning that if the LISN is not conscientiously unplugged from the power grid before the verification, our device would be severely damaged.

The device needs to have a "main brain" that controls and monitors everything at the same time that provides communications with the exterior and user interfaces. This control will be taken by some sort of embedded microprocessor.

This will be the first iteration of the design, so it is a good idea to feature various connectors that allow the different modules to be operated externally without the need of having everything functional during development stages.

All of these circuits will have to be powered up with their own voltage levels, requiring different power supplies. These power supplies, at the same time, also require to be powered up. My decision is to power everything up using batteries, this way high voltages are away from the device and there is no power cable during operation. This eliminates the need of some EMC tests like conducted emissions or surge immunity.

During the design phases of the project, 3 main software utilities have been used. These have been chosen for the features they offer but also because of my considerable previous experience with them.

- KiCad: a free and open source suite of Electronic Design Automation tools to develop PCBs. Despite being free it is a very powerful package that allows the design of very complex and high end boards and even competes with other big brands.
- LTSpice: a free professional SPICE based analog electronic circuit simulator produced by Analog Devices. Moreover, it is the most widely used SPICE simulator.
- Fusion 360: a professional multi-tool CAD solution. This software requires a valid license but, fortunately, there exists a free student license. Although its tools extend to many areas, I have only used their 3D modeling functionality.

### 3.2.1 Schematic

The schematic has been divided into different sheets trying to resemble to the previously designed block diagram.

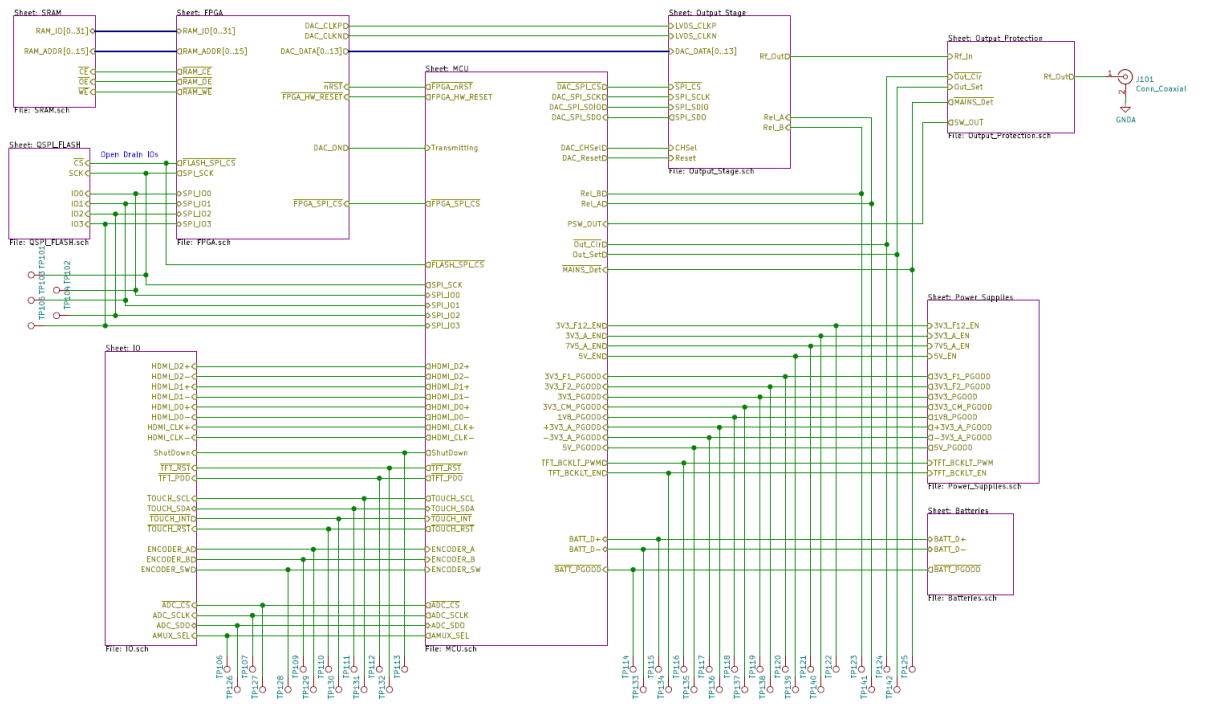



Figure 9: Main sheet of the schematic with all the blocks that conform the circuit (only data lines are represented)

### 3.2.1.1 Output stage sheet

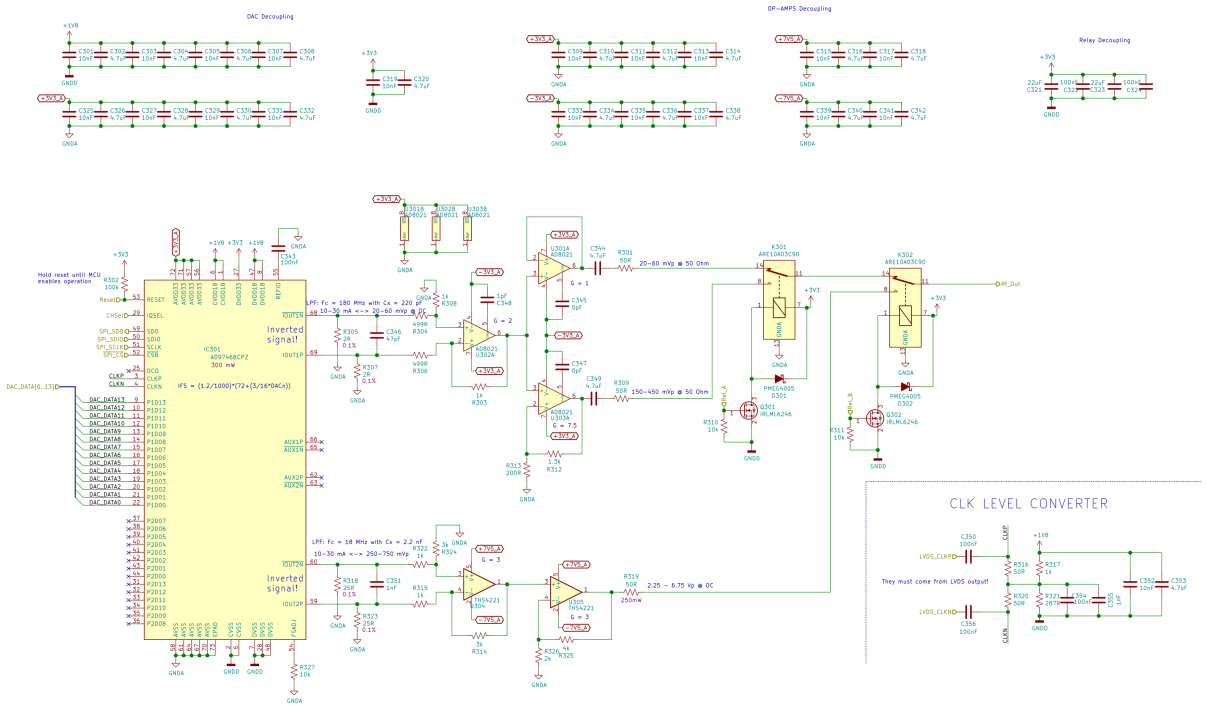
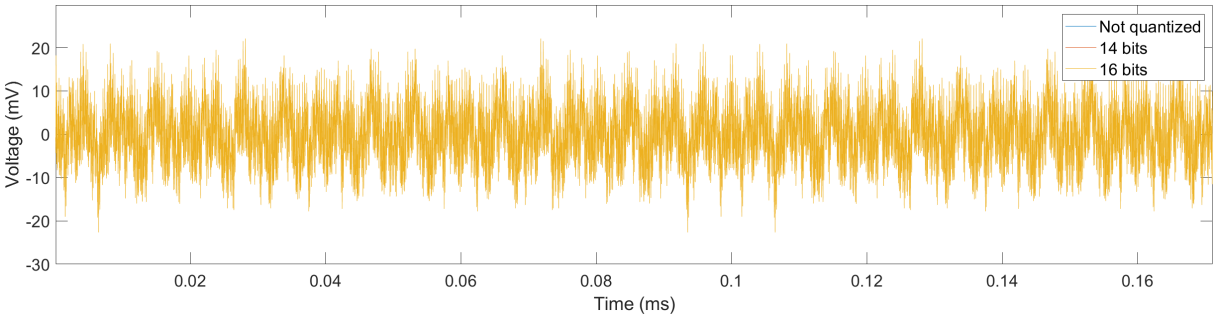



Figure 10: Schematic of the finished output stage

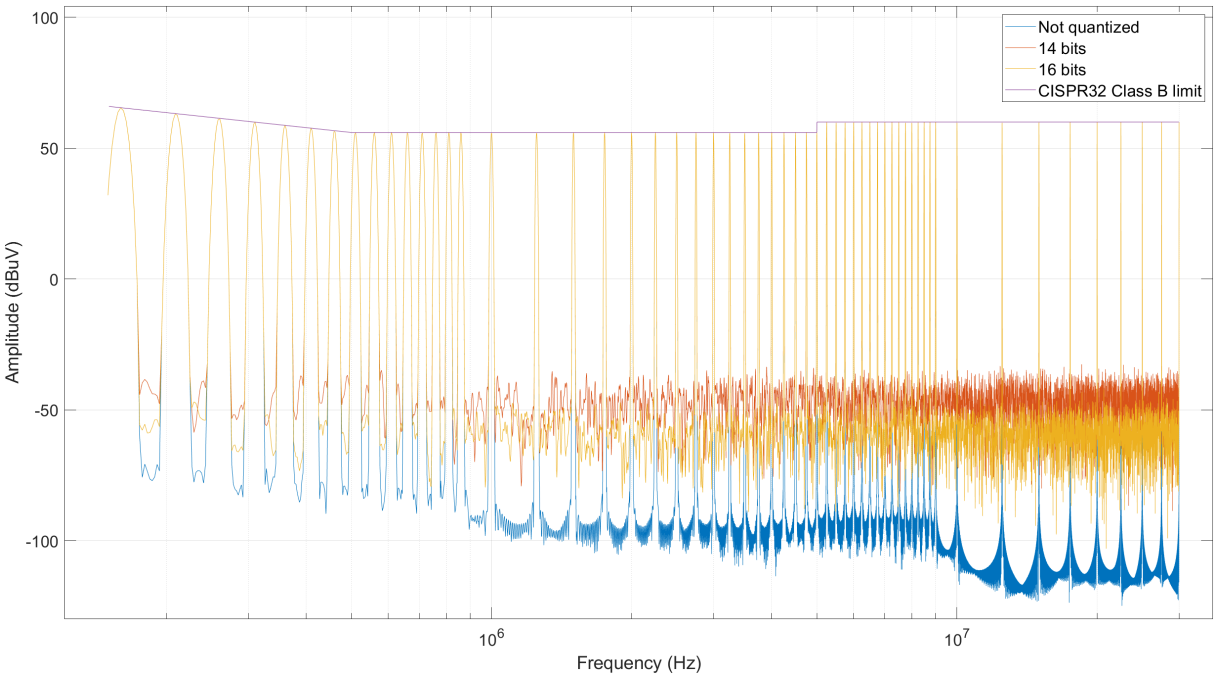
## DAC

A key aspect to decide for selecting a suitable DAC is its resolution. The DAC resolution affects the fidelity, the accuracy and the noise of the synthesized waveform. For generating high resolution waveforms a survey of the DACs available in the market was performed. After analysing the DACs specifications versus the required performance of the device, only DACs with 14-bit and 16-bit resolution were considered.

Then simulations with Matlab were carried out to observe how the idealized waveforms were affected by the quantization process at the two different resolution of the DAC. Figure 11 shows one of the performed simulations, in this case the result of the quantization with 14 and 16 bits a 60 tone waveform with Shapiro-Rudin phases. All the simulations corroborate that the only notable difference between the quantized waveforms is found in the noise floor of the spectrum. Due to the higher price of the 16-bit DACs and the fact that the noise floor of the measuring receiver itself is well above both of them (around 10 dBµV), it is decided to use a 14-bit DAC.




(a) Time domain signals




(b) Quasi Peak spectrum of the signals

Figure 11: 14 and 16 bit quantization of a 60 tone waveform with Shapiro-Rudin phases.

After comparing various 14 bit DACs from different manufacturers, the chosen option is an Analog Devices' AD9746BCPZ [10]. It can work at up to 200 Msps and features 2 independent differential main output channels with programmable full scale current from

10 mA to 30 mA, 2 auxiliary output channels and a precision internal voltage reference, all in a 10x10 mm QFN50 package. Data is fed, by default, through a 14 bit wide parallel interface per each channel with a common differential clock, but it can be configured to fed both channels through one single interface.

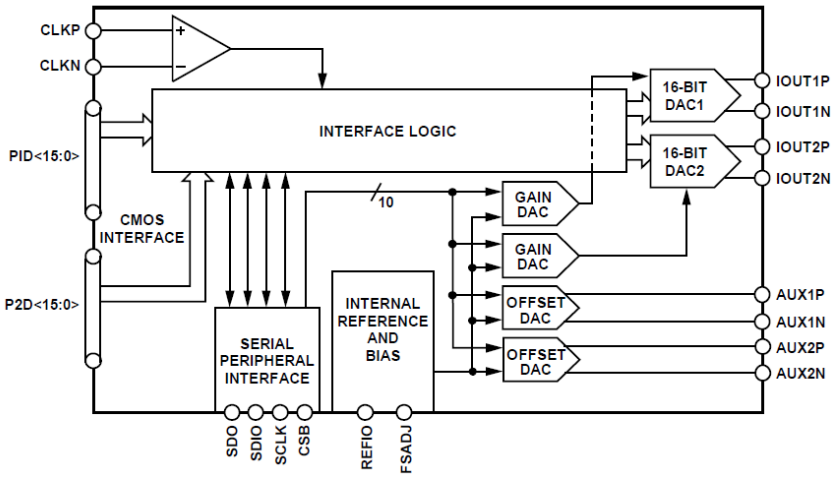



Figure 12: Internal block diagram of Analog Devices' AD9746 [10]

An important factor is that its SFDR is above 70 dB throughout our whole working frequency range (from 9 kHz to 30 MHz) as shows Figure 13.

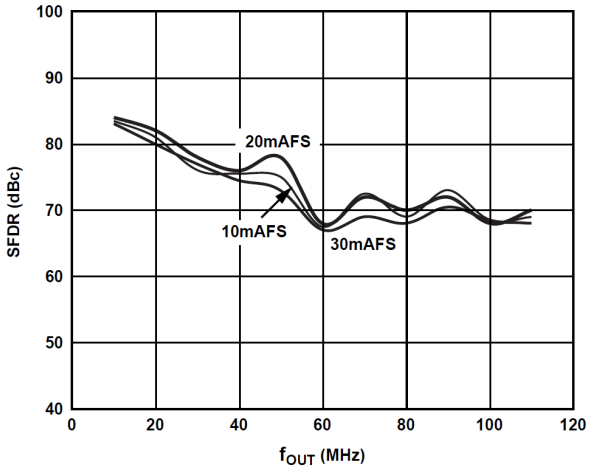



Figure 13: AD9746 SFDR vs. frequency over various Full Scale currents [10].

The clock input of the DAC requires a low voltage differential signal but specifies some tolerances that make the levels incompatible with the LVDS protocol. In order to solve this, in the datasheet it is provided an easy to implement conditioning circuit to match the voltage levels from LVDS to the DAC requirements [10]. The conditioning circuit is shown in Figure 14.

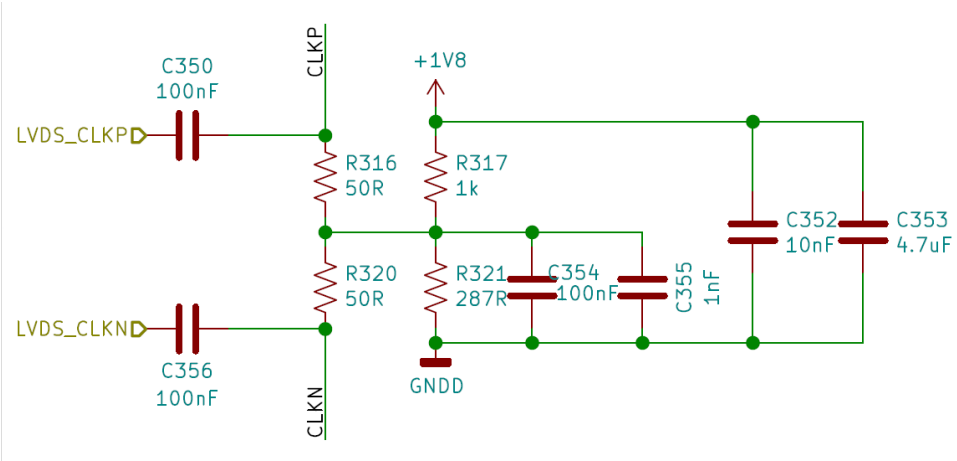
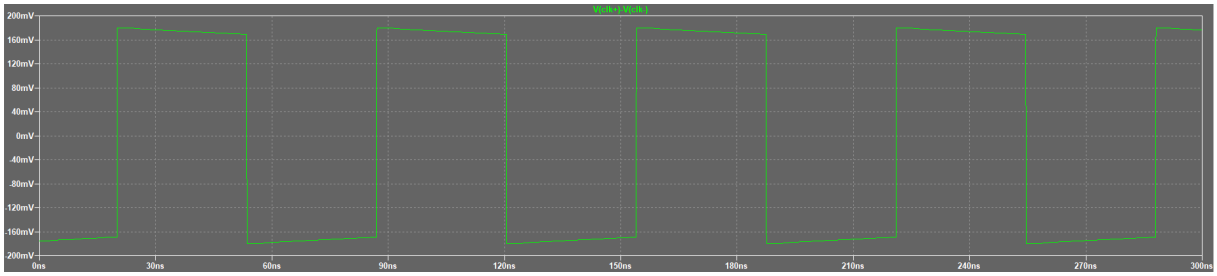
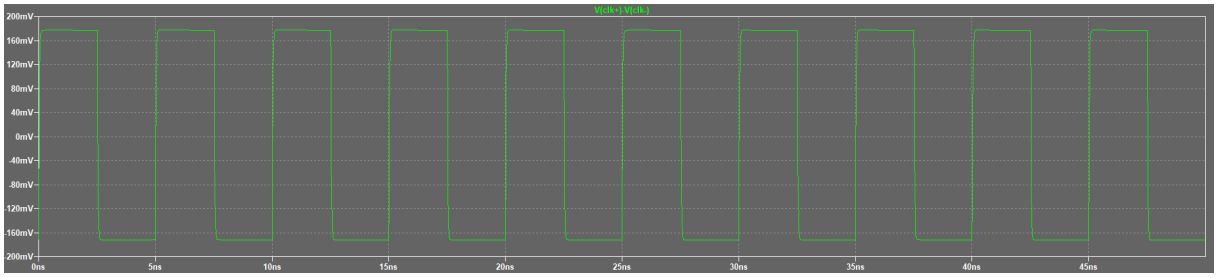



Figure 14: Recommended level shifting circuit.

Although the level shifting circuit is purposed in the datasheet, I decided to simulate it using LTSpice taking into account some non-idealities of the passive components to see if it is good enough for our purposes and Figure 15 demonstrates that the circuit fulfils the requirements.



(a) Response at 15 MHz



(b) Response at 200 MHz

Figure 15: Transient response simulation of the clock level shifting circuit for the DAC.

### Operational amplifiers

The wide variety of frequencies and voltage gains at which this device has to work makes the use of external amplification stages mandatory. With regard to the multi-tone signals and band B pulses, their working frequency range falls between DC and the lower portion of RF, but since RF components are not designed for frequencies as low as 9 kHz, components such as transformers and RF amplifiers are instantly discarded. This leaves high-speed op-amps as the only viable option for this signals.

The chosen amplifiers for the high-speed output stage are the Analog Devices' AD8021

low-noise high-speed operational amplifiers. They present a excellent frequency response even at low gains (some of the Op-Amps are only stable at G > 10), very low noise and their frequency response can be compensated by means of an external capacitor. They come encapsulated in a MSOP8 package.

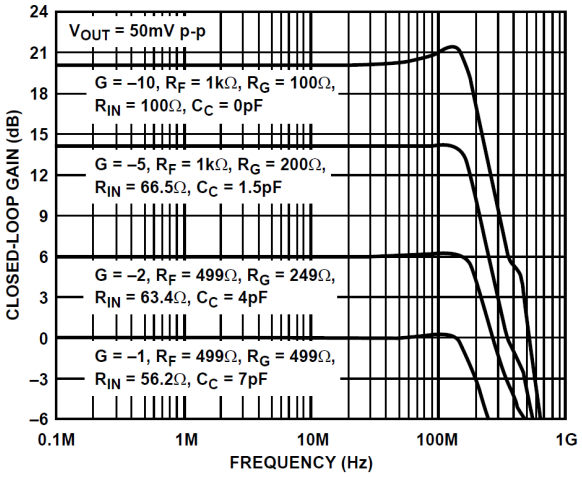



Figure 16: Theoretical small signal frequency response of AD8021 from [11].

Figure 16 from the AD8021 datasheet [11] shows the specified frequency response the operationals have at different gains. In theory they should work for the design purposes since they have a flat response throughout our whole working frequency range.

In the other hand, AD8021 Op-Amps are only able to provide 60 mA of current but the high voltage output stage will need to provide, at least, up to 3.25 Vp at a 50 Ω load, what equals to 65 mA of current. Fortunately, band A pulses do not have such high bandwidth but a higher amplitudes. In this case more traditional general purpose operational amplifiers can be used.

Finally, Texas Instruments' THS4221 [12] operational amplifiers are a suitable choice because they can deliver enough current at such high voltages. THS4221 exhibit a good frequency response for band A pulses and up to 100 mA of current at the needed voltages in a tiny SOT23-5 package.

### Low-voltage, high-speed output stage

Multitone waveforms require levels lower than 60 mVp open circuit and band B pulses require higher levels than that but always lower than 300 mVp open circuit. In order to maximize the DAC's dynamic range utilization, the signal needs to be split into 2 paths with different amplifications.

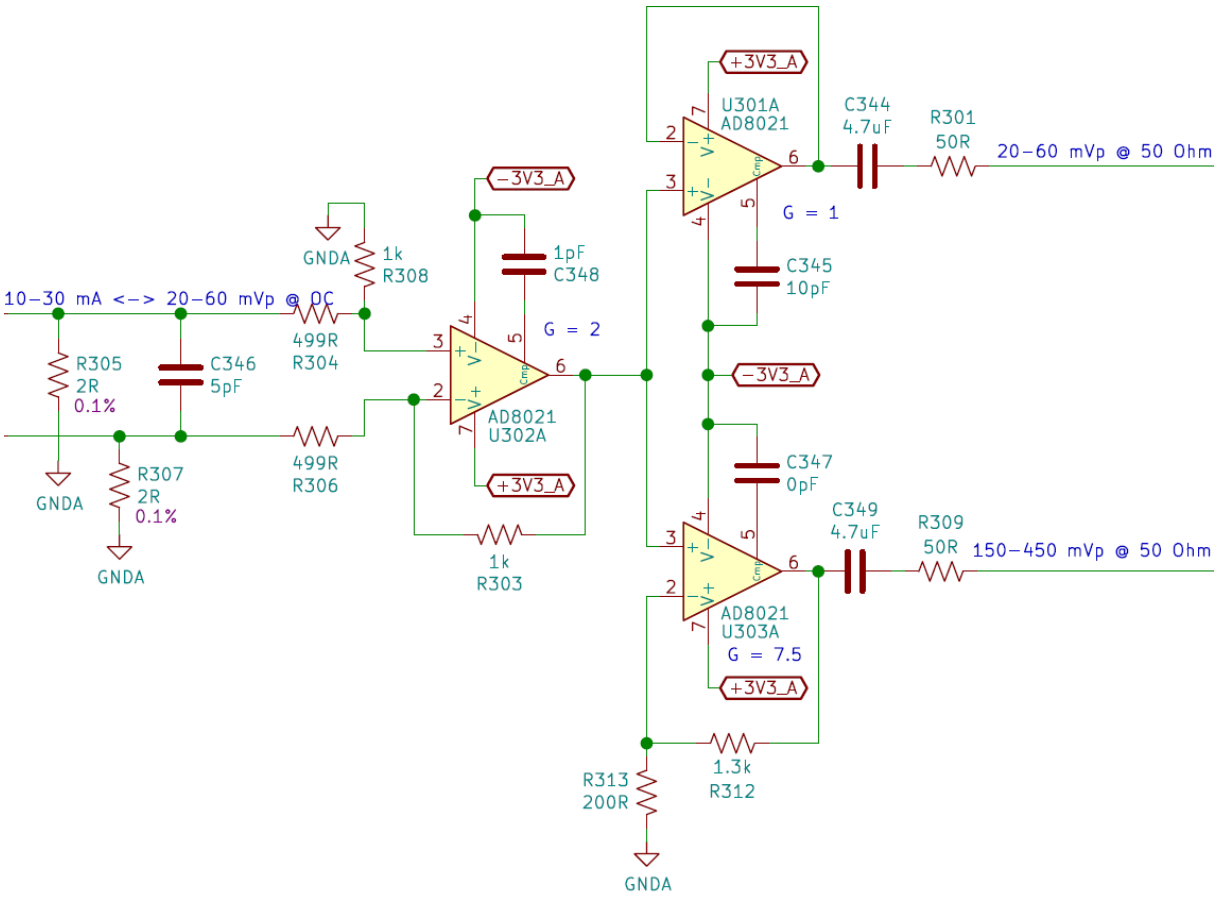



Figure 17: High-speed low-voltage output stage.

Following the recommendations in [8], the first stage after the DAC is a single ended output differential amplifier with a gain of 2 (U302A), as shown in Figure 17. It receives the differential signal from the 2 Ω loads at the output of the DAC and converts it into a single ended signal between 40 mVp and 120 mVp (open circuit) at the minimum and maximum full scales. Then, the signal is split into two and fed to a couple of different operational amplifiers. U301A acts as a voltage follower (to avoid loading effects to the differential amplifier), producing the same output voltage levels as U302A. The second one is configured as a non-inverting amplifier with a gain of 7.5, producing a maximum output voltage of 300 mVp open circuit at minimum FS and 700 mVp open circuit at the maximum FS. At the end of both signal paths, a series termination resistor is placed to avoid reflections along with an AC coupling capacitor.

The circuit was simulated using SPICE models provided by the manufacturer to fine tune the component selection and their values.

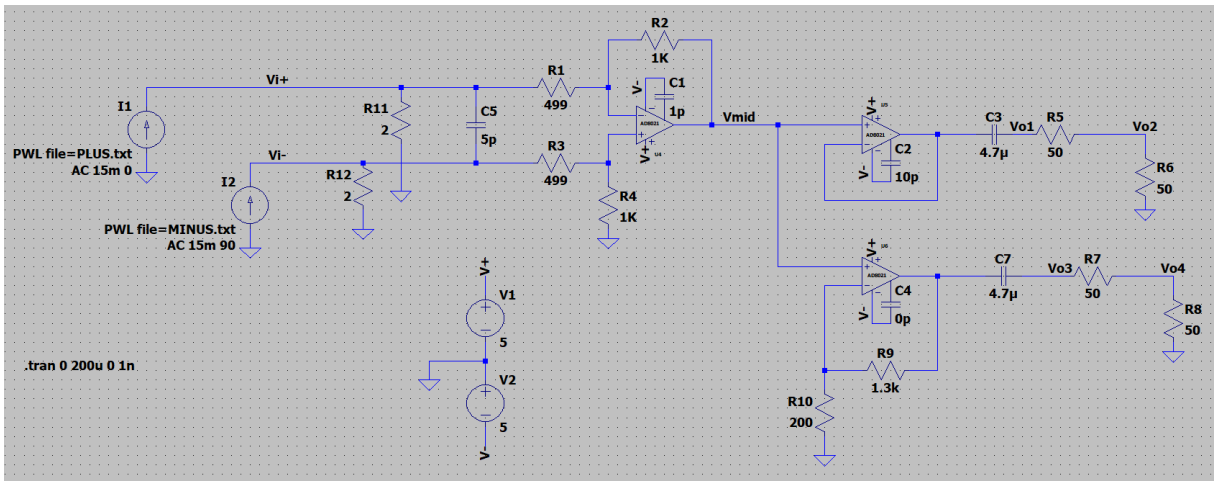



Figure 18: LTSpice schematic of the high-speed low-voltage output stage.

The final frequency response of the circuit is shown in Figure 19. The path through U301A corresponds to the green trace. The amplitude difference is only 0.1 dB throughout our whole frequency range, but the phase shifts 25°. The other path, coming through U303A, is represented with a yellow trace. The amplitude difference is around 0.5 dB and the phase shift is 25° as well. Again, because in this type of measurements the phase of the signal is not measured, both circuit responses are well within the requirements.

In order to check how will the circuit perform in its real task, some of the previously designed waveforms have been synthesized and inputted to the LTSpice circuit. Figure 20 shows the FFT of the output of the lower voltage stage to a multi-tone signal. Not many conclusions can be drawn from the amplitudes (since EMI measurements require special normative detectors) but it clearly maintains its intended shape.

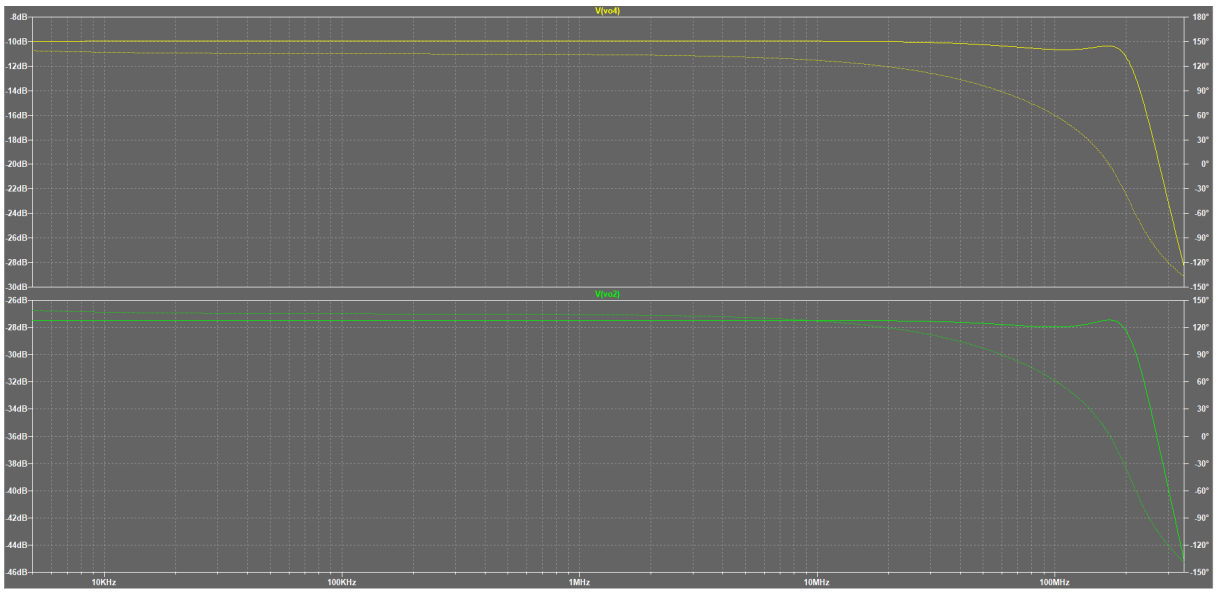



Figure 19: AC Simulation of the high-speed low-voltage output stage.

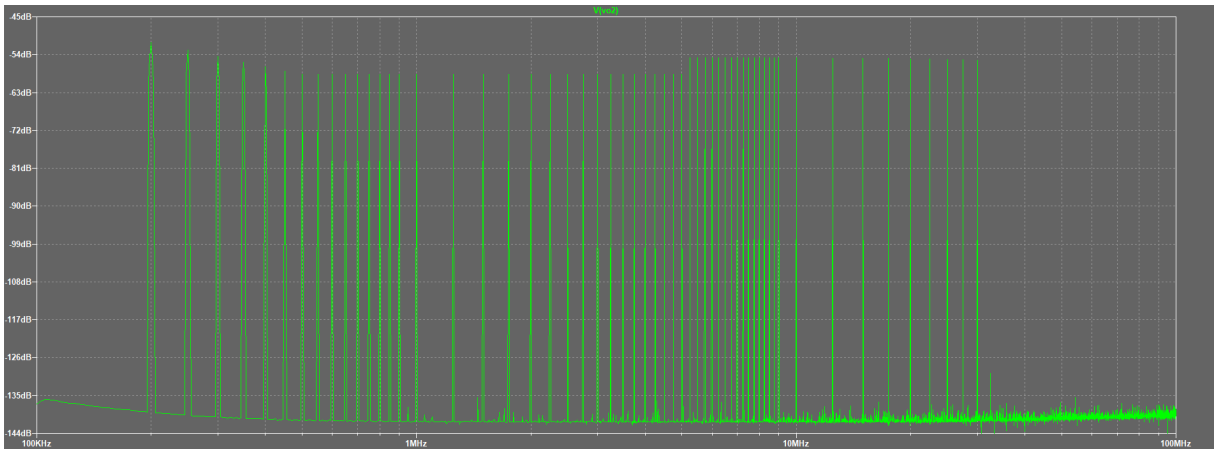



Figure 20: FFT of the transient response of the high-speed low-voltage output stage to a 59 tone signal with Shapiro-Rudin phases.

### Low-speed high-voltage operational amplifiers

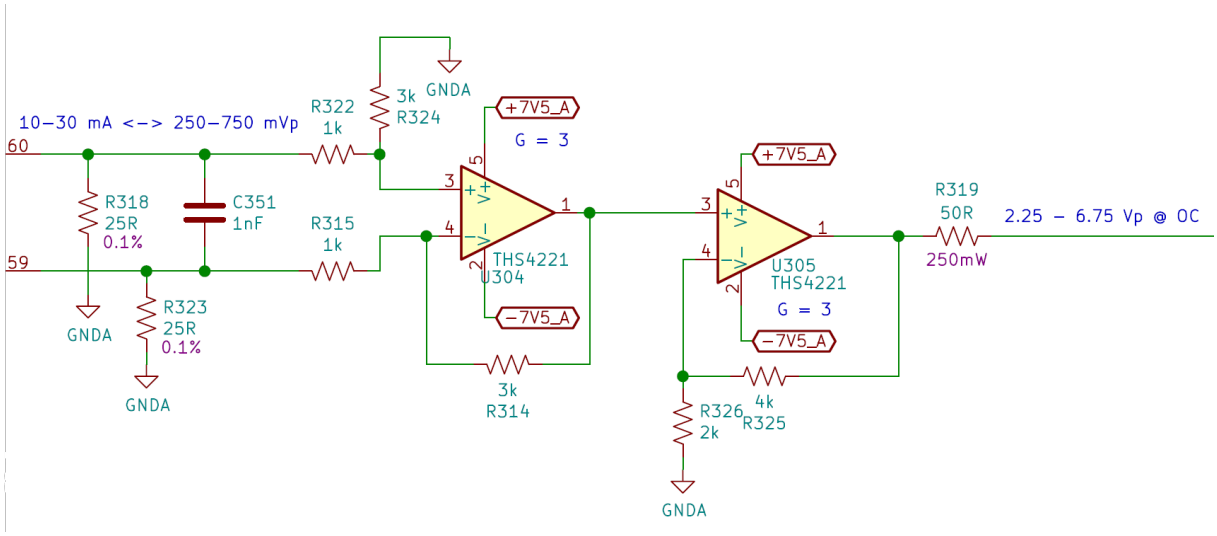



Figure 21: Low-speed high-voltage output stage.

In this case, the DAC output will be only used for band A pulses. This way, only a single path is needed. Following the same topology as in the high-speed paths, the first stage after the DAC is a differential amplifier, but the DAC termination resistors are now of 25 Ω and the gain of the amplifier is set to 3. In order to obtain a total gain of 9 and to maintain the gain-bandwidth product, a non-inverting amplifier is placed after the other with a gain of 3. As a result, the circuit's maximum output voltage at the minimum and maximum full scale currents should be 2.25 Vp and 6.75 Vp in open circuit, respectively.

Again, to fine tune and check the performance, the circuit has been simulated using LTSpice.

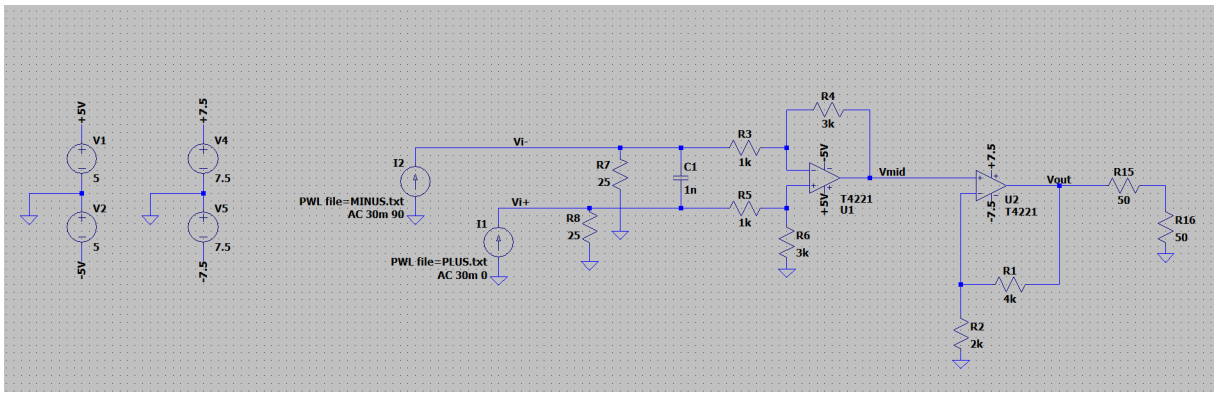



Figure 22: LTSpice schematic of the low-speed high-voltage output stage.

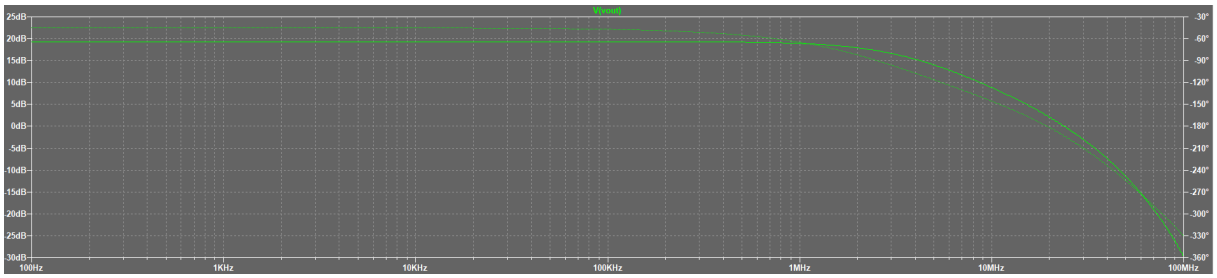
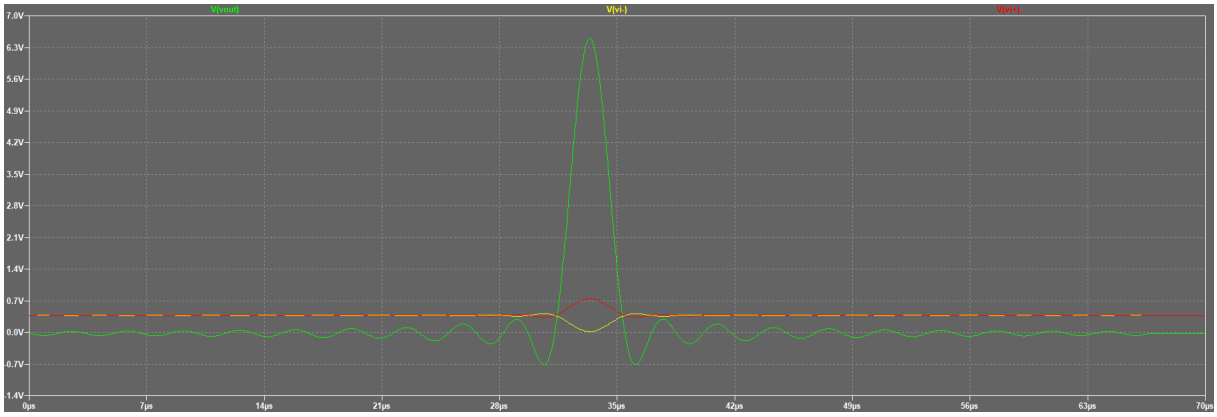


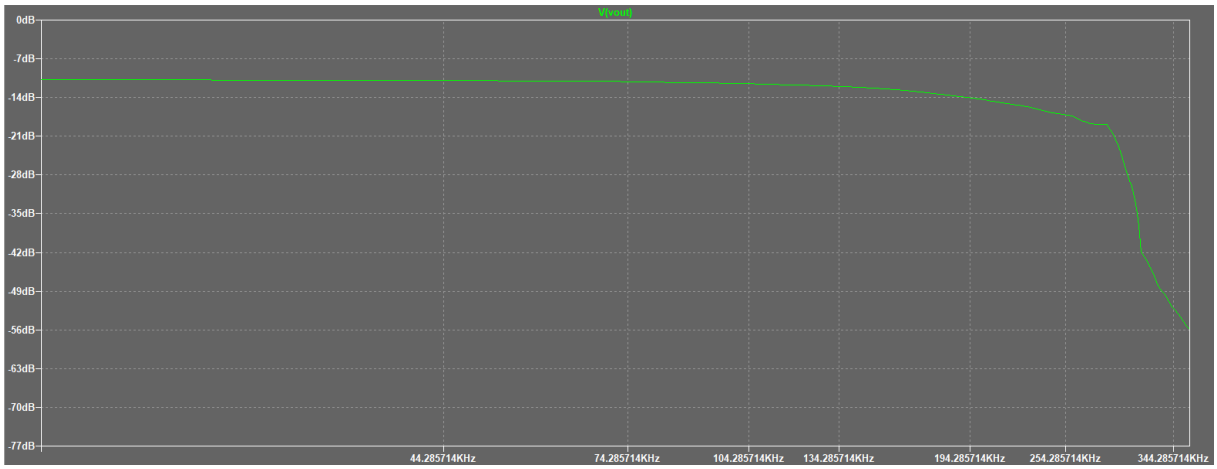

Figure 23: Simulation of the AC response of the high voltage output stage.

In Figure 23 is simulated the AC response of the circuit. The amplitude stays flat throughout the whole working frequency range and the phase shift is only of 1°.

If the synthesized waveform is inputted to the circuit, its transient response is seen in Figure 24a and its spectrum in Figure 24b. The spectrum shows that, in this case, the amplitude response is maintained too.




(a) Time domain band A pulse. Red anb yellow: differential source; green: output




(b) FFT of a)

Figure 24: Simulation of the response of the high voltage output stage to the band A pulse.

### Signal multiplexing

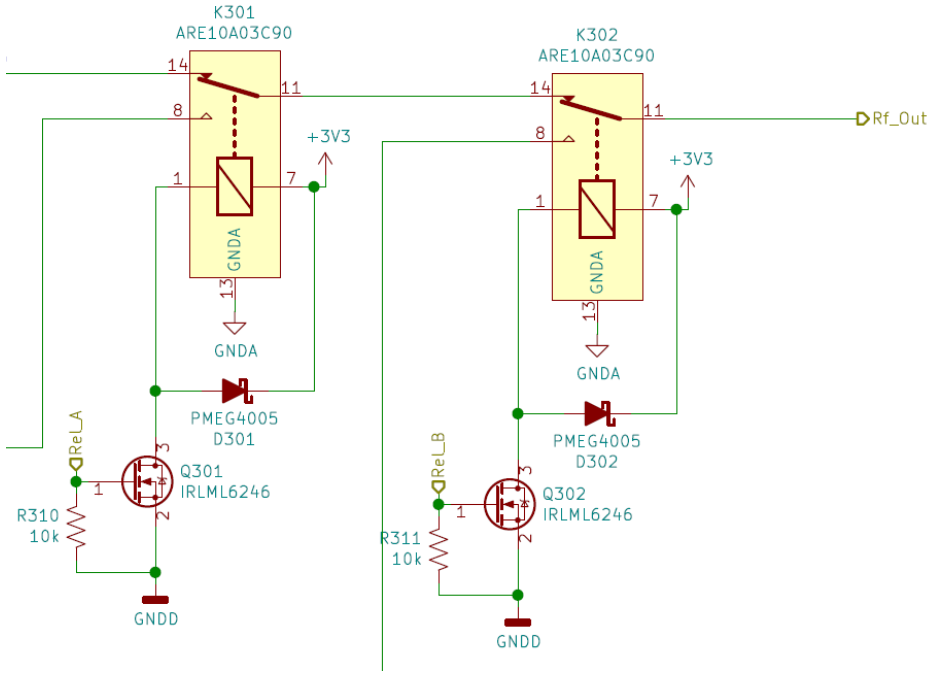



Figure 25: RF signal multiplexing.

Due to the fact that the signal is split into three different paths, they have to be multiplexed to reach the output one at a time. The overall best solution is to use RF relays (the exact selected model is a Panasonic ARE1003C90 [13]). Other options like RF switches and analog switches have been studied but their downsides make them unusable for our purposes. Specifically, RF switches were discarded because their behaviour and linearity is degraded in our working frequencies and their isolation is worse than the offered by an RF relay. On the other hand, analog switches were discarded because they add large series resistance (comparable to that of our system) that also depends on the

input voltage, almost none of them includes frequency response graphics, their isolation is very poor (around 20 dB) and the fastest ones do not support the voltage levels of band A pulses.

#### 3.2.1.2 Output protection sheet

As stated before, the output of the device will be plugged into the power port of a LISN. If the LISN is not conscientiously disconnected from the power grid before plugging in the reference signal source, our device would be instantly destroyed. In order to add an extra safety layer, some sort of protection circuitry has to be placed. The problem here resides in the fact that any components added into the RF line will modify the shape of the signal. A trade-off between safety and functionality is to add a high impedance monitoring circuit in parallel with the output and an RF relay that opens the circuit. The idea is to maintain the output always opened until the device has been plugged in. In that moment, the protection circuitry will monitor the output and if mains voltages are present, it will notify the user with a loud buzzer and will not allow the output relay to close. To make this more secure, this check will be done completely by hardware, making it impossible to close the output relay if the LISN is plugged into the power grid. One big problem that I am still not able to overcome appears if the user decides to plug in the LISN to the power grid while a verification is being performed. If the mains voltage happens to be near the zero cross, the protection circuitry will be able to immediately open the relay, but if the voltage happens to be near its peak, the circuitry will not be fast enough to disconnect the output before it is too late.

The resulting circuit is seen in Figure 26.

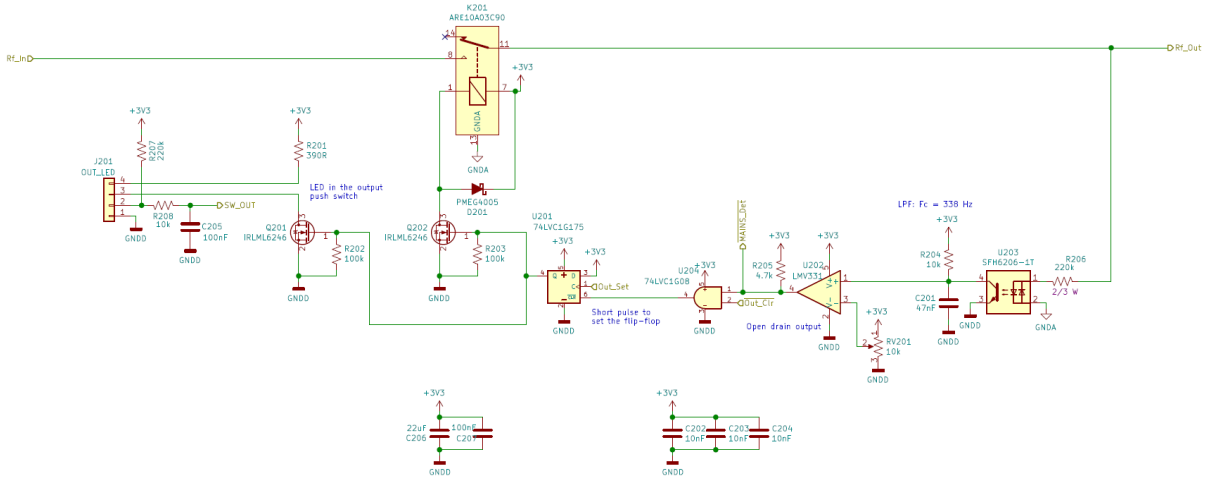



Figure 26: Schematic of the output protection.

Directly from the output connector, the signal is passed through a resistor to an AC optocoupler in an attempt to isolate the analog and digital parts. The series resistor value has to be selected so that the maximum current flowing through the optocoupler is less than 60 mA and the dissipated power is below the resistor's rating, at the same time that creates sufficient current flow though the coupled transistor. The output of the optocoupler is connected to a pull-up resistor (and a capacitor that acts as a low-pass filter) and into the non-inverting input of an LMV331 comparator. The other input of the

comparator is connected to a trimmer potentiometer that will be used to set the tripping voltage of the circuit. The potentiometer is needed since optocouplers present a wide tolerance for their current transfer ratio (which is the ratio between the current flowing through the input diodes and the current it creates at the output transistor). The output of the comparator is then fed into the input of an AND gate in conjunction with a clear signal coming from the microprocessor. The resulting signal is connected to the reset pin of a D-type flip-flop whose output controls the activation of the protection relay and an LED indicator located inside the output push button. This way, whenever mains voltage is present in the output connector, the flip-flop will be hold in reset and the output will not be able to be activated. To activate the output, the user has to push the output push button and the microprocessor creates a short pulse in the clock input of the flip-flop.

Figure 27 shows the push button that will be used to enable the output. It has a handy little red LED that will indicate the state of the output.

Figure 27: Push button used to enable/disable the output

### 3.2.1.3 FPGA sheet

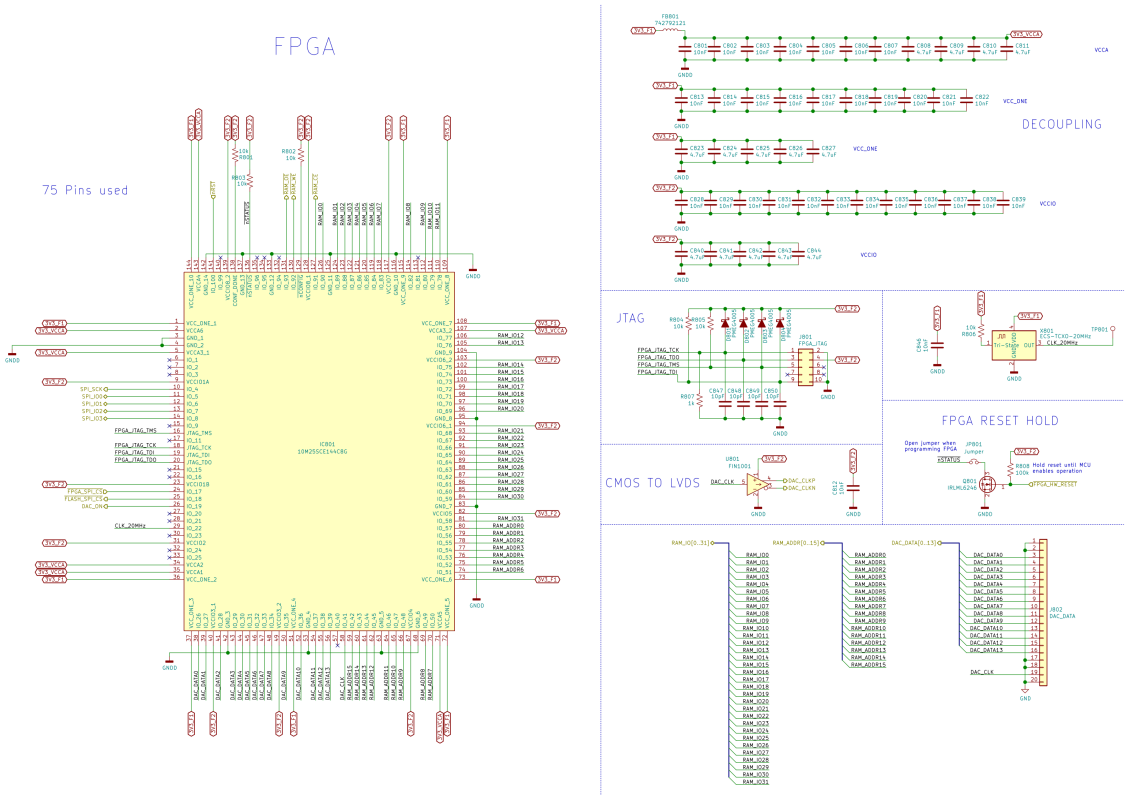



Figure 28: General view of the FPGA schematic sheet.

## FPGA

As stated before, an FPGA will be used to perform the interaction between different blocks. For this purpose, it needs to comply with some specific requirements:

- It has to feature internal boot flash so that the circuit is stored inside the FPGA and the biststream does not have to be uploaded everytime it is powered up.
- It needs to be capable of working at speeds higher than 200 MHz.
- It has to be able to function without the need of complex power supplies.
- It does not have to need very precise power supply ramping ups.
- It has to be able to be hot-socketed (the pins can be powered although the FPGA is not).
- It has to integrate a sufficient number of logic elements, embedded multipliers and RAM memory.
- It has to have enough I/O pins for our purposes.
- It has to integrate various PLLs capable to output their signal to the output pins.

- Its output pins have to be tri-state (they feature a high impedance state).
- Its development tools have to be available for free.

With these requirements in mind, the selected FPGA is a 10M25SCE144C8G from Intel's Max 10 family. Some of its main features are:

- It has 25000 logic elements.
- It works at frequencies up to 450 MHz.
- It has more than 100 I/O pins.
- It contains boot flash memory and some flash memory usable by the user.
- It includes 675 kb of on board RAM memory that can be used in case the external RAM solution does not work as intended.
- It can deliver up to 20 mA of current per I/O pin.
- It can work with a single 3.3 V voltage level.
- It can be hot-socketed.
- All of the pins are tri-stated.
- The bitstream can be uploaded via JTAG.
- Intel Quartus Prime development platform is free for the Max 10 family.

Usually an FPGA requires complex power supplies with precise ramping up orders and times so that they can boot up and function correctly, but, in this case, the chosen FPGA can work with 2 simple 3.3 V switching power supplies as Figure 29 shows. In spite of being simple, these power supplies need to be good enough so that they can provide up to 6 W of power with ripple values that not exceed 5 %.

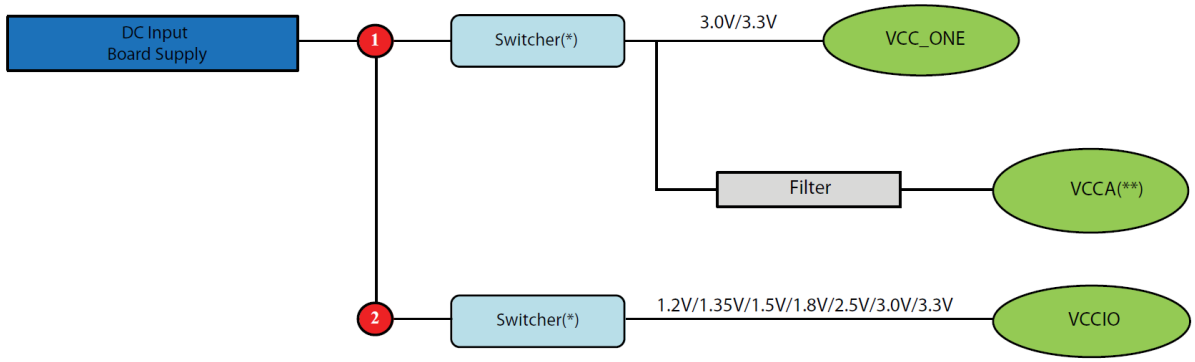



Figure 29: Single voltage power supply configuration for the FPGA [14].

### Reset hold

In normal use, the microprocessor will hold the FPGA in a reset state until it has booted up and everything is configured. This serves as a safety feature as well as a power saving method when the device is not injecting any waveform.

In order to program the FPGA, the reset hold has to be bypassed. This strategy will be accomplished with the simple circuit from Figure 30.

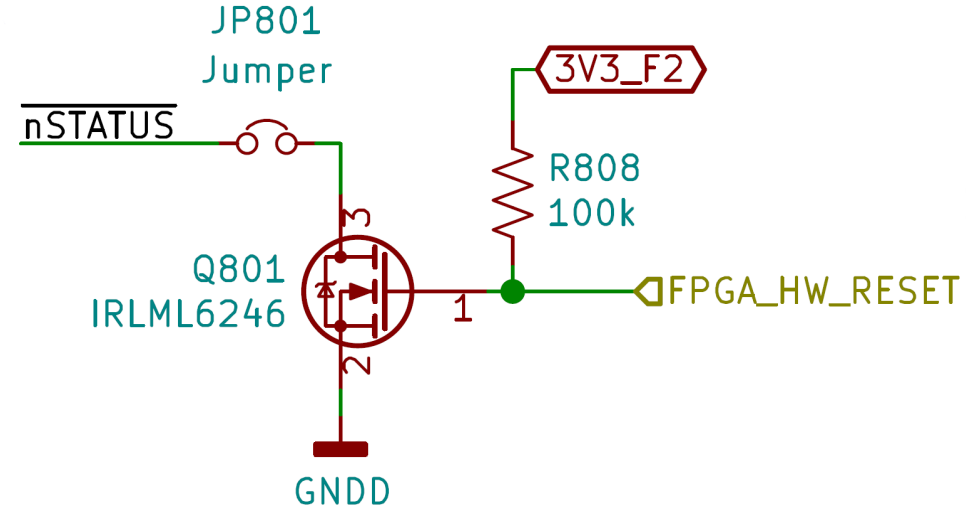



Figure 30: FPGA reset hold circuit.

### Oscillator

The nature of this device makes the FPGA having to work at frequencies as high as 360 MHz. These frequencies will be generated by the internal PLLs of the FPGA but, to be able to perform properly, they need very precise clock references. This reference will be provided by an external 20 MHz TCXO (Temperature Compensated crystal Oscillator). This oscillator ensures that the frequency will be stable throughout its whole temperature working range. In this case, the chosen TCXO is a CMOS output ECS-TXO-2016-33-200-TR whose overall frequency stability of $\pm 2.5$ ppm from -30 to 85 °C.

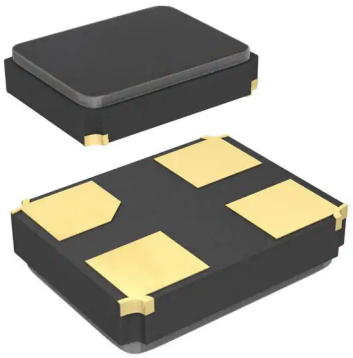


Figure 31: Picture of the TCXO package [15].

### LVDS driver

The main clock signal for the DAC will come from one of the FPGA outputs. As seen before, this clock signal needs to comply with the LVDS standard. The FPGA itself is capable of generating LVDS signals but, then, the whole bank where the differential pins belong have to be fed with the lower voltage levels needed for the LVDS protocol. Since this clock signal is going to be the only LVDS signal in the circuit and the FPGA does not have enough pins to sacrifice a whole bank, I have decided to use an external LVDS driver to convert the clock line coming from an standard single ended CMOS output. This driver will add a delay to the clock signal that will have to be compensated inside the FPGA.

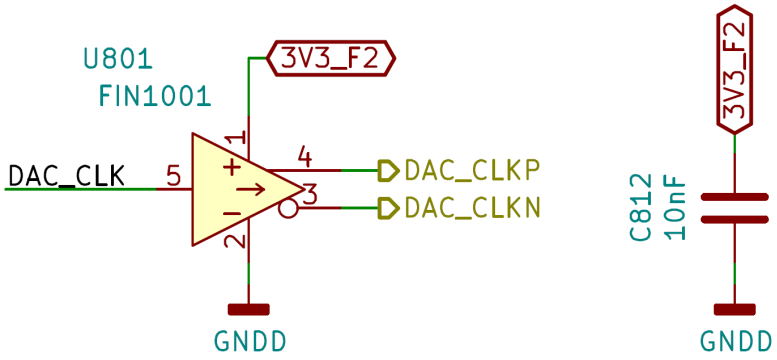



Figure 32: LVDS clock driver.

### JTAG connector

The uploading of the bitstream into the FPGA has to be done using an Intel proprietary programmer, called USB Blaster, that is connected using the common JTAG standard.


Figure 33: Picture of a USB blaster manufactured by Terasic.

The USB blaster uses an standard 2x5 pin 0.1" pitch connector. Figure 34 shows the additional circuitry needed in accordance with the FPGA datasheet [14].

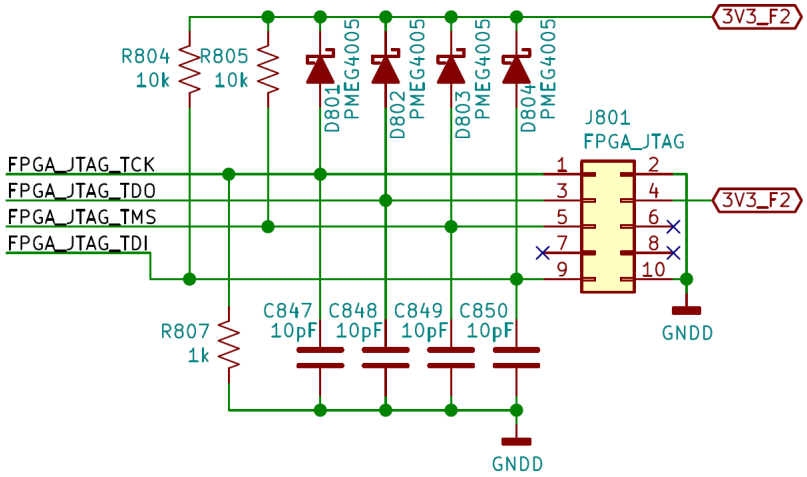



Figure 34: JTAG connection.

#### 3.2.1.4 Flash memory

Some external flash memory is needed in early development stages to store the waveforms until the microprocessor software has been developed, moment from which they will be stored inside the microprocessor's embedded memory because it is faster and easier to use.

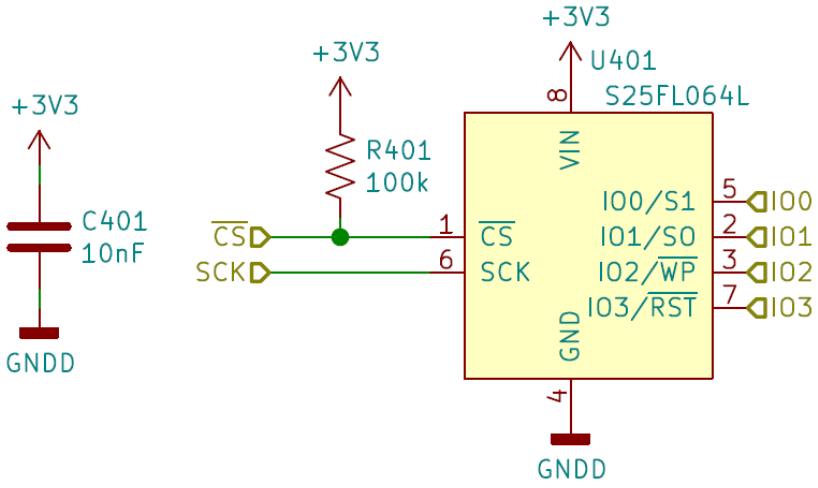



Figure 35: QSPI flash circuit.

To ease the use of the external memory, I decided to employ a quad SPI flash memory from Cypress, specifically a S25FL064L. The use of a quad SPI interface remove the needs of special protocols and interfaces, and can be easily programmed with inexpensive programmers from the exterior. Another key factor to bear in mind is its compatibility with 3.3 V CMOS signals.

#### 3.2.1.5 RAM memory

The samples of the waveforms have to be loaded into a very fast memory in order to be sent to the DAC at the required speeds. As of today, the only viable solution is to

use RAM memory. There are different types of memory but, in theory, SRAM should be the fastest one and, at the same time, the easiest to use. Despite that, I have not been able to find an of the shelf SRAM memory chip fast enough for our purposes (they all work up to 100 MHz). Although a DRAM memory would fulfil the speed requirements, it would increase drastically the complexity of the interface. Reason for which the selected RAM configuration is two 16-bit data lane SRAM chips sharing the address bus as seen in Figure 36. This will allow the FPGA to retrieve 2 14-bit samples per each read. These chips come in a 44 pint TSOP-II package.

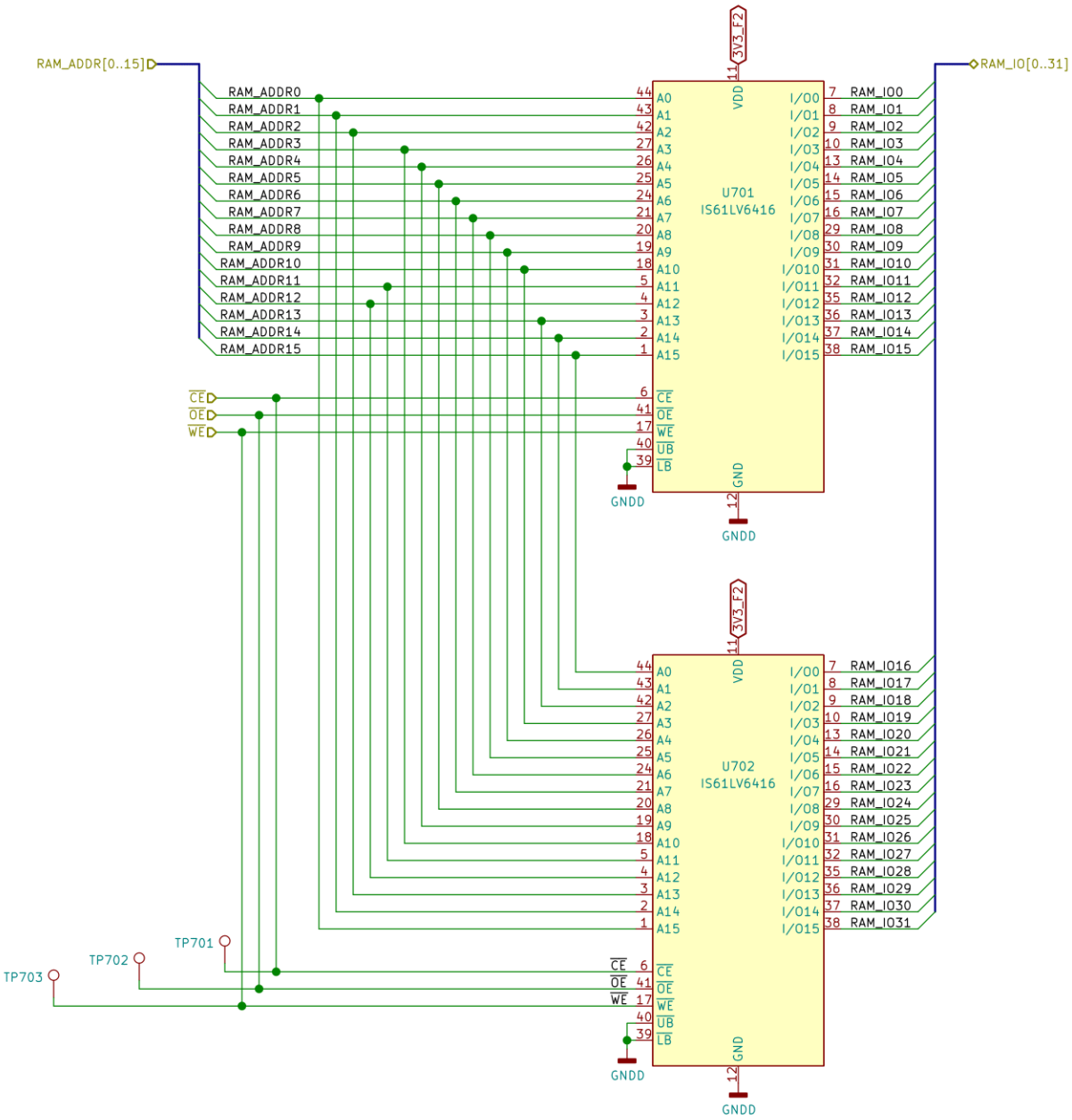



Figure 36: SRAM circuit.

#### 3.2.1.6 Microprocessor sheet

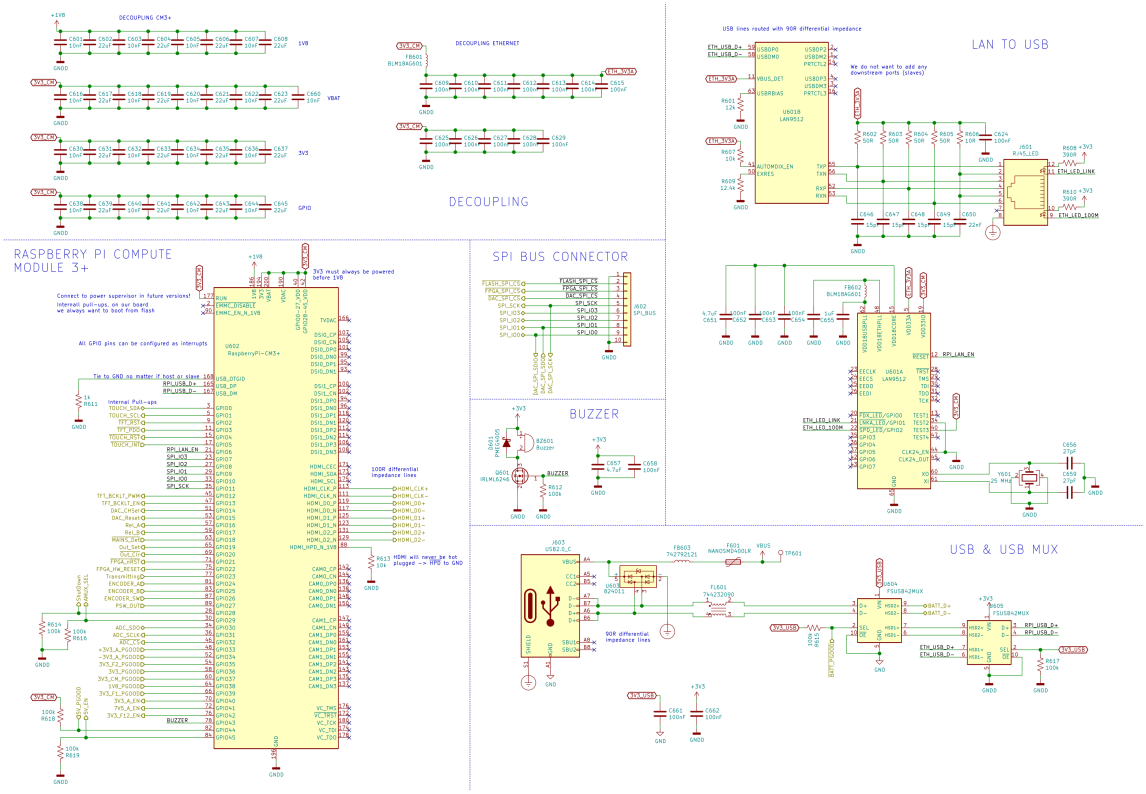



Figure 37: General view of the MPU schematic sheet

The microprocessor unit (MPU) will be in charge of the management of the whole device. As such, it has to comply with various requirements:

- It has to have a small form factor.
- It has to be able to develop some of the tasks of a microcontroller.
- It has to incorporate all the necessary elements for its operation.
- It has to be able to run a Linux operating system.
- It has to feature some sort of connection for a screen.
- It should be easy to develop software.

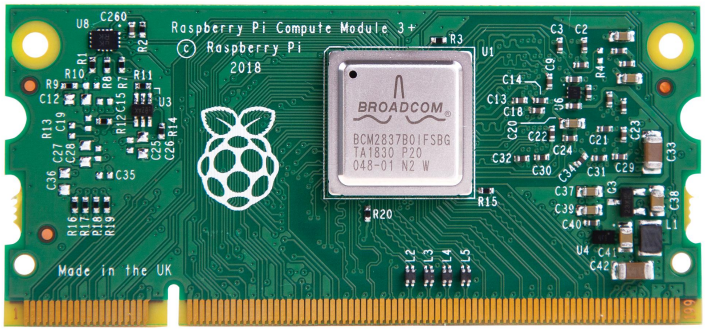
**Raspberry Pi compute module 3+**

As the microprocessor unit I have opted for a modular solution like the Raspberry Pi compute module 3+ [17].

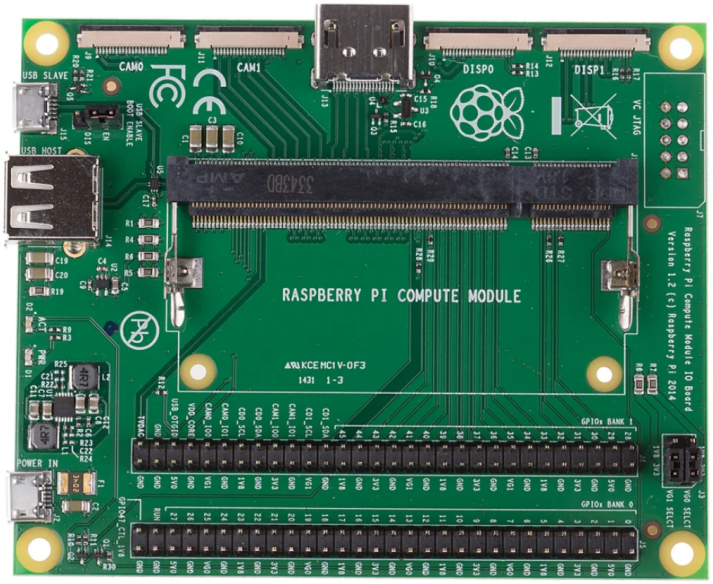
Specifically, the compute module 3+ comes in a DDR2 memory form factor (Figure 38a) that makes it perfect for embedded projects. This modular form factor leaves

the door open to developing a more customized microprocessor unit in the future to be able to improve some of the functions without the need of redesigning the whole device.

The Raspberry Pi foundation has also produced an external development board, on which the CM3+ connects (Figure 38b), specially designed to facilitate the development process.




(a) Raspberry Pi compute module 3+




(b) Raspberry Pi compute module development board

Figure 38: Raspberry Pi compute module.

### LAN to USB

A LAN connection is very useful to debug and communicate with the microcomputer but, unfortunately, the CM3+ does not have an Ethernet controller. The first Raspberry Pi models, in order to feature an Ethernet connection, used the LAN9512 from Microchip [18]. Following the part datasheet and the publicly available schematics from the old Raspberry Pis, I have designed the ethernet controller with the LAN9512. The chip also offers other features like GPIOs or downstream USB ports but, in this case, I am only interested in its USB to Ethernet conversion.

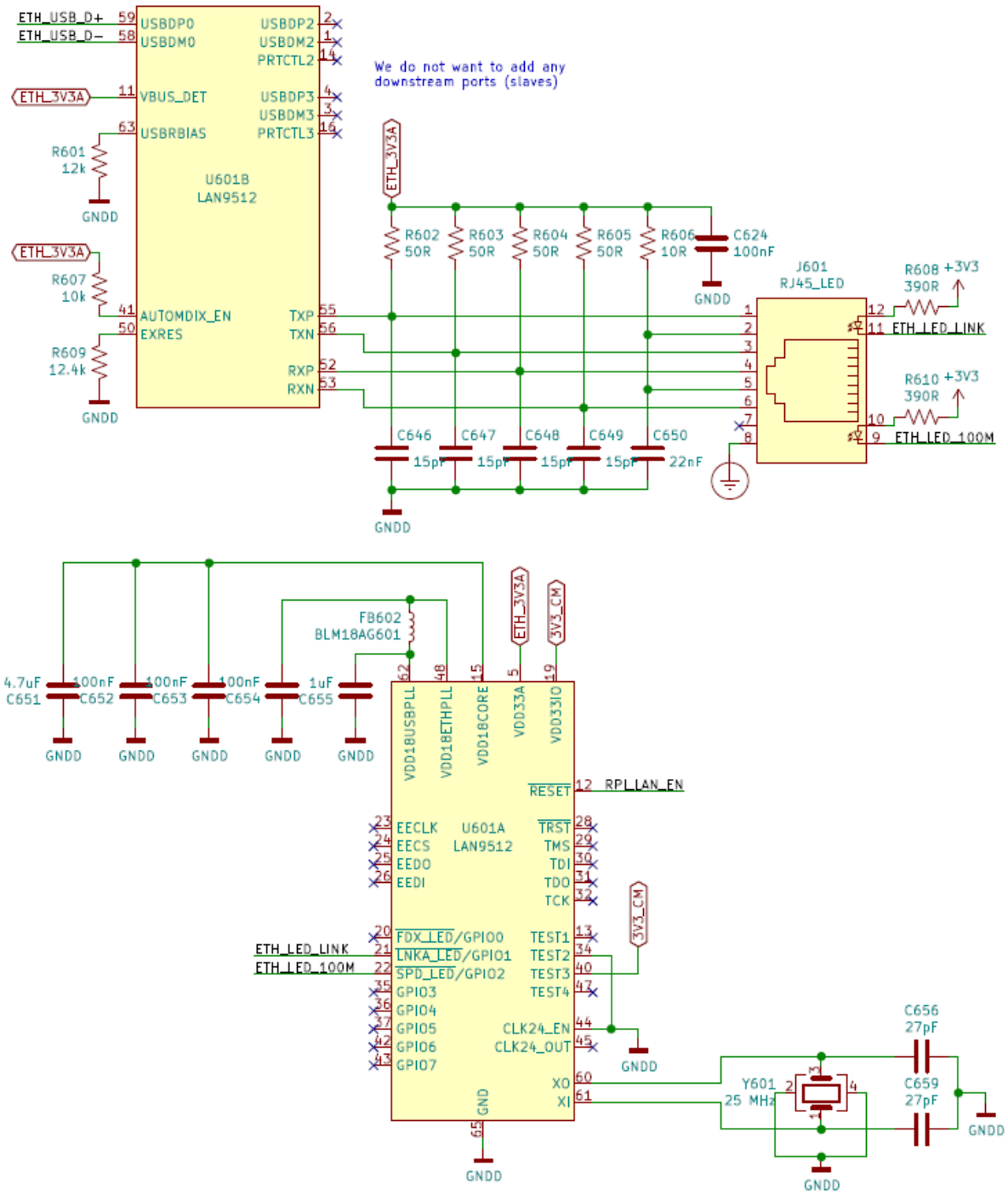



Figure 39: Picture of the LAN to USB converter

The device will have a protective earth connection, so it is a good idea to connect the RJ45 receptacle's shell to it. This will provide better EMI shielding in case shielded cables are used (the use of shielded cables only works well if both endings are earthed otherwise it could even be counterproductive). An example of the used RJ45 receptacle is seen in Figure 40.

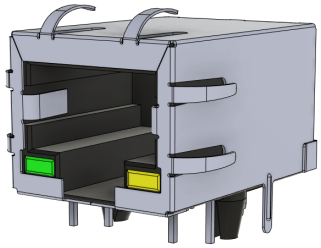


Figure 40: Picture of the RJ45 repectacle

### USB connector

The Ethernet connection is only intended for developing purposes, so in order to be able to update the device's software there should be some sort of connection with a PC. The most standard way of achieving it is using a USB connection.

Before, it has been seen that the Ethernet communication will be converted to USB and, as will be seen later on in the document, the battery management system also needs a USB connection. Despite what its name might suggest, the USB interface is not a multi point connection so, to be able to interconnect all these devices, some sort of multiplexer will have to be used. To perform such task, the chosen option is the FSUSB42 from On Semiconductor [19], a USB specific double-pole double-throw switch encapsulated in a very tiny UQFN10 1.8x1.4 mm package.

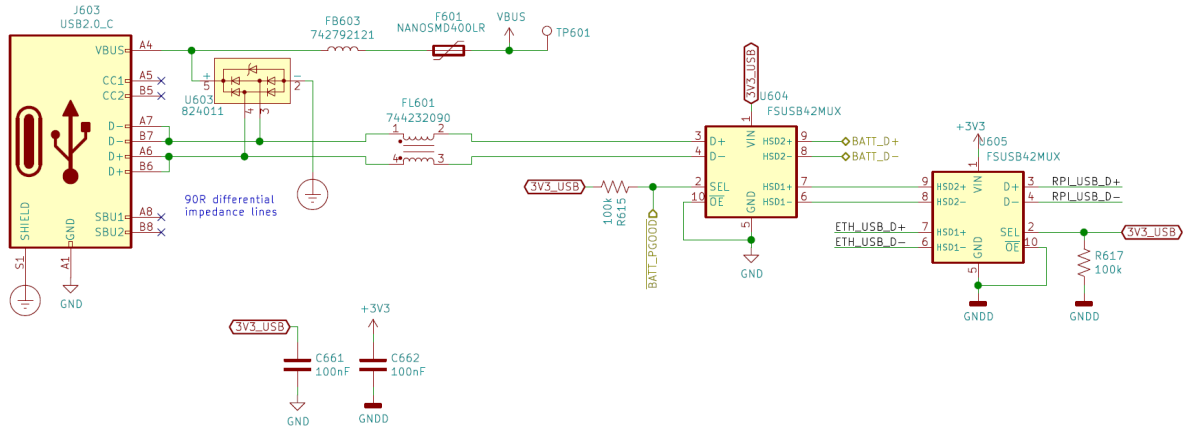



Figure 41: USB circuit.

Nowadays, the market seems to be leaning towards the USB type C connection due to the benefits it brings. For this reason, the device will feature a type C USB connector in a USB 2.0 configuration.

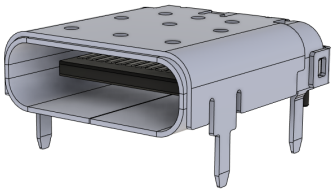


Figure 42: Picture of the USB C repectacle.

All connections that reach the exterior have to be carefully studied in order to mitigate foreseeable EMC problems. In this case, because USB connections are so common, the solutions are rather standard (all component values have to be correctly calculated for their application):

- ESD protection in the form of in chip integrated TVS diodes between all the input lines and protective earth (because the device shield will be connected to PE).
- A common mode choke in series with data lines.
- A low DC resistance ferrite in series with Vbus.
- An specifically rated self resettable fuse (although it is not an EMC protection it is always needed).

**Buzzer**

Audible feedback is a nice touch to have for the user when they are operating the device. This becomes even more important when having to notify problems like the presence of mains voltage on the output or the failure of some element.

The easiest implementation of audible feedback is by means of a buzzer. I will be using here a simple generic 2.73 kHz buzzer.


Figure 43: Picture of the buzzer.

### Analog to Digital Converter

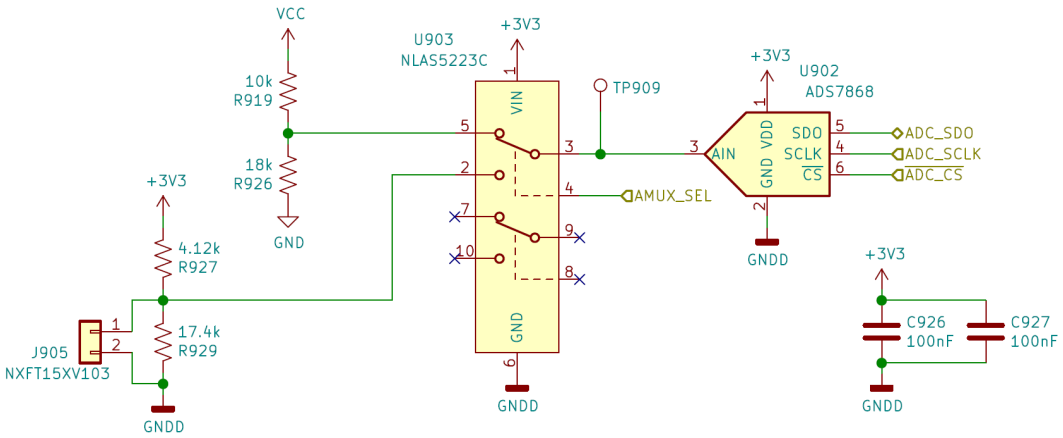



Figure 44: External ADC circuit.

In a complex system like this one, it is necessary to monitor multiple state indicator variables. Some of them are analog like the battery voltage or the voltage readings from thermistors. This signals need to be digitized utilizing an ADC so that the MPU is able to process them. The FPGA itself incorporates an ADC but, due the fact that I did not want to mix the digital and analog domains and there is a shortage of FPGA pins, the solution has been to use a generic external ADC.

#### 3.2.1.7 User interfaces

This device is intended to be used by itself, without the need of external equipment like a computer, which implies that some user interfaces have to be added. As standalone piece of equipment, a display becomes a crucial element and, although not strictly needed, a touchscreen would add a great value when it comes to usability. However, in some cases, a touchscreen is not the best solution. In this situations, as an addition to the touch interface, having a rotary encoder simplifies the usability of the device.

The output of the device is a critical part of the system that requires to be controlled independently. Moreover, the device also needs to be powered on. For this cases, push buttons with integrated LED indicators have been chosen.

### Display

The Raspberry Pi compute module 3+ presents 3 different interfaces for connecting screens: HDMI, 8-bit Digital Parallel Interface (DPI) and Digital Serial Interface (DSI). The documentation of the DSI interface has not been made publicly available, leaving HDMI and DPI as the 2 only possible solutions. The block diagram from Figure 45 represents the possible strategies to connect a screen to the CM3+.

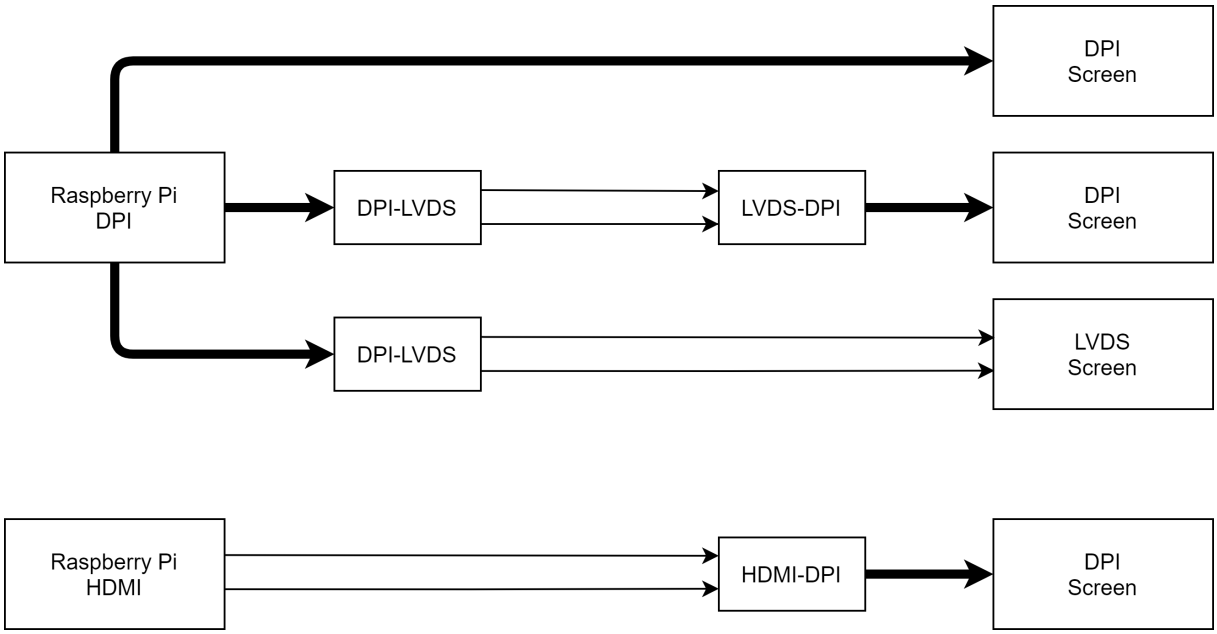



Figure 45: Block diagram of the feasible screen connections.

DPI displays are widely available for very cheap prices, but the option to directly connect the screen through DPI would be the easiest one to implement but it has been instantly discarded because long runs of parallel buses create lots of noise, which would become in an important EMI problem. On top of that, the DPI interface from the CM3+ takes the vast majority of the I/O pins. It instantly discards the possibility of using the native DPI interface, leaving HDMI as the only viable option.

In order to use an HDMI interface, the company wanting to make use of the interface has to be registered as an HDMI adopter. Otherwise you are not even allowed to buy any of the controllers widely available in the market. However, if only video signals are needed and as long as the device does not stream encrypted HD content, the protocol used to transmit video through HDMI is the same that uses DVI. Knowing this, I have been able to source a DVI to 8-bit DPI converter that some people have already used for the same purpose. The controller is the TFP401 from Texas Instruments and it comes in a 100-pin HTQFP package.

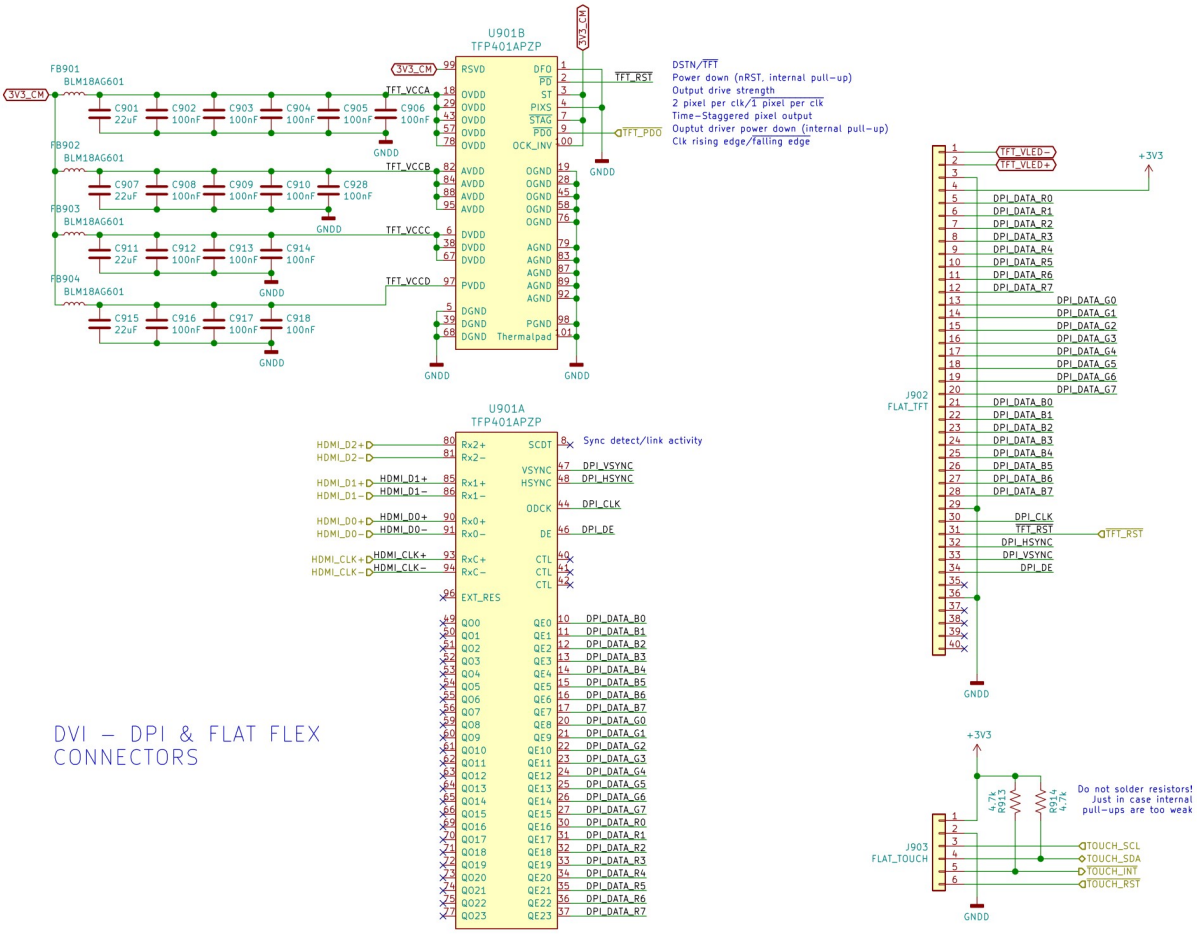



Figure 46: Circuit of the display driver.

The selected option is a 5", 800x480, 8-bit RGB DPI touchscreen from a company called Newhaven [20]. This display incorporates the Focaltech FT5426 I2C touchcreen controller that happens to be from the same family as the one used by the official Raspberry Pi screen, which in theory should be compatible out of the box without the need of creating custom drivers for it.


Figure 47: Picture of the Newhaven 5" capacitive touchscreen.

**Rotary enconder**

Figure 48: Picture of the rotary encoder.

In this device, the rotary encoder will be in charge of reading the direction of rotation of the knob and its speed, which is the exact function of an incremental encoder. Within the incremental encoders, there exist various methods of sensing this motion. They can be made using mechanical switches, hall effect sensors, optic transducers and capacitive sensors among others. Due to its simplicity, the mechanical types are the cheapest and most available ones. For this reason I have chosen a simple quadrature mechanical encoder that includes a push button.

Mechanical encoders use metal contacts to register the movement of the shaft. In the same way as mechanical switches, they do suffer severely from contact bounce. This phenomenon occurs when, after an actuation of the shaft, the metal plates of the contacts bounce quickly before settling to their final position due to their mass and elasticity. This bounce causes hundreds of false activations that need to be carefully treated. This problem can be solved either by software or by hardware. Since software debouncing would require to spend processor time just monitoring the encoder, I have opted for the hardware approach.

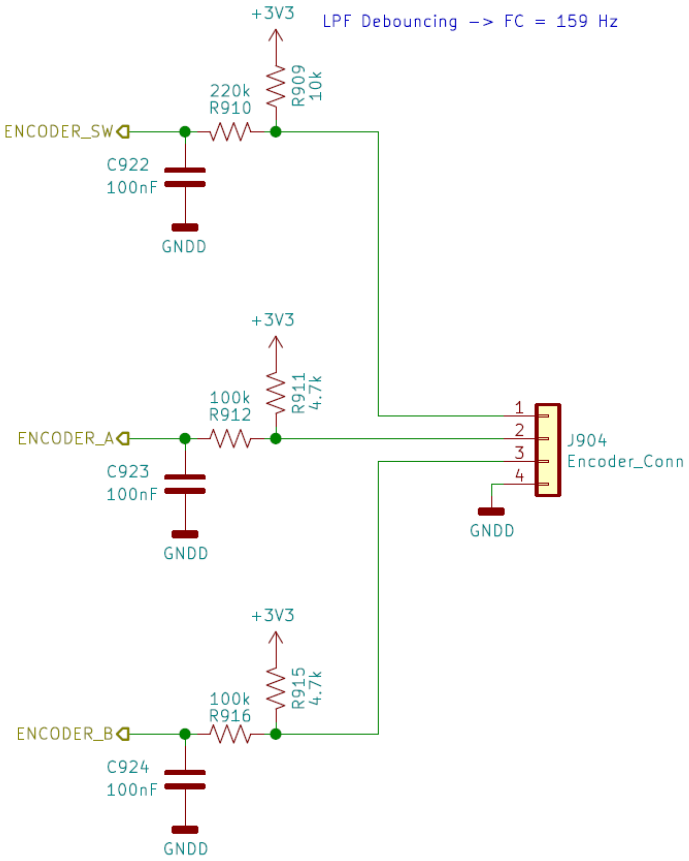



Figure 49: Rotary encoder debouncing circuit.

An easy to implement debouncing solution is to implement a low pass filter at the sensing output of the encoder as seen in Figure 49. In this case the chosen encoder does have 20 dents. Taking conservative maximum rotation speed of the knob of 2 revolutions per second, this gives a maximum of 40 pulses per second. The manufacturer's datasheet states that the maximum bouncing time of these encoders is around 5 ms, which means that the time constant has to be greater than 5 ms but less than 25 ms. With the component values of Figure 49 the encoders' charging and discharging time constants are close to 10 ms.

Regarding the push button included in the encoder, the actuation frequency will be much lower, making possible to increase the time constant of the circuit beyond 22 ms.

### Power switch

The user of the device has to be able to turn it on and off. This can be easily accomplished using a standard latching switch. The problem comes when the MPU detects an error or the battery is reaching dangerously low levels. With this method it is not able to self shut down. A very clever solution to this problem is a soft-latching power circuit that allows the user to turn on and off the system using a push button but also allows the MPU to shut it down.

Figure 50: Picture of the power button.

Among all the different reviewed options, I have not been able to find any that offer standalone operation. This is specially useful in the event that the system stops responding. If the MPU is in charge of reading the switch in order to actuate in accordance and it is not responding, the user is not able to manually reset the device, having to rely on the MPU's watchdog. To solve this problem, I have ended up designing a soft-latching circuit that should be able to power up and turn off the system with the press of a push button apart from allowing the MPU to also shut down the device.

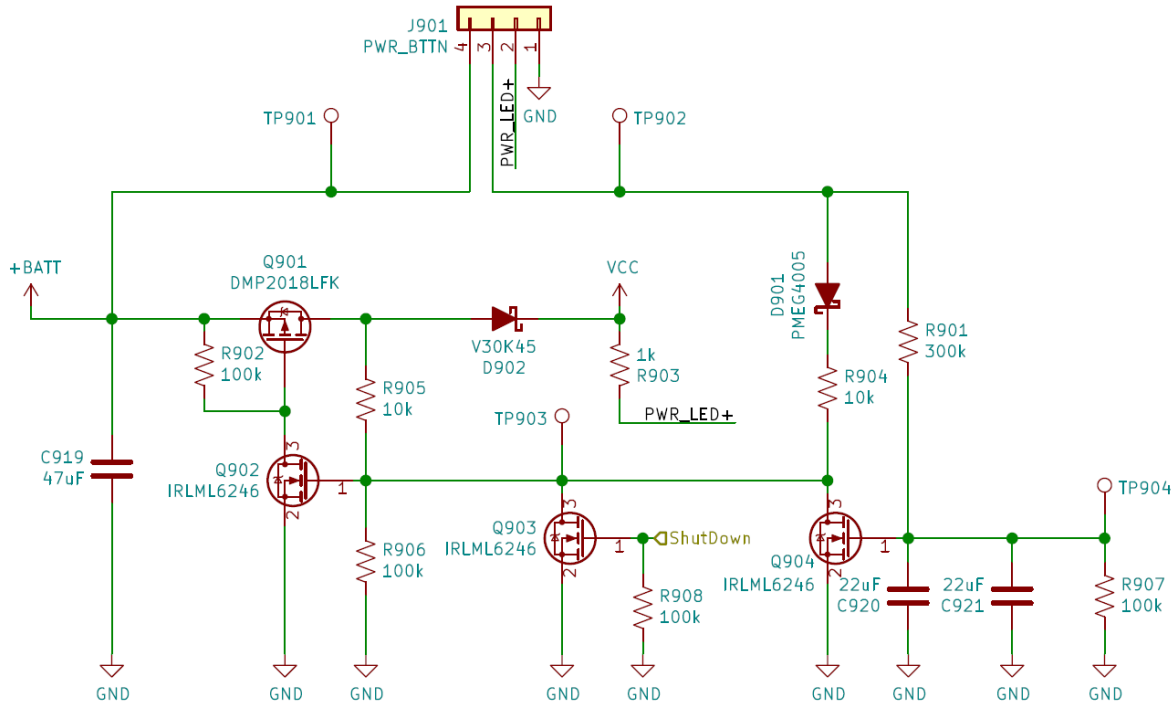


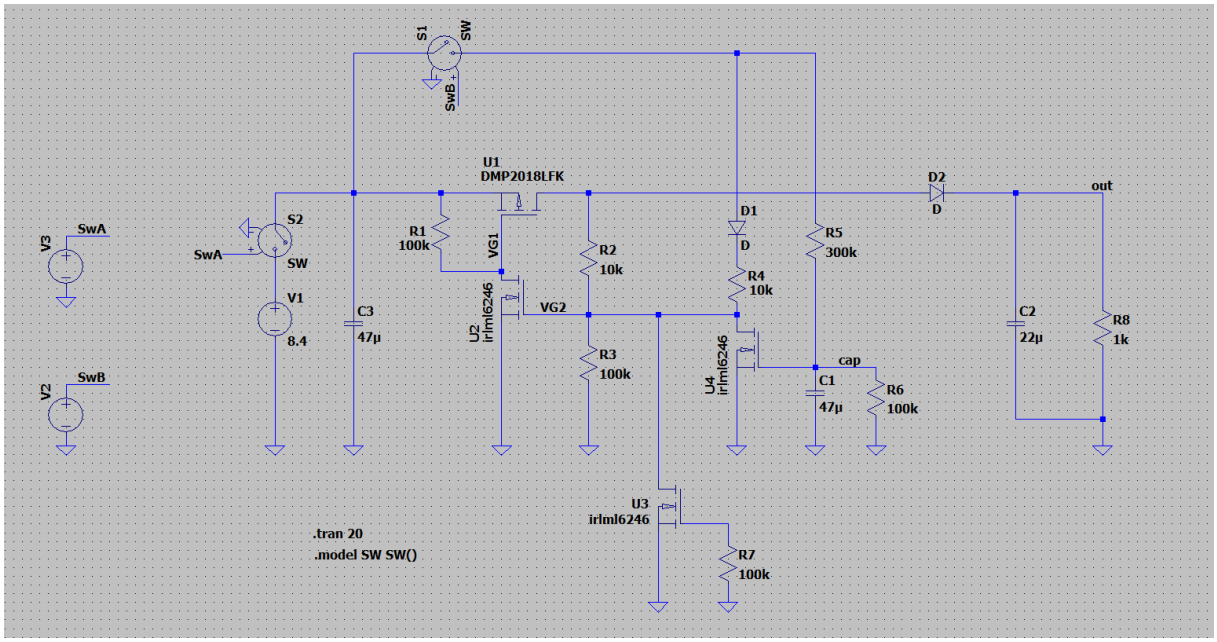

Figure 51: Soft latch power circuit.

The mentioned circuit is shown in Figure 51. When the batteries are connected R902 keeps Q901 in cutoff, not allowing to flow any current to the system. When the user presses the button (connected between pins 3 and 4 of the connector) the gate of Q902 is pulled high which, at the same time, pulls low the gate of Q901. From that moment on the circuit is activated and R905 keeps high the gate of Q902. When the button is pressed, some current starts to flow into C920 and C921, charging them slowly. If the button is pushed long enough, the voltage of the capacitors reaches the threshold voltage of Q904, moment when it activates and pulls the gate of Q902 low and, thus, cutting off

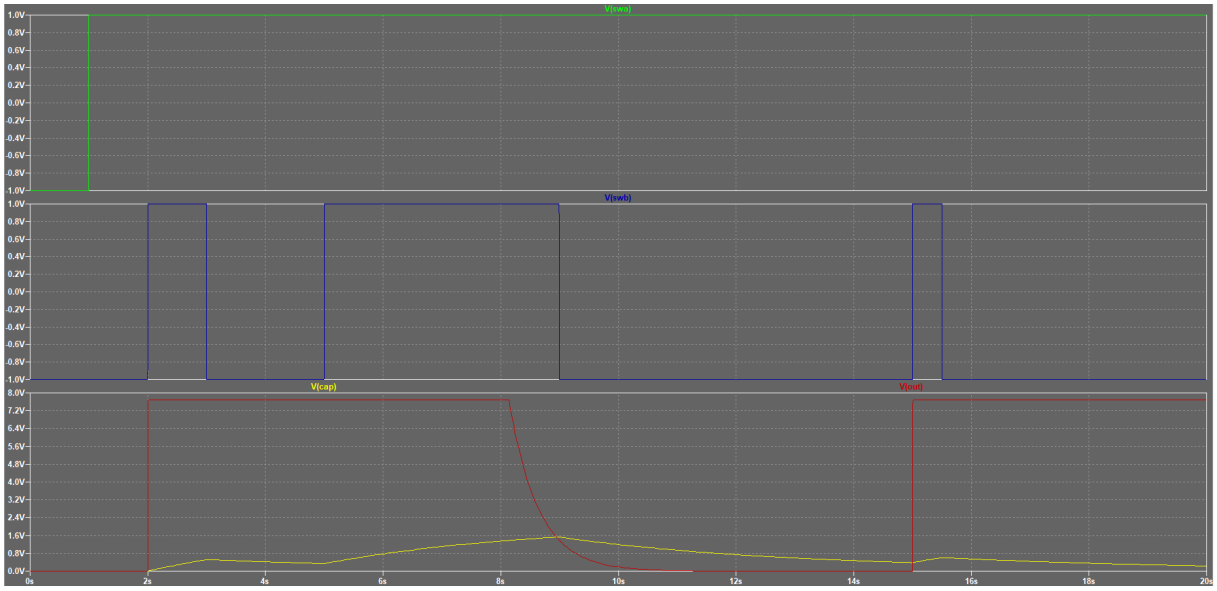
the current through Q901. If the MPU needs to shut down the device, it only has to activate Q903, which pulls down the gate of Q902, immediately turning off the device.

In this case, the bouncing of the switch is not concerning because, once the circuit is turned on, opening and closing the contacts of the switch does not have any effect. On the other hand, when the circuit shuts down, the capacitors act as a debouncing circuit keeping it in off state.

To fine tune the values of the components and to check that the circuit behaves as expected, the circuit has been simulated using the SPICE models of what will be its final components.




(a) LTSpice schematic.




(b) Transient response simulation.

Figure 52: Simulation of the soft-latching circuit.

In the transient response analysis from Figure 52b the green trace represents the moment when the batteries are connected. The blue trace represents the position of the switch, high - closed, low - open. The red trace shows the output voltage and the yellow represents the capacitor's voltage. When the batteries are connected to the circuit, because the input capacitors are still not charged, the voltage on the gate of Q901 is low, making it conduct for a small amount of time until the voltage on the capacitor rises enough. This event should only happen once because the batteries will not be meant to be taken out. Then, when the button is pressed, the output voltage rises instantly to its intended value. If the button is pressed for long enough, around 3 s, the yellow trace rises above the threshold voltage and shuts down the circuit. If the button is pressed for an even longer period of time, it only makes the capacitor's voltage increase more, creating an even more consistent 'low' on the gate of Q902. Once the capacitor has been discharged enough (about 3 s after releasing the button) the circuit can be reactivated.

#### 3.2.1.8 Power supplies

After all the elements conforming the device have been selected, it is time to design the power supplies that will power them.

There exist 2 differentiated power domains within the circuit: the analog part formed mainly by the DAC and the output stages, and the digital part which comprises the rest of the circuitry. The digital portion tends to create a lot of noise and does not require extremely precise power supplies, whereas the analog part does require very stable and low-noise bipolar power rails.

To dimension correctly the power supplies, a rough power budget has to be created taking into account all the possible power consumptions.

Table 4: Inflated rough power budget

| **Element** | **Voltage (V)** | **Current (mA)** |
|---|---|---|
| Screen + touch | 3.3 | 150 |
| TFT backlight | Constant current | 60 |
| TFP401A | 3.3 | 370 |
| FPGA_A | 3.3 | 2000 |
| FPGA_B | 3.3 | 2000 |
| CM3+_A | 3.3 | 1500 |
| CM3+_B | 1.8 | 300 |
| LAN9512 | 3.3 | 250 |
| DAC_A | +3.3 (analog) | 70 |
| DAC_B | 3.3 | 15 |
| DAC_C | 1.8 | 60 |
| Buzzer | 3.3 | 80 |
| Output_A | ± 3.3 (analog) | 40 |
| Output_B | ± 7.5 (analog) | 80 |
| Relays | 3.3 | 120 |
| SRAM | 3.3 | 50 |
| Flash | 3.3 | 20 |
| Output protection | 3.3 | 2 |
| Fan | 5 | 200 |
| ADC | 3.3 | 10 |
| TCXO | 3.3 | 6 |

The rough power budget from Table 4 indicates that the maximum power the circuit would draw if all the components were working at the same time is 25 W, which at the lowest working battery voltage (6.2 V) translates to approximately 4 A. Since these circuits will be drawing so much current, all the power supplies need to be very efficient. For this reason, switching converters will be used whenever possible.

The various elements have been arranged depending on their proximity and their requirements into different power blocks. Figure 53 shows the arrangement with each topology and voltage.

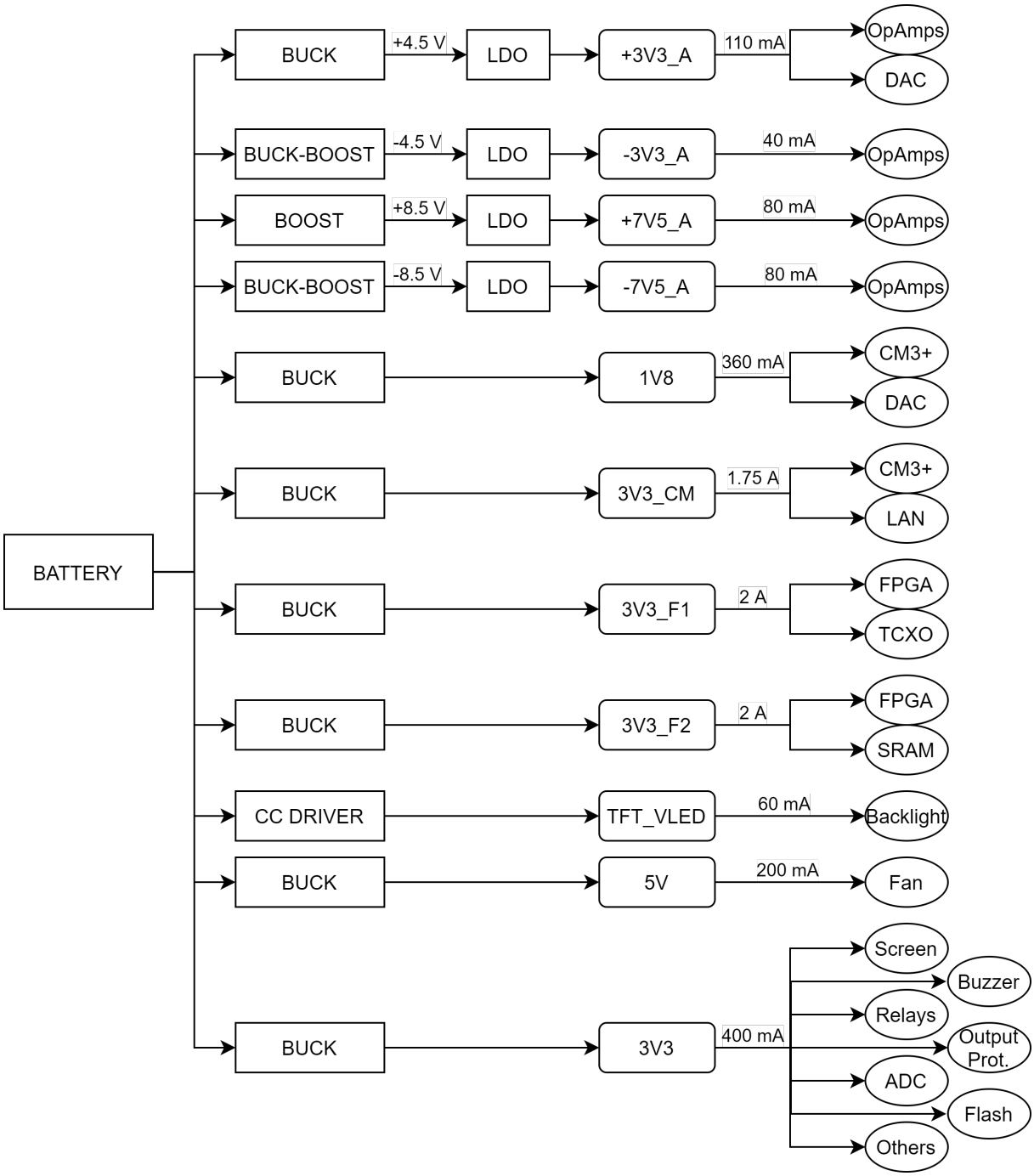



Figure 53: Block diagram of the power supply arrangement with their topology and current consumption.

### Buck converters

As seen in the block diagram, all the digital power supplies and the 3.3 V analog rail are always going to be below the battery voltage, making it possible to use buck converter topologies for them.

The TLV62130 from Texas Instruments [21] is a buck converter that offers efficiencies over 80 % at any load and comes in a 3x3 mm VQFN-16 package. Figure 54 shows the efficiency in function of the load at different output voltage levels.

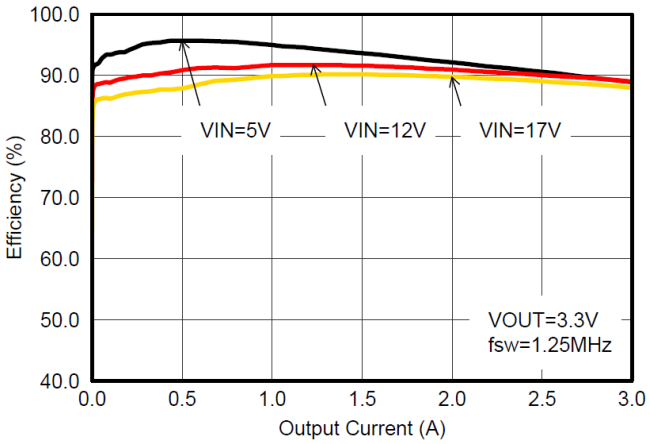



Figure 54: Efficiency vs. load at different output voltages of the TLV62130 [21].

TLV62130 offers internal over current and over temperature protection, continuous output current of up to 3 A and programmable soft start along with a very extensive and comprehensive datasheet. It also features an enable input and a power good output to indicate the state of the converter. Its switching frequency can be chosen between 2.5 MHz for an increased efficiency or 1.25 MHz for increased EMI performance. Since the design will feature so many power supplies, the efficiency is the most concerning aspect. However, as EMI can become a huge problem, every power supply will be provided with a solder jumper so that the switching frequency can be changed afterwards.

The output of the buck converters is given by the resistor values of a simple voltage divider. The output voltage is given by (6) where:

- $R_{TOP}$ is the resistor on the top of the voltage divider.
- $R_{BOT}$ is the resistor on the bottom of the voltage divider.
- $V_{FB}$ is the voltage at which the converter tries to regulate the FB pin. In this case $V_{FB} = 0.8\,\mathrm{V}$

$$V_{out} = (1 + \frac{R_{TOP}}{R_{BOT}}) \cdot V_{FB} \tag{6}$$

The feedback network has to be designed to ensure a minimum of 2 µA of current for its correct operation. Taking into account that lower resistor values yield higher accuracy and more robust designs, it is decided to use a combined value of around 100 kΩ.

The next step is to define the inductor values. (7) gives L in function of:

- $V_{in_{MIN}}$, the minimum input voltage.
- $V_{out}$, the output voltage.
- $t_{on_{MAX}}$, the maximum ON time.
- $\Delta_I$, the ripple current.

Setting the ripple current between 20 % to 50 % of the maximum load current provides an optimal operating point because this converter features a power save mode that increases efficiency with light loads by decreasing the switching frequency and thus decreasing switching losses.

$$L = (V_{in_{MIN}} - V_{out}) \cdot \frac{t_{on_{MAX}}}{\Delta_I} \tag{7}$$

On buck topologies the ON time is given by (8) where $f_{SW}$ is the switching frequency.

$$t_{on_{MAX}} = \frac{V_{out}}{V_{in_{MIN}}} \cdot \frac{1}{f_{SW}} \tag{8}$$

Once the inductor is chosen, its minimum value (given by the tolerance specified by the manufacturer) is inputted to (7) but this time to isolate the maximum current ripple $\Delta_{i_{MAX}}$.

There are some equations that can be used to calculate the needed output capacitance but this buck converter is internally compensated, what means that the output capacitance has to be chosen in accordance with the datasheet because otherwise it could become unstable. In this case the chosen capacitance will be around 47 µF for all of the converters.

This buck converter also features a configurable soft-start ramp time that is controlled by the value of a capacitor. The needed capacitor can be found using (9) where $t_{SS}$ is the ramp up time and $C_{SS}$ the capacitance.

$$C_{SS} = t_{SS} \cdot \frac{2.5\,\mu A}{1.25\,V} \tag{9}$$

The only rise time restrictions are given by the FPGA, which needs its power supplies to rise in less than 2.5 ms, and the CM3+ needs the 3.3 V rail to ramp up faster than the 1.8 V rail does.

All the buck converters will be configured as in Figure 55. The enable and power good signals will be controlled and read by the MPU except for the enable signal of its own converters that will be always powered on.

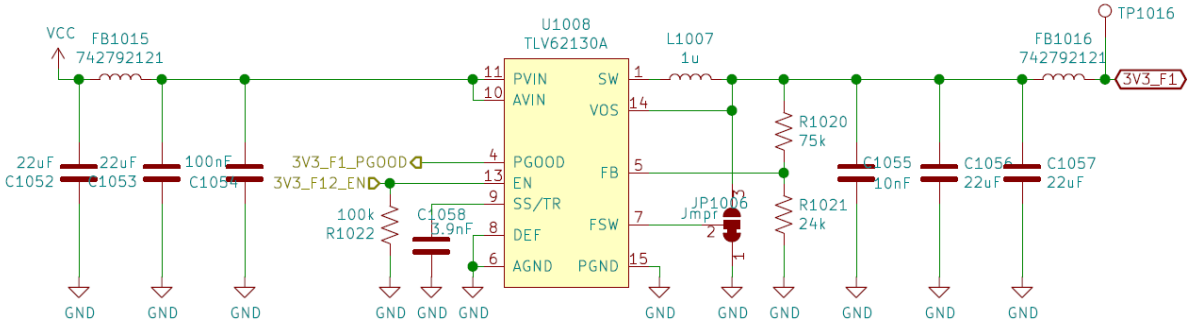



Figure 55: Example of a digital power supply circuit.

To try to isolate the noise within the power supply a high-frequency ferrite bead is placed at the input and the ouptut of each converter.

### Analog power supplies

As seen before, the analog part of the circuit needs 4 different power rails: ±3.3 V and ±7.5 V. These rails have to be very stable and need to be ripple and noise free. To achieve that, the idea is to create a higher voltage than the needed (approximately 1 V above) using switching converters and then regulate it down to the needed value using low dropout linear regulators since the analog circuitry will not draw a lot of current (less than 100 mA for each rail) and thus not much power will be wasted.

An LDO is a type of DC linear voltage regulator that can regulate the output even when the input voltage is very close to the output voltage but with the disadvantage that they must dissipate power in order to perform the regulation and thus have low efficiencies. A simplified internal structure of an LDO can be seen in Figure 56.

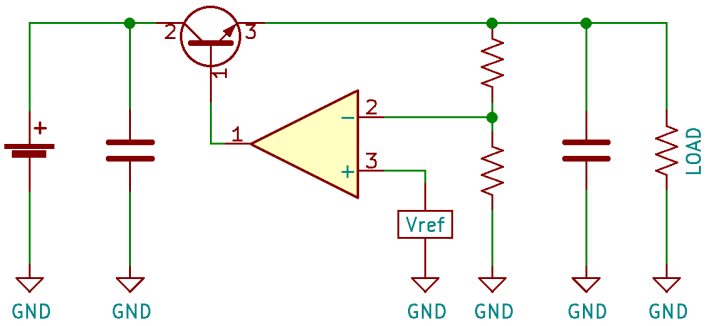



Figure 56: Simplified internal structure of an LDO.

The LDOs will ensure that the rails are free of low-frequency ripple but the analog circuitry will have to work at frequencies of up to tens of MHz and the PSRR from operational amplifiers and LDOs decrease drastically as the frequency increases. To try to solve this problem and prevent the noise from spreading towards the output, a pi-filter formed by a ferrite bead and 2 capacitors is placed on each rail before the LDOs and even in the GND line, isolating it from the noisy digital ground.

### ±3 V analog power supply

As stated before, the positive output is always below the battery voltage, making it possible to use the same buck converter as for the digital power supplies, the TLV62130A. On the other hand, for the negative rail, although in absolute value is also below the battery voltage, a buck-boost topology offers negative output without the need of special configurations. In this case, the ADP5074 [22] from Analog Devices has been the chosen option. It is an inverting DC-DC regulator capable of providing currents of up to 2.4 A that offers overcurrent protection , overvoltage protection and thermal shutdown in a 3x3 mm LFCSP-16 package. They also feature a selectable switching frequency of 2.4 MHz or 1.2 MHz.

For the LDOs, I decided to use the dual output TPS7A39 from Texas Instruments [23] which are dual, monolithic, high-PSRR, positive and negative low-dropout voltage regulators capable of sourcing and sinking up to 150 mA of current in a 3x3 mm VSON-10 package.

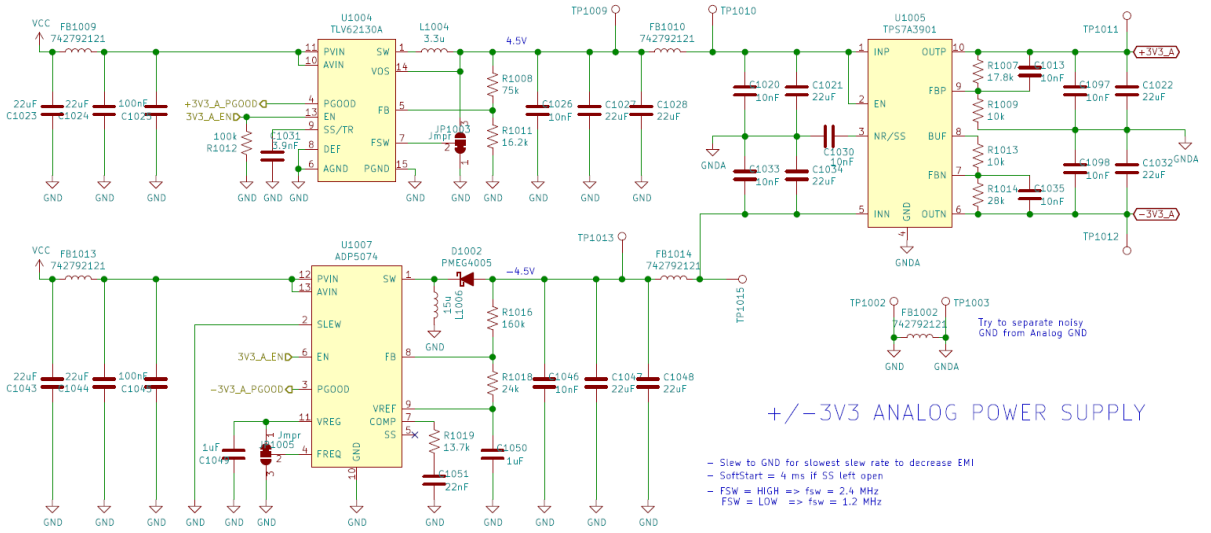



Figure 57: ±3 V analog power supply schematic.

The output of the ADP5074 is given by (10). Where $V_{Ref} = 1.6\,\text{V}$ and $V_{FB} = 0.8\,\text{V}$.

$$V_{OUT_N} = V_{FB} - \frac{R_{TOP}}{R_{BOT}}(V_{Ref} - V_{FB}) \tag{10}$$

This buck-boost converter also features a soft start that can be controlled with the value of a resistor $R_{SS}$. The relationship between the soft start time ($t_{SS}$) and $R_{SS}$ is given by (11). $R_{SS}$ has to comply with $50\,\text{k}\Omega \leq R_{SS} \leq 268\,\text{k}\Omega$ for maximum performance and stability.

$$t_{SS} = 38.4 \cdot 10^{-3} - 1.28 \cdot 10^{-7} \cdot R_{SS} \tag{11}$$

This converter needs to incorporate an external diode. This diode has chosen to be a schottky diode for its reduced voltage drop compared with a standard silicon diode, in this case is around 400 mV. The voltage drop across the diode is needed in order to calculate the duty cycle of the converter.

Using (12), the needed inductance value can be calculated. Being the maximum ON time given by (13) and the duty cycle by (14). $\Delta I_L$ is the maximum current ripple allowed through the inductor which, again, for best performance, is chosen around 30 % of the nominal current.

$$L = \frac{V_{IN} \cdot t_{ON}}{\Delta I_L} = \frac{V_{IN} \cdot t_{ON} \cdot (1 - D_{MAX})}{0.3 \cdot I_{OUT}} \tag{12}$$

$$t_{ON_{MAX}} = \frac{D_{MAX}}{f_{SW}} \tag{13}$$

$$D = \frac{|V_{OUT}| + V_D}{V_{IN} + |V_{OUT}| + V_D} \tag{14}$$

ADP5074, unlike the buck converter, is not internally compensated. It produces a right half plane zero in the regulation feedback loop that requires to be compensated so

that the crossover frequency occurs well below the frequency of the right half plane zero. The right half plane zero frequency is determined by (15).

$$f_Z = \frac{R_L \cdot (1-D)^2}{2\pi \cdot L \cdot D} \tag{15}$$

To stabilize the regulator it has to be ensured that the regulator crossover frequency is less than or equal to one-tenth of the right half plane zero frequency ($f_Z$). To achieve this, the compensation resistor $R_C$ has to comply with (16). Where $C_{OUT}$ is the output capacitance, $V_{OUT}$ the output voltage and $V_{IN}$ the input voltage of the converter.

$$R_C < \frac{2094 \cdot f_Z \cdot C_{OUT} \cdot |V_{OUT}| \cdot (V_{IN} + 2 \cdot |V_{OUT}|)}{10 \cdot V_{IN}} \tag{16}$$

After the compensation resistor is selected, the zero formed by $C_C$ and $R_C$ has to be set to one-tenth of the crossover frequency using (17).

$$C_C = \frac{10 \cdot 2}{\pi \cdot f_Z \cdot R_C} \tag{17}$$

The positive rail needs to be powered up first. With the selected regulator configuration it is easy to achieve just by selecting a slower ramp up time for the negative rail. Leaving the SS pin of ADP5074 open configures the converter with its fastest ramp up time, which is 4 ms, twice the time of the buck converter.

The positive output of the LDO is configured as a non-inverting Op-Amp, whereas the negative output is configured as an inverting amplifier. Their outputs are given by (18) and (19), being the typical value for $V_{NR/SS}$ 1.19 V. Feedback resistors are recommended to be between 10 kΩ and 200 kΩ.

$$V_{OUT_P} = V_{NR/SS} \cdot (1 + \frac{R_{P_{TOP}}}{R_{P_{BOT}}}) \tag{18}$$

$$V_{OUT_N} = V_{NR/SS} \cdot \frac{-R_{N_{BOT}}}{R_{N_{TOP}}} \tag{19}$$

Linear regulators dissipate power in order to regulate the output. This power increases linearly with the current supplied to the load, so it is very important to ensure that the package can withstand it.

Equation (20) gives the power dissipated by the regulator in function of the input voltage ($V_{IN}$), the output voltage $V_{OUT}$, the output current ($I_{OUT}$) and the regulator's current consumption ($I_{OUT}$).

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_{Reg} \approx (V_{IN} - V_{OUT}) \cdot I_{OUT} \tag{20}$$

Equation (21) calculates the maximum ambient temperature the regulator is able to withstand without exceeding its maximum junction temperature ($T_{J_{MAX}}$) given its junction to air thermal resistance ($\theta_{JA}$) and the maximum power dissipated by the regulator ($P_{D_{MAX}}$).

$$T_{A_{MAX}} = T_{J_{MAX}} - P_{D_{MAX}} \cdot \theta_{JA} \tag{21}$$

### ±7.5 V analog power supplies

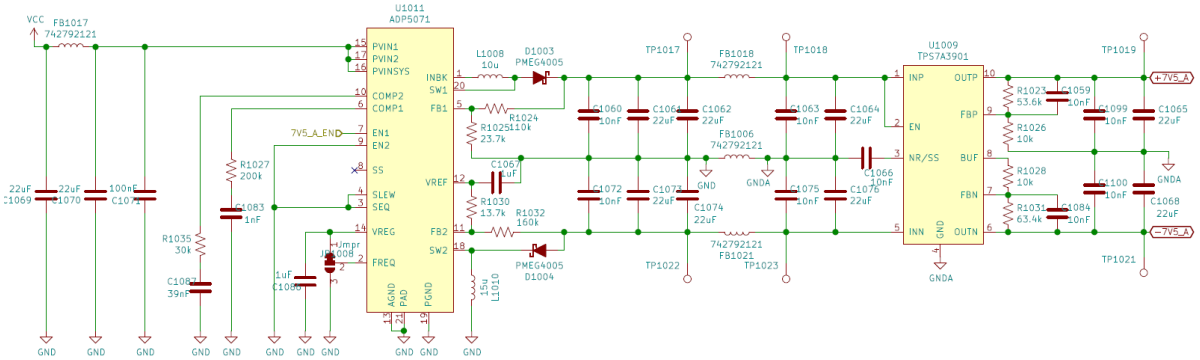



Figure 58: ±7.5 V analog power supply schematic.

The high voltage rails are based on the Analog Devices' ADP5071 [24] dual DC-DC converter. It offers two independent outputs, one positive (boost topology) and the other negative (buck-boost topology) in a 4x4 mm 20-pin LFCSP package. The idea is to boost the battery voltage up to ±8.5 V and then regulate it down to ±7.5 V with the same low drop out linear regulators as in section "±3 V analog power supply".

The ADP5071 switching converter is from the same family as ADP5074, what makes that equations (10), (11), (12), (13), (14), (15), (16) and (17) from ADP5074 also apply to the negative output of ADP5071.

As for the positive output, due to the fact that it uses a boost topology, not all the equations from ADP5074 can be used. The duty cycle of this output is defined by (22) and to calculate the loop compensation components, equations (23) and (24) have to be used.

$$D = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D} \tag{22}$$

$$f_{Z_{POS}} = \frac{R_L \cdot (1 - D)^2}{2\pi \cdot L} \tag{23}$$

$$R_{C_{POS}} < \frac{2094 \cdot f_{Z_{POS}} \cdot C_{OUT} \cdot V_{OUT}^2}{10 \cdot V_{IN}} \tag{24}$$

### Power rail status LEDs

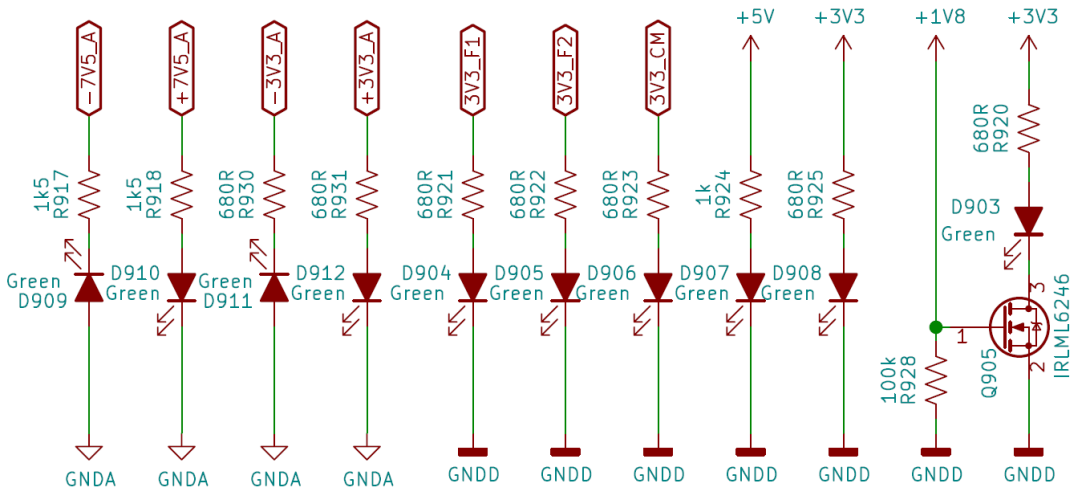



Figure 59: LEDs showing the status of each power rail.

For the purpose of making the troubleshooting progress easier, one LED with its proper current limiting resistor has been connected to each power rail. This makes possible to identify visually which power supplies are not working.

The +1V8 power rail, as its name indicates, has a working voltage of 1.8 V, which is less than the forward voltage drop of the used green LED. For this reason, its LED is connected to the +3V3 line and the +1V8 power rail is tied to the gate of a NMOS transistor that controls it.

### Standalone linear regulator

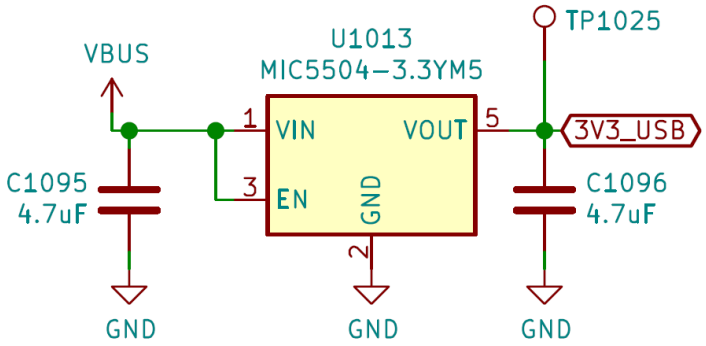



Figure 60: 3.3 V linear regulator from Vbus.

One of the USB mux from section "USB connector" needs to be powered up whenever the USB cable is connected in order to multiplex the signal coming from the USB connector although the device is turned off. To supply the needed power to this mux, a simple Microchip MIC5504-3.3YM5 [25] 3.3 V linear regulator will be used.

### Backlight LED driver

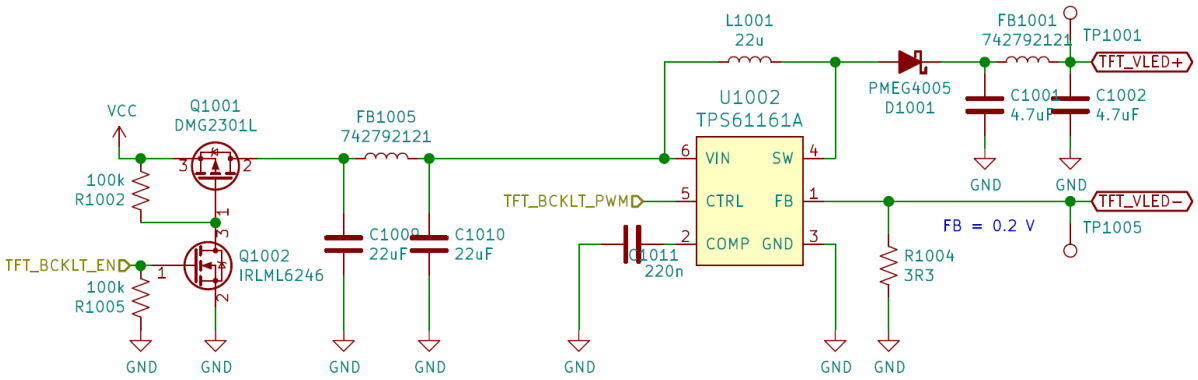



Figure 61: LCD backlight constant current driver.

To drive the LED backlight from the TFT LCD, a Texas Instruments' TPS61161A, PWM dimmable constant current LED driver will be used. The manufacturer recommends to use inductances from 10 µH to 22 µH, being 22 the best option to reduce ripple and improve efficiency at low currents.

This driver does not feature an enable pin because there is an inductor in parallel between its input and output. In order to add this feature, a simple PMOS is added in series with the input.

#### 3.2.1.9 Battery charging and management system

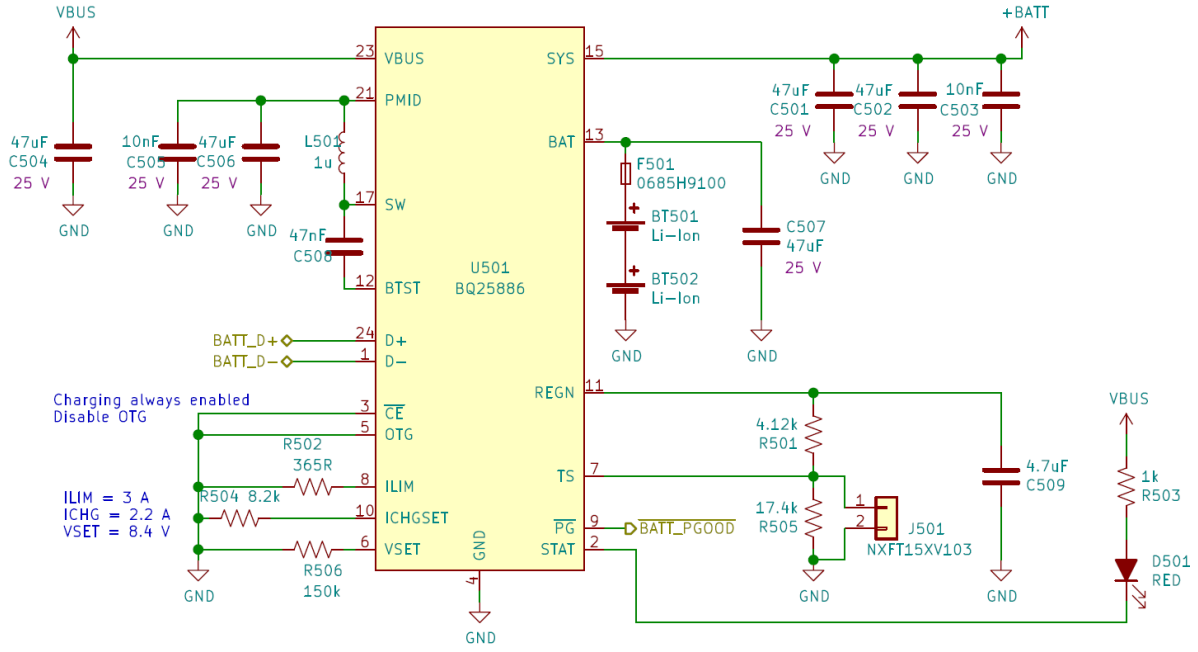



Figure 62: Battery charging and management circuit.

Of all types of batteries, lithium ion type batteries offer remarkable performance at an affordable price. They feature a very high power density with a relatively large discharge rate, more than enough for the hypothetical absolute maximum current consumption of

4 A. A common type of Li-Ion battery cell is the 18650 (shown in Figure 63 compared to an AA battery) which usually offer capacities around 9 Wh per cell.


Figure 63: Comparison between a 18650 cell and an AA battery.

Li-Ion batteries are not recommended to be connected to the load while charging. The main reasons, as [26] carefully explains, are:

- The charge might never end. Lithium ion battery chargers are based on Constant Current Constant Voltage modes and the termination is based on the ratio of charge current. If the system draws current from the battery while it is charging, the charge current will never meet the termination value and, thus, it will never terminate.
- The total system current is limited by the charge current because the charger is not able to determine how much current the system is drawing.
- Normally, a switch is introduced between the battery and the system in order to turn it off which, then, makes the batteries to stop charging.

Instead, some sort of load sharing circuitry is needed. In normal use, the batteries will power the loads, but when the system is connected to a power supply the external power source will charge the batteries at the same time that provides power to the loads.

When dealing with lithium ion batteries, extra precautions have to be taken in order to ensure that they do not represent a risk for the user. This is extremely important at the moment of charging them, when they tend to become dangerous if overcharged or exposed to high temperatures. For this reason, JEITA (Japan Electronics and Information Technology Industries Association) released back in 2007 a set of guidelines to improve battery charging safety. The solution then has to be fully JEITA compliant.

For this reason, it is decided to use the Texas Instruments' BQ25886 [27], fully JEITA compliant, 2-cell lithium ion battery charging/management in a 24-pin VQFN package monolithic solution. This chip offers various features:

- Standalone functionality.
- USB current negotiation (USB BC1.2 standard).

- Voltage boosting.
- Charging currents up to 2.2 A (if the USB host is capable).
- The ability of delivering up to 5 A of current to the system.
- Battery over-voltage, under-voltage and over-current protection.
- Constant current - constant voltage algorithm.
- Dynamical system voltage regulation, keeping it always above the set minimum.
- It automatically terminates the charging and keeps to provide power to the system.
- In order to be JEITA compliant, it continuously monitors the battery temperature with an NTC thermistor.
- It automatically stops the charging if a fault is encountered and it automatically resumes once the fault goes away.

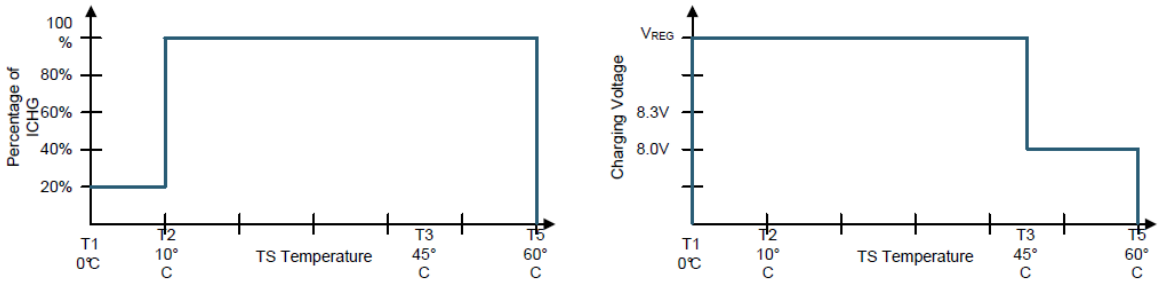



Figure 64: JEITA compliant charging curves of the BQ25886 [27].

In order to use any type of NTC thermistor, the manufacturer recommends a parallel linearization of the the thermistor by means of two resistors whose values have to be chosen in accordance with (25) and (26). Where:

- $V_{Tn}$ are the percentages of the voltages stated in Figure 64.
- $R_{TOP}$ and $R_{BOT}$ are the top and bottom resistors of the thermistor conditioning circuit.
- $R_{NTC_{Tn}}$ are the thermistor resistance values at the given temperatures.

$$R_{BOT} = \frac{R_{NTC_{T1}} \cdot R_{NTC_{T5}} \cdot (\frac{1}{V_{T5}} - \frac{1}{V_{T1}})}{R_{NTC_{T1}} \cdot (\frac{1}{V_{T1}} - 1) - R_{NTC_{T5}} \cdot (\frac{1}{V_{T5}} - 1)} \tag{25}$$

$$R_{TOP} = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC_{T1}}}} \tag{26}$$

The maximum current drawn from the USB input is determined by the minimum between USB BC1.2 detection and the limit fixed by $R_{ILIM}$, being $K_{ILIM} = 1110\,\Omega \cdot \mathrm{A}$.

$$I_{IN_{MAX}} = \frac{K_{ILIM}}{R_{ILIM}} \tag{27}$$

The charging current is also set by a resistor as stated in (28) but, this time, the datasheet does not provide $K_{CHGSET}$ but the resistor values for the minimum and maximum currents: $114\,\Omega \Leftrightarrow 30\,\mathrm{mA}$ and $8\,\mathrm{k}\Omega \Leftrightarrow 2.2\,\mathrm{A}$.

$$I_{CHGSET} = \frac{K_{CHGSET}}{R_{CHGSET}} \tag{28}$$

The battery charging voltage is also determined by the value of a resistor ($R_{VSET}$), in our case $150\,\mathrm{k}\Omega \Leftrightarrow 8.4\,\mathrm{V}$.

To determine the inductance needed for the boost conversion (29) needs to be followed. The manufacturer recommends a similar criterion as in the other power supplies: ripple current between 20 % and 40 % of the maximum current. Again, 30 % is a safe value. The inductance value has to comply with (29).

$$L > \frac{V_{BUS} \cdot (V_{SYS} - V_{BUS})}{V_{SYS} \cdot f_{SW} \cdot I_{Ripple}} \tag{29}$$

For increased protection, a non-resettable fuse is placed in series with the positive terminal of the battery pack.

#### 3.2.1.10 Thermal management

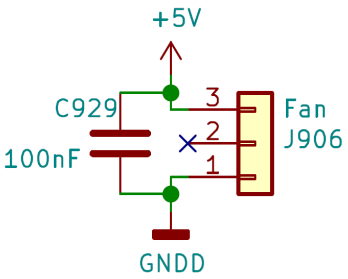



Figure 65: Fan connection.

Thermal management is a key aspect in every electronic design. It has to be ensured that the device will be capable of performing its intended function throughout its whole lifetime without these being degraded.

Inside this specific device, there will be many high-performance circuits that will dissipate a lot of power in the form of heat, making thermal management specially important. However, many of the components' power consumption is very dependant on its software or its load, making it nearly impossible to dimension accurately a heat management solution without performing complex simulations and testing. Since this device is the first

prototype and neither the software nor the FPGA circuit are still developed, these simulations will not be performed but, instead, for this first iteration the heating management will be over-estimated. An exhaust fan along with an air intake will be placed strategically inside the enclosure and each component susceptible of generating heat will be equipped with a big heat-sink. The fan will be controlled by the MPU which will activate it in accordance with the temperature readings of an NTC thermistor.

### 3.2.2 Enclosure and PCB layout

After the whole circuit has been designed and assured that it is free of errors, it comes the moment of choosing an enclosure for the device.

The device has to incorporate some type of protective earth connection. Taking advantage of this, if the enclosure is made out of a conductive metal and at the same time connected to PE, it should help mitigate some electromagnetic emissions and make it more robust against immunity tests. However, this approach does not assure a good performance. In some cases, if not implemented correctly, it can actually make problems worse.

The enclosure chosen for the device has to be big enough to fit all the components such as the display and the other user interfaces as well as the PCB and the fan. For this reason, after carefully checking some fitment of the components as seen in Figure 66, a light extruded aluminium box with rails at different heights from Hammond Manufacturing has been selected.

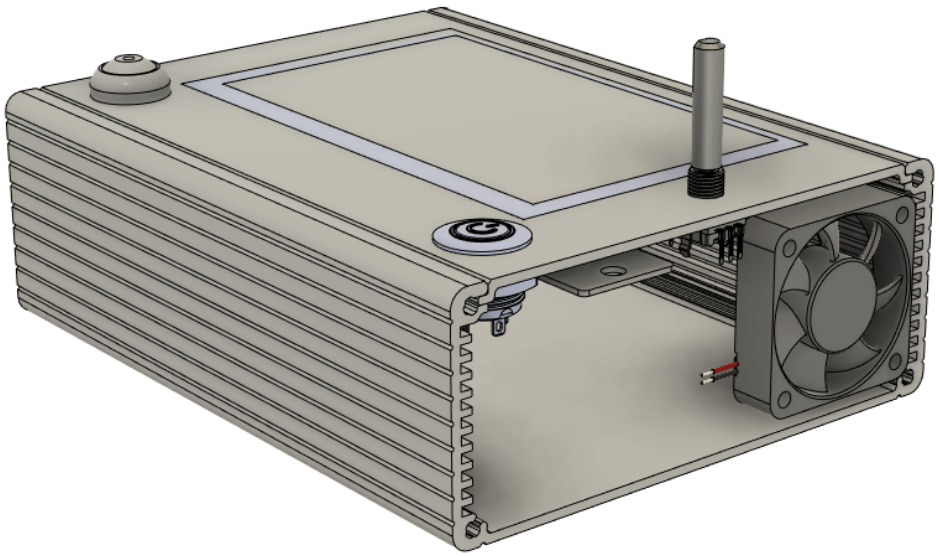


Figure 66: Mock up of the external components in the chosen enclosure.

With this enclosure, the PCB can be mounted and secured on the rails without the need of screws. Therefore, the board needs to be 160 mm long by 120 mm wide with a notch to clear the fan.

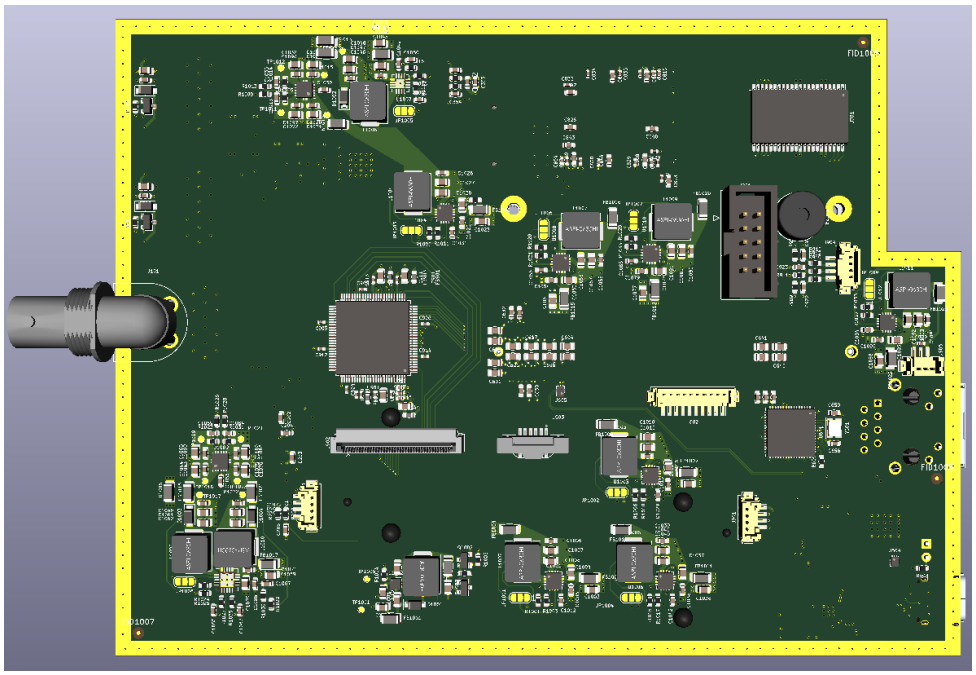
Prior to beginning with the layout design, it must be ensured that the design rules and the layer stackup are set properly according to the manufacturer guidelines and capabilities. In this case, due to the complexity of the design and the existence of controlled

impedance traces, I have opted for a 1.6 mm thick, 6 layer stackup shown in Figure 67. This stackup is made out of a special substrate with well defined dielectric relative permittivity constant and a predefined precise layer distance. This information is used to calculate the needed track width and spacing for each track impedance. To facilitate the task, the manufacturer provides an easy to use calculator with their own parameters already preloaded.

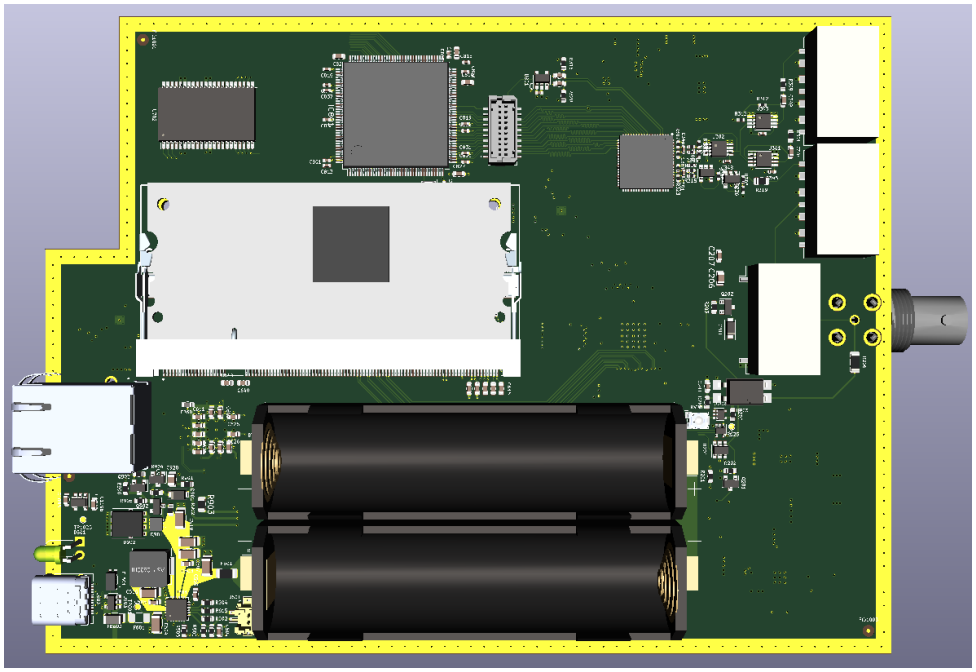
| Layer | Material Type | Thickness |
|---|---|---|
| Top Layer1 | Copper | 0.035 mm |
| Prepreg | 2313*1 | 0.1 mm |
| Inner Layer2 | Copper | 0.0175 mm |
| Core | Core | 0.565 mm |
| Inner Layer3 | Copper | 0.0175 mm |
| Prepreg | 2116*1 | 0.127 mm |
| Bottom Layer4 | Copper | 0.0175 mm |
| Core | Core | 0.565 mm |
| Inner Layer5 | Copper | 0.0175 mm |
| Prepreg | 2313*1 | 0.1 mm |
| Bottom Layer6 | Copper | 0.035 mm |

Figure 67: Layer stackup from the selected manufacturer.

The current state of the PCB is shown in Figure 68, where all the components have been placed and the routing process has began. Next, it is proceeded to explain the design decisions that have led to this layout.



(a) Top view



(b) Bottom view

Figure 68: 3D view of the PCB.

Instead of using a cable to create the PE connection to the PCB, benefiting from the fact that the PCB will be in contact with the aluminium enclosure, a protective earth path is created around the whole PCB. This will further contribute to maintaining the noise within the board and will make PE available anywhere on the PCB.

It is decided to place components on both sides of the PCB in order to get everything to fit the assigned PCB size. This implies that if, in a future, the board is decided to be assembled by an external company the production costs will be superior. However, for now, this board is going to be assembled by hand in the department. Because of that,

great care will have to be taken when soldering in order to not melt the solder from the bottom components that have been already soldered.

The most complex and time consuming but yet so important part of the design is the component placement. It has to be done first to ensure that everything fits although there are some prearranged structures that are routed before placing them, this is the case of the power supplies. Some parts do have a predefined position within the PCB as is the case of screen, USB and Ethernet connectors. Then, large-sized components are positioned, after which the important sections are placed together with their power supplies and decoupling capacitors. By last, least important components are placed.

There are a couple components on the design that need external crystal resonators. These crystals create large square signals that are easily coupled with other parts and cables and can easily become an EMC problem. To try to isolate these signals, the crystals are positioned on a GND island that can not be crossed by any other signal at any of the layer.

Power supplies are likely to create high frequency noise that can get worse if they are not arranged properly. To mitigate this problem, the design guidelines and layouts purposed by the manufacturers are used. Also, they are tried to be positioned near the elements they have to feed so that parasitic inductance is reduced and they can respond faster to current demands. Despite that effort, decoupling capacitors are still needed.

Some of the components create higher frequency noise than others. This makes that some of them, like the FPGA, need to incorporate very tiny capacitors (0402 or even 0201 because the smaller the capacitor size the smaller the parasitic inductance) as close to the pads as possible.

An other important factor to bear in mind when routing the power paths is the minimum needed trace width in order to withstand a certain current. The maximum current that a trace can handle is given by (30), where:

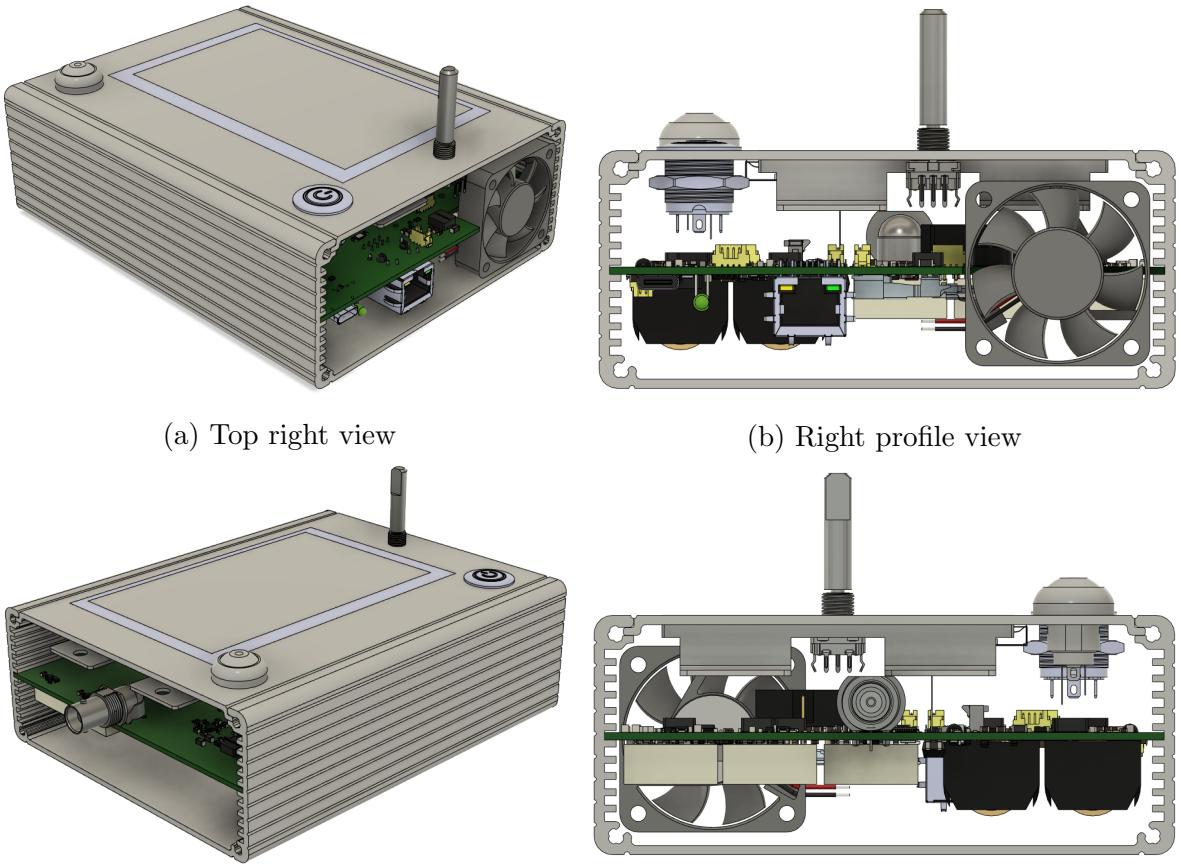
- $I$ is the maximum current in amps.
- $K$ is a constant of value 0.024 for external traces and 0.048 for internal traces.
- $\Delta T$ is the temperature rise above ambient in ℃.
- $W$ is the width of the track in mils.
- $H$ is the thickness of the track in mils.

$$I = K \cdot (\Delta T)^{0.44} \cdot (W \cdot H)^{0.725} \tag{30}$$

Some of the interfaces are governed by a clock and their data signals do have to comply with very strict setup and hold times. When working at high frequencies, the simple length of the tracks can cause the signals to arrive out of phase with each other. To avoid this, these tracks have to be length matched. In particular, the HDMI and data lines of the DAC. On the other hand, the DPI signals that go from the HDMI-DPI converter to the screen connector will only work at frequencies of up to 50 MHz. If those lines are routed without trying to match their lengths, the length difference is around

40 mm which is equivalent to 170 ps of skew. Compared to the setup and hold times of the screen, the skew is 60 times smaller, making this length mismatch negligible.

In figure Figure 69 is shown the current PCB inside its enclosure without its side covers.



(a) Top right view

(b) Right profile view

(c) Top left view

(d) Left profile view

Figure 69: 3D model of the device.

# 4 Conclusions and future work

In order to perform its function, this device has been carefully designed in conjunction with the signals it will have to reproduce because there are many waveforms that are capable of creating the needed spectrums, but not all of them can be reliably reproduced in an easy and efficient way.

This is an innovative project not because of the device performance, since it is based on what would be a mid range arbitrary waveform generator, but due to the fact that all elements it incorporates have been exclusively designed for the strict requirements of EMC laboratories.

This project has involved a complex development in a wide range of engineering areas and tasks that are usually carried out by large teams. Specifically, the device required: working in an accurate analog design to be able to recreate the signals without them being distorted; a digital part capable of communicating and controlling all the elements of the circuit without errors; an efficient design in terms of power distribution; and designing a structure that is capable of housing all the components while being functional, safe, and good looking. All of this while paying special attention to possible EMC problems that such integration may entail.

Although it is far from being completed, the device already incorporates novel elements and methodologies that do have the possibility of being further developed to be exploited commercially and could even be patented because up to date, to our knowledge, such device with similar characteristics and made for this purpose does not exist.

Once this project is complete, some of the ideas used for verification of the electromagnetic emissions test benches could be extrapolated to other EMC tests following the work of institutions from all over the world. However, this would imply totally different approaches, not only because of the different hardware they would have to incorporate, but also the verification methodologies and strategies would need to be changed.

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