A Study on Statistical Reliability Analyses in Silicon Oxide and Magnesium Oxide Films due to Localized Defects

　　　　　　　　　　パク　ヒョンウ
氏　　　　　名　朴　　賢雨
研究科，専攻の名称　東北大学大学院工学研究科（博士課程）技術社会システム専攻
学 位 論 文 題 目　A Study on Statistical Reliability Analyses in Silicon Oxide and Magnesium Oxide Films due to Localized Defects（シリコン酸化膜およびマグネシウム酸化膜における局所的欠陥起因の統計的信頼性解析に関する研究）
論 文 審 査 委 員　主査　東北大学教授　須川　成利　東北大学教授　中村　健二
　　　　　　　　　　　　東北大学教授　石田　修一　東北大学准教授　黒田　理人

論文内容要約

Since 1960 that the metal-oxide-semiconductor field effect transistor (MOSFET) was invented, the performance of the integrated circuit (IC) has been upgraded with the great speed over decades. The performance of semiconductor memory has also been greatly developed. For examples, NAND flash memory has upgraded itself by renovating the cell structure into 3-dimensional structure, and some memory structure for the next generation (Such as Magnetic RAM, Phase Change RAM, or Resistive RAM.) were invented using new tunnel barrier materials such as magnesium oxide (MgO) or hafnium oxide (HfO_2).

However, some reliability problems have also been significant as the semiconductor devices were upgraded with downscaling MOSFETs or memory cells. The representative reliability problems are such as time dependent dielectric breakdown (TDDB) or stress-induced leakage current (SILC). Especially these two phenomena are well known as the major problems degrading the reliability of dielectric films well used as tunnel barrier in flash memory.

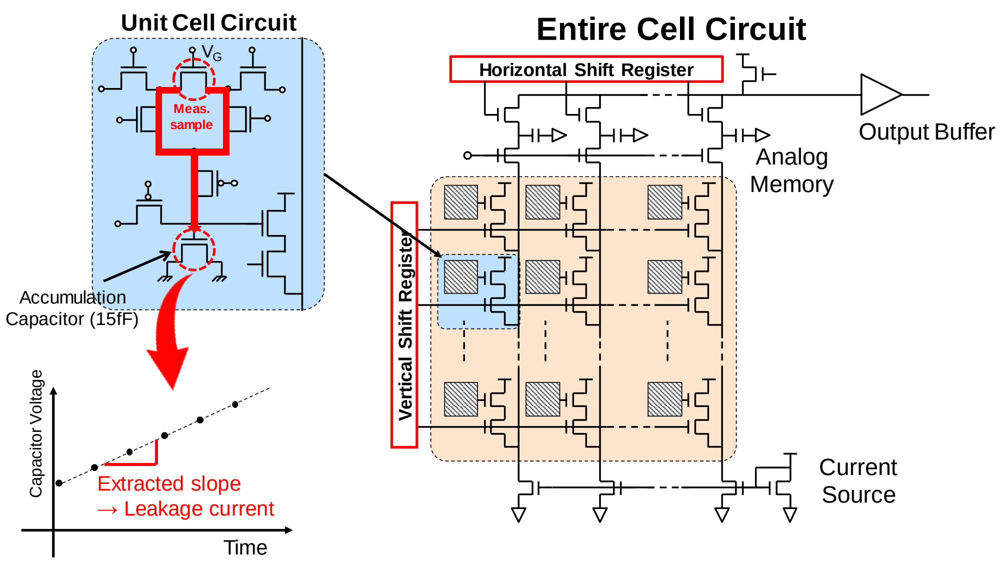

Figure 1. The circuit diagram of the large-scale array test circuit for measuring the localized SILC in SiO_2 films.

While TDDB is considered as the phenomenon occurring on a localized defects, SILC is considered as an average phenomenon that occurs equally in every places of SiO_2 films. On the contrast, some previous studies have reported the measurement of anomalously large SILC in local area (defined as “Localized SILC” in this dissertation.) using the array test circuit. Figure 1. shows the circuit diagram of the large-scale array test circuit. By employing the horizontal and vertical shift registers for rapid sample selection and accumulation capacitor (15fF) in each unit cell circuit, this array test circuit can measure very small leakage current from 10^{-17} to 10^{-14} A of a large number of silicon oxide samples (larger than 87,000) with very high speed (0.1 sec/frame). With this circuit, the localized SILC can be statistically measured. However, the characteristics of this localized SILC in different dielectric film area are not investigated yet. Therefore, in this dissertation, TDDB and localized SILC are statistically measured and analyzed in SiO_2 and MgO films, then a reliability analyses method based on localized defects is established which can universally applied to several types of dielectric films.

In Chapter 1, the introduction was shown.

In Chapter 2, the localized SILC of SiO_2 films with different (1×1, 0.5×0.5, 0.25×0.25 μm^2) are statistically measured and their data are analyzed. As a result, the localized SILC respectively measured in different area, are not normalized by current density. And it was found that the localized SILC distribution are normalized by localized defects following Poisson distribution. Finally, the defect density causing localized SILC was successfully extracted from the SILC measurement results. Additionally, the direct correlation between TDDB and localized SILC were investigated. As a result, the TDDB-SILC correlation becomes higher as the SiO_2 film area becomes smaller. It is because the smaller area includes fewer SILC defects, and the SILC defects becomes more critical to that small-area SiO_2 films to cause early breakdown.

In Chapter 3, The reason causing localized defects in SiO_2 films were investigated. Firstly, Si surface roughness was investigated. The localized SILC of SiO_2 films with two different surface roughness was statistically measured using the array test circuit, and compared to each other. Although the roughness difference does not impact on the average SILC, but the rougher surface greatly impacts on the increase of localized SILC. It was found that the number of localized SILC defects are reduced to 10% by applying the atomically flattening process. The reason why the rougher surface causing more localized defects was found to be the electric field concentration by some device simulation. Therefore, the rougher surface is found to increase the localized defects, which occur both localized SILC and early breakdown. The model diagram is shown in Figure 2. Secondly, hole injection to SiO_2 films were investigated. The hole charge to breakdown is reported to be independent of the stress current while measuring TDDB characteristics. Then it can be considered that the hole charge may be related to the localized SILC. In prior to the localized SILC measurement, the hole injection – average SILC relationship was investigated using substrate hot carrier injection (SHCI) method. The results showed that the average SILC values are totally decided by the injected hole charge, and independent of any other parameter such as

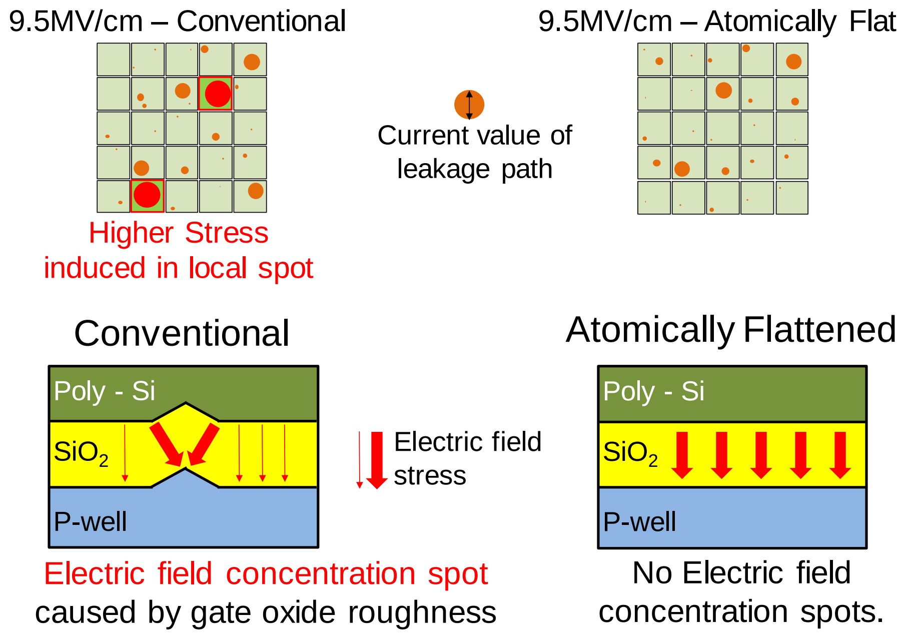

Figure 2. A model diagram explaining how local roughness impacts on both TDDB and localized SILC in SiO_2 films

oxide field or hole energy. However, this universality of average SILC to hole injection charge was not expanded to the localized SILC. The localized SILC was statistically measured by array test circuit exclusively fabricated to measure the hole current while stress application. The results showed no correlation between hole injection and the localized SILC.

In Chapter 4, the electric reliability of MgO films, which is essentially utilized in STT-MRAM device, were statistically measured and analyzed. Firstly, the impact of the MgO surface roughness to electric reliability was investigated. As a result, MgO films with large surface roughness causes larger current. One of the reasons were found to be electric field concentration in MgO film. And it was also confirmed with the electric field concentration simulation results. Secondly, the electric reliability degradation by pattern-edge of MgO films was investigated. Ion beam etching is widely utilized in forming MRAM structure. However, it was found that conventional etching process condition can cause the critical TDDB degradation in MgO films. With this TDDB degradation by the edge impact, the number of defects causing TDDB in MgO edge was quantitatively calculated. Also, the reduction of the edge defect was confirmed by controlling IBE angle with small angle divergence.

The conclusion of this dissertation was written in Chapter 5. The model diagram of TDDB and SILC characteristics in dielectric films which is clarified in this dissertation is shown in Figure 3. The localized SILC was found to be randomly distributed in entire dielectric films area, and its probability was found to follow the Poisson distributions as TDDB characteristics. Another finding is that the local defects where the large SILC is generated, is highly probable to occur the early dielectric breakdown in case of small area (smaller than 0.5×0.5 μm^2). As one parameter to cause the TDDB and localized SILC, the surface roughness of SiO_2 was found from the localized SILC measurement and electric field concentration simulation. This reliability analysis method based on localized defects were also applied into magnesium oxide (MgO) films. Then the MgO surface roughness, and the pattern-edge by ion beam etching (IBE) were found to cause large localized TDDB defects. It is considered that this reliability analysis method based on localized defects can be utilized widely for evaluation, prediction, and improvement of reliability in many dielectric films as well as silicon oxide films.

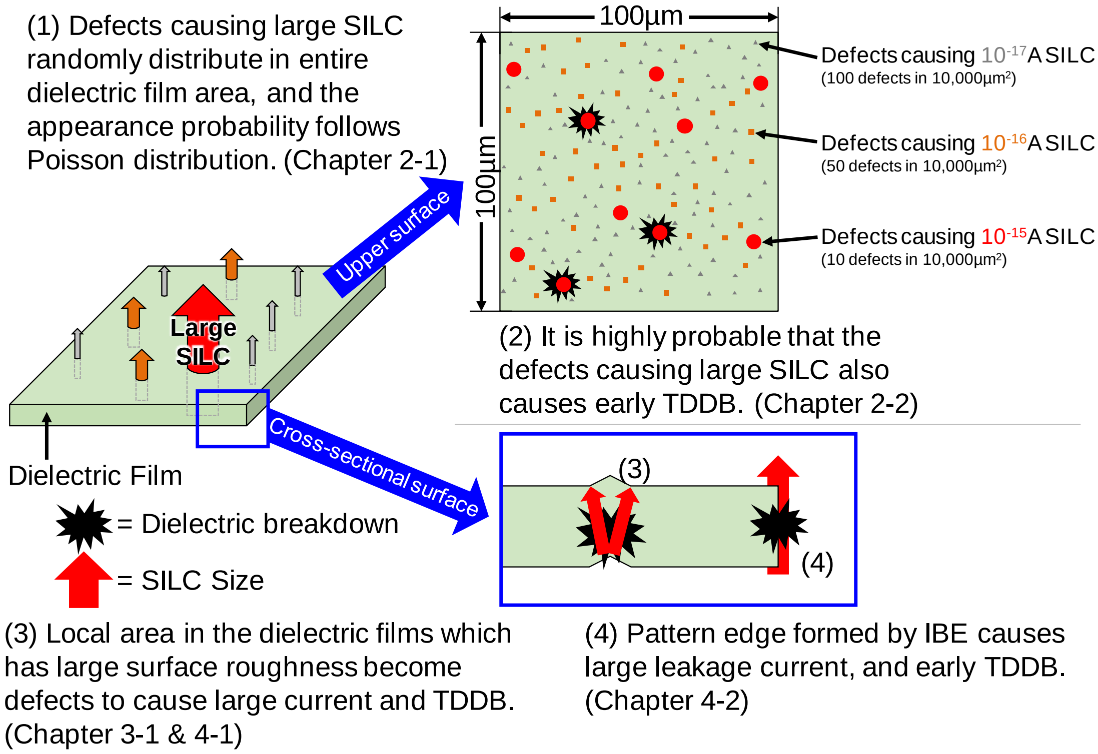

Figure 3. A model diagram of SILC and TDDB in a dielectric film, which summarizes the entire achievements of the doctoral dissertation.