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Design and Fabrication of Micro-Electro-Mechanical Structures for Tunable Micro-Optical Devices

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DESIGN AND FABRICATION OF MICRO-ELECTRO-MECHANICAL STRUCTURES FOR TUNABLE MICRO-OPTICAL DEVICES

THESIS

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Abstract
Tunable micro-optical devices are explected to be vital for future military optical communication systems. In this research I seek to optimize the design of a microeletromechanical (MEM) structure integrated with a III-V semiconductor micro-optical device. The resonant frequency of an integrated optical device, consisting of a Fabry-Perot etalon or vertical cavity surface emitting laser (VCSEL), may be tuned by applying an actuation voltage to the MEM Flexure, thereby altering the device's optical cavity length. From my analysis I demonstrate tunable devices compatible with conventional silicon 5V integrated circuit technology. My design for a Fabry-Perot etalon has a theoretical tuning range of 200 nm, and my VCSEL design has a tuning range of 44nm, both achieved with actuation voltages as low as 4V. Utilizing my theoretical device designs I planned a new microelectronics fabrication process to realize a set of prototype MEM-tunable devices with a peak central emission wavelength at 980nm. I designed a mask set consisting of 8 mask levels and 252 distinct device designs, all within a die size of one square centimeter. My unique fabrication process utilizes a gold MEM flexure with a Si3N4/Si02 dielectric distributed Bragg reflector (DBR) mirror, grown on an all-semiconductor VCSEL or Fabry-Perot substrate. I successfuly fabricated a complete set of MEM-tunable test structures using the cleanroom laboratory facilities at the Air Force Institute of Technology (AFIT) and the Air Force Research Laboratory (AFRL). The initial devices display minimum electrostatic actuation voltages as low as 1.8 V, which is comparable to existing MEM tunable VCSEL designs. In order to enhance device performance, I developed improvements to my laboratory process for incorporation in future fabrication runs. These results form the fundamental basis for advanced development of manufacturable MEM-tunable optical emitting and detecting arrays.

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AFIT/ENG/GEO-02M-01

DESIGN AND FABRICATION OF MICRO-ELECTRO-MECHANICAL STRUCTURES FOR TUNABLE MICRO-OPTICAL DEVICES

THESIS

Presented to the Faculty of the Graduate School of Engineering and Management
of the Air Force Institute of Technology
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In Partial Fulfillment of the
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"If we knew what it was we were doing, it would not be called research, would it"

Albert Einstein (1879 - 1955)

First I would like to thank my fiance for her loving support and patience throughout my thesis research. She wasn't expecting to move into an empty house while I spent my days and nights working in the lab.

I would also to thank my thesis advisor, Lt Col Lott, for providing me the knowledge and resources I needed to conduct my research, and then allowing me to work independently.

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To the scientists, engineers, and laboratory technicians at the Air Force Research Laboratory Sensors Directorate, I give my heartfelt appreciation. I look forward to working with these dedicated professionals in the years to come.

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List of Symbols

Symbol		Page
Au	Gold	1-3
Si_3N_4	Silicon Nitride	1-3
KOH	potassium hydroxide	2-1
ϕ_{xyz}	Potential Voltage	2-5
σ	Surface Charge (C/m^2)	2-5
$E_\perp$	Perpendicular Electric Field (V/m)	2-5
q	Electric Charge (C)	2-8
V	Voltage (V)	2-8
C	Capacitance (F)	2-8
U	Stored Energy	2-8
A	Area (m^2)	2-8
d	Distance Between Capacitor Plates (m)	2-8
ε	Permittivity (F/m)	2-8
ε_0	Permittivity of Free Space (F/m)	2-8
k	Spring Constant (N/m)	2-9
E	Young's Modulus (GPa)	2-9
Au	Gold	2-9
GPa	GigaPascal	2-9
MPa	MegaPascal	2-9
I	Moment of Inertia (m^4)	2-10
M(x)	Bending Moment (Nm^2)	2-10
h	Thickness of Rectangular Beam (m)	2-11
w	Width of Rectangular Beam (m)	2-11
L	Length of Rectangular Beam (m)	2-11
GaAs	Gallium Arsenide	2-19

Symbol		Page
AlAs	Aluminum Arsenide	2-19
SiO_2	Silicon Oxide	2-19
TiO_2	Titanium Oxide	2-19
M	transfer matrix	2-22
L	layer in transfer matrix method	2-22
N_L	complex index of refraction for layer L	2-23
P_L	propagation matrix for layer L	2-23
d_L	thickness of layer L	2-23
k_{Lx}	x component of the wave vector	2-23
ρ	Reflectivity Coefficient	2-23
$Al_xGa_{1-x}As$	Aluminum Gallium Arsenide	2-29
$In_{0.2}Ga_{0.8}As$	Indium Gallium Arsenide	2-29
Ti	Titanium	4-4
AlO_x	Aluminum Oxide	4-6
CHF_3O_2	Freon Etchant CF-23	4-10
CF_4	Freon Etchant CF-14	4-19
Ge	Germanium	4-21
Ni	Nickel	4-21

List of Abbreviations

Abbreviation		Page
DUV	Deep Ultra-Violet	4-12
DIW	Deionized Water	4-22
IFM	Interferometer Microscope	5-10
CVD	Chemical Vapor Deposition	C-4
PMGI	Polymethylglutarimide	C-6

Abstract

Tunable micro-optical devices are expected to be vital for future military optical communication systems. Those aerospace systems utilizing wavelength-division multiplexing (WDM) techniques will have access to vastly increased bandwidth for voice, imagery, and RF data streams. In this research I seek to optimize the design of a microelectromechanical (MEM) structure integrated with a III-V semiconductor micro-optical device. The resonant frequency of an integrated optical device, consisting of a Fabry-Perot etalon or vertical cavity surface emitting laser (VCSEL), may be tuned by applying an actuation voltage to the MEM flexure, thereby altering the device's optical cavity length. By optimizing the design and fabrication of the MEM structure, Fabry-Perot etalon and VCSEL tuning voltages as low as 5 V may be achieved across a broad spectral bandwidth.

I conduct in-depth modeling of MEM tunable Fabry-Perot and VCSEL designs by first composing a mathematical computer software toolset. From my analysis I demonstrate tunable devices compatible with conventional silicon 5V integrated circuit technology. My design for a Fabry-Perot etalon has a theoretical tuning range of $\Delta\lambda = 200\ nm$, and my VCSEL design has a tuning range of $\Delta\lambda = 44\ nm$, both achieved with actuation voltages as low as 4 V. Utilizing my theoretical device designs I plan a new microelectronics fabrication process to realize a set of prototype MEM-tunable devices with a peak central emission wavelength at $\lambda_o = 980\ nm$. I design a mask set consisting of 8 mask levels and 252 distinct device designs, all within a die size of one square centimeter. My unique fabrication process utilizes a gold MEM flexure with an Si_3N_4/SiO_2 dielectric distributed Bragg reflector (DBR) mirror, grown on an all-semiconductor VCSEL or Fabry-Perot substrate. I then successfully fabricate a complete set of MEM-tunable test structures using the cleanroom laboratory facilities at the Air Force Institute of Technology (AFIT) and

the Air Force Research Laboratory (AFRL). I characterize the structures by optical interferometry measurements with nanometer scale resolution. The initial devices display minimum electrostatic actuation voltages as low as 18 V, which is comparable to existing MEM tunable VCSEL designs. In order to enhance device performance, I develop improvements to my laboratory process for incorporation in future fabrication runs. These results form the fundamental basis for advanced development of manufacturable MEM-tunable optical emitting and detecting device arrays.

DESIGN AND FABRICATION OF MICRO-ELECTRO-MECHANICAL STRUCTURES FOR TUNABLE MICRO-OPTICAL DEVICES

I. Introduction

1.1 Motivation

Information superiority is one of the six Air Force core competencies for global engagement in the 21st century. The Air Force must develop technologies and systems which enable battle management and command-and-control systems to provide real-time control and execution of air and space missions. Tunable micro-optical devices are expected to be vital for future military optical communication systems. Those aerospace systems utilizing wavelength-division multiplexing (WDM) techniques will have access to vastly increased bandwidth for voice, imagery, and RF data streams.

1.2 Tunable Vertical Cavity Surface Emitting Lasers

The first surface emitting lasers were demonstrated circa 1979 [3]. These devices operated at liquid nitrogen temperatures with very high activation currents. Improvements were slow until the mid-1980's, when they became known as vertical cavity surface emitting lasers (VCSELs). VCSELs utilized all semiconductor distributed Bragg reflector (DBR) mirrors, replacing the semitransparent metal films used previously. Unlike edge-emitting lasers, VCSEL devices lase vertically, in the direction of epitaxial growth. While edge-emitting lasers emit a highly astigmatic laser beam lateral to the growth direction, VCSELs typically produce a circularly symmetric Gaussian beam. This enables VCSEL devices to easily couple light into

optical fibers without any intervening optics. The vertical laser output enables the fabrication of large two-dimensional laser arrays on a single wafer, and greatly eases testing of the lasers prior to packaging. These VCSEL arrays are extremely useful for wavelength division multiplexing (WDM).

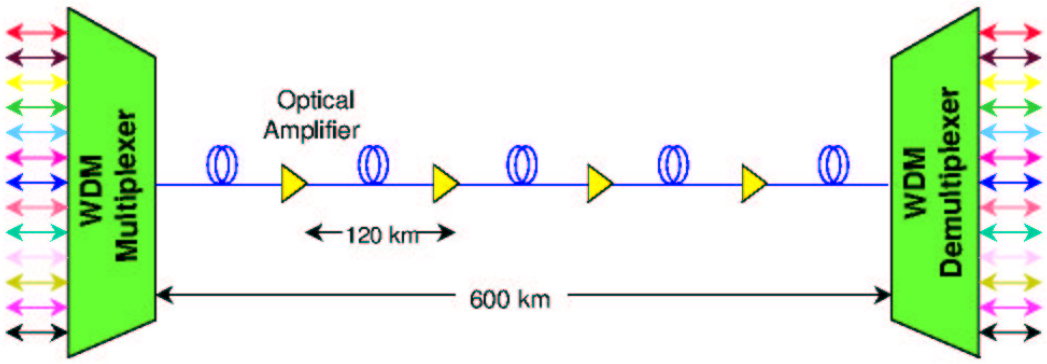

Figure 1.1 Simplified schematic overview of Wavelength Division Multiplexing (WDM). Multiple laser frequencies share the same optical fiber, thereby vastly increasing the available transmission bandwidth.

WDM provides substantially increased bandwidth to long-haul telecommunications and local-area networks by allowing multiple optical frequencies to share the same optical fiber, as shown in figure 1.1. WDM systems provide this capability without the need to replace current optical network backbones, since they utilize the millions of miles of fiber optical cable already installed worldwide. Current WDM devices are limited as they only support network topologies that are either entirely static, or capable of very limited reconfiguration. Utilizing tunable VCSEL arrays in WDM systems will allow precise control over laser wavelength separation. This results in more wavelengths packed into a single optical fiber. In addition, tunable lasers will ease the reconfiguration and maintainability of WDM interconnects. The ability to adaptively tune the VCSELs to a precise frequency means systems will be more robust to temperature variations and component aging.

1.3 Problem Statement

WDM has provided a substantial benefit to long-haul telecommunications, and its deployment in this commercial market is well underway. However, currently available WDM systems are predominantly constructed of fiber-coupled discrete components. This macro-scale approach to device integration results in WDM modules with far too large a footprint for military platforms. In addition, many WDM devices will only support network topologies that are either entirely static, or capable of limited reconfiguration [1]. The shorter transmission distances that characterize the data networks of military platforms may limit the insertion opportunities of long-haul commercial off-the-shelf (COTS) WDM equipment [2]. Typically, military systems require robust network and communication hardware capable of operating in extreme conditions. Strain reduces the useful lifetime of optoelectronic devices. As a result, COTS hardware designed for commercial applications may not operate under the conditions placed on military equipment. Future military platforms would gain substantial benefit from WDM components that provide high-levels of chip-scale integration and support dynamically reconfigurable topologies. In order to facilitate these requirement, research is needed to optimize the design of microelectromechanical tunable laser diodes for use in military WDM systems.

1.4 Research and Scope of Thesis

In this thesis I simulate, design, fabricate, and characterize microelectromechanical (MEM) tunable optical devices operating near 980 nm. I use custom software tools to design and model MEM structures integrated with III-V semiconductor optical devices. I develop and test a custom micromachining laboratory process. I design all-semiconductor optical structures and have them grown via molecular beam epitaxy (MBE). I then fabricate MEM structures placed on MBE grown Fabry-Perot etalons and resonant cavity light emitting diodes (RCLEDs). I investigate multiple MEM flexure designs composed of gold (Au) and silicon nitride (Si_3N_4). I then char-

acterize the electrical response of the fabricated mechanical structures. From these results I develop process improvements and pave the way for continued research.

1.5 Methodology

I divide my research into four stages. The first stage is a background review of the current literature and computer modeling to analyze design configurations. The second stage is the development of a MEM fabrication process utilizing the Air Force Institute of Technology (AFIT) and Air Force Research Laboratory (AFRL) cleanroom facilities. While developing my process, care is taken to reduce risk by utilizing existing fabrication techniques when possible. After settling on a device design and fabrication process, a complete photolithographic mask set is created using computer aided design (CAD) software. Stage three is the complete fabrication of a full-scale test structure to verify the MEM construction process. Stage four is the fabrication and testing of MEM structures integrated with an epitaxially grown semiconductor DBR in order to achieve a tunable Fabry-Perot (FP) etalon. The final stage is construction and characterization of a tunable VCSEL. All devices are fabricated at AFRL and AFIT laboratory facilities.

1.6 Main Results

The research I present in this thesis shows that complex surface micromachined MEM structures can be fabricated and integrated with III-V semiconductor optical devices. Towards this end, I have conducted in-depth modeling of MEM tunable Fabry-Perot and VCSEL designs, centered at $\lambda_o = 980\ nm$. Calculations show that a wide Fabry-Perot tuning range of $\Delta\lambda = 200\ nm$, and a VCSEL tuning range of $\Delta\lambda = 44\ nm$ can be achieved using MEM flexures with theoretical actuation voltages as low as 4 V. In order to construct these devices I developed a unique laboratory fabrication process and created a set of eight photolithographic masks incorporating over 252 individual device designs into a 1 cm^2 die. I successfully

fabricated and electrostatically tested a complete array of MEM structures. The initial devices display minimum electrostatic actuation voltages as low as 18 V, which is comparable to existing MEM tunable VCSEL designs. In order to enhance device performance, I developed improvements to my laboratory process which will be incorporated in future fabrication runs. This work forms the fundamental basis for advanced development of manufacturable MEM-tunable optical emitting and detecting device arrays.

1.7 Sponsor

My thesis research is sponsored by the Air Force Research Laboratory Sensors Directorate, Electron Devices Branch (AFRL/SNDD), Wright-Patterson Air Force Base, Ohio. This research is also partially funded by the Air Force Office of Scientific Research (AFOSR).

1.8 Thesis Organization

This thesis is organized into six chapters. In Chapter II, I give an overview of processing techniques required for the fabrication of MEM devices and VCSELs, as well as a review of MEM and VCSEL design characteristics. I also discuss current MEM tunable VCSEL research. Chapter III discusses the results of computer simulation for integrated MEM tunable Fabry-Perot and VCSEL designs. In addition, I determine the semiconductor epitaxial growth recipe required to achieve VCSEL lasing. In Chapter IV I present the design and layout of my photolithography mask set as I use it to process the first device fabrication run. In Chapter V, I present the results and analysis of my MEM device research. Finally in Chapter VI, I present my conclusions and recommendations for future research.

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II. Background

2.1 Chapter Overview

In this chapter I present background material relevant to my research objectives. The goal of my research is to design and fabricate MEM structures integrated with epitaxially grown substrates to create tunable optical devices. With this in mind, I give a brief overview of MEM device fabrication in section 2.2, followed by an analysis of the voltage vs. deflection characteristics of MEM piston micromirrors in section 2.3. After this, I discuss relevant optical and electrical characteristics of Fabry-Perot etalons and VCSELs in section 2.4, including an introduction to oxide DBR mirrors. Finally, I review the characteristics of tunable VCSELs in section 2.4.6, and present current research in section 2.5.

2.2 MEMS Overview

2.2.1 Bulk Micromachining. At present, there are two methods for fabricating microelectromechanical systems (MEMS). The first, referred to as bulk micromachining, was specifically developed for MEMS applications. The most common material for bulk micromachining is single crystal silicon due to the anisotropic nature of the silicon material [4]. The lattice orientation causes certain chemical etchants to exhibit crystal plane dependent etch rates. Bulk micromachining may also be used to pattern single crystal III-V semiconductors [9]. Bulk micromachining techniques, such as Reactive Ion Etching (RIE) produce extremely straight sidewalls (see figure C.9). Wet etchants such as potassium hydroxide (KOH) exhibit highly crystal plane dependent etch rates on the order of 300:1. By taking advantage of this crystal plane selectivity, complex patterns can be etched in bulk crystalline semiconductor (see figure 2.1).

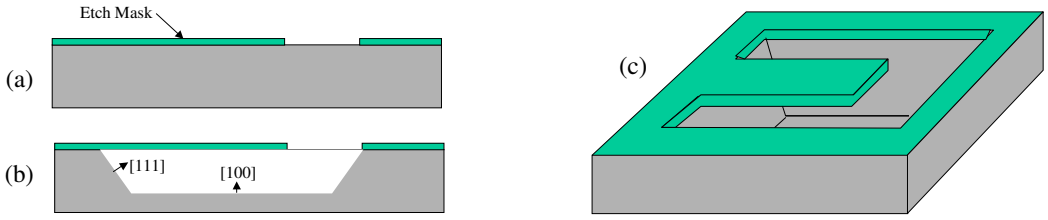
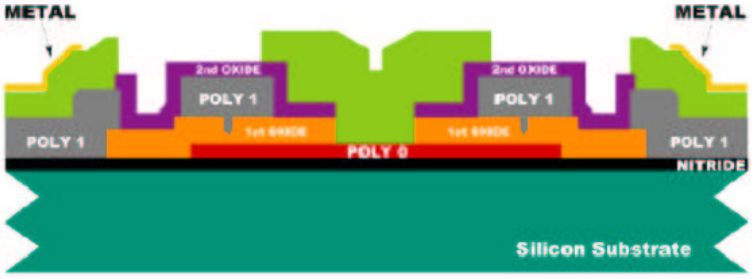


Figure 2.1 Cantilever fabricated by the wet etching of single crystal semiconductor using a crystal plane selective etchant, after [9].

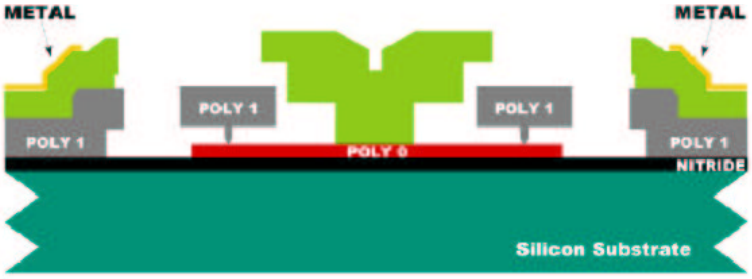
2.2.2 Surface Micromachining. Of more interest to my research is a second fabrication method know as surface micromachining. In this case the wafer substrate serves as a foundation on which structural and sacrificial material layers are selectively deposited and etched to fabricate mechanical structures.

An example of this fabrication method is the Multi-User MEMS Process (MUMPs®), which is a commercial micromachining foundry process used to create prototype MEMS structures [14]. The MUMPs® process uses two polysilicon layers to form mechanical components, two phosphosilicate glass (PSG) sacrificial layers, and a gold (Au) layer on the top surface (see figure 2.2).

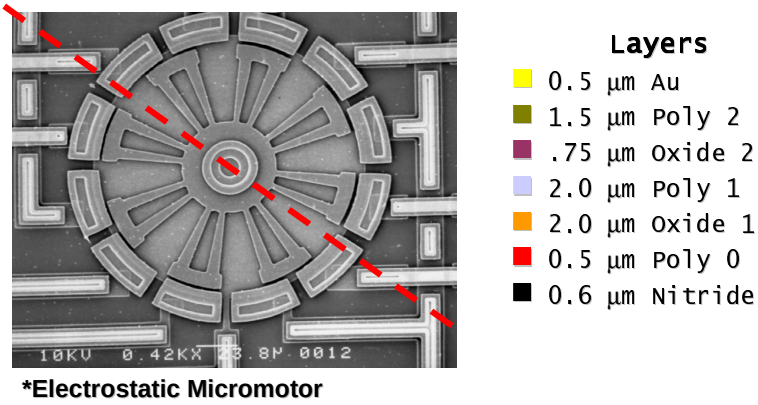
Surface micromachined material layers are deposited and patterned one at a time. As each new layer is deposited, it conforms to the surface beneath it. It is possible to create complex electrically or thermally actuated mechanical devices using combinations of material depositions and selective layer etching as shown in figure 2.3.



(a)

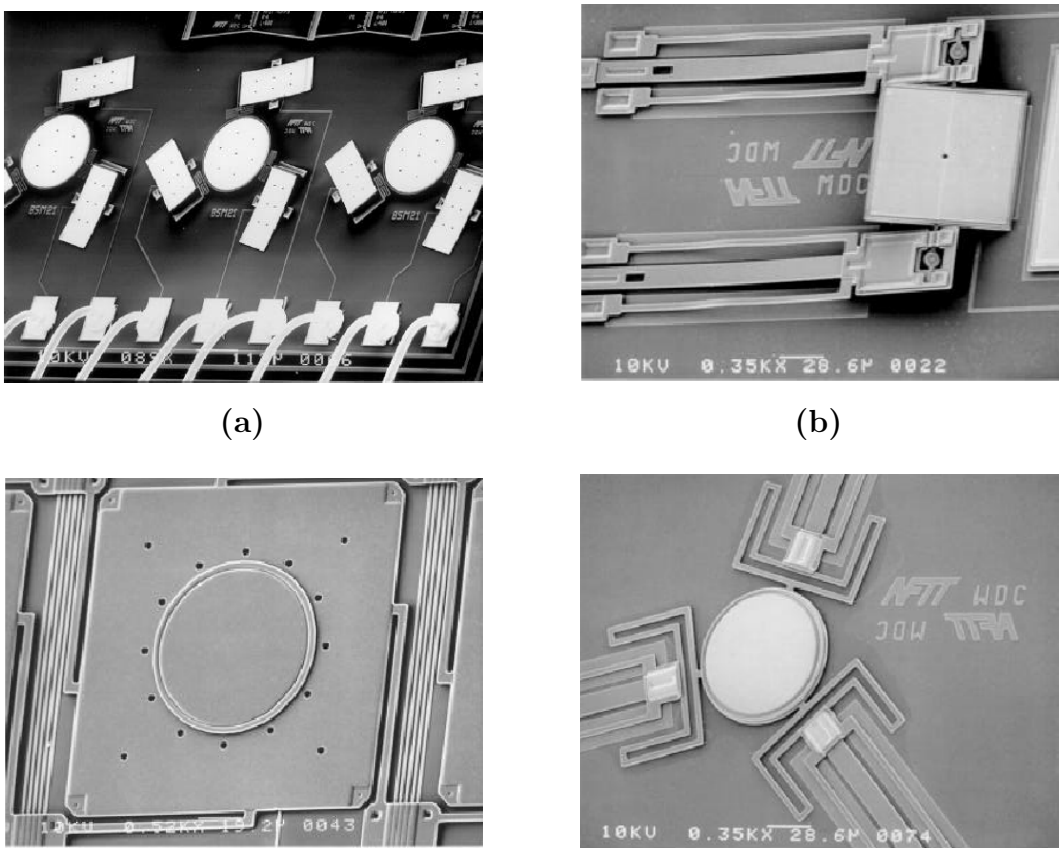


(b)



(c)

Figure 2.2 Example of a surface micromachining process showing the cross-section of a MUMPs® fabricated electrostatic motor (a) before and (b) after release. (c) is a top view of the completed device. Note the conformal nature of the deposited mechanical layers. The structure is released by the removal of the oxide sacrificial layers [8].



(a) **(b)**

(c) **(d)**

Figure 2.3 Example complex surface micromachined devices using the MUMPs® foundry process [4].

2.3 Electrostatic Actuation

The physics describing the operation of parallel plate MEMS devices is well understood and can be easily described to a high degree of accuracy using either numerical or analytic analysis. The actuation mechanism for the deflection of micromechanical mirror devices is electrostatic attraction of the movable membrane to an electrode. A full numerical analysis of the electrostatic forces acting on a conductor can be accomplished by solving LaPlace's Equation in 3-dimensions:

$$\nabla^2 \phi_{xyz} = \frac{\delta^2 \phi_{xyz}}{\delta x^2} + \frac{\delta^2 \phi_{xyz}}{\delta y^2} + \frac{\delta^2 \phi_{xyz}}{\delta z^2} = 0 \qquad (unitless) \tag{2.1}$$

where ϕ_{xyz} is the electrostatic voltage at a point in space defined by the coordinates x, y, and z (m). This equation can be solved numerically using a finite element method (FEM) to obtain the electrostatic potential at every point in a 3-dimensional space. Once ϕ_{xyz} has been solved, it is simple to calculate the downward force on a structure by applying the Coulomb force equation

$$F = \sigma E_{\perp} \qquad (N) \tag{2.2}$$

where σ is the charge per area (C/m^2) on the surface of the conductive MEMS flexure, and $E_{\perp}$ is the magnitude of the electric field (V/m) perpendicular to the surface.

By summing the combined force applied at each point on a mechanical structure, the total force is determined. This technique gives results that match actual laboratory measurements to a high degree of accuracy. Since the solution requires thousands of iterations of a 3-D volume of space that contains thousands of mesh points (depending on the desired resolution), the number of computations required may be in the billions. Although time consuming, the advantage of this type of analysis is the ability to determine stress and force distributions on complicated

structures. Commercial modeling packages such as CoventorWare MEMCAD [1] combine electrostatic and mechanical modeling, providing the ability to determine actuation voltages, stress distributions, and displacement information related to the mechanical flexing of materials.

2.3.1 Membrane Deflections. The deflection vs. voltage relationship of a flexable membrane with all four sides anchored is due solely to the bending of the membrane as the electrostatic force increases. The governing differential equations describing the membrane movement can be derived assuming the lateral deflections of the membrane are small compared with it's overall area. When neglecting higher order effects, the governing equation reduces to [18]:

$$\frac{\delta^2 w}{\delta x^2} + \frac{\delta^2 w}{\delta y^2} = -\frac{p_z(x,y)}{\sigma h} \qquad (unitless) \tag{2.3}$$

where $w(x,y)$ is the downward deflection at each point on the membrane (μm), $p_z(x,y)$ is the electrostatic force distribution across the membrane (N), h is the thickness of the membrane (μm), and σ is poisson's ratio (*unitless*), which is defined as the ratio of the transverse strain to the axial strain ($\sigma \approx 0.3$ for gold).

Equation 2.3 can be solved for the membrane deflection w(x,y), by applying Navier's method [18]. The solution must be iteratively calculated until it reaches a steady state, and is given by

$$w(x,y) = \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} W_{mn} sin\frac{m\pi x}{a} sin\frac{n\pi x}{b} \qquad (m) \tag{2.4}$$

where $a \times b$ are the dimensions of the membrane surface (μm$\times$ μm), m and n are iterations of the numerical calculation (integer), and x and y indicate the point on the surface being calculated (μm). The value of W_{mn} is determined by

$$W_{mn} = \frac{P_{mn}}{\pi^2[(m^2/a^2) + (n^2/b^2)]h\sigma} \qquad (m) \tag{2.5}$$

where P_{mn} represents the value of the electrostatic force applied at each point along the membrane. This is difficult to determine as the force changes at every point on the membrane surface as it deflects. Due to time constraints a numerical solution to this problem was not calculated.

2.3.2 Piston Micromirrors. When dealing with simple structures, such as flat plates, it is easier and less time consuming to develop a simple analytic solution. One technique is to treat the electrostatically actuated parallel plate device as a simple capacitor, with two conductive objects separated by some distance, d (as shown in figure 2.4).

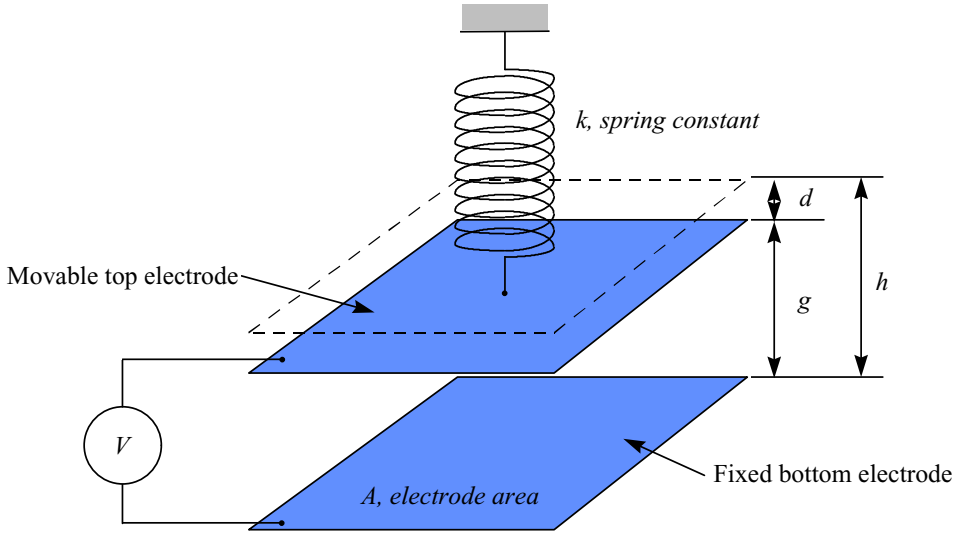


Figure 2.4 Schematic view of basic electrostatic piston micromirror [4].

Electrical energy is stored by attracting and repelling free electrons within the conductors. The capacitance is defined as the amount of electric charge stored per voltage, and is related by the expressions:

$$q = CV \qquad (C) \tag{2.6}$$

$$U = \frac{1}{2}CV^2 \qquad (J) \tag{2.7}$$

where q is the electric charge (C), V is the voltage, C is the capacitance (F), and U is the stored energy (J). The capacitance is defined as

$$C = \varepsilon\frac{A}{d} \qquad (F) \tag{2.8}$$

where A is the area of the plates (m^2), d is the distance between the plates (m), and ε is the permittivity of the gap material (F/m).

Note that equation 2.8 is only exact for infinite plate capacitors where fringing effects are ignored. Since the capacitance is inversely proportional to the distance between plates, a decrease in gap spacing, x, will result in an increase in capacitance which follows the relationship:

$$C = \varepsilon\frac{A}{(d-x)} \qquad (F) \tag{2.9}$$

For the purposes of this research, the gap material between the capacitor plates is air. The permittivity of free space (air) is given as $\varepsilon_0 = 8.85 \cdot 10^{-12} F/m$.

As a voltage potential is applied to the parallel plate capacitor, an electrostatic force is created which is related to the potential energy by the equation:

$$F = -\frac{\delta U}{\delta x} = -\frac{\delta}{\delta x}\left(\frac{1}{2}\frac{\varepsilon_0 A V^2}{(d-x)}\right) \qquad (N) \tag{2.10}$$

Solving this differential equation results in

$$F = \frac{1}{2}\frac{\varepsilon_0 AV^2}{(d-x)^2} \qquad (N) \tag{2.11}$$

This downward force is countered by the spring force of the flexures as given by Hooke's Law, $F = kx$, where k is the spring constant (N/m) and x is the deflection distance (m). Setting these forces equal to each other gives the force balancing equation for this system:

$$kx = \frac{1}{2}\frac{\varepsilon_0 AV^2}{(d-x)^2} \qquad (N) \tag{2.12}$$

Solving equation 2.12 for Voltage (V), provides a useful relationship for determining the voltage vs. deflection of a flat plate actuator:

$$V = \sqrt{\frac{2kx}{\varepsilon_0 A}}\,(x-d) \qquad (V) \tag{2.13}$$

Equation 2.13 relies on the accurate calculation of the spring constant k, which can be tricky due to the number of variables involved. The spring constant is determined by a combination of mechanical and material characteristics, such as the width, thickness, and length of the flexures, and the characteristics of the flexure material. While the geometry of any device can be accurately described, the mechanical properties of the flexure material can be a source of uncertainty. The elastic modulus, or Young's modulus (E) of thin film gold (Au) is reported to be 79 GPa [9], and more recently in the range 53-55 GPa [6]. The yield stress for 1.0 μm thick gold flexures with widths of 2.5, 5, and 10 μm was found to vary from 90 to 55 MPa, with yield stress decreasing as width increases [6]. All of this uncertainty in material characteristics leads to error when calculating the electrostatic response of MEMS devices.

In order to find an analytic solution for the spring constant, the four flexures can be modeled as rigid beams with a single fixed end as shown in figure 2.5.

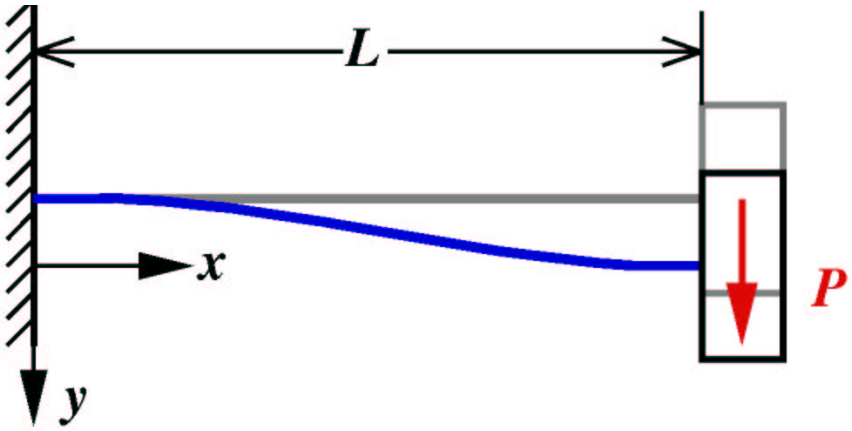


Figure 2.5 Deflection of a flexure beam with a single fixed end [22].

This is a simple problem described by the second-order linear differential equation [2]:

$$\frac{d^2y}{dx^2} = \frac{M(x)}{EI} \qquad (unitless) \tag{2.14}$$

where E is Young's modulus (Pa), and I is the moment of inertia (m^4). Together, EI is known as the 'flexural rigidity' of the beam. M(x) represents the bending moment (Nm^2), and for this case is simply applied force (F) times the distance (x). Integrating this equation twice and applying the appropriate boundary conditions results in an expression relating beam deflection y to force:

$$y = -\frac{FL^3}{12EI} \qquad (m) \tag{2.15}$$

Finally, the moment of inertia (I) for a rectangular beam is defined as [2]:

$$I = \int_{-\frac{h}{2}}^{\frac{h}{2}} dy \int_{-\frac{w}{2}}^{\frac{w}{2}} x^2 dx = \frac{hw^3}{12} \qquad (m^4) \tag{2.16}$$

giving the final equation relating force (F) to distance (y) as:

$$y = -\frac{FL^3}{16Ehw^3} \qquad (m) \tag{2.17}$$

where h is the thickness of the beam (m), w is the width of the beam (m), and L is the length of the beam (m).

Now plugging equation 2.17 back into Hooke's law ($x = F/k$), and remembering the force is spread evenly between four flexures, the spring constant k is given as:

$$k = \frac{4Ehw^3}{L^3} \qquad (N/m) \tag{2.18}$$

Note this is a simplified solution for k which doesn't take into consideration the spring constant due to residual material stress. The equation for k is placed into equation 2.13, resulting in an analytic solution for voltage vs. deflection

$$V = \sqrt{\frac{L^3 x}{2Ehw^3 \varepsilon_0 A}}(x - d) \qquad (V) \tag{2.19}$$

Experiments have shown [4] that equation 2.19 is accurate within a few percent of measured results, and is certainly a good approximation for initial design purposes. Figure 2.6 shows the resulting Voltage vs. displacement curve for a 150 μm $\times$ 150 μm piston micromirror with four 150 μm flexures, and a 2 μm starting airgap. For this simulation the flexure material is 1 μm thick gold (Au) with a Young's modulus of $E = 79\ GPa$. A key feature of figure 2.6 is the expected "snap-down" of the mirror at 1/3 of the airgap distance. This occurs when the exponentially increasing electrostatic force overwhelms the linear spring force and the top electrode snaps into contact with the surface.

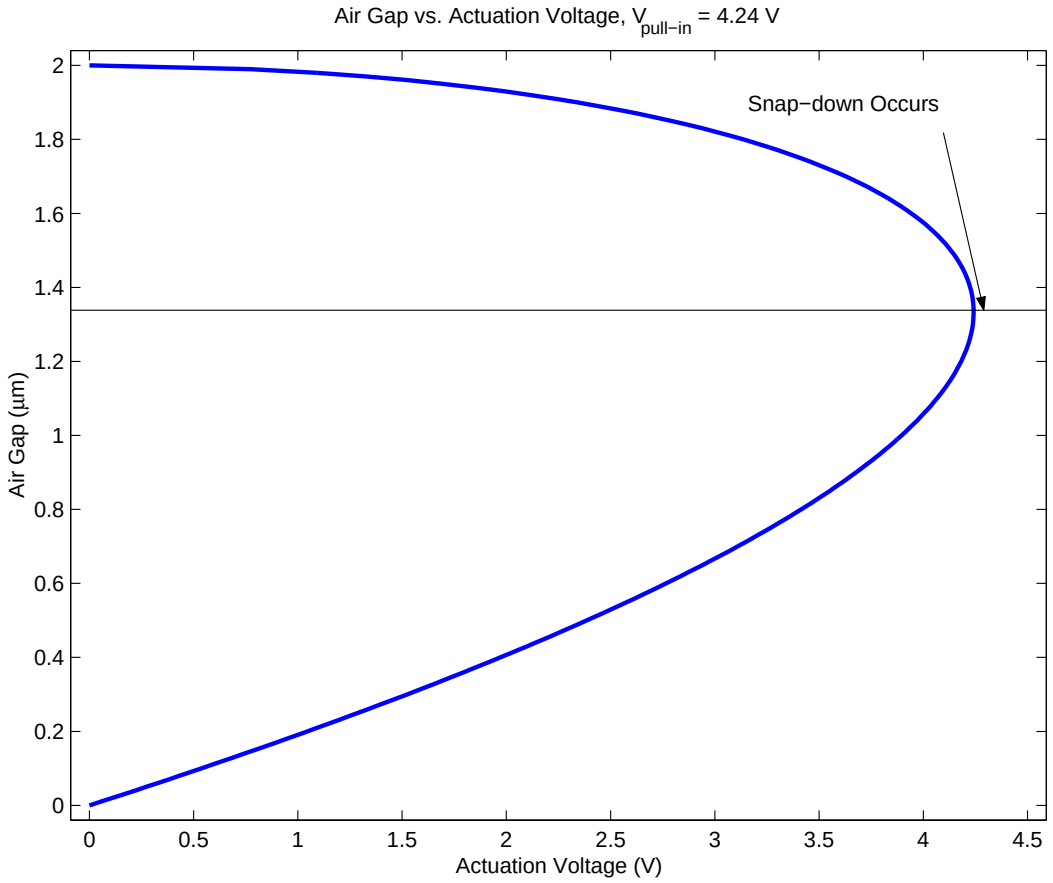


Figure 2.6 Calculated voltage vs. deflection for a 150 μm $\times$ 150 μm mirror with four 150 μm flexures, and a 2 μm starting airgap. The flexure material is 1 μm thick gold (Au) with $E = 79\ GPa$. Note that this piston mirror is expected to "snap-down" to the substrate after deflecting 1/3 of the airgap distance. Snap down voltage (4.2 V as shown) is the figure of merit determined from this calculation.

2.4 VCSEL Design

Many details of VCSEL design will not be discussed in this document since the focus of this research is the fabrication and integration of the mechanical portion of the tunable VCSEL structure. Instead, a brief overview is presented.

2.4.1 Fabry-Perot Etalon. The Fabry-Perot etalon consists of two semi-transparent parallel flat plates separated by some distance d and aligned to a high degree of accuracy. As shown in figure 2.7, light-rays are reflected back and forth

between the mirrored surfaces, but at each reflection a small fraction of the light is transmitted.

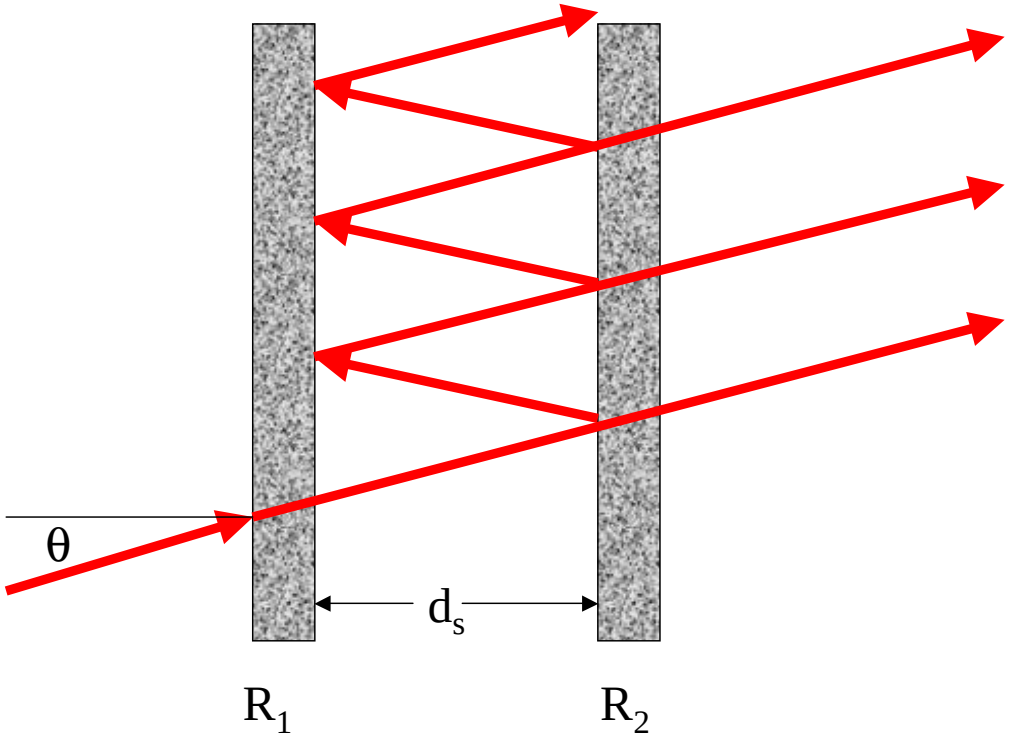


Figure 2.7 Basic Fabry-Perot etalon structure. Light rays that are only slightly inclined eventually escape. Rays will also escape if the mirrors are not perfectly parallel.

The optical path length between each successive transmitted ray is $2nd$, which leads to a phase shift between successive rays of

$$\delta = \frac{4\pi nd}{\lambda} \qquad (radians) \tag{2.20}$$

If $\delta = 2\pi$ then all the transmitted waves are in phase and they interfere constructively. If $\delta = \pi$, each pair of waves is in phase and destructive interference occurs. If the plates are highly reflective, the intensity of the ray trapped in the cavity decreases little between reflections and the transmitted waves have almost zero

intensity. However, if the phase shift is $\pi/2$, the first transmitted ray will interfere destructively with the 3rd, and the 2nd with the 4th, and so on. For very highly reflecting plates, only waves for which $\delta = 2\pi$ can be transmitted.

For real mirrors with a finite reflectivity, it can be shown [16] that transmitted intensity (I_t) as fraction of incident intensity (I_i) is given by

$$\frac{I_t}{I_i} = \frac{1}{1 + \left(\frac{2r}{1-r^2}\right)^2 \sin^2\left(\frac{\delta}{2}\right)} \qquad (unitless) \tag{2.21}$$

where r is the fraction of the amplitude of the wave that is reflected at each boundary. The unitless factor $F = \left(\frac{2r}{1-r^2}\right)^2$ is known as the Finesse [7]. The larger the Finesse, the sharper the peak around $\delta = 2\pi$.

Figure 2.8 shows the resonant transmission frequencies of the cavity separated by the Free Spectral Range (FSR) of the optical cavity which is given by

$$\nu_F = \frac{c}{2d} \qquad (Hz) \tag{2.22}$$

where $c = c_o/n$ is the speed of light through the cavity medium. If the cavity was a perfect lossless resonator with a $Finesse = \infty$, each peak would be a delta function. Since real optical resonators experience some loss, the peaks are spread out with a full-width-at-half-maximum (FWHM) given by [7]

$$\delta\nu = \frac{c(1-r)}{2\pi d\sqrt{r}} = \frac{\nu_F}{F} \qquad (Hz) \tag{2.23}$$

2.4.2 Resonator Cavity Losses. There are two principle sources of loss in optical resonator cavities: the losses due to absorption and scattering of the medium between the mirrors, and losses arising from imperfect reflection of the mirrors [16]. The various cavity losses can be combined into a single absorption coefficient α_s. The round-trip power attenuation factor due to the optical cavity of thickness d is

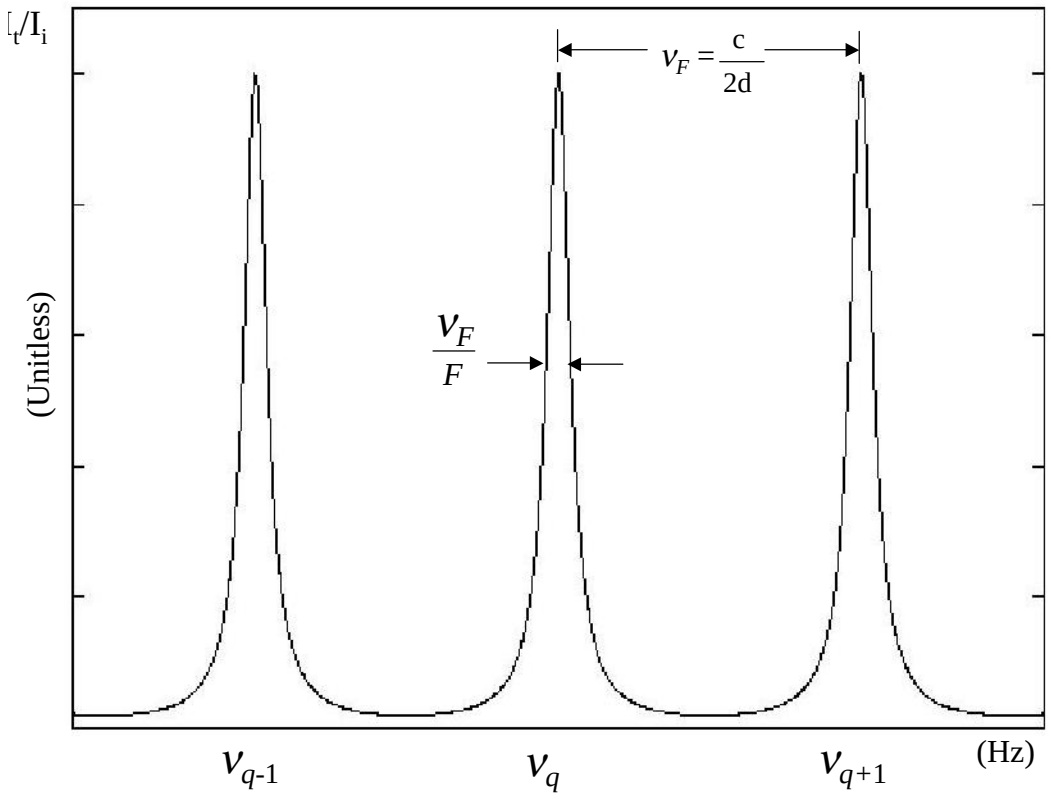


Figure 2.8 Transmission spectra of a Fabry-Perot resonant cavity showing three peaks separated by the Free Spectral Range (ν_F).

then given by $e^{-2\alpha_s d}$. The losses due to the imperfect mirrors are represented by the mirror reflectances $\Re_1$ and $\Re_2$. The complete round-trip attenuation factor including all sources of loss becomes

$$r^2 = \Re_1 \Re_2 e^{-2\alpha_s d} \qquad (unitless) \tag{2.24}$$

or more commonly

$$r^2 = e^{-2\alpha_r d} \qquad (unitless) \tag{2.25}$$

The overall loss coefficient can be written as

$$\alpha_r = \alpha_s + \alpha_{m1} + \alpha_{m2} \qquad (cm^{-1}) \tag{2.26}$$

where

$$\alpha_{m1} = \frac{1}{2d} ln \frac{1}{\Re_1} \qquad (cm^{-1}) \tag{2.27}$$

and

$$\alpha_{m2} = \frac{1}{2d} ln \frac{1}{\Re_2} \qquad (cm^{-1}) \tag{2.28}$$

The terms α_{m1} and α_{m2} are the loss coefficients due to mirrors 1 and 2. Finally, the finesse of the cavity is now given by the relation

$$F = \frac{\pi e^{\frac{-\alpha d}{2}}}{1 - e^{-\alpha d}} \qquad (unitless) \tag{2.29}$$

2.4.3 Distributed Bragg Reflectors. For the purposes of my research, the mirrors utilized to form resonant cavities are constructed of precisely grown multi-layered semiconductor or dielectric materials. Mirrors of this type are known as distributed Bragg reflectors (DBRs). As shown in figure 2.9, DBR mirrors are periodic structures consisting of alternating quarter-wave ($\lambda/4$) layers of low and high refractive index materials. The term quarter-wave refers to the optical thickness of each layer, and corresponds to a physical thickness $d = \lambda_o/4n$ for non-absorbing material, where n is the real refractive index of the layer [11].

Reflectance greater than 99.9% (at the design wavelength λ_o) can be obtained from a quarter-wave mirror stack. The magnitude of the reflectance is determined by the ratio of high and low index of refraction, and the number of quarter-wave periods in the stack (one period is one set of low-high $\lambda/4$ pairs). The reflectance of the stack shown in figure 2.9, at the design wavelength (λ_o), and assuming normal incidence and no absorption is given by [12]

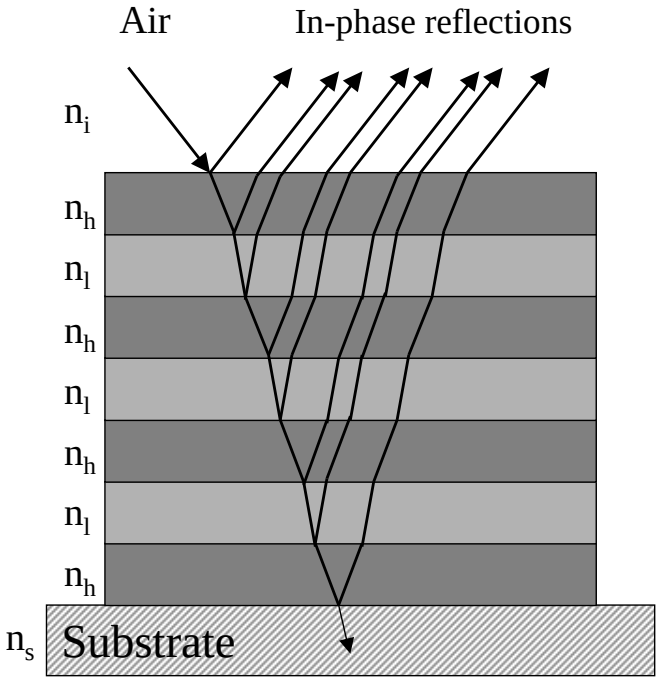


Figure 2.9 Schematic of a basic DBR structure of the form HLHLHLH [7].

$$R_{2p+1} = \left(\frac{1 - (n_h/n_l)^{2p}(n_h/n_i)(n_h/n_s)}{1 + (n_h/n_l)^{2p}(n_h/n_i)(n_h/n_s)} \right)^2 \qquad (unitless) \qquad (2.30)$$

where p is the number of periods in the stack, and n_h, n_l, n_i and n_s are the high, low, incident and substrate indices of refraction, respectively. Equation 2.30 only holds true for a stack consisting of an odd number of quarter-wave layers, such as HLHL...HLH, or if the high and low layers are switched, LHLH...LHL. The reflectance of a stack consisting of even numbers of the high and low layers, such as HLHL....HL or LHLH...LH is given by [11]

$$R_{2p} = \left(\frac{1 - (n_h/n_l)^{2p}(n_s/n_i)}{1 + (n_h/n_l)^{2p}(n_s/n_i)} \right)^2 \qquad (unitless) \qquad (2.31)$$

Equation 2.30 and equation 2.31 are quick methods for determining the theoretical reflectance of a quarter-wave stack, but they don't take into account losses due to absorption as light passes through the stack materials. Nor do they allow for

variations in layer thickness or material composition, or light incident at any angle other than perpendicular to the surface. A more robust method for calculating reflectance uses a characteristic 2×2 matrix to describe each layer of the quarter-wave stack. The characteristic matrix $[M]$ for an arbitrary layer is [12]

$$[M] = \begin{bmatrix} \cos\delta & (i\sin\delta)/\eta_r \\ i\eta_r \sin\delta & \cos\delta \end{bmatrix} \tag{2.32}$$

where δ is the optical thickness of a the given layer

$$\delta = \frac{2\pi N d \cos\theta}{\lambda} \qquad (radians) \tag{2.33}$$

N is the complex refractive index ($N = n - ik$) of the layer and η_r is the tilted optical admittance which varies for each layer depending on the polarization of the electric field and the value of N. For p-waves η_r is given by

$$\eta_p = \frac{N\gamma}{\cos\theta} \qquad (Siemens) \tag{2.34}$$

and for s-waves

$$\eta_s = N\gamma\cos\theta \qquad (Siemens) \tag{2.35}$$

The free space optical admittance has the value $\gamma = 2.6544 \times 10^{-3}\ S$ (Siemens), and θ is the angle of incidence of the incoming light with respect to the surface normal (radians).

A 1×2 matrix representing the entire DBR stack is obtained by multiplying the individual characteristic matrices (Note that the order of multiplication is important)

$$\begin{bmatrix} B \\ C \end{bmatrix} = [M_1][M_2]...[M_q] \begin{bmatrix} 1 \\ \eta_m \end{bmatrix} \tag{2.36}$$

where η_m is the substrate admittance, and the matrix elements B and C are used to calculate the power reflectance, power transmittance, power absorptance, and reflectivity phase as given by

$$R = \left(\frac{\eta_o B - C}{\eta_o B + C}\right)\left(\frac{\eta_o B - C}{\eta_o B + C}\right)^* \qquad (unitless) \tag{2.37}$$

$$T = \frac{4\eta_o Re(\eta_m)}{(\eta_o B + C)(\eta_o B + C)^*} \qquad (unitless) \tag{2.38}$$

$$A = \frac{4\eta_o Re(BC^* - \eta_m)}{(\eta_o B + C)(\eta_o B + C)^*} \qquad (unitless) \tag{2.39}$$

$$\psi = \arctan\left(\frac{Im[\eta_m(BC^* - CB^*)]}{(\eta_m^2 BB^* - CC^*)}\right) \qquad (radians) \tag{2.40}$$

This method is time consuming and impractical if solving a large stack equation by hand, but is optimized for numerical stack calculations by a computer. Using a computer, it is a simple matter to calculate the reflectance of a large DBR stack across a broad range of wavelengths. I accomplished this calculation for a semiconductor DBR with 31 pairs of alternating quarter wave layers of gallium arsenide (GaAs) and aluminum arsenide (AlAs), as shown in figure 2.10. This DBR stack has a design wavelength of $\lambda_o = 980\ nm$.

Traditionally, VCSEL devices have utilized semiconductor DBR mirror stacks to obtain the power reflectance needed for lasing. Dielectric DBRs offer several advantages over semiconductor DBRs. The index of refraction of dielectric materials ranges anywhere from $n = 1.45$ for silicon oxide (SiO_2) to $n = 3.0$ for titanium oxide (TiO_2). Since the magnitude of the power reflectance (R) increases with the ratio of n_h/n_l (as shown by equation 2.30), fewer dielectric periods are required to achieve the same power reflectance as a semiconductor DBR stack. Fig-

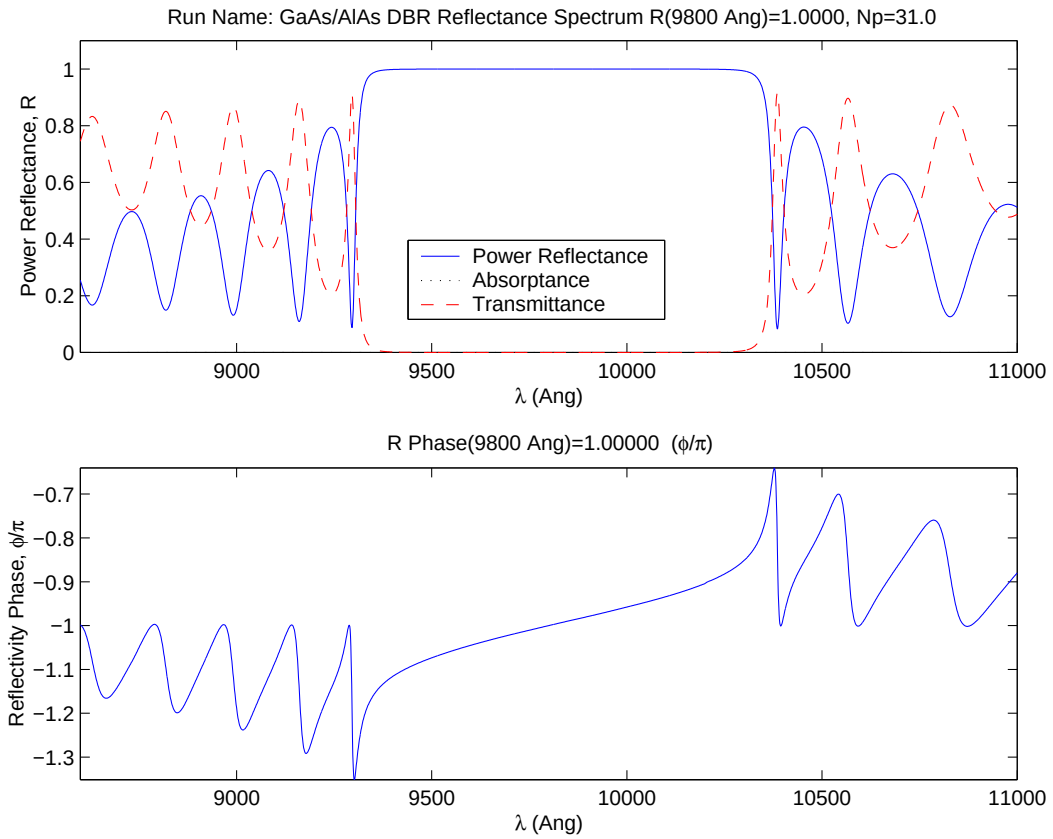
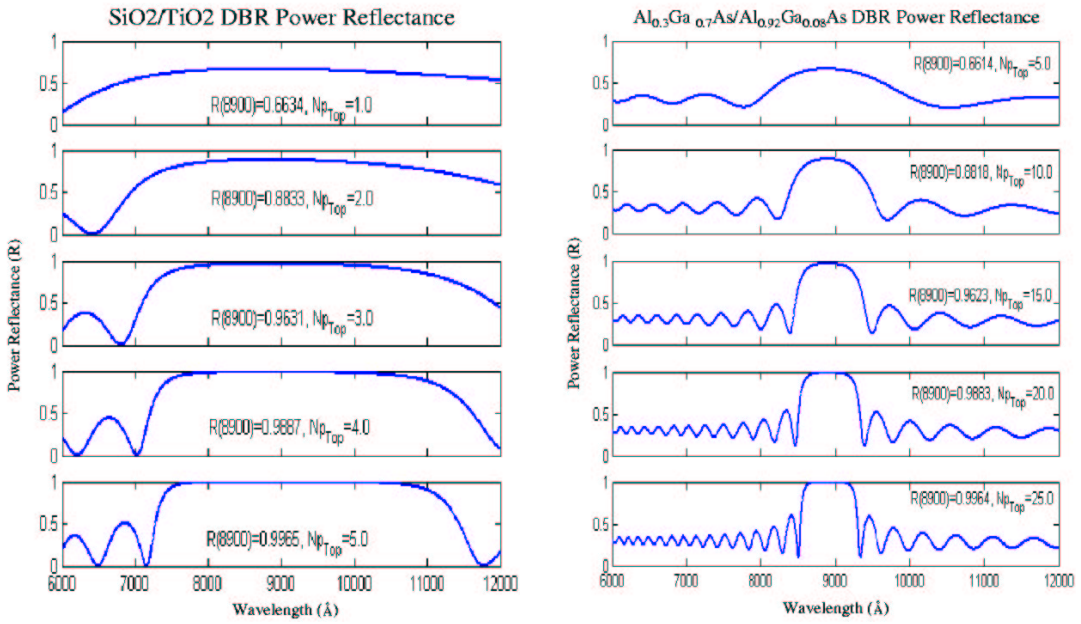


Figure 2.10 Power reflectance and reflectivity phase plots of a 31 period GaAs/AlAs quarter-wave DBR stack on a GaAs substrate. The design wavelength is $\lambda_o = 980\ nm$.

ure 2.11 compares the number of dielectric DBR periods to semiconductor periods in order to achieve a given reflectance. In this case, it requires five times as many $Al_{0.3}Ga_{0.7}As/Al_{0.92}Ga_{0.08}As$ semiconductor periods to match the reflectance of a SiO_2/TiO_2 dielectric stack.

In addition, as the index remains stable over a wide range of frequencies (see figure C.11) and fewer layers are required, dielectric DBR's allow for a much larger frequency bandwidth. Semiconductor DBR stacks are crystalline in nature, and must be epitaxially grown, monolayer by monolayer. Dielectric DBR's, on the other hand, are composed of amorphous materials, and can be applied using techniques such as reactive sputtering or plasma enhanced chemical vapor deposition (PECVD,

as discussed in Appendix C. Since the index of refraction is low (1.45 to 3.0), the dielectric quarter-wave layers are thick compared to their semiconductor counterparts, providing them a higher tolerance to errors in deposited layer thickness.



(a) **(b)**

Figure 2.11 Comparison of the number of (a) dielectric DBR periods to (b) semiconductor periods in order to achieve a given power reflectance. This example was calculated using a SiO_2/TiO_2 dielectric stack, and an $Al_{0.3}Ga_{0.7}As/Al_{0.92}Ga_{0.08}As$ semiconductor quarter-wave stack, both on a GaAs substrate. It requires five times as many semiconductor periods to match the reflectance of this dielectric stack. In addition, note the large bandwidth of the dielectric DBR.

2.4.4 Resonant Periodic Gain. When resonance occurs within a high finesse optical cavity, an electromagnetic standing wave is formed by overlapping counter-propagating waves, as shown in figure 2.12. The accurate placement of this standing wave is critical for VCSEL operation, and is determined by the design of the microcavity and the DBR mirrors.

A numerical calculation of the standing wave can be accomplished using the transfer matrix approach [24]. A series of 2×2 propagation (P) and dynamical (D)

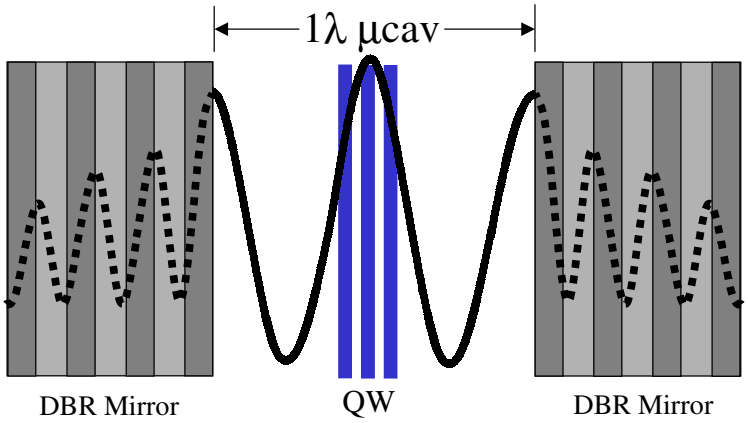


Figure 2.12 Resonant electromagnetic standing wave in 1λ optical cavity resulting from counter-propagating waves between the highly reflective DBR mirrors. Since the DBR is not a perfect mirror at the cavity interface, phase penetration of wave into the DBR stack occurs. The peak antinode of this standing wave overlaps the active gain region.

matrices are used to represent the incident and reflected electric field vectors at each material interface. The incident and reflected fields on opposite sides of the material stack can be related by [11]

$$\begin{pmatrix} E_o^+ \\ E_o^- \end{pmatrix} = \begin{pmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{pmatrix} \begin{pmatrix} E_s^+ \\ E_s^- \end{pmatrix} \tag{2.41}$$

where the transfer matrix M for the entire stack is

$$\begin{pmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{pmatrix} = D_o^{-1}[\prod_{L=1}^{N} D_L P_L D_L^{-1}] D_s \tag{2.42}$$

and L is the layer number (0,1,2,...,N,s). At normal incidence, the two dynamical matrices for any layer of the stack L are given by

$$D_L = \begin{pmatrix} 1 & 1 \\ N_L & -N_L \end{pmatrix} \tag{2.43}$$

and

$$D_L^{-1} = \frac{1}{2}\begin{pmatrix} 1 & \frac{1}{N_L} \\ 1 & -\frac{1}{N_L} \end{pmatrix} \tag{2.44}$$

where N_L is the complex index of refraction for layer L. The propagation matrix for each layer P_L is given by [11]

$$P_L = \begin{pmatrix} e^{i\varphi_L} & 0 \\ 0 & e^{-i\varphi_L} \end{pmatrix} \tag{2.45}$$

where

$$\varphi_L = k_{Lx} d_L \tag{2.46}$$

and

$$k_{Lx} = N_L \frac{\omega}{c_o} = N_L \frac{2\pi}{\lambda_o} \tag{2.47}$$

and d_L is the thickness of layer L and k_{Lx} is the x component of the wave vector. The electric field amplitude through the structure is then given by [11]

$$E(x) = \begin{cases} E_o^+ e^{-ik_{ox}(x-x_o)} + E_o^- e^{ik_{ox}(x-x_o)} & : \quad x < x_o \\ E_L^+ e^{-ik_{Lx}(x-x_L)} + E_L^- e^{ik_{Lx}(x-x_L)} & : \quad x_{L-1} < x < x_L \\ E_s^+ e^{-ik_{sx}(x-x_t)} + E_s^- e^{ik_{sx}(x-x_t)} & : \quad x_t < x \end{cases} \tag{2.48}$$

From equation 2.41, the reflectivity coefficient (ρ) when $E_s^- = 0$ is given by

$$\rho = \frac{M_{21}}{M_{11}} \tag{2.49}$$

This method is flexible, and may be used to model the standing wave for any given material stack configuration. It has been implemented as a numerical toolkit for the MATLAB® programming environment [13], and is used extensively in Chapter III.

The active gain material of a VCSEL is confined to an narrow quantum well, typically on the order of 60 Å to 100 Å-thick. A net optical gain only occurs when the value of the standing wave in the quantum well is greater than zero, and an electromagnetic field is present to stimulate the gain medium. By placing the active material at the antinode (peak) of the optical standing wave it is possible to maximize the effective optical gain [15]. A misplacement of the gain material at the nodes of the standing wave results in zero net gain, and therefore no lasing. Figure 2.13 shows the calculated standing wave for a typical 980 nm all-semiconductor VCSEL device. The antinode of the wave overlaps the quantum wells at the resonant wavelength of $\lambda_o = 980\ nm$.

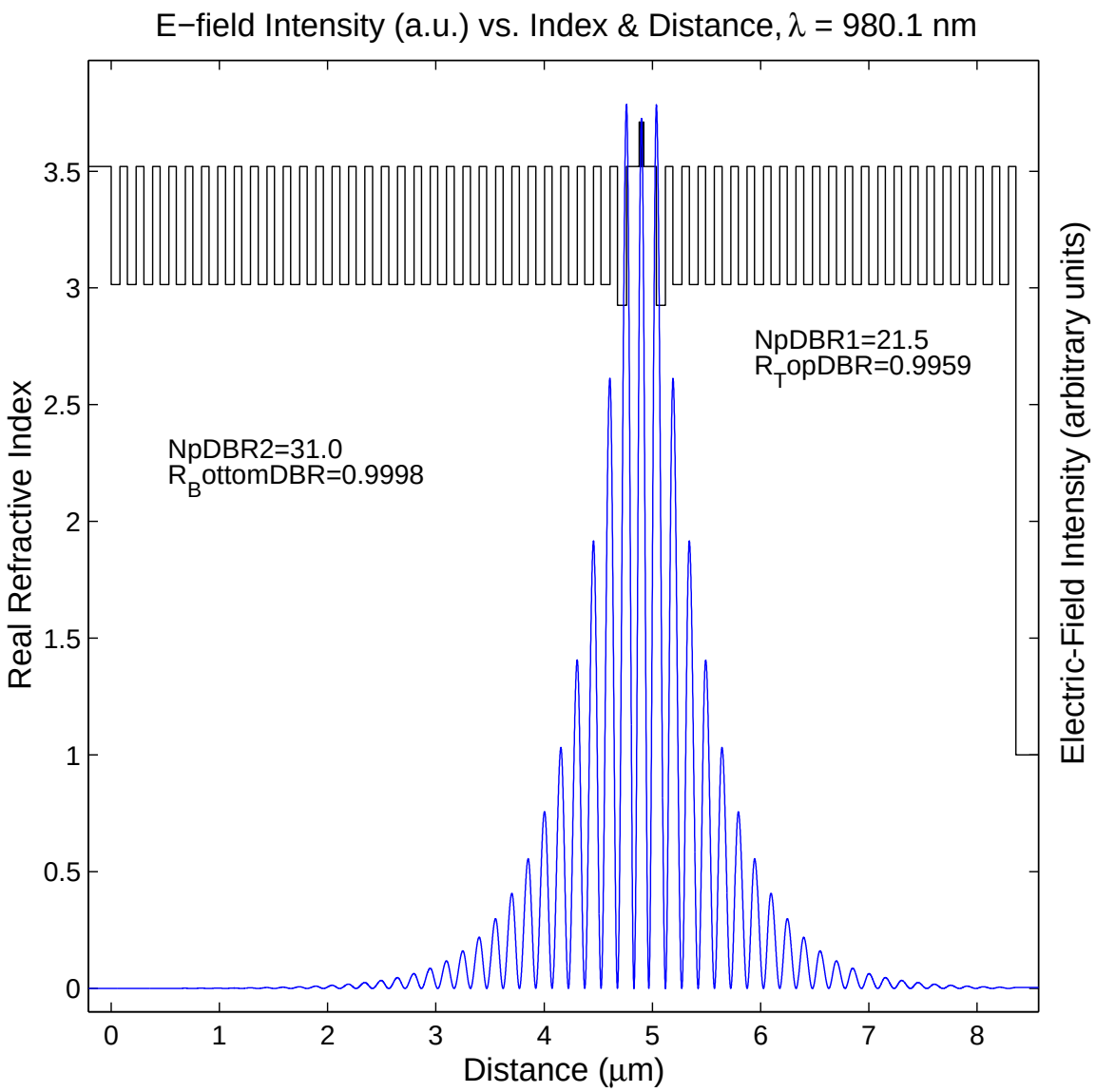


Figure 2.13 Calculated electromagnetic standing wave for 1λ optical cavity with 99.9% reflective semiconductor DBR mirrors. The peak antinode of this standing wave overlaps the active gain region of the VCSEL.

2.4.5 VCSEL Threshold Conditions. In this section I discuss the requirements for a VCSEL to reach minimum lasing threshold conditions. The model presented is simplified and doesn't take into account many of the loss mechanisms present in the optical cavity. These losses will drive up threshold gain requirements. In general, the threshold equation for a VCSEL is given as [15]

$$\int_{L_{cav}} F(z) g_{th}(z) dz = \frac{1}{2\Gamma_t} \ln\left(\frac{1}{R_1 R_2}\right) \tag{2.50}$$

where g_{th} is the gain at threshold along the direction of the cavity z (cm^{-1}), L_{cav} is the cavity length (m), R_1 and R_2 are the reflectivities of the mirrors, Γ_t is the transverse confinement factor of the lasing mode within the active area and F(z) is the normalized magnitude of the optical standing wave given by [15]

$$F(z) = \frac{L_{cav}|E_{xy}(z)|^2}{\int_{L_{cav}} |E_{xy}(z)|^2 dz} \tag{2.51}$$

and $E_{xy}(z)$ is the standing wave electric field perpendicular to the cavity axis z.

If the transverse dimension of the VCSEL gain region is much larger than the lasing wavelength, the confinement factor Γ_t approaches 1.0. Assuming the gain per pass through the cavity is small ($\ll 1$), equation 2.50 becomes [15]

$$\Gamma_L g_{th} N d_{qw} \approx \alpha_{cav} L + \frac{1}{2\Gamma_t}(1 - R_1 R_2) \tag{2.52}$$

where N is the number of active quantum wells of thickness d_{qw} (m) with gain g_{th} (cm^{-1}) at threshold. α_{cav} (cm^{-1}) is the absorption coefficient throughout the remainder of the cavity material with length L. The longitudinal confinement factor Γ_L ($0 \leq \Gamma_L \leq 2$) is determined by the placement of the quantum wells with respect to the optical standing wave. If the quantum wells are centered at the peak antinode of the wave, then Γ_L approaches 2 [15].

2.4.6 Tunable VCSEL. The tuning range of a MEM tunable VCSEL (MTV) is determined by the smallest of three factors [3]: the wavelength variation due to maximum deflection of the top mirror, the minimum free spectral range (FSR) of the Fabry-Perot etalon, or the bandwidth of the active gain region.

The maximum deflection of the top mirror is determined by the mechanical and material characteristics of the MEM structure, and is typically 1/3 of the airgap height as shown in figure 2.6. At this point the attractive electrostatic force can no longer be balanced by the mechanical spring force of the flexures holding up the mirror. This results in the collapse of the mirror membrane onto the substrate.

In order to achieve a maximum tuning range, it appears that increasing the airgap returns the best results. Unfortunately, a larger airgap means a longer cavity length which results in a narrow FSR, and therefore a shorter tuning range. To achieve a maximum tuning range these two parameters must be optimized. Figure 2.14 shows the calculated resonant frequency for a MEMS tunable VCSEL device using 9.5 pairs of quarter-wave Si_3N_4/SiO_2 as the top DBR mirror. The optimum tuning range chosen for my research occurs with an airgap thickness centered at 17150 Å. This airgap provides enough space between the membrane and substrate to reduce the possibility of snap-down while still providing a wide tuning range of 35.9 nm (centered at $\lambda = 980$ nm).

The active gain material used for this research project is $In_{0.2}Ga_{0.8}As$ with a GaAs cladding. An optimal QW thickness of 80 Å has been determined experimentally for lasing at 980 nm [5]. Gain bandwidth calculations for this QW configuration have been calculated elsewhere [11]. Figure 2.15 shows the calculated gain bandwidth spectra for an 80 Å $In_{0.2}Ga_{0.8}As$ QW at multiple carrier densities.

Selecting a minimum gain threshold of $g_{th} = 500$ cm^{-1}, the gain bandwidth, as shown in figure 2.15, stretches from 950 nm to 1010 nm. The calculated tuning range due to airgap deflection is from 960 nm to 996 nm. Therefore, the FSR of this device is the limiting factor.

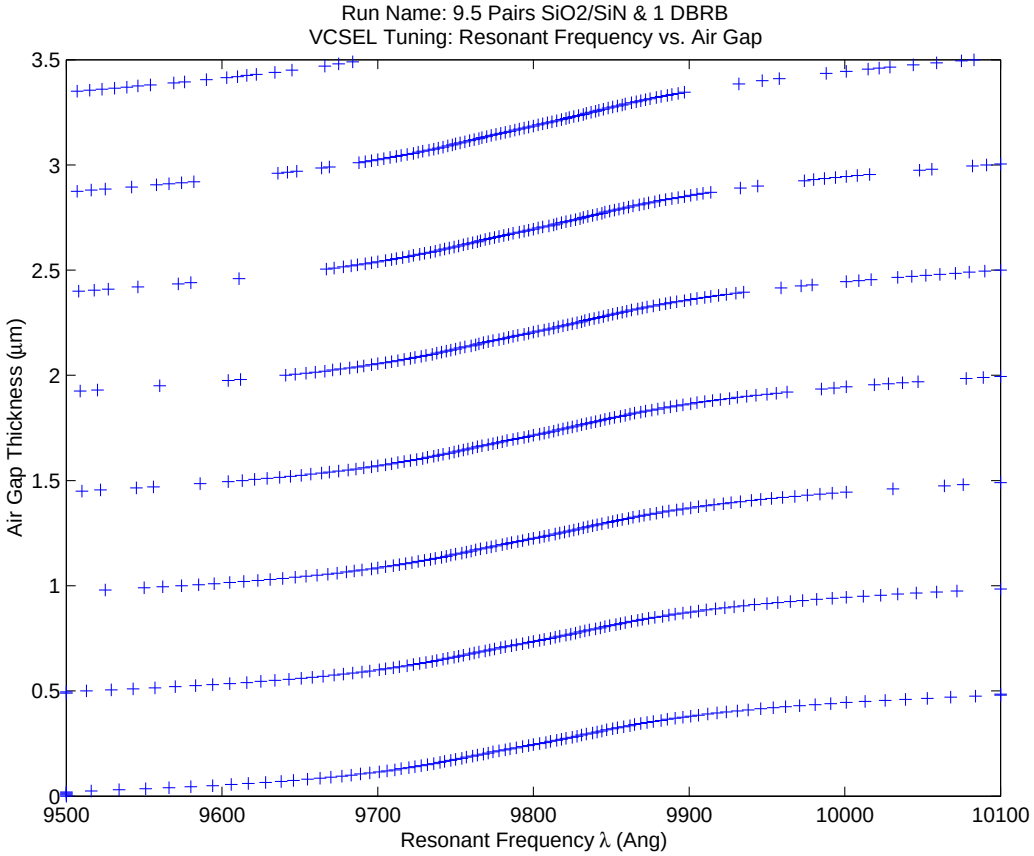


Figure 2.14 Calculated resonant frequency vs. airgap thickness of a MEM tunable VCSEL device with a Si_3N_4/SiO_2 top DBR mirror.

2.5 Current Research

Several research groups have demonstrated working tunable VCSEL devices utilizing MEM electrostatically actuated mechanical mirrors. These devices can be broken into three categories: cantilever VCSELs [3], membrane VCSEL devices [17] [10], and tunable VCSELs utilizing a half-symmetric cavity [20] [19] [21] [23]. Since this research effort is primarily concerned with VCSEL tuning utilizing electrostatically actuated membranes, this section concentrates on membrane and half-symmetric cavity devices. For more information on cantilever VCSELs, see the work of Chang-Hasnain et al. [3].

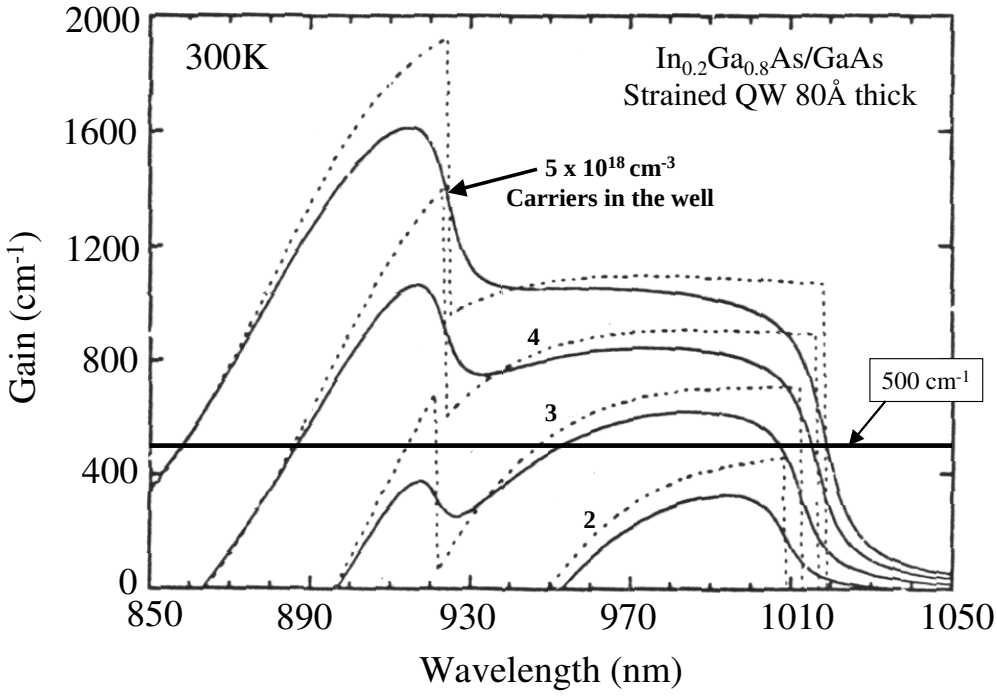
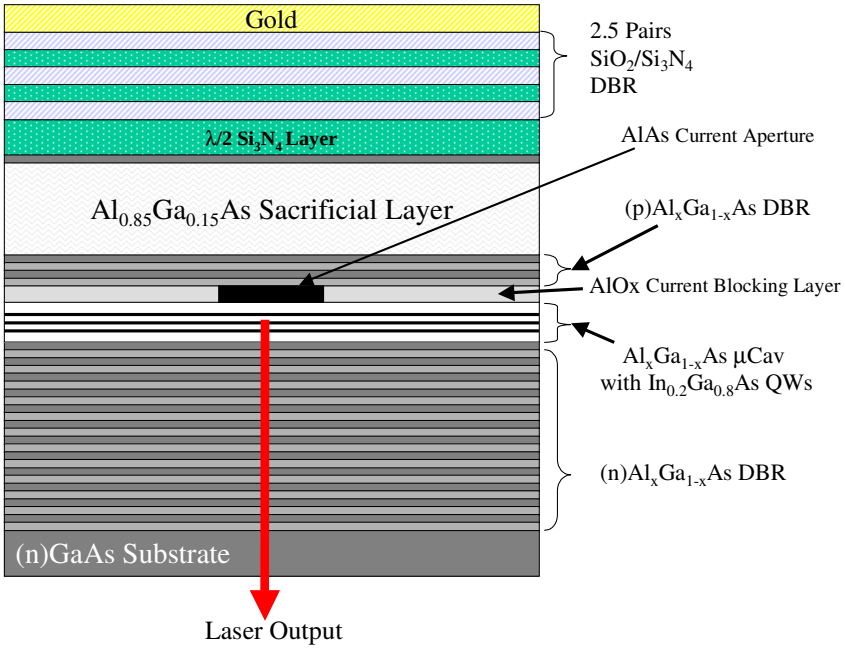


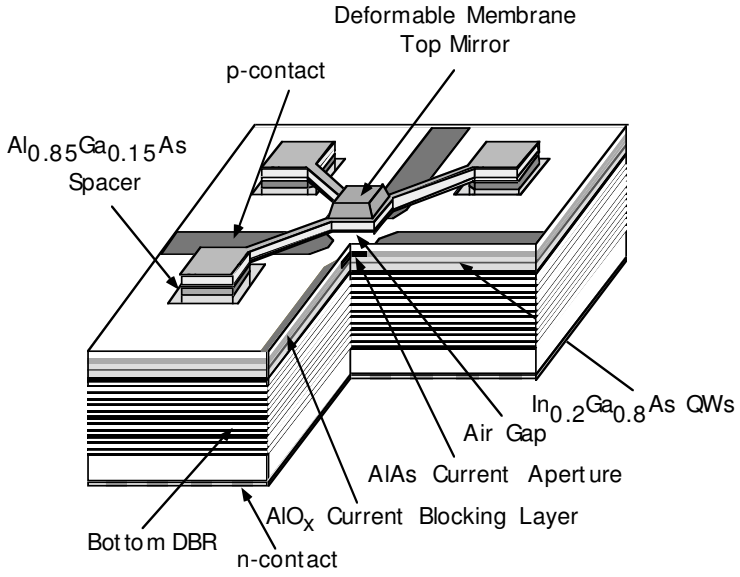
Figure 2.15 Calculated gain bandwidth spectra for 80 Å $In_{0.2}Ga_{0.8}As$ QW with multiple carrier densities [11]. Note the bandwidth range at $g_{th} = 500\ cm^{-1}$ is 950 nm to 1010 nm ($\Delta\lambda = 60\ nm$).

2.5.1 Membrane VCSEL Devices. A team of researchers at Stanford University successfully fabricated a series of micromachined tunable VCSEL devices lasing near 970 nm [17]. These lasers utilize a deformable membrane to vary the airgap and thus increase or decrease the cavity resonance. A schematic of the basic design is shown in figure 2.16.

The heterostructure, starting from the bottom n-doped GaAs substrate, includes an n-type aluminum gallium arsenide ($Al_xGa_{1-x}As$) DBR, an $Al_xGa_{1-x}As$ μcavity with indium gallium arsenide ($In_{0.2}Ga_{0.8}As$) quantum well active gain layers, a short (p)$Al_xGa_{1-x}As$ DBR section, an $Al_{0.85}Ga_{0.15}As$ sacrificial layer, and a top quarter-wave p-doped GaAs layer. After the completion of the epitaxial growth, a $\lambda/2$ Si_3N_4 optically inert layer is deposited, followed by 2.5 pairs of $\lambda/4$ SiO_2/Si_3N_4 dielectric layers to form the top DBR mirror. Figure 2.17 shows the step by step fabrication process which results in a MEM device.



(a)



(b)

Figure 2.16 Schematic diagrams of the Stanford MEM tunable VCSEL (a) pre-fabrication material cross section, and (b) completed device [17].

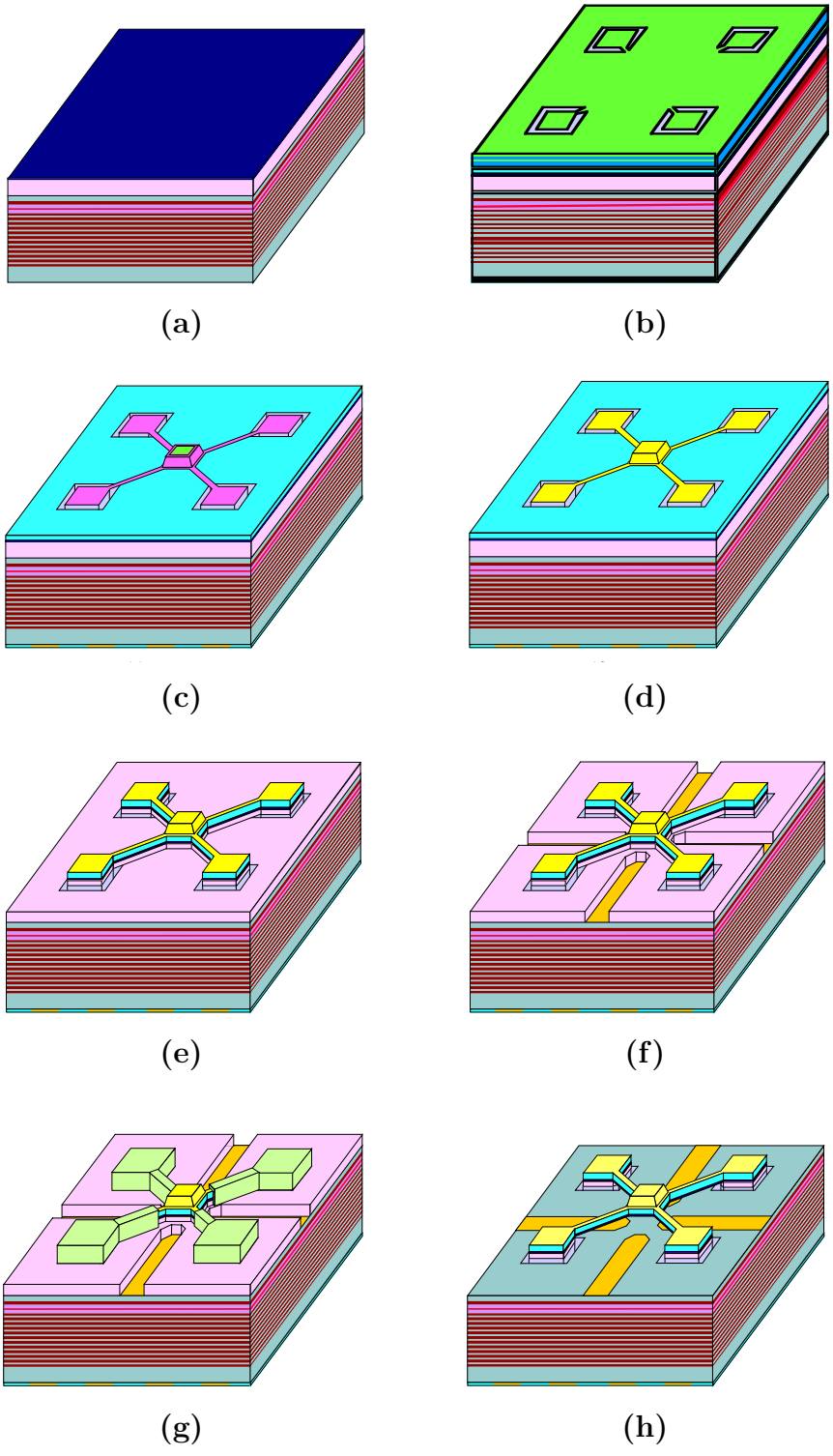


Figure 2.17 Step by step device fabrication schematic for Stanford MEMS tunable VCSEL [17].

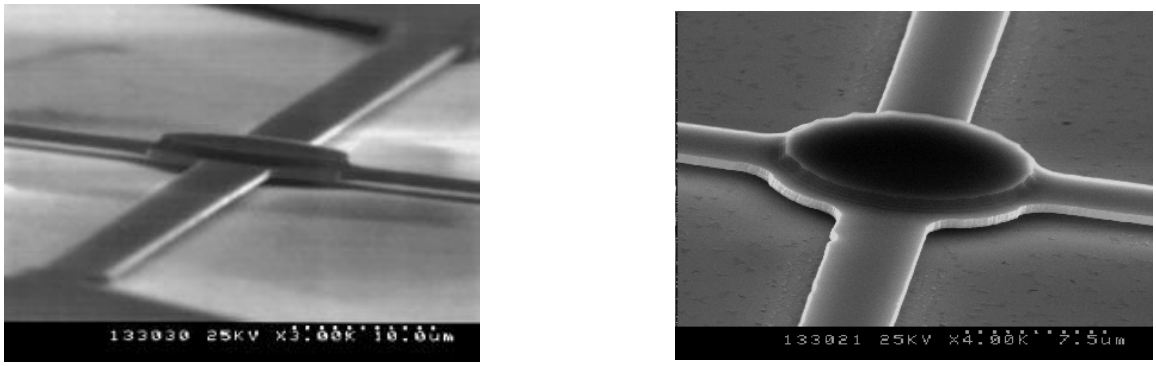
After deposition of the top DBR mirror, the wafer surface is wet etched, as shown in figure 2.17b, in an H_2SO_4 / H_2O_2 / H_2O (1:8:40) solution which patterns the Si_3N_4/SiO_2 and exposes a $\lambda/4$ AlAs layer directly above the μcavity. A VCSEL current aperture is formed by oxidizing the AlAs in saturated water vapor, which converts part of the AlAs to AlO_x. After completion of the oxidation step, the 2.5 pairs of dielectric DBR are patterned and RIE etched in a CHF_3O_2 plasma to create the central reflector region as shown in figure 2.17c. This etch is stopped just above the $\lambda/2$ Si_3N_4 layer in order to form the thin flexures attached to the central mirror. A thick layer of gold (Au) is then deposited, patterned, and etched (Figure 2.17d).

This layer of gold is used to increase the reflectivity of the central mirror, acts as a conductor for the electrostatic actuation of the device, and is used as a masking layer while etching the unwanted portions of the $\lambda/2$ Si_3N_4 and $Al_xGa_{1-x}As$ sacrificial layers. Masked by the gold layer, CHF_3O_2 RIE etches the Si_3N_4, and $BCl_3/Cl_2/Ar$ RIE etches through the $Al_{0.85}Ga_{0.15}As$ sacrificial layer (Figure 2.17e). All that's left is to add the intercavity contacts by wet etching the remaining $Al_xGa_{1-x}As$ sacrificial layer using diluted hydrochloric acid, which stops at the highly p-doped GaAs contact layer as shown in figure 2.17f.

Ohmic contacts are added with a lift-off process, and the remaining sacrificial $Al_xGa_{1-x}As$ is removed with hydrochloric acid to release the membrane (Figure 2.17h). SEM images of the completed device are shown in figure 2.18.

Laser emission from this device occurs out the bottom through the transparent GaAs substrate (at this wavelength). This membrane device has a tuning range of approximately 30 nm, with a central wavelength of 965 nm as shown in figure 2.19.

2.5.2 Half-Symmetric Cavity VCSEL Devices. A group of researchers at CoreTek Inc. [20] have developed a MEM tunable VCSEL device with a curved top mirror, giving the device a half-symmetric optical cavity. The curved top mirror is



(a) **(b)**

Figure 2.18 SEM images of completed membrane VCSEL device [21].

designed to match the Gaussian curvature of the light oscillating within the optical cavity. This creates a single fundamental spatial lasing mode.

Single mode operation is difficult to achieve in typical VCSEL devices due to their flat DBR mirrors. The large lateral area of the optical cavity allows the creation of multiple lasing modes. Single fundamental spatial mode operation in a VCSEL is usually achieved by shrinking the current injection area of the device, performing a lateral oxidation step, or by etching a narrow mesa formation until only a single lasing mode is allowed to oscillate within the cavity [20].

The device depicted in figure 2.20 consists of a bottom GaAs/AlAs DBR mirror grown on an n-type GaAs substrate. Since this device is designed to lase at 960 nm, the VCSEL active gain region consists of multiple $In_{0.2}Ga_{0.8}As$ quantum wells QW surrounded by $Al_xGa_{1-x}As$ cladding layers. Above the optical cavity several pairs of $Al_xGa_{1-x}As$ DBRs are grown for current spreading, and a 50 nm heavily doped p^+ $Al_xGa_{1-x}As$ layer is grown for ohmic contacts. A current aperture is then formed by etching away (150 nm deep) of the p^+ layer everywhere except a 20 μm diameter circle defining the lasing aperture. Before ohmic contacts are made, a dielectric layer of either Si_3N_4 or SiO_2 is deposited by PECVD for current isolation.

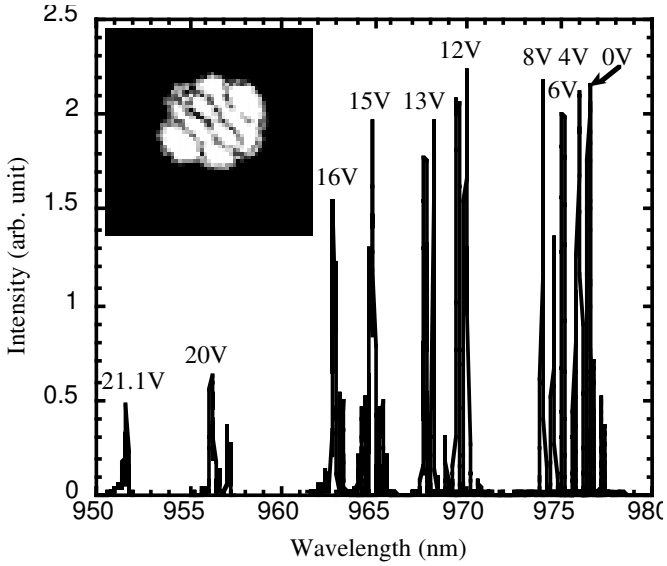


Figure 2.19 Membrane VCSEL lasing wavelength vs. tuning voltage. This device has an active tuning range of approximately 30 nm centered at 965 nm. [17].

Upon completion of these steps, a mechanical structure is fabricated to support a movable top DBR mirror [20]. A sacrificial layer of polyimide is first spun-on to define the airgap thickness of the device. The electrostatically actuated membrane is constructed from a 200 nm-thick layer of PECVD deposited silicon nitride followed by 100 nm of aluminum. These layers are then patterned and etched to define the top electrode and flexures. After post holes are etched into the sacrificial polyimide, thick aluminum posts are deposited to attach the device flexures to the substrate and support the structure. The top DBR mirror is constructed of 7.5 pairs of SiO_2/TiO_2 deposited by selective deposition at the center of the device. Finally the device is released by etching away the sacrificial polyimide. An SEM of the completed structure is shown in figure 2.21.

The CoreTek research team was able to tune this VCSEL device by applying a voltage to the top electrode. The tuning range of this laser was approximately 44 nm, centered at a wavelength of 950 nm. The max tuning voltage was 14 V (see figure 2.22).

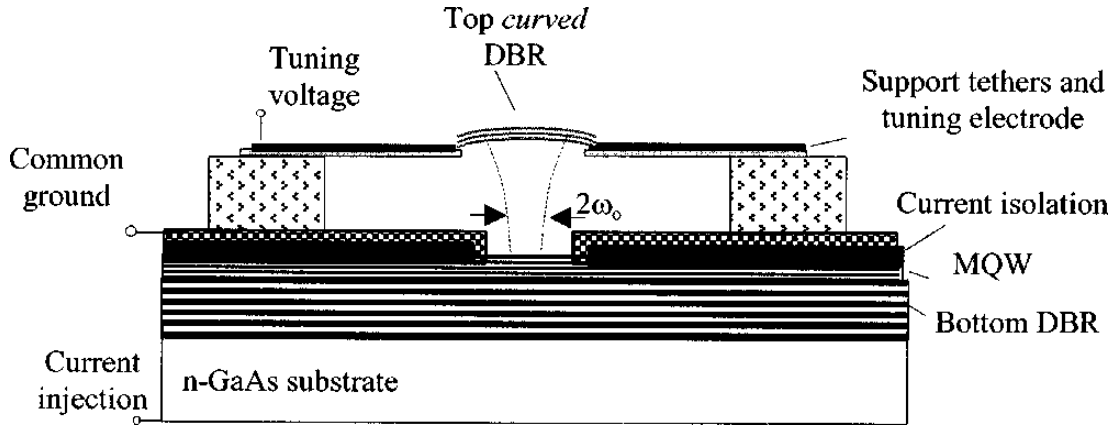


Figure 2.20 Schematic diagram of a Half-Symmetric Cavity tunable VCSEL device centered at 960 nm [21].

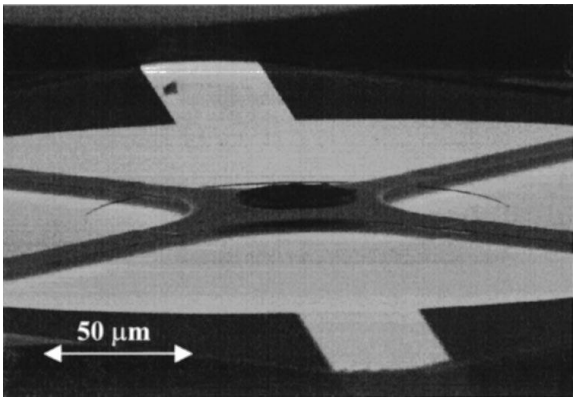
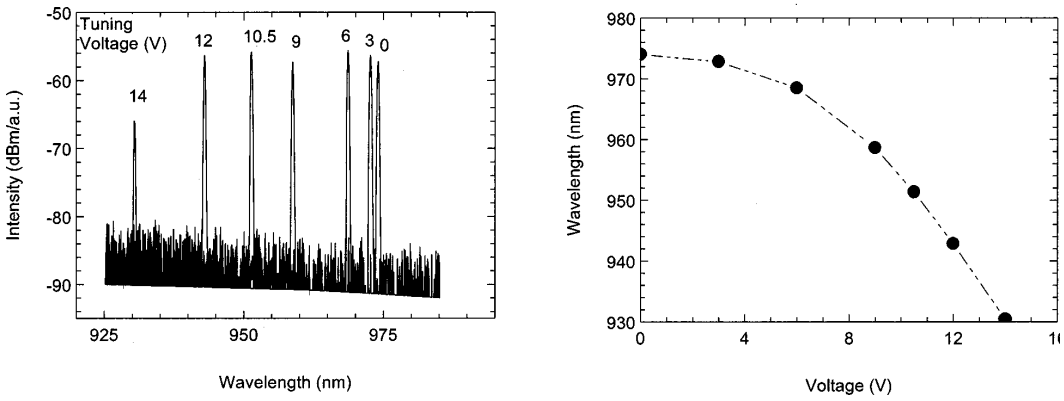


Figure 2.21 Scanning Electron Microscope image of a Half-Symmetric Cavity tunable VCSEL device centered at 960 nm [21].

2.6 Conclusion

In this chapter I presented background material relevant to my research objectives, I gave a brief overview of MEM device fabrication in section 2.2, followed by an analysis of the voltage vs. deflection characteristics of MEM piston micromirrors in section 2.3. I discussed the design of Fabry-Perot etalons and VCSELs in section 2.4. Finally, I reviewed the characteristics of tunable VCSELs in section 2.4.6, including current research detailing the design and fabrication of tunable VCSELs.



(a) **(b)**

Figure 2.22 Tuning spectra (a) and tuning curve (b) of the half-symmetric tunable VCSEL device centered at 960 nm [21].

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III. Modeling and Device Design

3.1 Device Modeling Introduction

The goal of my research is to design and fabricate MEM flexures integrated with epitaxially grown substrates to create tunable micro-optical devices. Specifically, the MEM structures are utilized to electrically tune resonant Fabry-Perot etalons or vertical cavity surface emitting lasers (VCSELs). In order to construct these optical systems, wafers need to be epitaxially grown with nanometer accuracy, and a set of photolithographic masks must be developed to accomplish the device fabrication.

The first step is to determine the design requirements for both the tunable Fabry-Perot etalon and the tunable VCSEL. As the growth of epitaxial material and construction of the MEM devices is carried out at AFRL/SN and AFIT research facilities, care must be taken to ensure compatibility with existing equipment and fabrication capabilities. With this in mind, an optical design wavelength of 980 nm was utilized for both the Fabry-Perot etalon and VCSEL devices [4].

I performed all computer modeling using Mathworks Inc. MATLAB® software. I have written a set of modeling applications which simplify the task of determining the optical characteristics of any given design. These applications are based on the MATLAB® optical engineering toolbox developed at AFIT [5]. This toolbox uses the equations discussed in section 2.4.3 which allow for the quick calculation of power reflectance, transmission, and absorption, and the optical reflectivity phase for any given stack of materials at the wavelengths of interest. The toolbox also solves for the electromagnetic standing wave using the equations from section 2.4.4. Figure 3.1 shows the graphical user interface (GUI) I developed to simplify and streamline optical modeling.

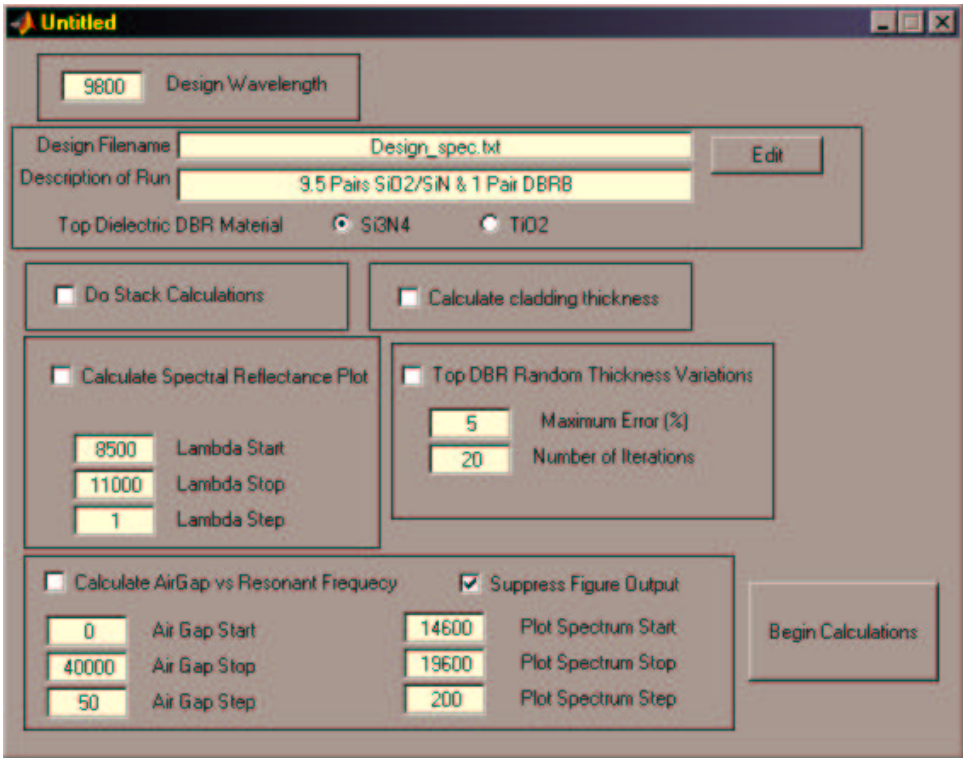


Figure 3.1 Application developed by the author to simplify modeling of optical devices.

3.2 VCSEL Lasing Requirements

For the purposes of this research, I am interested in constructing a laser with three 80 Å active quantum wells placed at the central antinode of a 1λ-thick optical cavity (as shown in figure 3.2). Applying the conditions for threshold lasing given by equation 2.52, and assuming a gain of 500 cm^{-1}, Γ_L=2, Γ_t=1, and minimal cavity losses, the required mirror reflectivity is $R_1R_2 = 0.9952$ (*Note this simplified VCSEL gain model ignores the loss mechanisms present in the optical cavity which may drive up threshold gain requirements). Therefore, a reflectance of 99.76% is required from equal mirrors. Since a value this high cannot be obtained from metallic mirrors, distributed Bragg reflectors (DBR) must be used.

3.2.1 VCSEL Bottom DBR Design. As the desired laser is top emitting, the bottom DBR must have a higher reflectance than the top DBR. Setting the bottom

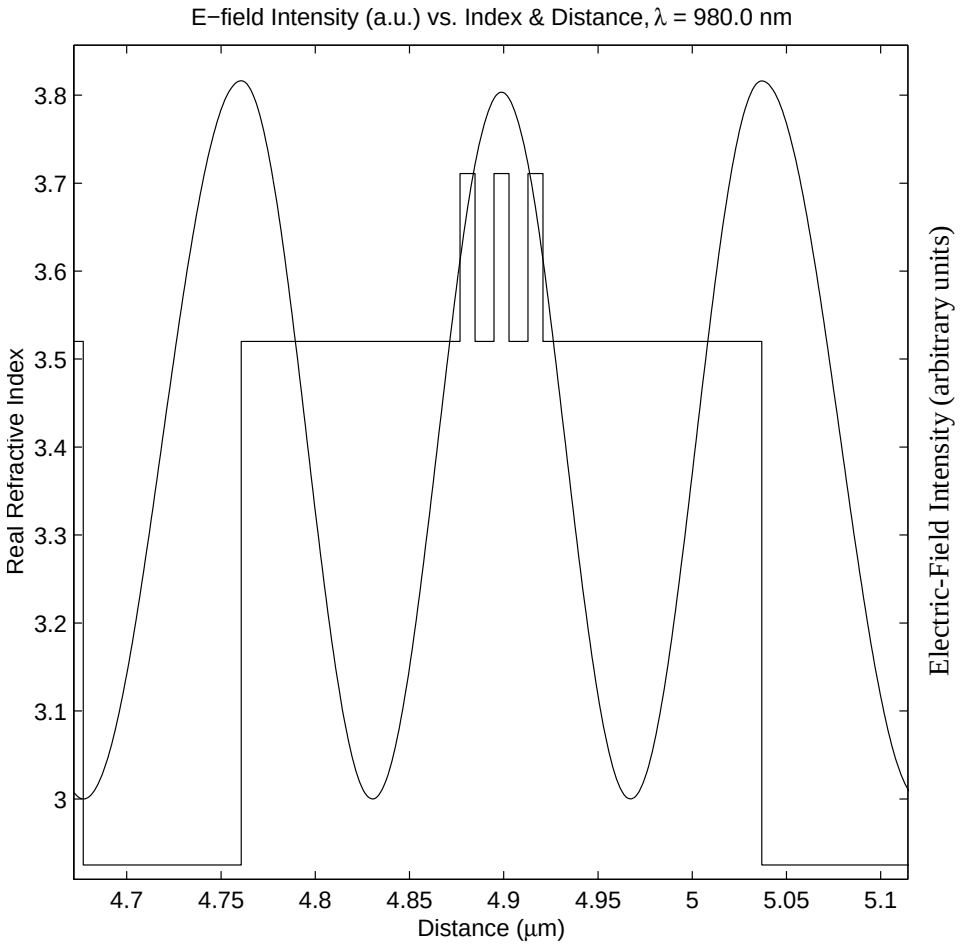


Figure 3.2 Three 80 $\mathring{A}$ quantum wells centered at an antinode in a 1λ-thick microcavity.

reflector to R_2=0.999 means the top reflector must have a value of R_1=0.9962 in order for lasing to occur. The reflectance of a non-absorbing alternating quarter wave DBR stack at normal incidence can be quickly calculated using equation 2.30 as discussed in section 2.4.3. The bottom DBR for this laser design will be epitaxially grown on a GaAs substrate. GaAs has a measured index of refraction at 980 nm of n_s=3.52 (see figure C.10). The quarter-wave stack grown on the substrate consists of alternating layers of GaAs and $Al_{0.9}Ga_{0.1}As$, where $Al_{0.9}Ga_{0.1}As$ has a real index of refraction of n_l=3.015 at 980 nm. The incident medium in this case is a GaAs optical microcavity. In order to determine the minimum number of required quarter-wave

pairs in the DBR stack, the desired reflectance value of R_2=0.999 and the measured index values are plugged into equation 2.30. Solving for the number of pairs results in a minimum value of p=26.

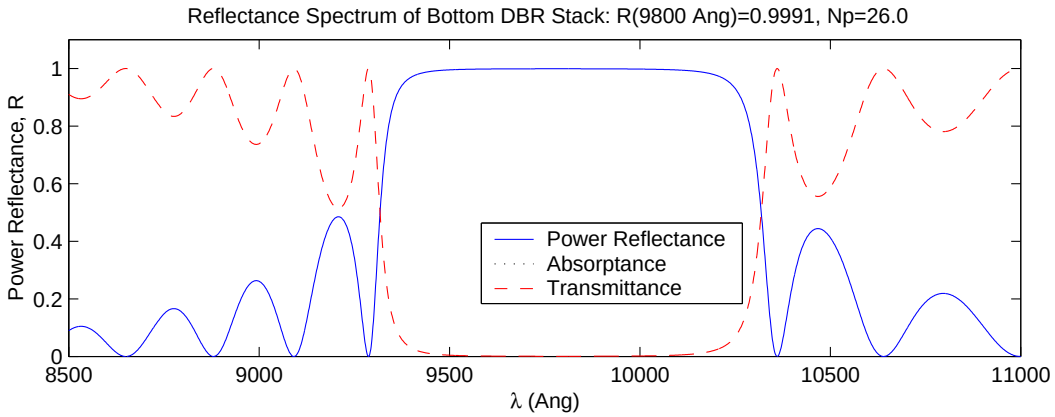


Figure 3.3 Calculated reflectance spectrum of a bottom DBR stack with a design wavelength of $\lambda = 980nm$, consisting of 26 alternating quarter-wave $Al_{0.90}Ga_{0.10}As$/GaAs pairs, on a GaAs substrate.

The thickness of each quarter-wave layer can easily be determined by the relation $d = \lambda/4n$, where $\lambda = 980nm$ is the design wavelength and n is the real index of refraction of the layer. For GaAs and $Al_{0.9}Ga_{0.1}As$, the quarter-wave thicknesses are calculated as 696 Å and 813 Å, respectively.

3.2.2 Coupled Cavity Optical Resonator. Due to the mechanical nature of the MEM tunable device, the determination of the top mirror design is significantly more complicated than the bottom DBR stack. Figure 3.4 shows a simplified schematic of the desired device design.

The completed VCSEL device consists of two separate optical cavities, a 1λ-thick GaAs cavity containing active quantum well gain layers, and an adjustable airgap cavity. These two cavities are separated by a short stack of quarter-wave layers, forming a coupled cavity as shown in figure 3.5.

The shared mirror with transmittance T controls the amount of coupling between the optical resonator cavities. Since the thickness of the GaAs cavity is fixed

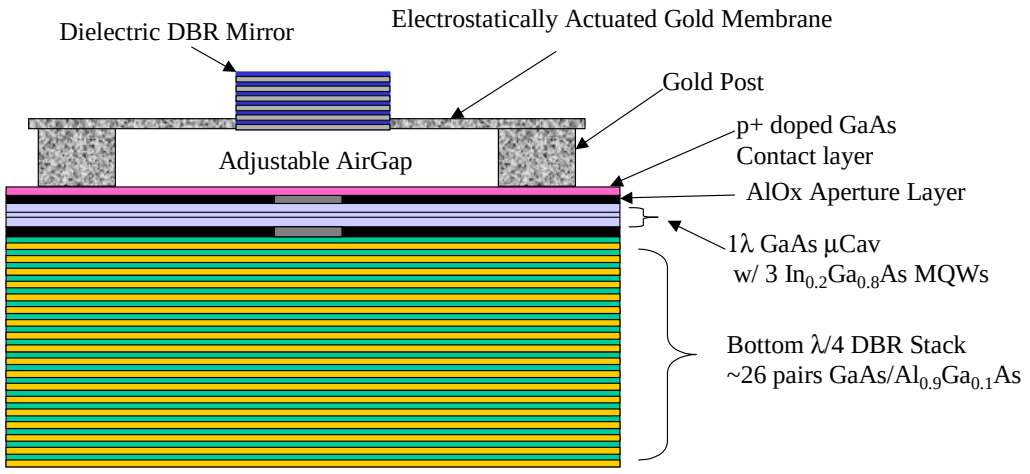


Figure 3.4 Simplified schematic of the desired tunable VCSEL design. Tuning occurs by electrically actuating the top membrane, which reduces the airgap between the top dielectric mirror (SiO_2/Si_3N_4) and the highly doped p+ top contact layer.

at the time of epitaxial growth, the resonant frequency of the combined optical cavity is dependent on the width of the airgap. The mathematical derivation of the resonant frequencies from such a cavity configuration is quite complicated and can be found in Chow [1].

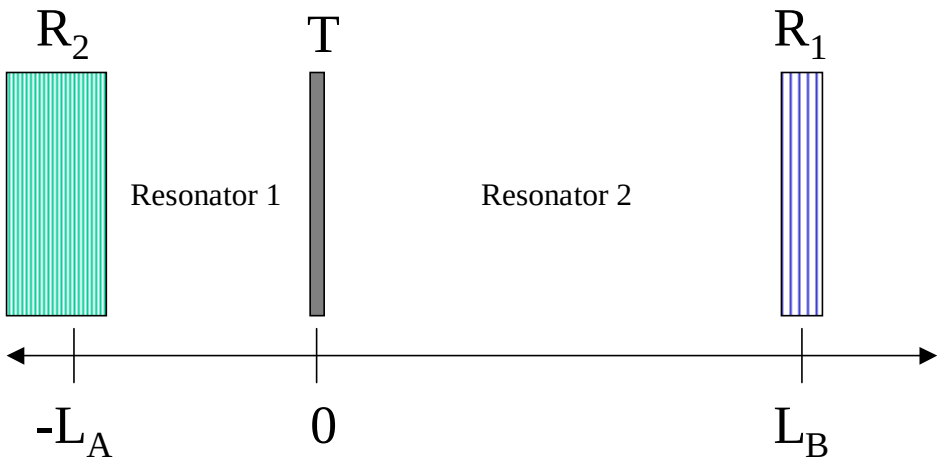


Figure 3.5 Two coupled optical resonators. The three mirrors are located at z=-L_A, L_B, and 0, respectively [1]. The shared mirror with transmittance T controls the amount of coupling between resonators.

For the purposes of this research, the resonant wavelength for various configurations has been calculated numerically by finding the reflectance dip of the device over a series of airgap widths. Figure 3.6 shows the reflectance dip at 980.1 nm for two coupled optical resonator cavities separated by a single pair of coupling DBR mirrors. In general, a coupling mirror with higher transmittance results in a tighter coupling between the optical cavities and a wider tuning range (see section 3.3).

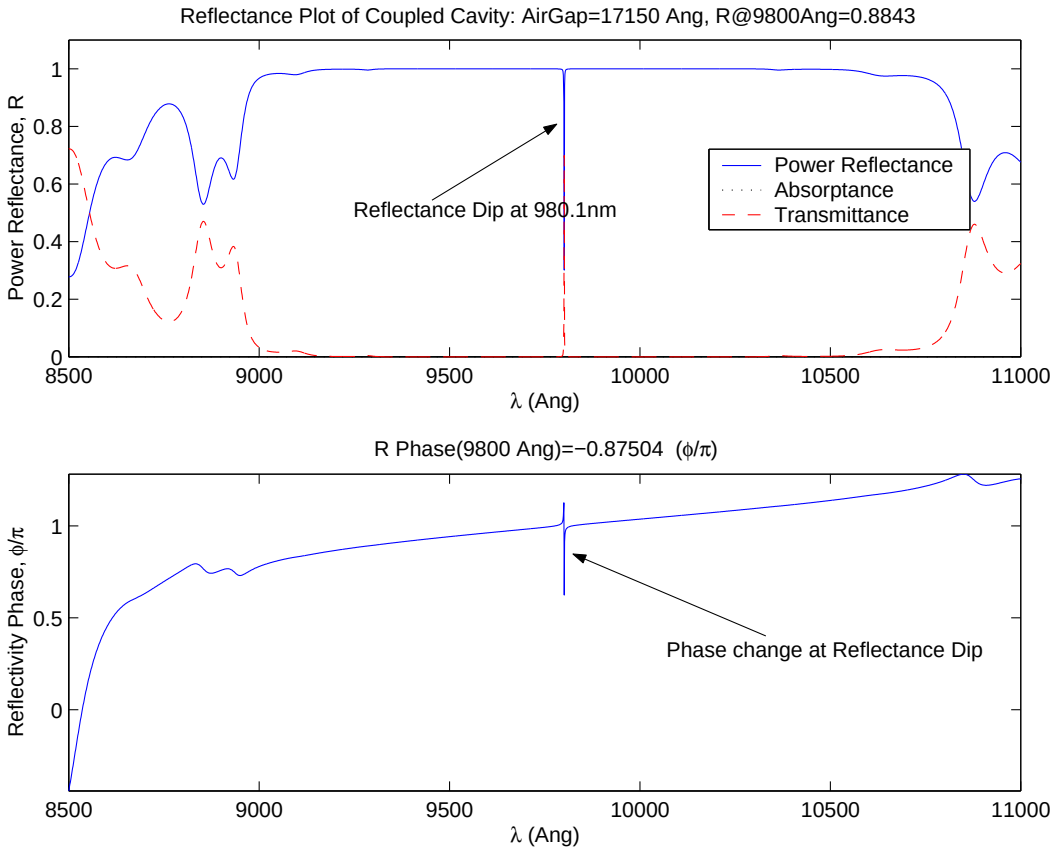


Figure 3.6 Reflectance spectrum of two coupled optical resonators separated by a single pair of quarter-wave mirrors. The resonant frequency is determined by the location of the reflectance dip. In this case the airgap has a width of 17500 Å, and the resulting resonant frequency is found at $\lambda = 9801$ Å.

3.2.3 VCSEL Top DBR Design. Recalling the calculations from section 3.2.1, the minimum reflectance of the top mirror must be greater than R_1=0.9962 for lasing to occur. In this case, the top mirror starts at the boundary of the gain

cavity, and consists of the coupling stack between the two optical resonators, the airgap, and a quarter-wave mirror of alternating dielectric layers. As discussed in section 2.4.3, DBR mirrors consisting of dielectric layers typically have a much larger index of refraction ratio. Therefore fewer layers are required to achieve high reflectance. Due to limitations of available dielectric materials, the optimal dielectric combination, TiO_2 and SiO_2, was not utilized. The dielectrics chosen for this research were SiO_2 and Si_3N_4. Both materials are easy to deposit via either PECVD or sputtering, and may be anisotropically RIE etched with the freon based CF-23. The measured indexes of refraction for SiO_2 and Si_3N_4 are $n = 1.45$ and $n = 2.004$ at $\lambda = 980\ nm$, respectively (see figure C.11).

Rather than deriving a complicated analytical relation to find the reflectance of the top mirror stack, it is easier to numerically calculate this value using the matrix method discussed in section 2.4.3. Figure 3.7 is a spectral plot of the reflectance looking up from the gain cavity towards the top of the device. For this calculation, a single pair of $Al_{0.98}Ga_{0.02}As/GaAs$ layers are acting as the coupling layer, and the dielectric top DBR consists of 8.5 pairs of Si_3N_4 and SiO_2. At the design wavelength, $\lambda = 980\ nm$, the combined reflectance is R_1=0.9961.

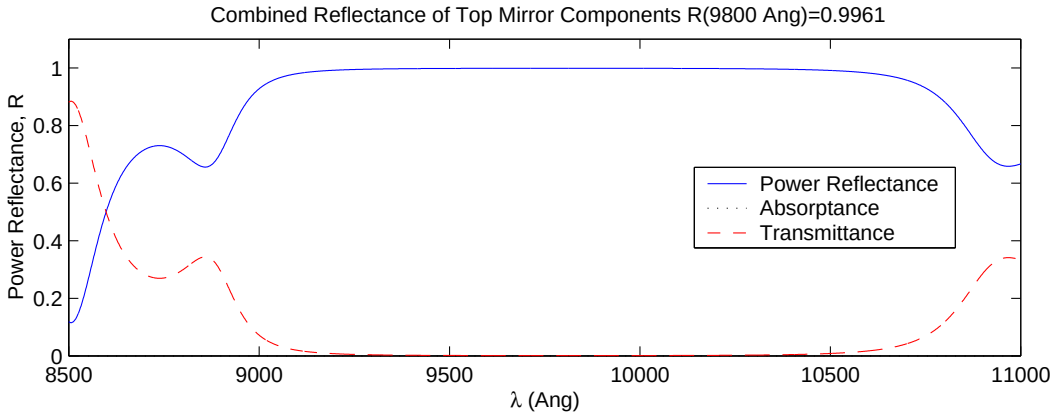


Figure 3.7 Reflectance spectrum of combined top mirror consisting of one quarter-wave pair $Al_{0.98}Ga_{0.02}As/GaAs$ layers, a 17150 Å airgap, and 8.5 pairs of quarter-wave Si_3N_4/SiO_2. The top limit of the plot is determined by the wavelength range of measured index data for the dielectric materials (6500 Å to 11000 Å).

A reflectance value of 99.61% is short of the required value of 99.62%. Adding another pair to the Si_3N_4/SiO_2 DBR stack (9.5 pairs) brings the reflectance measurement to 99.79% at $\lambda = 980\ nm$.

3.2.4 Electromagnetic Standing Wave. As discussed in section 2.4.4, an electromagnetic standing wave is present within any resonant optical cavity(see figure 3.8). By placing the active gain material ($In_{0.2}Ga_{0.8}As$ QWs) at the antinodes, or peaks, of the optical standing wave in the laser cavity, as shown in figure 3.9, it is possible to double the effective optical gain [6]. A misplacement of the active gain material at the nodes of the standing wave results in zero net gain, since there is no electromagnetic field to stimulate emission from the gain medium.

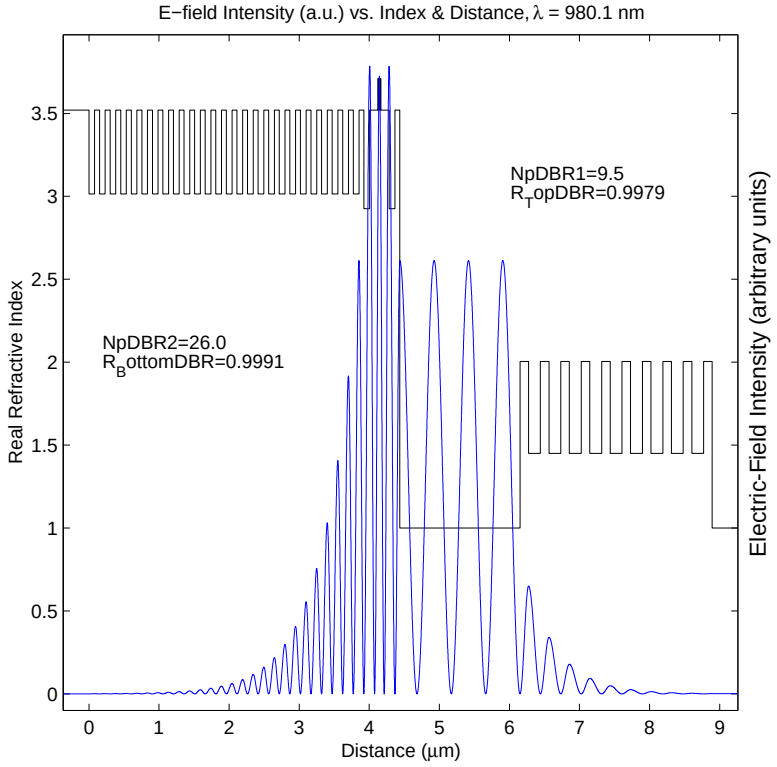


Figure 3.8 Electromagnetic standing wave pattern of a complete MEM tunable VCSEL device.

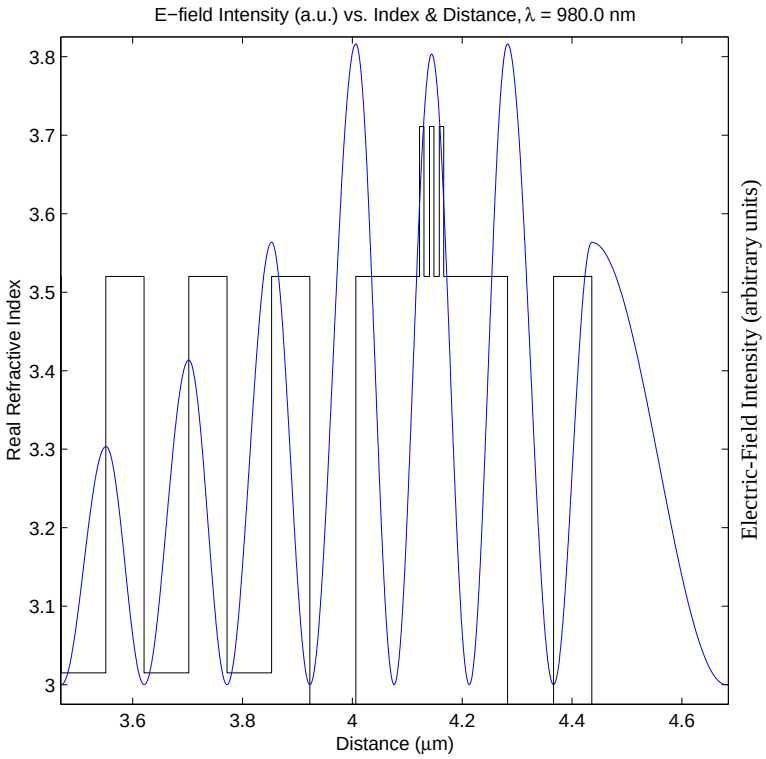


Figure 3.9 Correct placement of quantum wells at the center of a 1λ optical cavity standing wave antinode. The FWHM of the central antinode is calculated as $\nu_F = 700\ \mathring{A}$.

When designing a tunable VCSEL device, care must be taken to ensure that the antinode of the standing wave continues to overlap the quantum wells while tuning occurs. As the resonant frequency is tuned up or down by varying the airgap, the central antinode of the standing wave shifts it's position higher or lower within the optical cavity (see figure 3.10). The FWHM of the central antinode peak is calculated to be $\nu_F = 700$ Å, while the maximum deflection of the standing wave peak across a reasonable tuning range is less than 400 Å. As the peak of the antinode shifts away from the QWs, the value of the longitudinal confinement factor Γ_L, will be reduced to a value in the range $0 \leq \Gamma_L \leq 2$. This in-turn alters the threshold lasing requirement, requiring an increase in the threshold gain, or an increase in the mirror reflectivity.

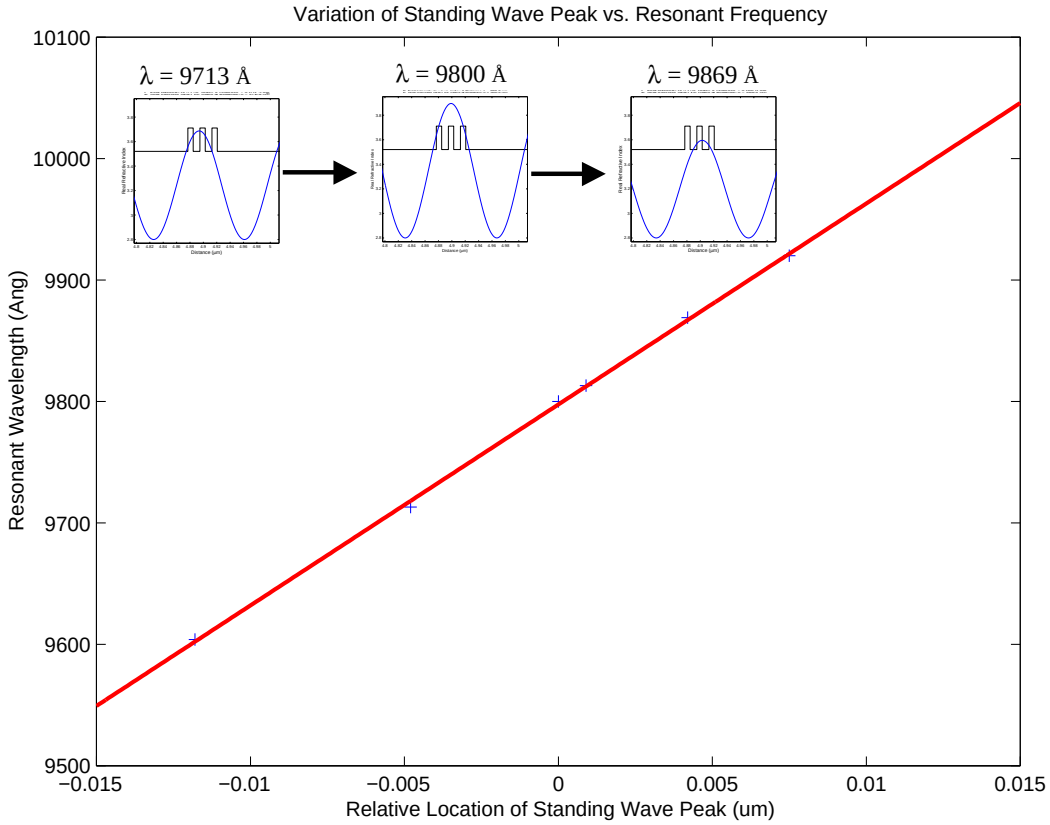


Figure 3.10 Location of standing wave antinode relative to center of quantum well as the resonant frequency is tuned. The relationship between tuning frequency and peak location fits a linear relationship described by $d = 0.604\lambda - 0.592\ \mu m$, where d is the shift from the central QW in μm. The inset figures shows the shifting central antinode for λ =9713 Å, 9800 Å, and 9869 Å.

3.3 Airgap Tuning

The basic design parameters of the MEM tunable VCSEL device have been determined, but the response of the resonant frequency due to a change in the air-gap width must be measured for various configurations. No attempt has been made to find an analytical solution relating airgap to resonant frequency. It is far simpler to calculate the relationship numerically using the matrix method described in section 2.4.3. The following factors strongly influence the results: increasing or decreasing the number of high/low pairs in the coupling stack, a $\lambda/2$-thick microcavity vs. a 1λ-thick cavity, and the dielectric material used to fabricate the top DBR

mirror stack. This research project is limited to Si_3N_4/SiO_2 dielectric mirrors, but calculations for a device utilizing a TiO_2/SiO_2 mirror stack have been included for comparison (figure 3.15).

Figure 3.11 through figure 3.15 show the results of calculations for five different design scenarios. Each plot has been annotated with the minimum and maximum resonant wavelength for each tuning band as the airgap thickness increases. The minimum and maximum wavelengths are defined at the minimum and maximum airgaps where a single resonant dip is present in the spectral reflectance plot. Figure 3.16 through figure 3.18 show the increase in the resonant reflectance dip at the airgap is widened from 14650 Åto 19450 Å. Figure 3.16a and figure 3.18b are reflectance spectrums with multiple resonant frequency dips. These airgaps are considered outside the optimal tuning range of the device. Figure 3.19 and figure 3.20 show the calculated electromagnetic standing waves as the airgap changes from 14650 Åto 19450 Å.

It is apparent that an increase in the airgap relates to a decrease in the tuning range of any given device. This is due to fact that free spectral range (FSR) is inversely proportional to airgap thickness (equation 2.22). The first three design runs have a 1λ-thick resonant gain cavity, Si_3N_4/SiO_2 top DBR mirrors, and varying numbers of DBR mirror pairs in the coupling stack between optical cavities. Table 3.1 details the important parameters for eight separate device simulations and the resulting tuning range. The tuning range for each device is centered at an airgap thickness of 17150 Å and a resonant wavelength $\lambda = 980\ nm$. This was selected as the optimum airgap range to fabricate the MEM devices due to processing considerations discussed in section 4.5.

As discussed in section 3.2.2, Figure 3.11 through figure 3.15 show that an increase in the number of coupling quarter-wave layers results in a decrease in the tuning range. In addition, the devices with $\lambda/2$-thick microcavities require the fewest number of top DBR dielectric pairs. The best design option appears to be run #8,

Table 3.1 Details of eight MEM tunable VCSEL device tuning simulations

Run Num	**Top DBR**	**Coupling Stack Pairs**	**μCavity Length**	**Tuning Range**
1	9.5 Pairs Si_3N_4/SiO_2	1 Pair	1λ	35.9 nm
2	9.5 Pairs Si_3N_4/SiO_2	2 Pairs	1λ	26.0 nm
3	8.5 Pairs Si_3N_4/SiO_2	3 Pairs	1λ	17.4 nm
4	5.5 Pairs Si_3N_4/SiO_2	1.5 Pairs	$\lambda/2$	35.9 nm
5	5.5 Pairs TiO_2/SiO_2	1 Pair	1λ	43.0 nm
6	4.5 Pairs TiO_2/SiO_2	2 Pairs	1λ	27.1 nm
7	4.5 Pairs TiO_2/SiO_2	3 Pair	1λ	18.2 nm
8	2.5 Pairs TiO_2/SiO_2	1.5 Pairs	$\lambda/2$	40.1 nm

which requires only 2.5 pairs of dielectric top DBR layers and has a large 40.1nm tuning range. These fabrication options are unavailable at this time, so I chose to use the design described in run #1.

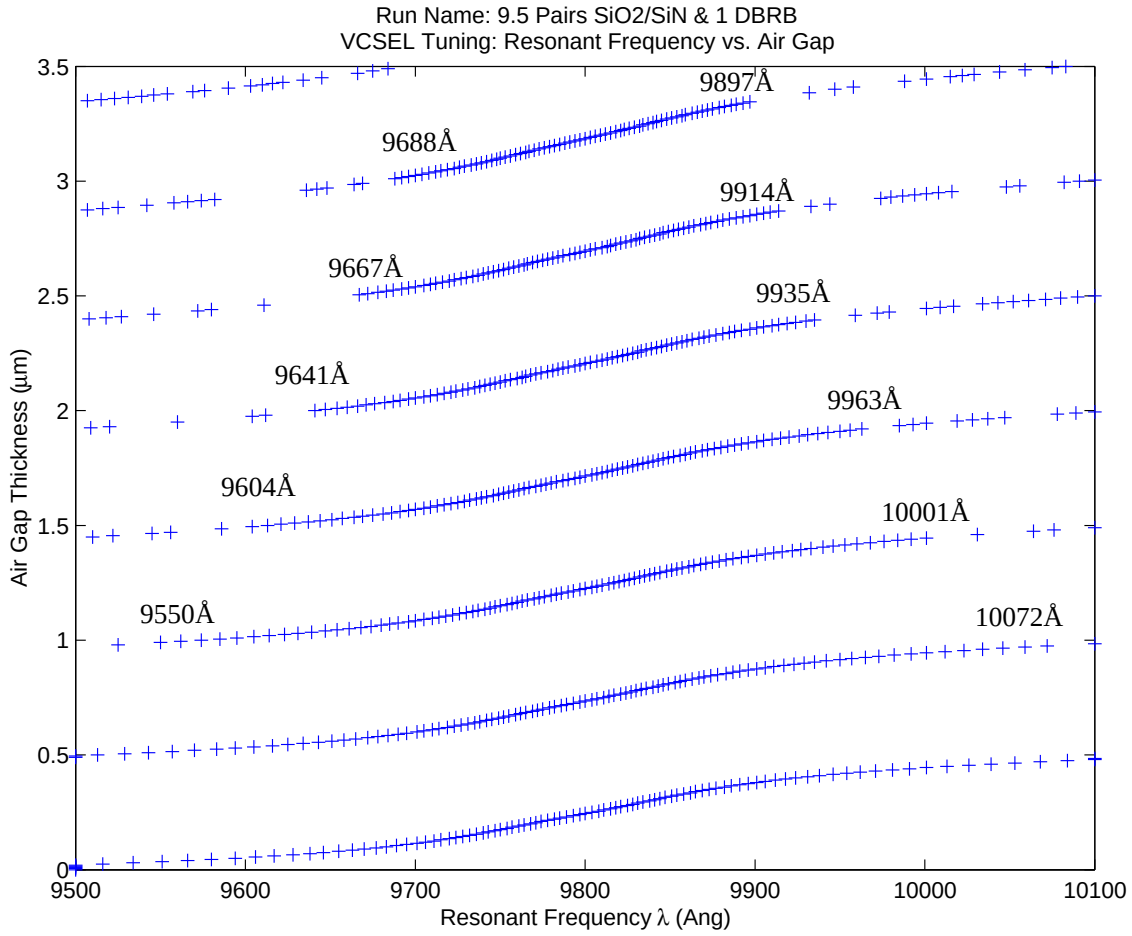


Figure 3.11 Run #1 resonant frequency of the coupled cavity vs. airgap thickness. This structure consists of a top DBR composed of **9.5 pairs** of $\mathbf{SiO_2}$ and $\mathbf{Si_3N_4}$ quarter-wave layers and **one pair** of quarter-wave layers in the coupling stack. The bottom DBR is constructed of 26 pairs of GaAs and $Al_{0.9}Ga_{0.1}As$ quarter-wave layers on a GaAs substrate. The **1λ-thick** μCavity consists of GaAs cladding surrounding three $In_{0.2}Ga_{0.8}As$QWs. As the airgap increases, the FSR of the coupled cavity decreases, defining a narrowing series of tuning bands. The minimum and maximum resonant frequency for each tuning range is shown.

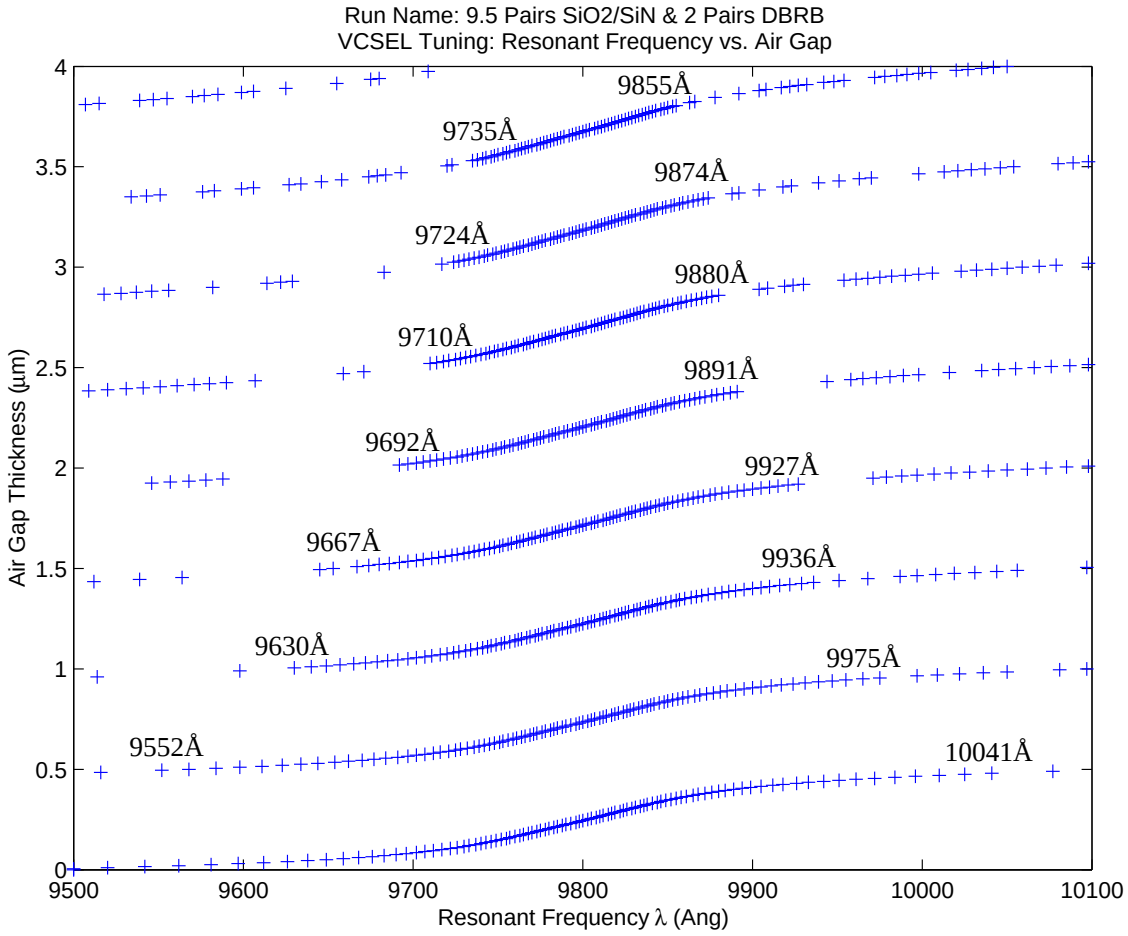


Figure 3.12 Run #2 resonant frequency of the coupled cavity vs. airgap thickness. This structure consists of a top DBR composed of **9.5 pairs** of $\mathbf{SiO_2}$ and $\mathbf{Si_3N_4}$ quarter-wave layers and **two pairs** of quarter-wave layers in the coupling stack. The bottom DBR is constructed of 26 pairs of GaAs and $Al_{0.9}Ga_{0.1}As$ quarter-wave layers on a GaAs substrate. The **1λ-thick** μCavity consists of GaAs cladding surrounding three $In_{0.2}Ga_{0.8}As$QWs. As the airgap increases, the FSR of the coupled cavity decreases, defining a narrowing series of tuning bands. The minimum and maximum resonant frequency for each tuning range is shown.

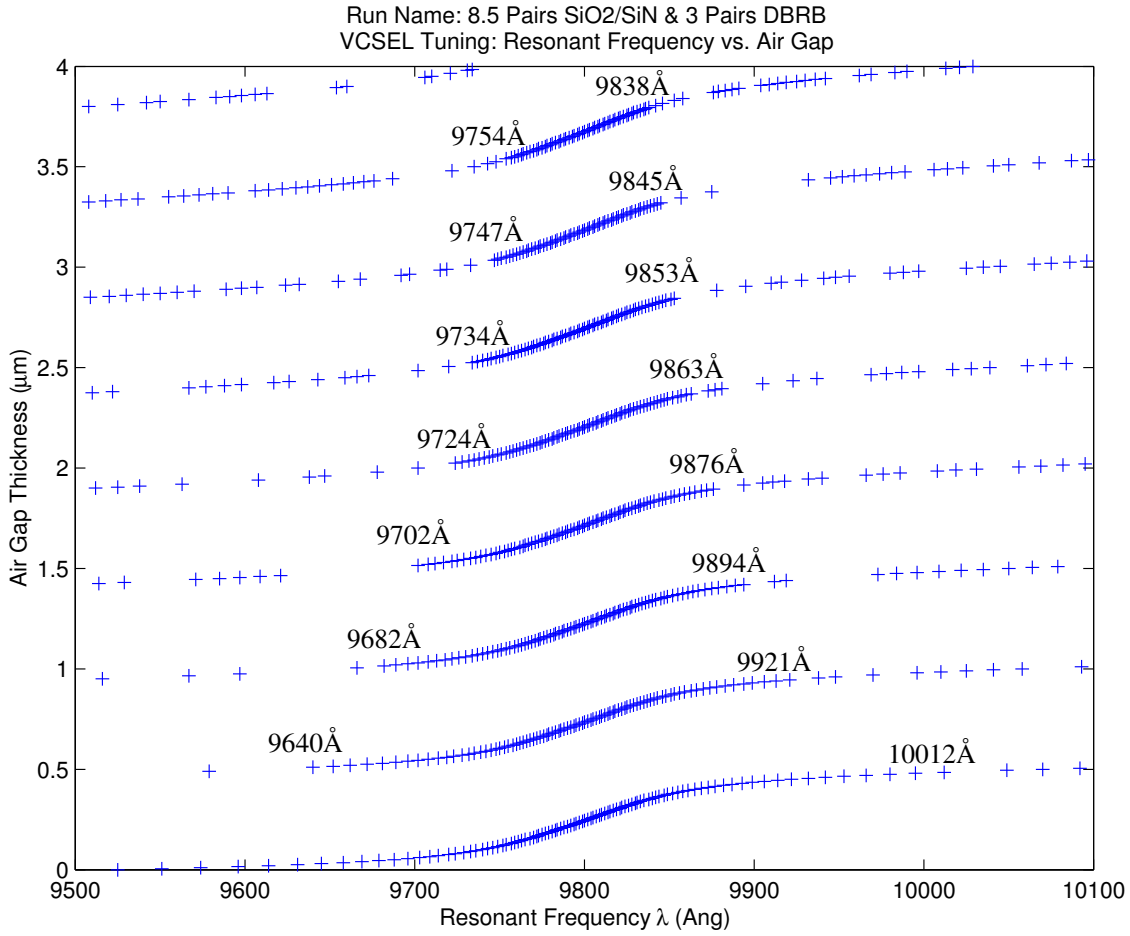


Figure 3.13 Run #3 resonant frequency of the coupled cavity vs. airgap thickness. This structure consists of a top DBR composed of **8.5 pairs** of $\mathbf{SiO_2}$ and $\mathbf{Si_3N_4}$ quarter-wave layers and **three pairs** of quarter-wave layers in the coupling stack. The bottom DBR is constructed of 26 pairs of GaAs and $Al_{0.9}Ga_{0.1}As$ quarter-wave layers on a GaAs substrate. The **1λ-thick** μCavity consists of GaAs cladding surrounding three $In_{0.2}Ga_{0.8}As$QWs. As the airgap increases, the FSR of the coupled cavity decreases, defining a narrowing series of tuning bands. The minimum and maximum resonant frequency for each tuning range is shown.

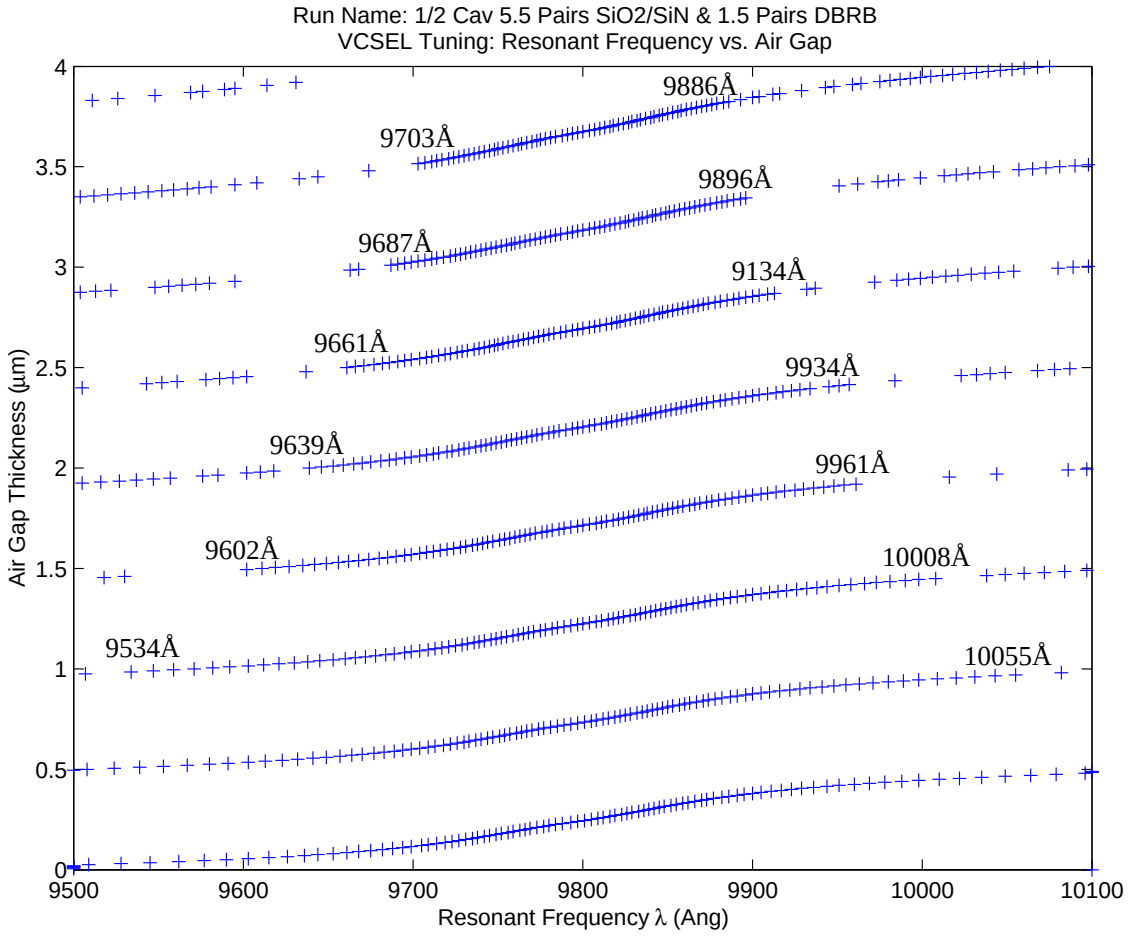


Figure 3.14 Run #4 resonant frequency of the coupled cavity vs. airgap thickness. This structure consists of a top DBR composed of **5.5 pairs** of $\mathbf{SiO_2}$ and $\mathbf{Si_3N_4}$ quarter-wave layers and **1.5 pairs** of quarter-wave layers in the coupling stack. The bottom DBR is constructed of 26 pairs of GaAs and $Al_{0.9}Ga_{0.1}As$ quarter-wave layers on a GaAs substrate. The $\lambda/2$**-thick** μCavity consists of GaAs cladding surrounding three $In_{0.2}Ga_{0.8}AsQWs$. As the airgap increases, the FSR of the coupled cavity decreases, defining a narrowing series of tuning bands. The minimum and maximum resonant frequency for each tuning range is shown.

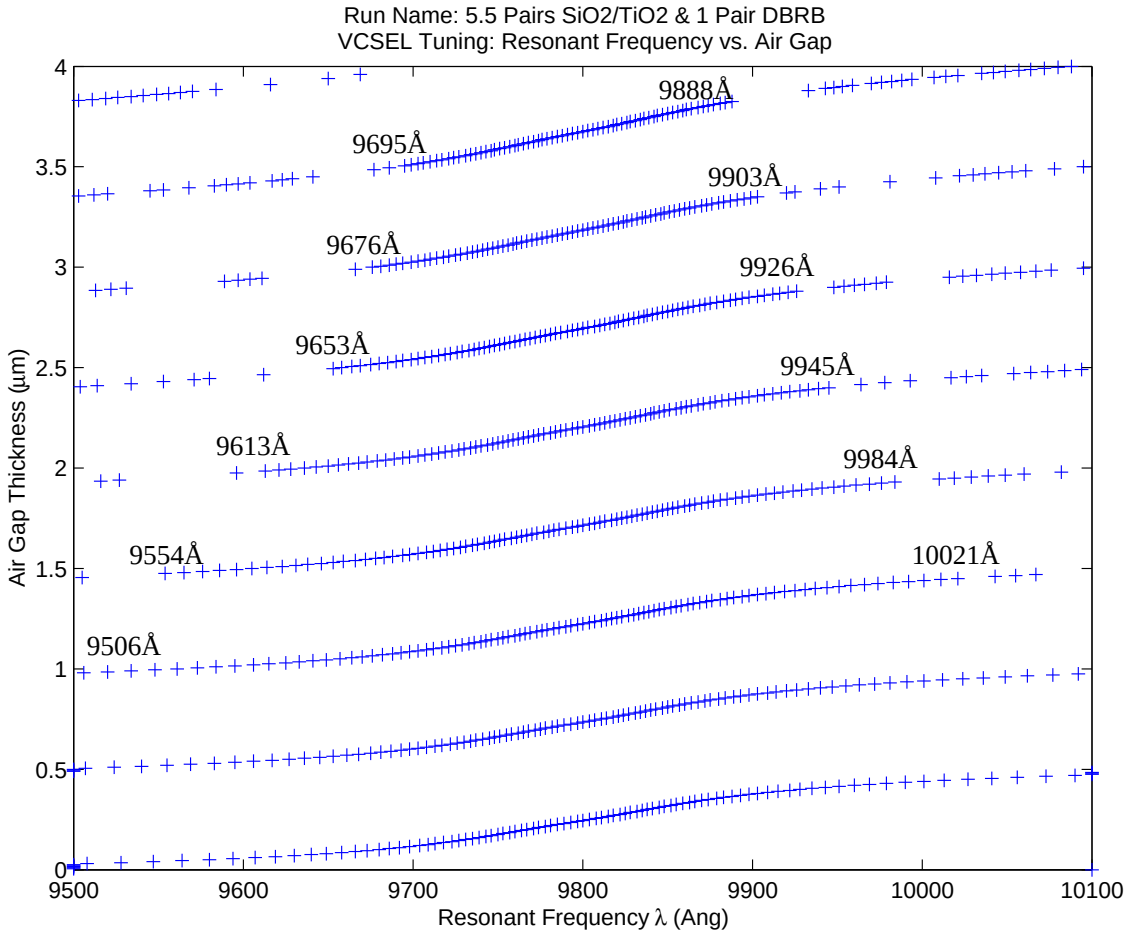
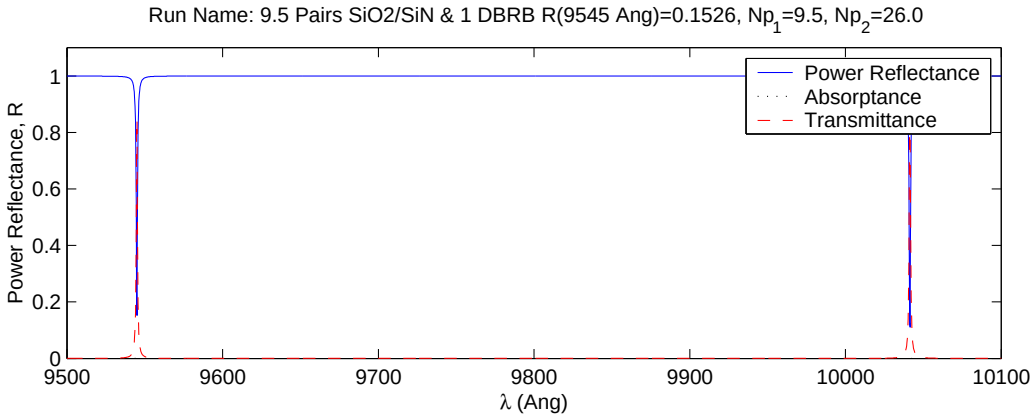
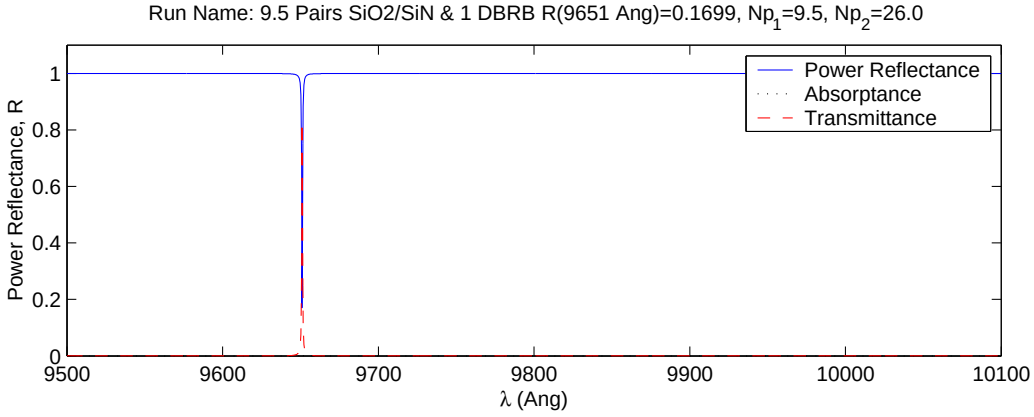


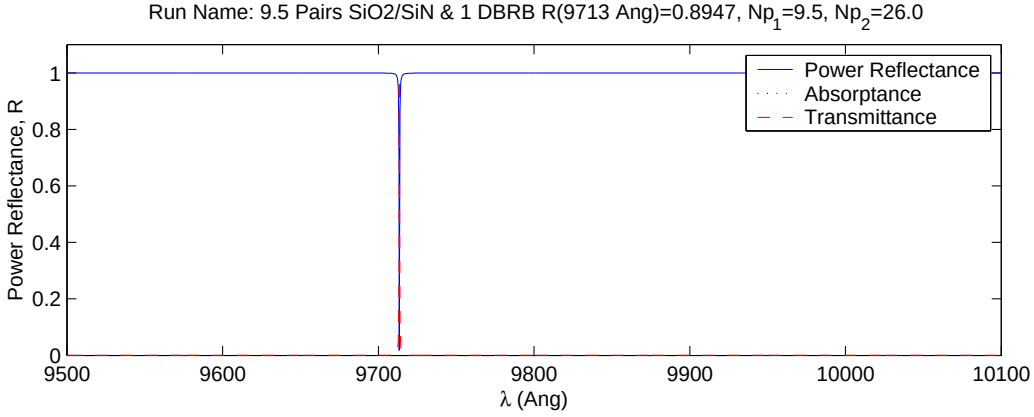
Figure 3.15 Run #5 resonant frequency of the coupled cavity vs. airgap thickness. This structure consists of a top DBR composed of **5.5 pairs** of $\mathbf{SiO_2}$ and $\mathbf{TiO_2}$ quarter-wave layers and **one pair** of quarter-wave layers in the coupling stack. The bottom DBR is constructed of 26 pairs of GaAs and $Al_{0.9}Ga_{0.1}As$ quarter-wave layers on a GaAs substrate. The **1λ-thick** μCavity consists of GaAs cladding surrounding three $In_{0.2}Ga_{0.8}AsQWs$. As the airgap increases, the FSR of the coupled cavity decreases, defining a narrowing series of tuning bands. The minimum and maximum resonant frequency for each tuning range is shown.



(a)

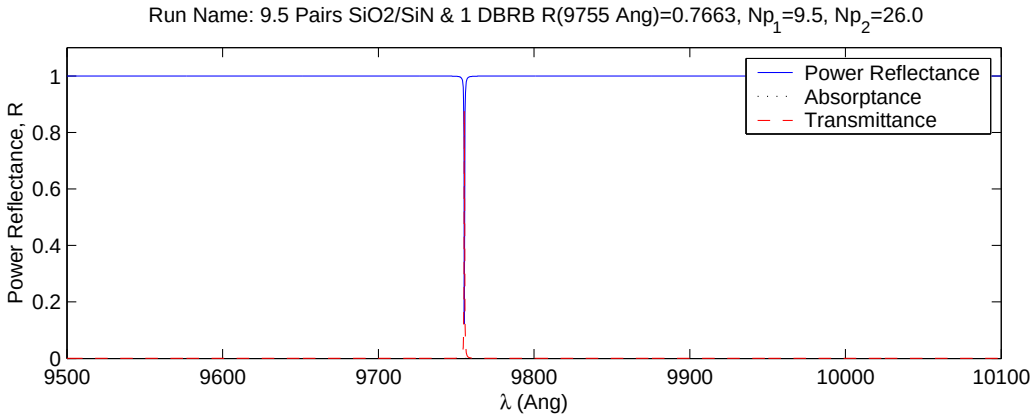


(b)

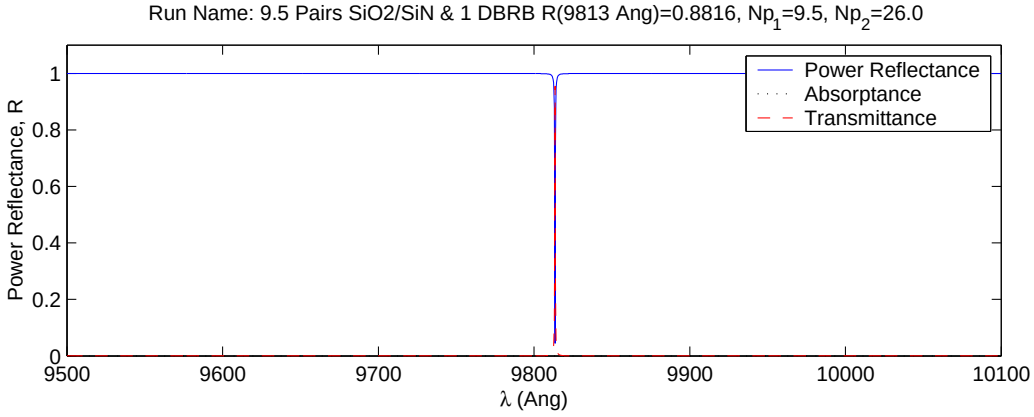


(c)

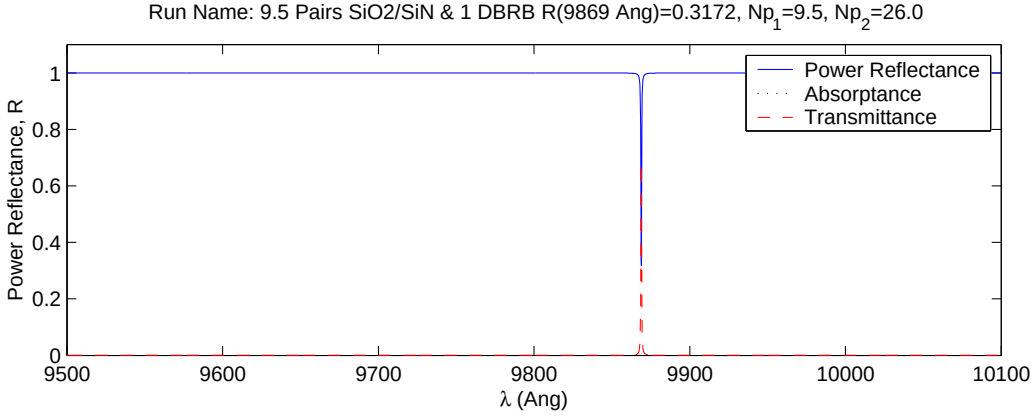
Figure 3.16 Run #1 calculated reflectance dip for different airgap thicknesses: (a) when the airgap = 14650 Å then λ_{dip} = 9545 Å and 10040 Å, (b) if the airgap = 15250 Å then λ_{dip} = 9651 Å (c) and if the airgap = 15850 Å then λ_{dip} = 9713 Å.



(a)

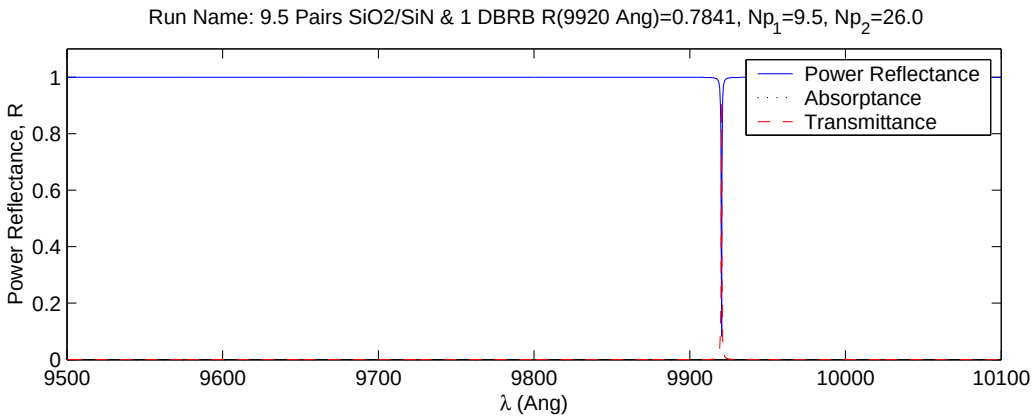


(b)

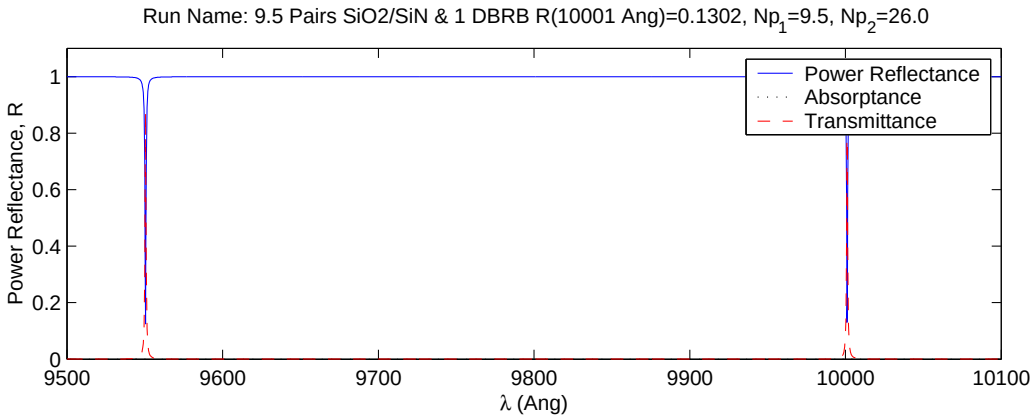


(c)

Figure 3.17 Run #1 calculated reflectance dip for different airgap thicknesses: (a) when the airgap = 16450 Å then λ_{dip} = 9755 Å, (b) if the airgap = 17350 Å then λ_{dip} = 9813 Å (c) and if the airgap = 18250 Å then λ_{dip} = 9869 Å.



(a)



(b)

Figure 3.18 Run #1 calculated reflectance dip for different airgap thicknesses: (a) when the airgap = 18850 Å then λ_{dip} = 9920 Å, (b) and if the airgap = 19450 Å then λ_{dip} = 9550 Å and 10001 Å.

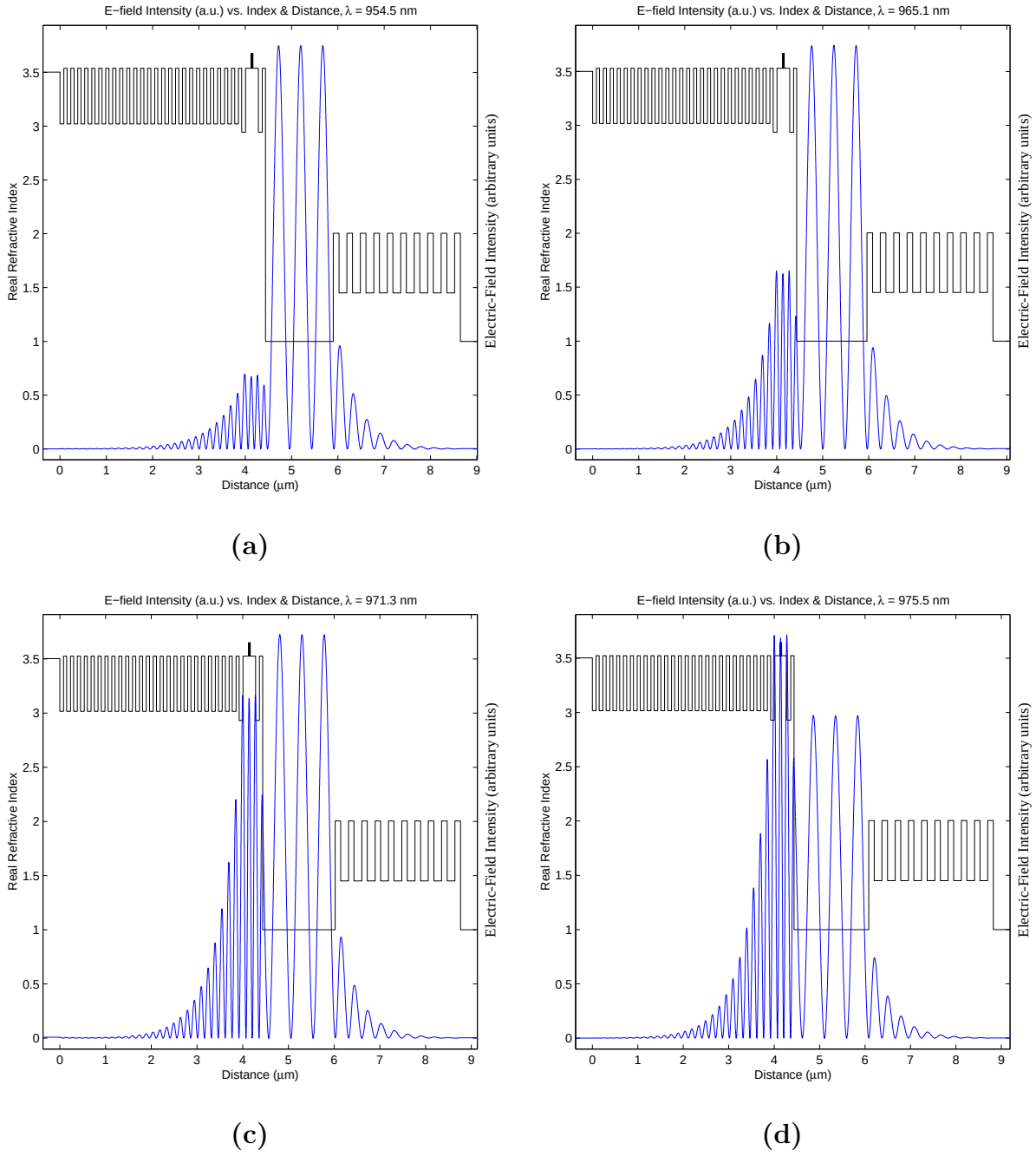


Figure 3.19 Calculated standing wave for MEM tunable VCSEL design run #1 for different airgaps: (a) when the airgap = 14650 Å then λ = 9545 Å, (b) if the airgap = 15250 Å then λ = 9651 Å, (c) if the airgap = 15850 Å then λ = 9713 Å, (d) and if the airgap = 16450 Å then λ = 9755 Å.

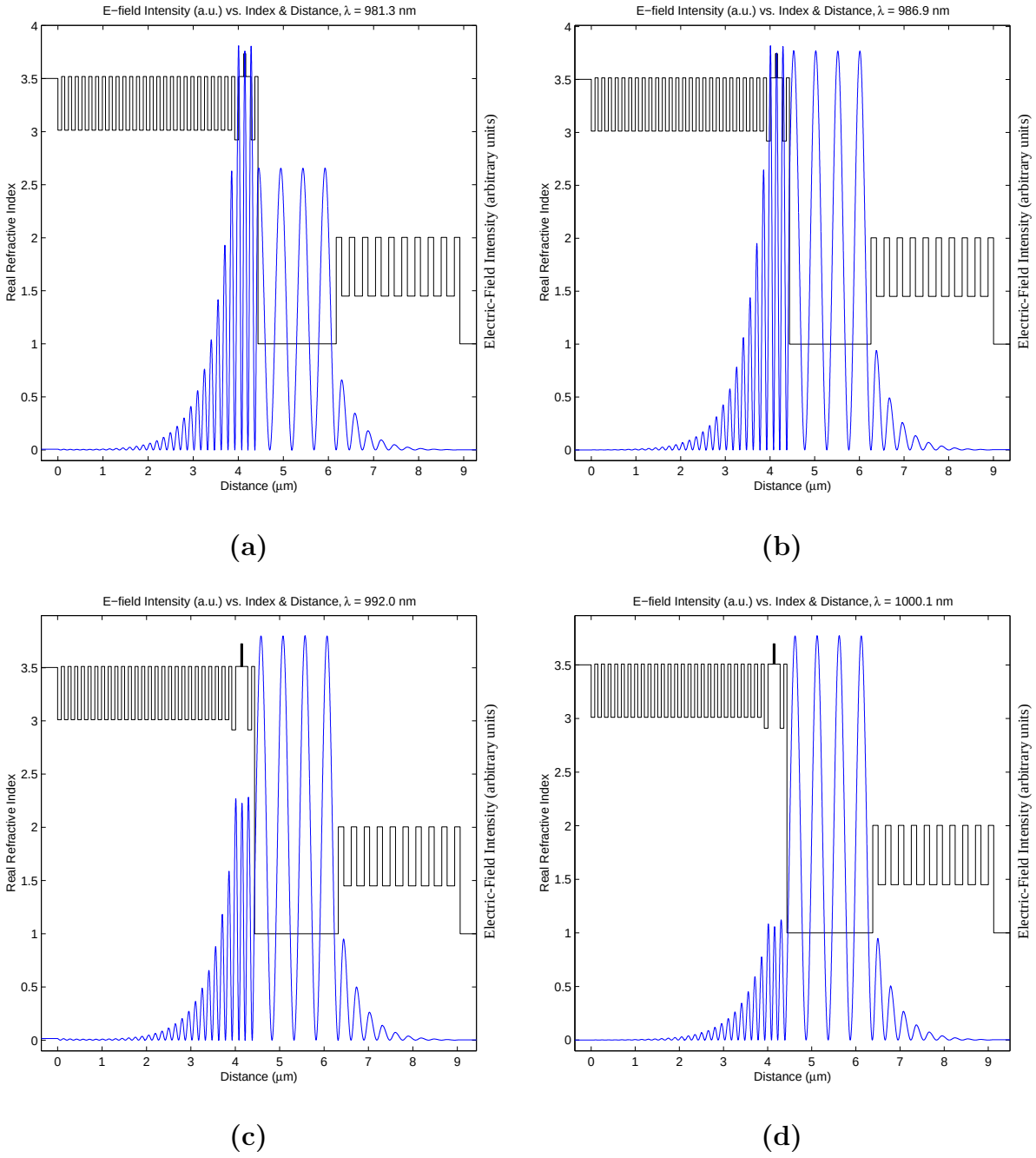


Figure 3.20 Calculated standing wave for MEM tunable VCSEL design run #1 for different airgaps: (a) when the airgap = 17350 Å then λ = 9813 Å, (b) if the airgap = 18250 Å then λ = 9869 Å, (c) if the airgap = 18850 Å then λ = 9920 Å, (d) and if the airgap = 19450 Å then λ = 10001 Å.

3.4 Tunable Fabry-Perot Etalon

Figure 3.21 shows a simplified schematic of a MEM tunable Fabry-Perot etalon, similar in design to the tunable VCSEL shown in figure 3.4.

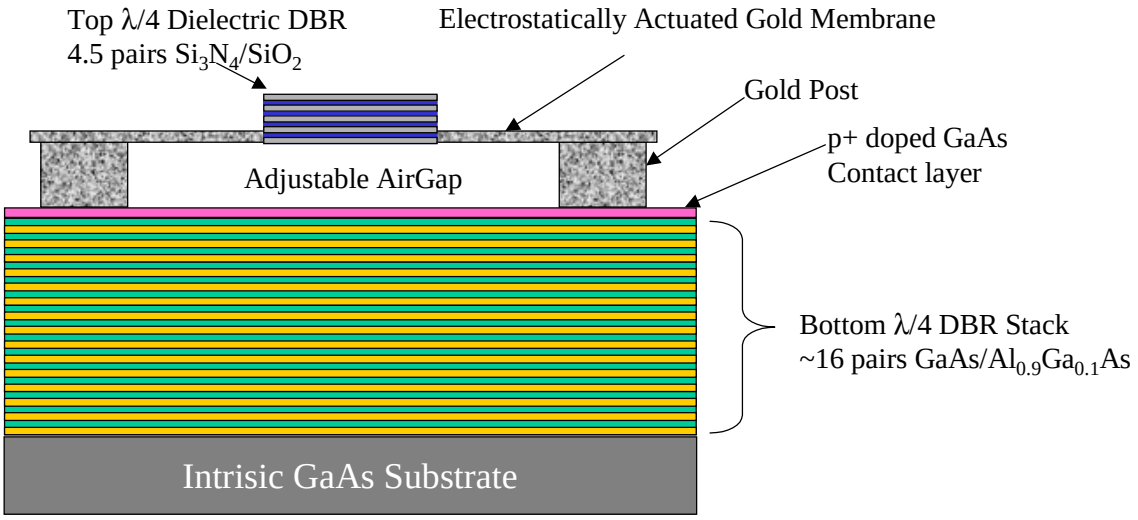


Figure 3.21 Simplified schematic of a tunable Fabry-Perot design. Tuning occurs by electrically actuating the the gold membrane and causing it to flex downward toward the highly doped p+ top contact layer. This is identical to the VCSEL design, except for lower reflectivity mirrors and no active gain region.

Compared with the tunable VCSEL design, the tunable Fabry-Perot etalon is simple and straight forward. As no gain medium is present, there is no need for a second optical microcavity, and the airgap becomes the only optical cavity. In addition, a high finesse cavity is not required for device operation, thus the mirror reflectance may be lowered significantly. In fact, a lower finesse is desired for research purposes as it results in a wide FWHM of the resonant transmission peak (see equation 2.23). This greatly simplifies detection and measurement of the device resonant frequency [4].

Figure 3.22 shows the resulting spectral power reflectance of a device with a bottom mirror consisting of 16 quarter-wave pairs of $GaAs/Al_{0.9}Ga_{0.1}As$ layers, and a top mirror fabricated from 4.5 quarter-wave pairs of Si_3N_4/SiO_2. At the design

wavelength of $\lambda = 980\ nm$ the reflectance of the bottom mirror is R_2=0.972 and the top mirror is $R_1 = 0.928$. The airgap is set at $3\lambda/2 = 14700$ Å. From equation 2.22 the calculated free spectral range (FSR) is $\nu_F = 326.7\ nm$. From equation 2.23, the value of the full-width-at-half-max (FWHM) at the transmission peak is $\delta\nu = 107$ Å.

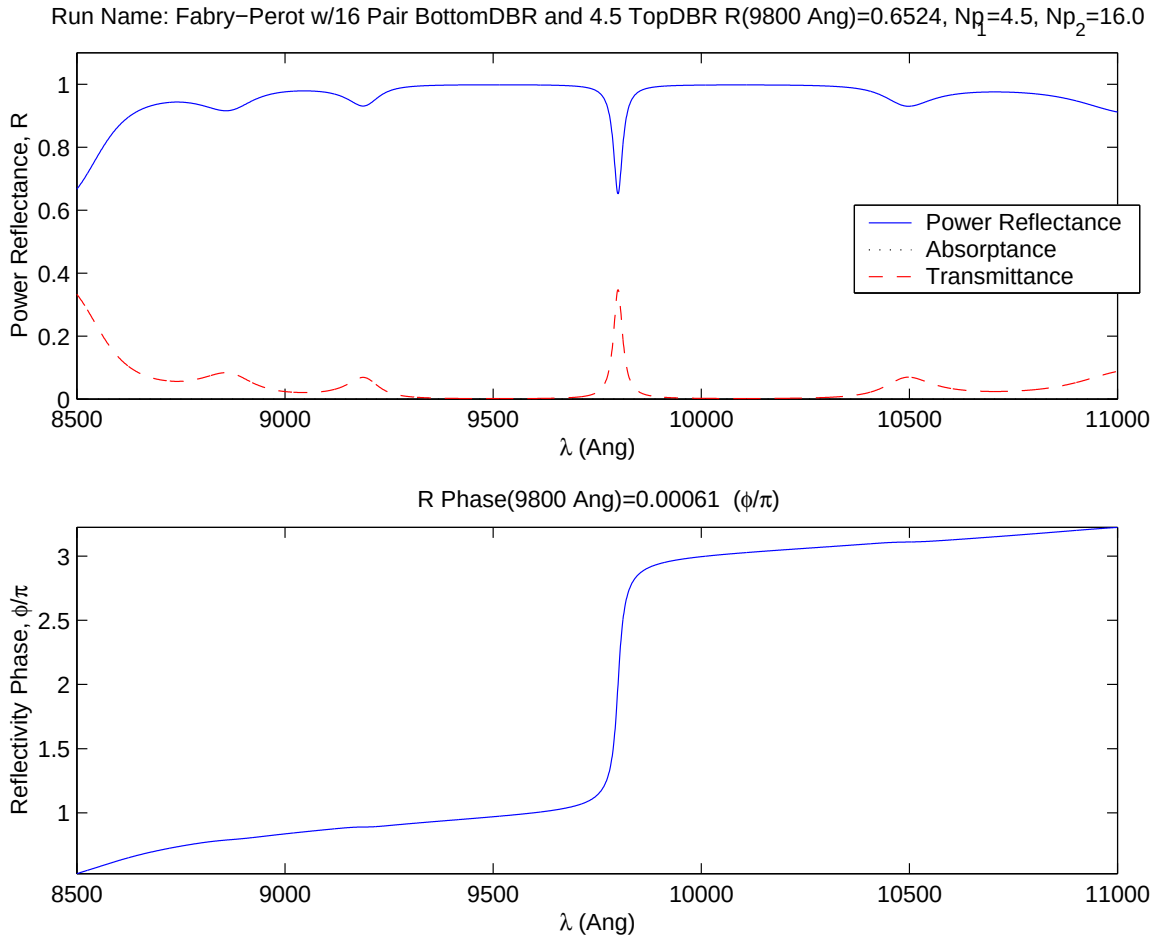


Figure 3.22 Spectral reflectance plot of resonant Fabry-Perot etalon with bottom DBR consisting of 16 pairs GaAs/$Al_{0.9}Ga_{0.1}As$ and top DBR fabricated from 4.5 pairs Si_3N_4/SiO_2. The air optical cavity has a thickness of 14700$\mathring{A}$.

Figure 3.23 shows the calculated electromagnetic standing wave of the multi-layer Fabry-Perot etalon design, and figure 3.24 is a plot of the resonant frequency vs. the airgap thickness for the structure shown in figure 3.21.

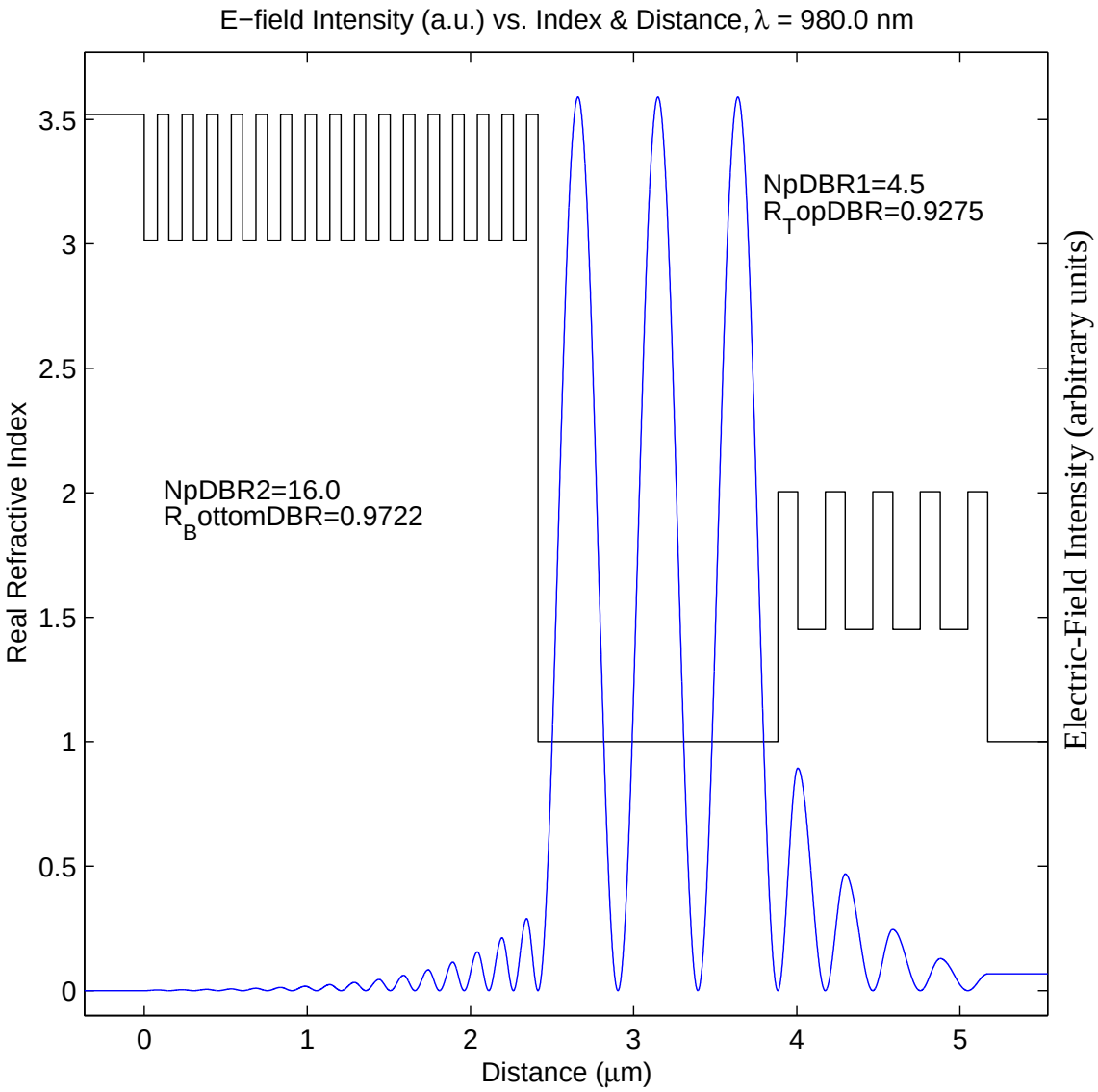


Figure 3.23 Electromagnetic standing wave of a multilayer Fabry-Perot etalon with bottom DBR consisting of 16 pairs $GaAs/Al_{0.9}Ga_{0.1}As$ on a GaAs substrate and top DBR fabricated from 4.5 pairs Si_3N_4/SiO_2. The air optical cavity has a thickness of 14700 Å.

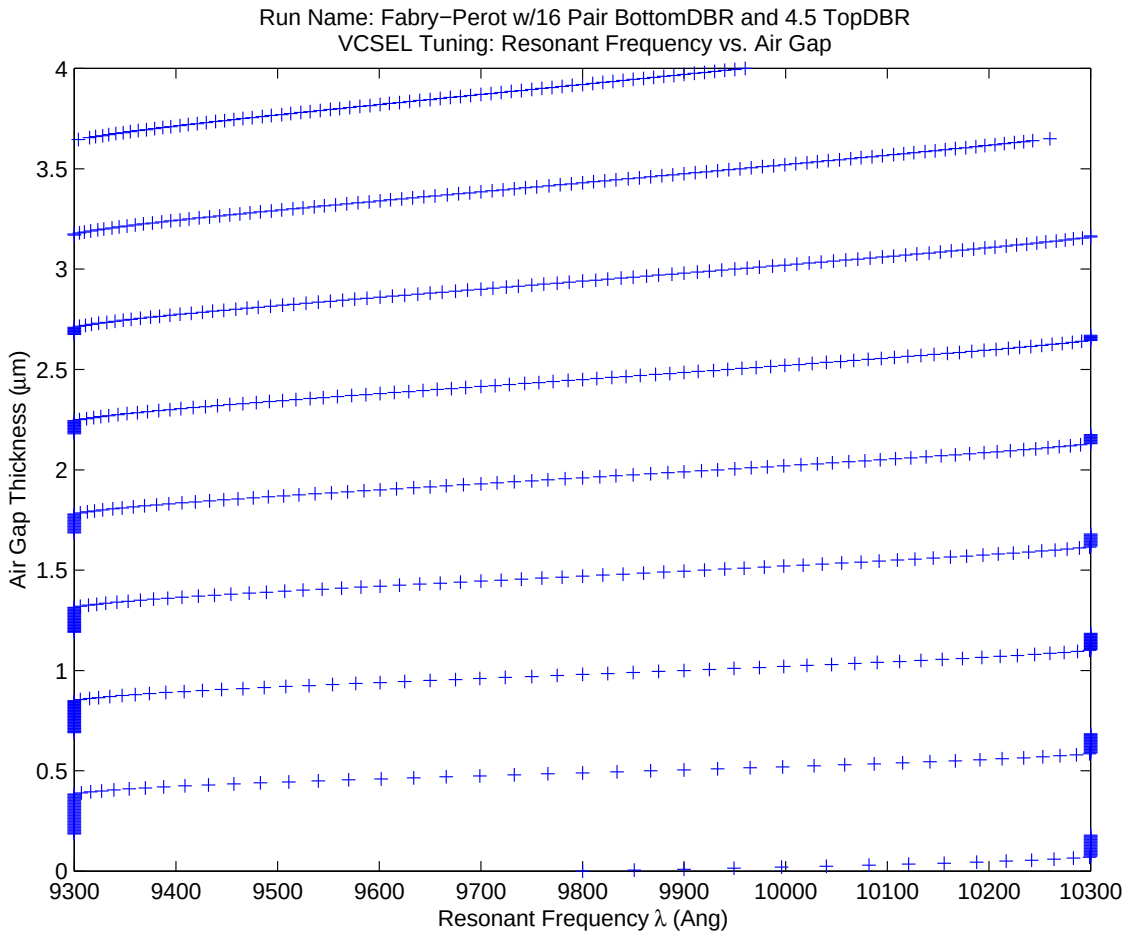


Figure 3.24 Resonant frequency of Fabry-Perot etalon vs. airgap thickness for the structure shown in figure 3.21. Note this plot only shows a resonant frequency range from $\lambda = 9300$ Å to 10300 Å due to computing limitations. The bottom tuning band extends from 8500 Å to 11000 Å. As the airgap increases the FSR of the tuning bands decreases.

3.5 Error Calculations

When depositing material by plasma enhanced chemical vapor deposition (PECVD) or by sputtering (see section C.2.4 and section C.2.2), it is difficult or impossible to control the thickness of the material down to an Angstrom. Test depositions I have accomplished show typical thickness variations on the order of ±5%, and as high as ±10%. Due to their low indices of refraction, the dielectric materials exhibit far more tolerance to thickness variations than the epitaxially grown semiconductor material.

I performed a Monte-Carlo analysis to calculate the effect of random dielectric thickness variations on the resonant frequencies of VCSEL and Fabry-Perot structures. Figure 3.25 details the results for the VCSEL device after 1000 iterations, assuming a maximum error of ±10% per iteration. Results for the VCSEL show a mean wavelength of $\lambda = 9800.9$ Å, with a standard deviation of 6.6 μm.

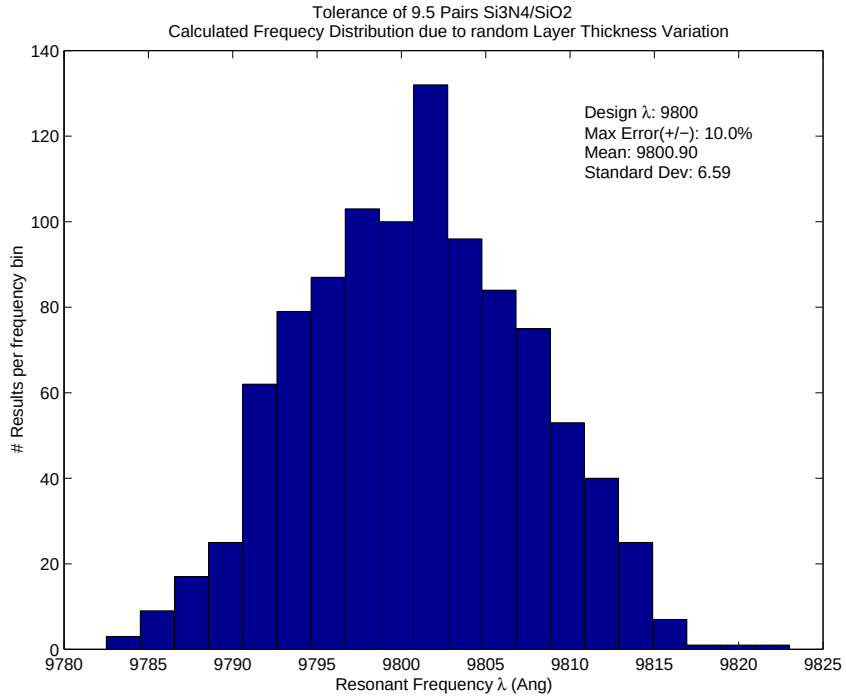


Figure 3.25 Monte-Carlo analysis of VCSEL resonant frequency distribution due to random thickness variations in the dielectric DBR layers. Maximum imposed error is ±10%, which translates into ±167 Åfor the SiO_2 layers, and ±122 Åfor the Si_3N_4 layers.

Figure 3.26 shows Monte-carlo results for the Fabry-Perot etalon structure discussed in section 3.4. Deviation in the thickness of the dielectric layers has a much greater impact on the frequency response of the Fabry-Perot vs. the VCSEL device.

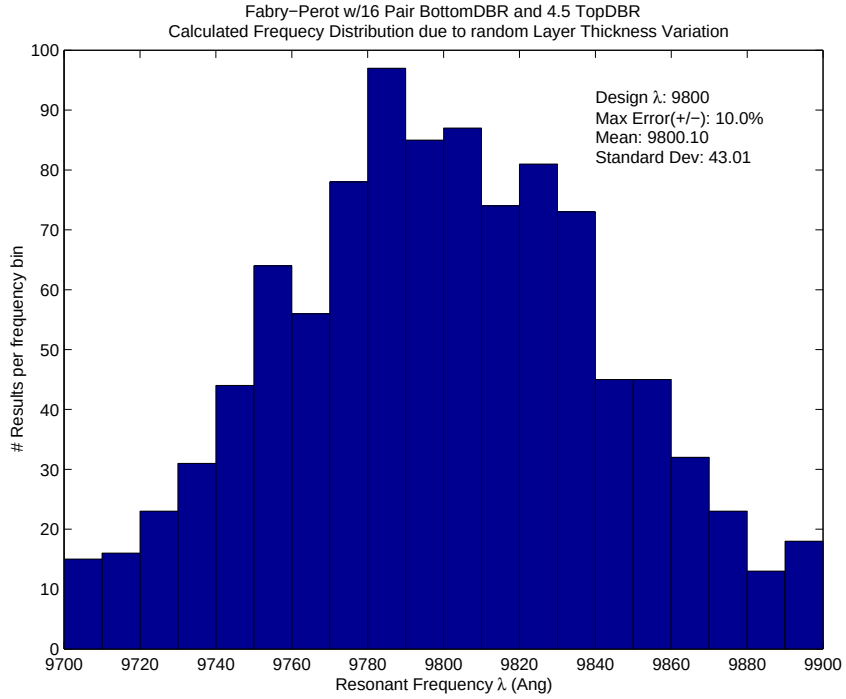


Figure 3.26 Monte-Carlo analysis of the Fabry-Perot resonant frequency distribution due to random thickness variations in the dielectric DBR layers (for the design shown in figure 3.4). The maximum possible error is ±10%, which translates into ±167 Åfor the SiO_2 layers, and ±122 Åfor the Si_3N_4 layers. The deviation of the Fabry-Perot resonant frequency is much larger than the VCSEL deviation.

3.6 Actuation Voltage Design Range

In order for tuning of my design to occur, a voltage controlled electrostatically actuated MEM structure must be fabricated on top of the epitaxially grown wafer. Before going to the CAD tools and designing the layout of the MEM devices, the actuation voltage vs. airgap was modeled in order to determine the proper device dimensions. Using the analytic equations derived in section 2.3, it is straight forward to calculate a relationship between voltage and airgap for any given MEM geometry.

For the purposes of this research, all MEM devices consist of a square top membrane suspended by four flexures attached to the wafer surface. Figure 3.27 shows the schematic layout of one such device.

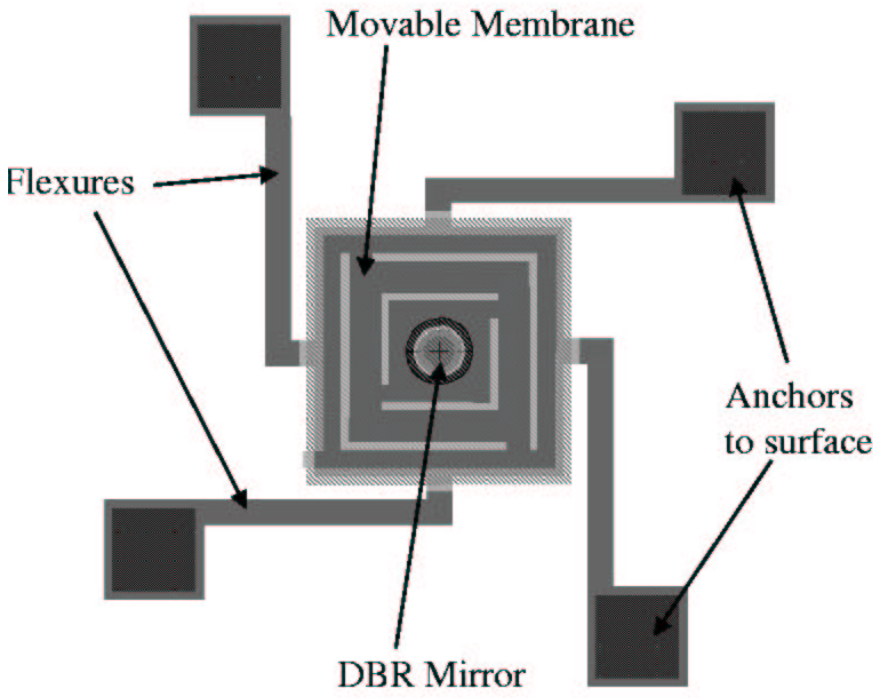


Figure 3.27 Schematic layout of MEM device with four flexures attached to the wafer surface and a 150 μm $\times$ 150 μm mechanical membrane.

As discussed in section 2.3, the following factors effect the membrane displacement vs. applied voltage relationship: flexure length, flexure width, flexure thickness, area of the top capacitor (membrane), initial airgap thickness, and the Young's modulus of the flexure material. Inserting these parameters into equation 2.18 results in a simple relationship between displacement and voltage:

$$V = \sqrt{\frac{L^3 x}{2Ehw^3\varepsilon_0 A}}(x-d) \qquad (V) \tag{3.1}$$

The goal of the this research is the design of a MEM device with a low actuation voltage. This may be accomplished by increasing the area of the membrane,

decreasing the airgap, or reducing the flexure width or thickness and increasing their length. Previous experimentation has shown that extremely narrow flexures may be difficult to fabricate correctly [3]. Therefore, a relatively wide flexure width of 15 μm is used for all device designs [2]. Gold (Au) was selected as the material for the flexure and membrane fabrication, as researchers at AFRL/SN have successfully used gold in their MEMS fabrication processes. The following calculations assume a Young's modulus value of $E = 79\ MPa$ for gold films.

I selected an initial airgap of 2 μm as the optimal gap width due to processing considerations. The thin-film polymer PMGI is utilized as the sacrificial material to define the airgap of the MEM device. The PMGI available at AFRL/SN is applied in 1 μm-thick layers, and may be spun-on twice to achieve 2 μm-thick layers.

A flexure and membrane thickness of 1 μm or 1.5 μm is used for all calculations. The remaining variables are flexure length and membrane area. Since the starting height of the airgap is 2 μm, the calculated snap-down occurs at an airgap thickness of 1.3 μm(see section 2.3). Table 3.2 presents the calculated snap-down voltage for various device configurations.

3.7 Conclusion

In this chapter the design requirements for both a tunable Fabry-Perot etalon and a tunable VCSEL were established and modeled. The design for the Fabry-Perot bottom DBR consists of 16 pairs of quarter-wave $GaAs/Al_{0.9}Ga_{0.1}As$ with a highly doped (4×10^{19} cm^{-3}) contact layer. The top DBR requires only 4.5 pairs of Si_3N_4/SiO_2 mirror layers. The requirements for VCSEL lasing were analyzed in order to determine the number of quarter-wave DBR pairs necessary to meet threshold conditions. A minimum of 26 Pairs $GaAs/Al_{0.9}Ga_{0.1}As$ are required for the bottom DBR, while a single pair on top of the microcavity was determined to provide the optimal coupling with the air cavity. Finally, at least 9.5 pairs of quarter-wave Si_3N_4/SiO_2 are required to form the top dielectric DBR stack.

Table 3.2 Calculated snap-down voltages for various device configurations with gold flexure thicknesses of 1 μm and 1.5 μm.

Top Membrane Area	**Flexure Length**	**Snap-down Voltage (1.0 μm thick)**	**Snap-down Voltage (1.5 μm thick)**
100 μm $\times$ 100 μm	70 μm	20.3 V	37.3 V
100 μm $\times$ 100 μm	80 μm	16.6 V	30.6 V
100 μm $\times$ 100 μm	90 μm	13.9 V	25.6 V
100 μm $\times$ 100 μm	100 μm	11.9 V	21.9 V
100 μm $\times$ 100 μm	110 μm	10.3 V	18.9 V
100 μm $\times$ 100 μm	120 μm	9.05 V	16.6 V
100 μm $\times$ 100 μm	130 μm	8.02 V	14.7 V
100 μm $\times$ 100 μm	140 μm	7.18 V	13.2 V
100 μm $\times$ 100 μm	150 μm	6.48 V	11.9 V
150 μm $\times$ 150 μm	100 μm	8.36 V	15.4 V
150 μm $\times$ 150 μm	110 μm	7.25 V	13.3 V
150 μm $\times$ 150 μm	120 μm	6.36 V	11.7 V
150 μm $\times$ 150 μm	130 μm	5.64 V	10.4 V
150 μm $\times$ 150 μm	140 μm	5.05 V	9.3 V
150 μm $\times$ 150 μm	150 μm	4.55 V	8.4 V
150 μm $\times$ 150 μm	160 μm	4.13 V	7.6 V
150 μm $\times$ 150 μm	170 μm	3.77 V	6.9 V
150 μm $\times$ 150 μm	180 μm	3.46 V	6.4 V
200 μm $\times$ 200 μm	120 μm	4.69 V	8.6 V
200 μm $\times$ 200 μm	130 μm	4.16 V	7.6 V
200 μm $\times$ 200 μm	140 μm	3.72 V	6.8 V
200 μm $\times$ 200 μm	150 μm	3.36 V	6.2 V
200 μm $\times$ 200 μm	160 μm	3.05 V	5.6 V
200 μm $\times$ 200 μm	170 μm	2.78 V	5.1 V
200 μm $\times$ 200 μm	180 μm	2.55 V	4.7 V
200 μm $\times$ 200 μm	190 μm	2.36 V	4.3 V

All optical modeling was performed using a tunable optical toolbox and GUI interface that I developed for the MATLAB® programming environment. This set of utilities, combined with the OENG775 toolbox [5], provides a powerful set of tools for the quick analysis of optical systems.

The actuation voltage vs. membrane deflection was calculated for every combination of membrane area and flexure length present on the final mask die (see figure 4.16). The snap-down voltage, the figure of merit for these calculations, varied from 2.36 V to 37.3 V (see table 3.2).

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IV. Mask Design and Fabrication Process

4.1 Chapter Overview

In this chapter I discuss my MEM tunable VCSEL (MTV) fabrication process, and the mask set I created to accomplish the photolithographic steps. Every attempt was made to use standard processing techniques already in place at the Air Force Research Laboratory, Sensors Directorate (AFRL/SN) and Air Force Institute of Technology (AFIT). This reduced the risk of using an untested process to fabricate a complex multi-layer MEM design. Figure 4.1 is an example schematic layout of a four flexure piston MEM device consisting of seven distinct layers. Each layer represents a photolithographic mask and a process fabrication step as presented in this chapter.

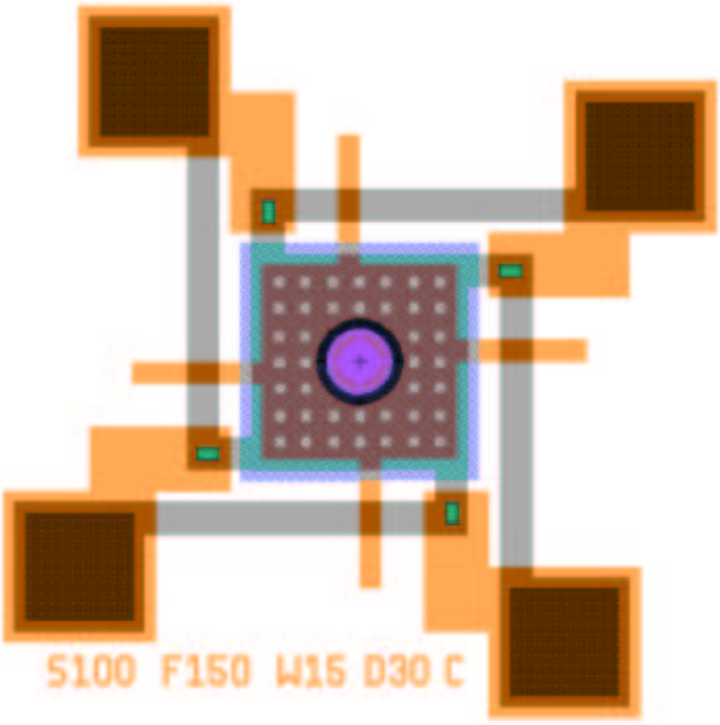
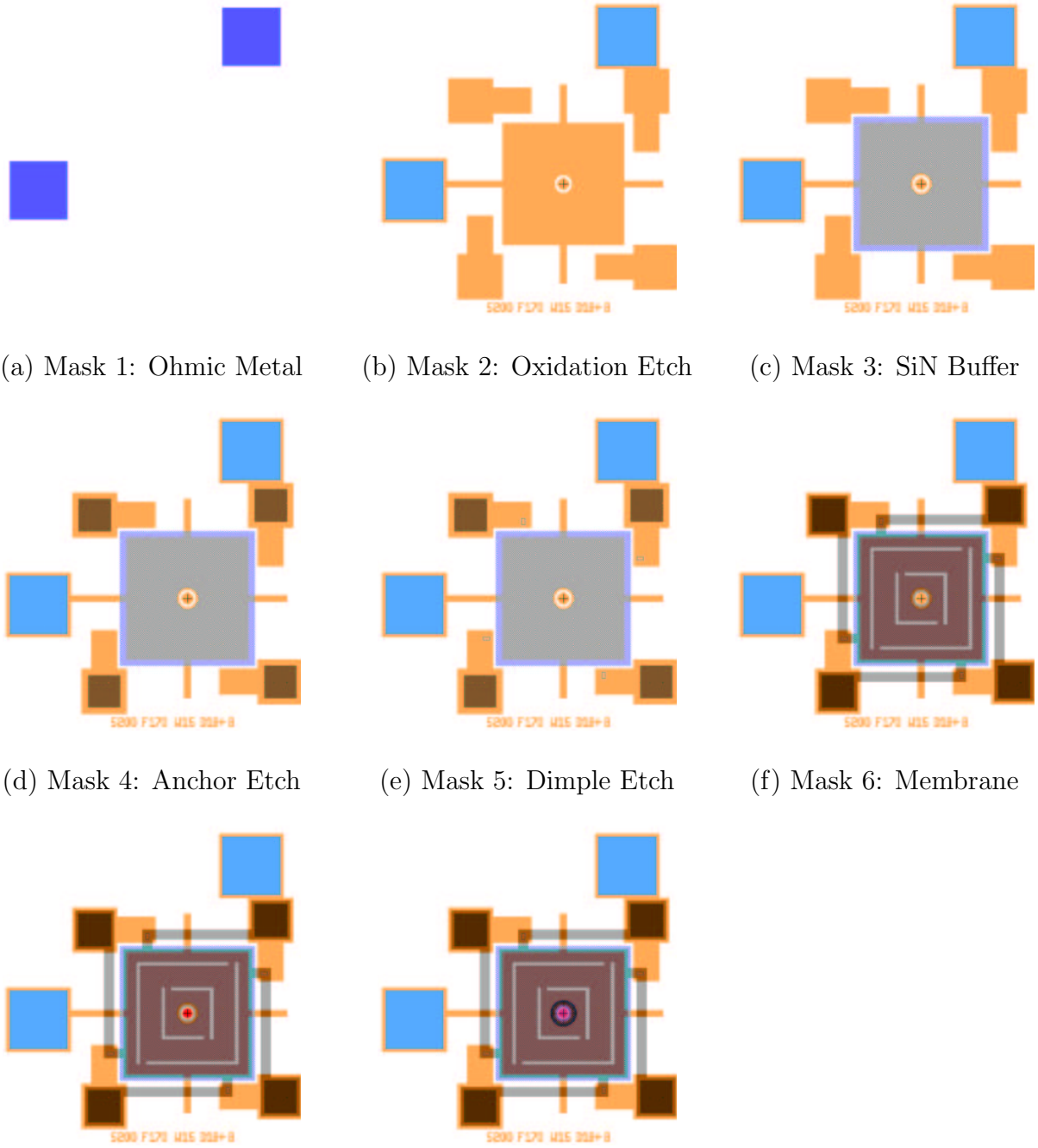


Figure 4.1 Schematic top view of a seven layer mask layout for an example MTV device.

Upon completion of the device epitaxial growth as discussed in Chapter III, the bottom DBR, the semiconductor microcavity, and the coupling mirror are in place. In order for lasing to occur, a high reflectivity top mirror must be fabricated. A voltage controlled, electrostatically actuated top DBR mirror is my design goal. In order to accomplish this, I developed a custom MEMS fabrication process consisting of nine primary construction steps. These steps include the deposition of metal contact pads and alignment marks, the RIE patterning of the wafer surface to define wires and device electrodes, an Si_3N_4buffer layer, the application and patterning of a sacrificial layer, deposition of the membrane and flexure material, deposition of the top DBR mirror, metallization of the wafer backside, and finally the release of the sacrificial material. I designed eight photolithographic masks to pattern the deposited thin film materials into a complete set of MEM devices. I later eliminated mask #7 from the design process, leaving a total of seven mask steps. Figure 4.2 shows the process flow for an example device. Laboratory processing steps are shown in detail in appendix A.

4.2 Ohmic Metal Deposition

4.2.1 Bond Pads. The first processing step is a simple ohmic metal deposition and lift-off using a positive lift-off resist (LOR) known as LOR-3A and a positive photoresist known as 1813 (see section C.3 for background information on photolithography). LOR-3A is applied directly onto the wafer surface by spinning-on, resulting in a layer thickness of 300 nm. The 1813 resist is then spun-on over the LOR-3A with a thickness of 1.3 μm, resulting in total resist height of 1.6 μm. The 1813 photoresist is exposed through mask #1 to ultra-violet (UV) light at a wavelength of $\lambda = 405$ μm. Mask #1 is a darkfield mask (defined in section C.3.1), and most of the resist remains un-exposed and therefore intact during development of the resist stack. This step removes the resist wherever bond pads and bottom alignment marks are to be placed onto the wafer surface.



(a) Mask 1: Ohmic Metal (b) Mask 2: Oxidation Etch (c) Mask 3: SiN Buffer

(d) Mask 4: Anchor Etch (e) Mask 5: Dimple Etch (f) Mask 6: Membrane

(g) Mask 7: Optional PMGI (h) Mask 8: Dielectric Top DBR

Figure 4.2 Process flow for MTV fabrication. Sacrificial PMGI, 2 μm-thick, is spun-on between deposition of the silicon nitride buffer layer (mask #3) and the anchor etch (mask #4).

Upon completion of the lithography the wafers are placed into a metallization system, where 400 Å of Titanium (Ti) and 2200 Å of Gold (Au) are evaporated onto the wafer surface. The Ti is an adhesion layer which helps to bond the gold to the wafer wherever there is an opening in the resist. After completion of the metallization step, the unwanted metal is easily removed via a tape lift-off or a simple acetone soak (see appendix A).

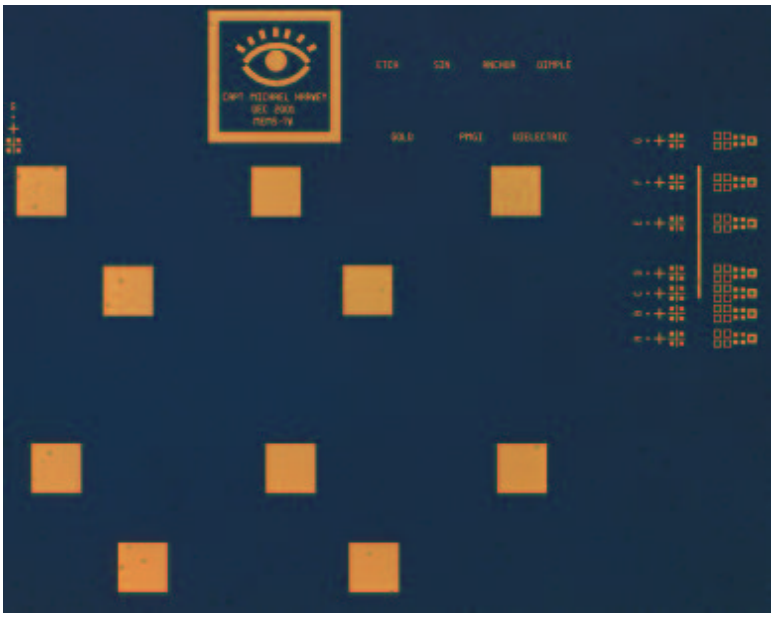


Figure 4.3 First Processing Step - spin-on resist is patterned before the metallization step. The small squares are the contact pads attached to each device. Each device has a ground contact and a positive contact to electrically actuate the mechanical membrane. After completion of ohmic metal evaporation (400 Å Ti/2200 ÅAu) and lift-off, alignment marks and contact pads are clearly defined on the surface.

Bond pads are fabricated on the wafer surface in order to provide a current path between the highly doped p+ GaAs wafer surface and any test probes or wire bonds. They are necessary to provide a voltage potential to actuate the MEM devices and activate the VCSELs. Each 5mm x 5mm square wafer die contains 63 separate devices. Figure 4.4b shows the primary bond pads for all 63 devices. One pad is reserved for the ground connection. The metal box enclosing the area is attached to the grounded bond pad and to the electrode of each device. In addition, each device

is fabricated with two smaller bond pads, as shown in figure 4.2-mask1. These 75 μm $\times$ 75 μm bond pads provide a set of contacts to activate individual devices directly (in case wire resistance is high).

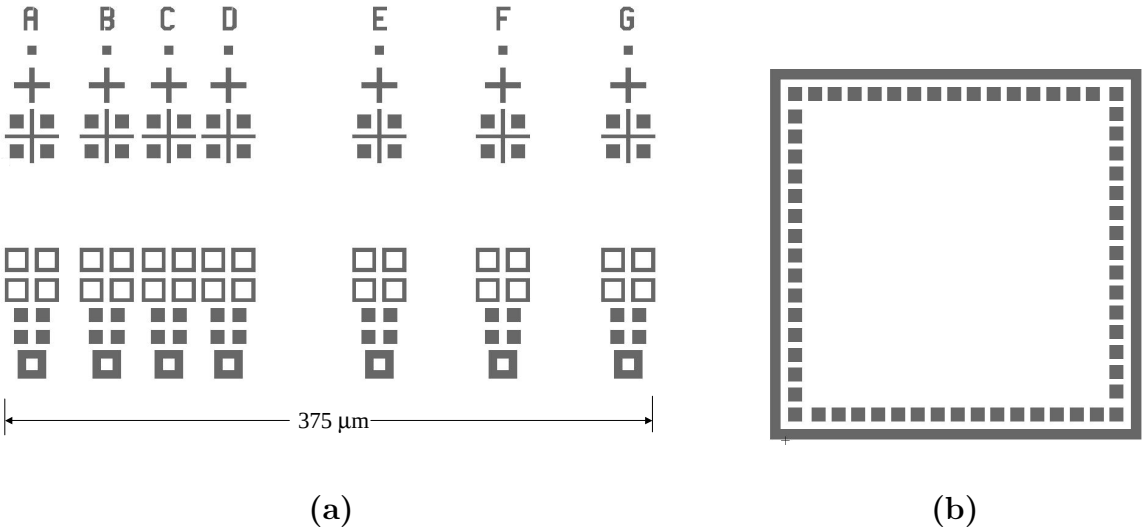


Figure 4.4 Schematic of (a) alignment marks fabricated during ohmic contact deposition and (b) 64 200 μm $\times$ 200 μm ohmic metal bond pads enclosing a 5 mm $\times$ 5 mm device fabrication area. A metal ground bar surrounds the bond pads.

4.2.2 Alignment Marks. Alignment marks were designed to ensure the accurate placement of eight device fabrication steps. Typically, in order to ensure the correct placement of a series of mask lithography exposures, a computerized mask aligner, known as a "stepper," is used to accurately align each layer. Due to limitations in the amount of material available for this research project, a full 3-inch wafer was broken into quarters before fabrication of the MEMS devices. Unfortunately, the stepper system at AFRL/SN isn't capable of processing quarter wafers. Therefore, each mask must be manually aligned before exposure of the photosensitive material on the surface. This requires a series of alignment marks to be placed on the surface during the first processing step. The second mask step (section 4.3) uses the alignment mark labeled "A", as shown in figure 4.4a. The third mask step uses "B", and so on, until the completion of the device with mask eight and alignment mark "G".

Since a certain amount of error is inevitable when aligning the masks, a tolerance of 5 μm was designed into the fabrication of the device mechanical components (i.e. flexures, anchors, membranes). A tolerance of 3 μm was built into the alignment of the optical components at the center of each device (i.e. dielectric DBR mirror, gold etch hole, SiN etch hole, oxidation etch holes). If the alignment error is between 3 μm and 5 μm, the VCSEL devices might still function, but with degraded performance. If the alignment is off by greater than 5 μm, the devices are not expected to function.

4.3 Oxidation Etch

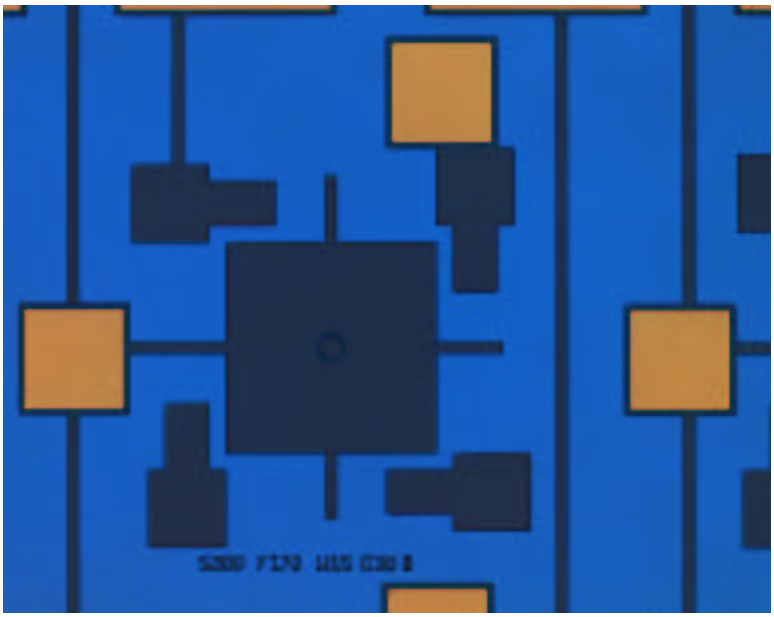
The purpose of the oxidation etch step is to create an oxide aperture which limits the area of the current passing through the active gain region of the VCSEL device. If the current aperture radius is designed correctly, the VCSEL device will be forced to operate in a single fundamental mode. Single mode operation is highly desirable for most VCSEL application, including fiber optic communications.

The oxidation etch is accomplished by etching through the epitaxially grown p-doped GaAs top layer and down through the microcavity. This performs two functions: it allows areas of the surface to be electrically isolated from each other (since the microcavity is primarily undoped GaAs), and it provides access to the $Al_{0.98}Ga_{0.02}As$ layers directly above and below the microcavity. The surface is then exposed to an oxidation system (steam at 400 $\circ$C), and the $Al_{0.98}Ga_{0.02}As$ is converted to aluminum oxide (AlO_x). While oxidation is occurring, the diameter of the $Al_{0.98}Ga_{0.02}As$ laser aperture is steadily reduced until removed from the steam environment. The dielectric AlO_x functions as a current aperture and stops current flow from occurring where it is not wanted. Figure 4.5 is a microscope image of the etch holes defining the laser aperture.

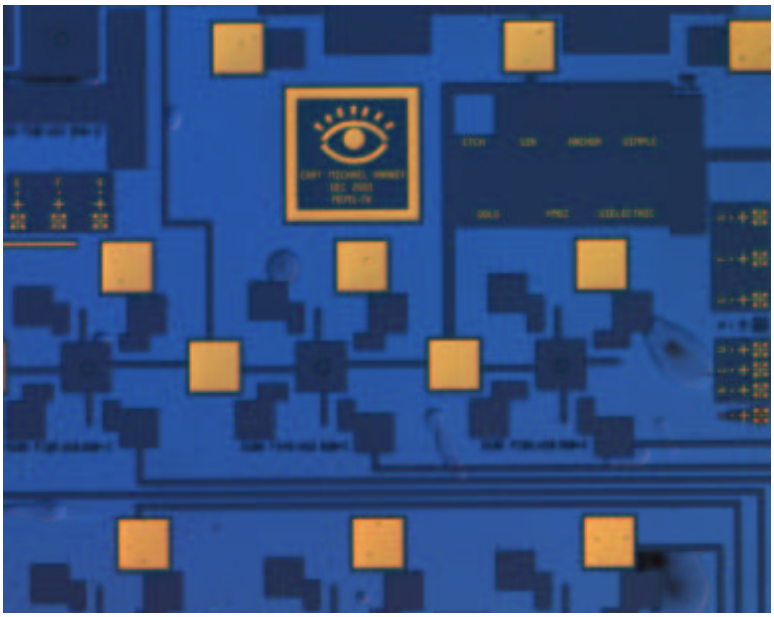
This etch step is accomplished by spinning on a layer of 1813 positive photoresist. Since the removal of the surface material is subtractive, a clearfield mask is

Figure 4.5 Microscope view of device oxidation etch holes. After etching by RIE, the $Al_{0.98}Ga_{0.02}As$ layer is exposed and oxidized in water vapor. The resulting oxide aperture acts as a current funnel for the VCSEL.

used when exposing the 1813 photoresist to UV radiation. The $Al_xGa_{1-x}As$ layers are dry etched by RIE using a mixture of boron trichloride (BCL_3) and chlorine gas at a rate of 5000 Å per minute. Moderate overetching won't have a negative effect on device operation, so the exact etch rates are not critical to this fabrication step. Figure 4.6 is a microscope image of the RIE patterned wafer surface, showing clear definition of the bottom electrodes and surface wiring.



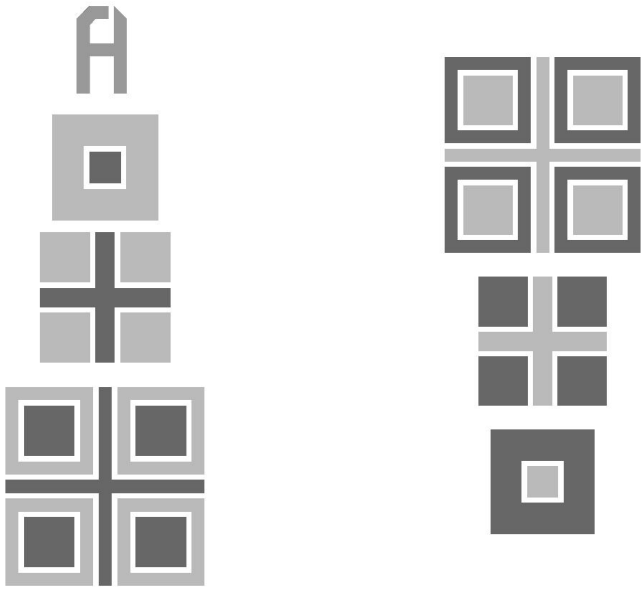
(a)



(b)

Figure 4.6 Microscope image of (a) resist pattern before etching of the wafer surface. The dark areas covered by a layer of resist are protected from the anisotropic RIE etch. Unprotected areas are exposed to the RIE plasma etchant, and the top DBR mirror stack is removed. (b) After etching, the protected areas have a step height of approximately 2.5 μm over the etched surface. Note that portions of the etched surface appear uneven. This is due to resist "scum" left on the surface before etching, and was fixed in later runs by performing a oxygen plasma etch before RIE etching.

Since this process step requires a clearfield mask, the alignment marks must be appropriately designed. Figure 4.7 shows a close up of the top and bottom alignment marks for the oxidation etch patterning aligned with the previously deposited ohmic metal alignment marks. When designing the alignment marks for a clearfield mask, the opaque pattern must be placed so the metal on the wafer surface can be clearly seen through the transparent gaps in the mask and correctly aligned.



(a) **(a)**

Figure 4.7 Schematic design layout of top (a) and bottom (b) alignment marks for a clearfield mask such as Mask 2 (oxidation etch). The dark material is gold deposited during the first ohmic metal step. The lighter material represents the chromium on the surface of the quartz mask. These marks must be visually aligned at locations throughout the mask pattern to ensure correct alignment of every device.

4.4 Silicon Nitride

One difficulty when dealing with MEM actuated devices such as piston micromirrors, is the phenomenon known as stiction. Stiction occurs when the top electrode of a deformable microstructure is forced into contact with the substrate

and won't release. Stiction problems are most prevalent during the wet release of the sacrificial layer [1], but are also known to occur during operation of a device after "snap-down". "Snap-down" of a top membrane to the bottom electrode takes place when the downward pressure of the electrostatic force overcomes the spring force of the flexures. This typically happens as the membrane is deflected past the 1/3 point of the device's airgap (see section 2.3). Sometimes the device will snap back into place when the electric field is removed, but often the device will remain stuck to the electrode permanently. Snap-down of the top membrane to the bottom electrode will also short out the contacts and may cause permanent damage to the device or its wiring.

To help reduce stiction and eliminate the possibility of shorting the device, a dielectric buffer 3000 Å thick is deposited via PECVD or sputtering directly over the bottom DBR as shown in figure 4.8. Note in figure 4.9, that a circle of Si_3N_4 has been removed from the center of the electrode in order to eliminate optical interference due to the dielectric layer. Therefore, it isn't necessary to precisely monitor the step height of the Si_3N_4 layer to match it to the optical cavity resonance frequency.

Positive 1813 photoresist is then spun-on and patterned using mask 3. As the removal of the SiN is a subtractive process, mask #3 is clearfield and uses alignment marks identical to mask #2 as shown in figure 4.7. After developing (removing) the unwanted resist, an RIE dry etch is performed using a freon etchant known as CF-23 (CHF_3O_2). This removes the SiN layer at a rate of approximately 100-200 Å per minute [2].

4.5 Anchor

At this point in the fabrication process, it is necessary to deposit a layer of sacrificial material. All addition fabrication steps will be performed on top of this layer. Upon completion of the entire device structure, the final processing step will be the release, or etch removal, of the sacrificial material. This will leave the device

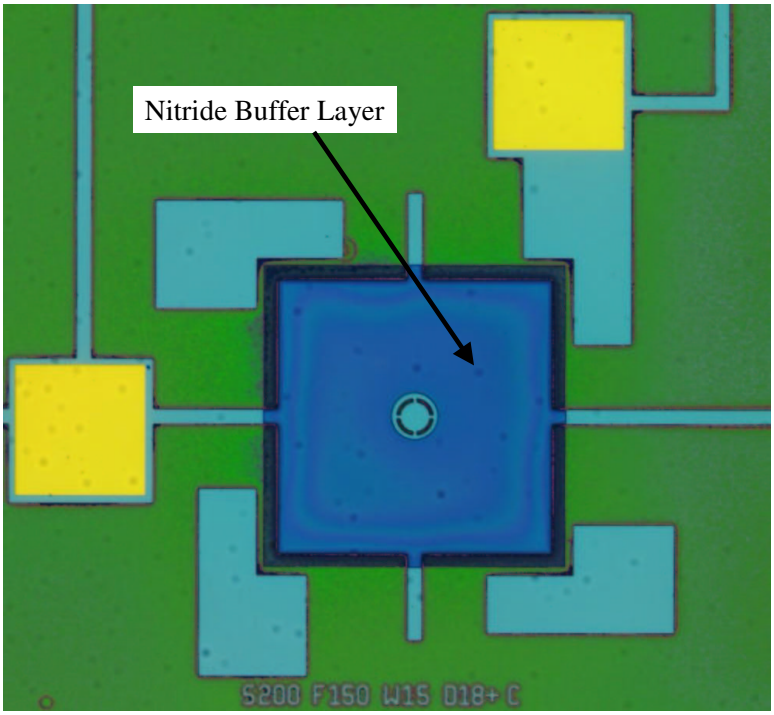


Figure 4.8 Microscope top view showing silicon nitride dielectric buffer alignment on device. A circle is left open over the optical aperture to ensure no interference with the optical cavity.

structures standing freely with an airgap where the sacrificial layer was previously located. Therefore, the thickness of the sacrificial layer defines the airgap of the device. Since the VCSEL portion of the device has been designed to operate at $\lambda = 980\,nm$, an airgap starting at 2 μm will allow deflection of the top mirror through a complete tuning range before snap-down occurs at 1.33 μm(see figure 3.11).

An existing MEMS fabrication process at AFRL/SN utilizes a PMGI known as SF-11 [4]. SF-11 is spun-on in 1 μm layers. Therefore it is necessary to spin-on and softbake two layers of SF-11 to achieve the desired thickness (see appendix A). Two layers of SF-11 have an experimentally determined thickness of approximately 2.15 μm. This is close enough to have only a minor impact on device operation.

Before deposition of the top membrane, post holes must be etched through the PMGI layer. These post holes allow the membrane flexures to be anchored to

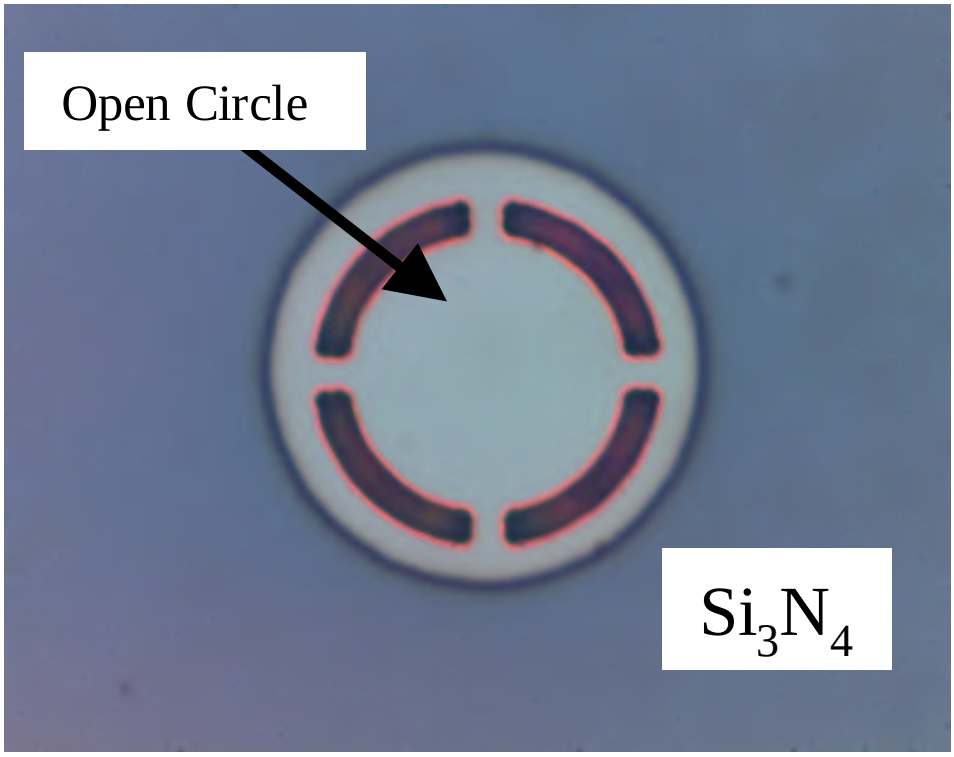
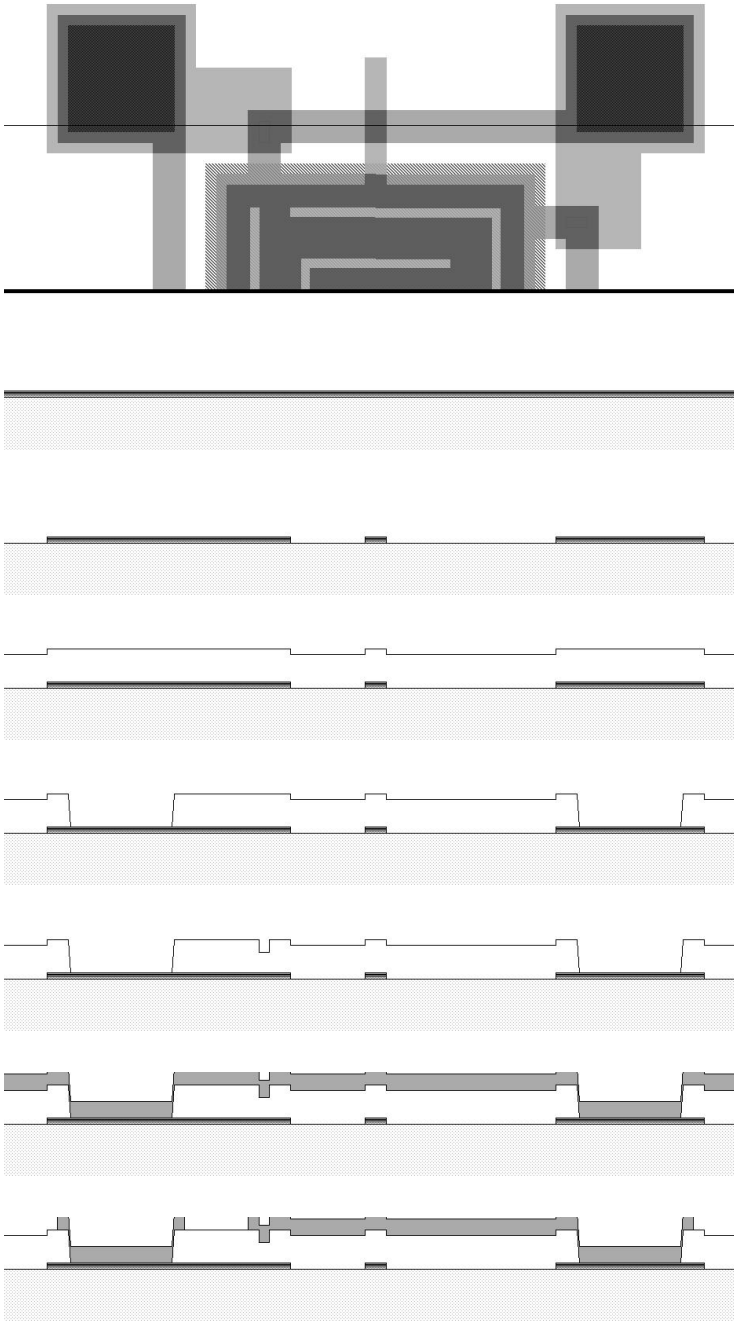


Figure 4.9 Microscope top view of silicon nitride dielectric buffer over GaAs wafer. A circle is left open over the optical aperture to ensure no interference with the optical cavity.

the surface of the device and provide a path for current to reach the top electrode. Figure 4.2d shows the placement of four post holes over small contact pads on each corner of the device. Note the top right anchor is attached directly to a bond pad. Figure 4.10 details the process flow for fabrication of the anchors.

Patterning of the PMGI is accomplished by spinning-on a layer of 1813 photoresist, exposing it to the anchor mask (mask 4), and removing (via 351 developer) the unwanted portions. Since 1813 photoresist is only removed where an anchor hole is needed, mask 4 is darkfield. The wafer is then exposed for 200 sec to a deep ultraviolet (DUV) source and developed in a PMGI developer known as SAL 101. Due to the thickness of the PMGI layer, the DUV and develop step must be repeated a second time to completely remove the PMGI down to the wafer surface. Figure 4.11 is a microscope view showing the anchor holes through the PMGI sacrificial layer.



(a) *Initial Substrate*

(b) *Mask 2: Oxidation Etch*

(c) *2 μm PMGI Deposition*

(d) *Mask 4: Anchor Holes*

(e) *Mask 5: Dimple Holes*

(f) *1 μm Au Evaporation*

(g) *Mask 6: Au Lift-off*

Figure 4.10 Cross section of process flow for fabrication of anchors. Note that several steps with no impact on anchor construction have been skipped, including ohmic metal deposition, SiN buffer deposition, and fabrication of the dielectric DBR mirror.

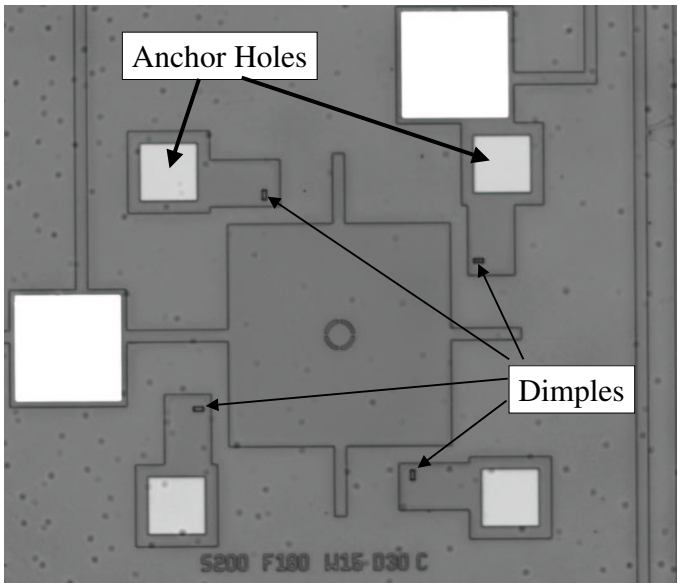
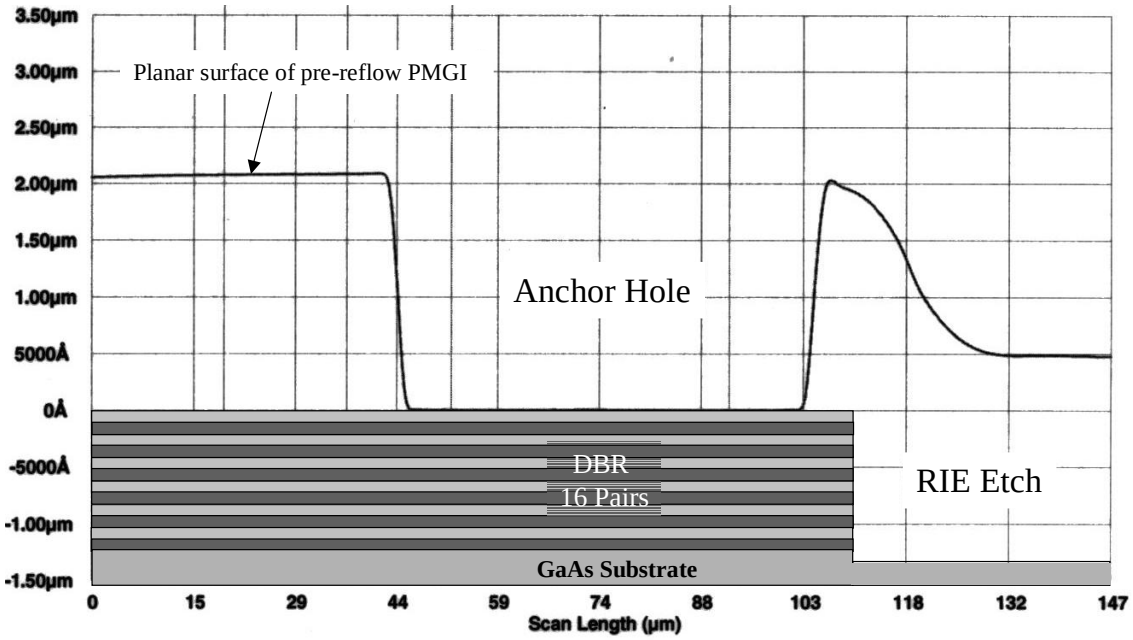
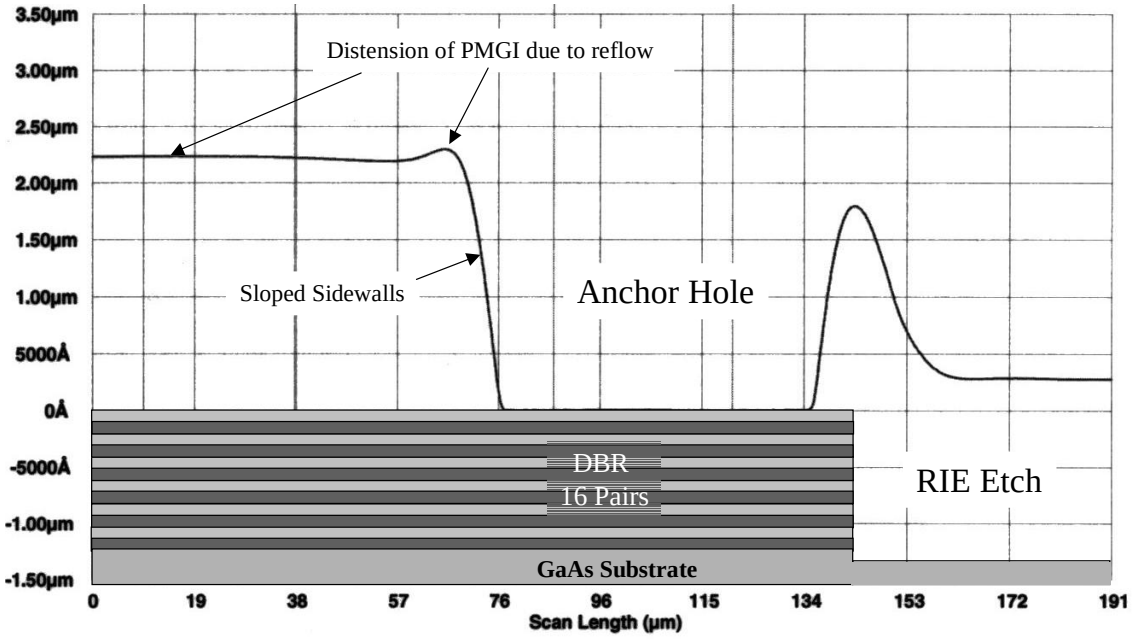


Figure 4.11 Microscope image highlighting anchor and dimple patterning of PMGI sacrificial layer. The anchor holes are clear down the surface of the wafer (2 μm deep). The dimple holes are only 0.75 μm deep.

After stripping the remaining 1813, the PMGI goes through a process known as "reflow". Although the PMGI was softbaked after application, it will soften and begin to flow at the relatively low temperature of 250 °C. After 90 sec in a hot air bake oven, the PMGI has begun to reflow and the previously sharp 90 ° sidewalls of the post holes are well rounded (see figure 4.12). The rounded edges of the post holes will allow the 1 μm of gold evaporated as the top membrane layer to cover the sidewalls of the holes and anchor to the surface.



(a)



(b)

Figure 4.12 Surface profile measurements of (a) pre-reflow and (b) post-reflow anchor holes. After reflow processing, the sidewalls of the PMGI anchor openings are sloped. Evaporated metal will stick to these sidewalls and connect the movable membrane to the wafer surface. Note that these plots are on different scales.

4.6 Dimple

In order to decrease the possibility of stiction of the membrane to the bottom electrode, one dimple is placed on each flexure as shown in figure 4.13. These dimples hang 0.75 μm below the flexures, and are the first objects to make contact with the surface when snap-down occurs. The dimples keep the membrane from contacting the electrode, thereby reducing the possibility of short-circuit and stiction.

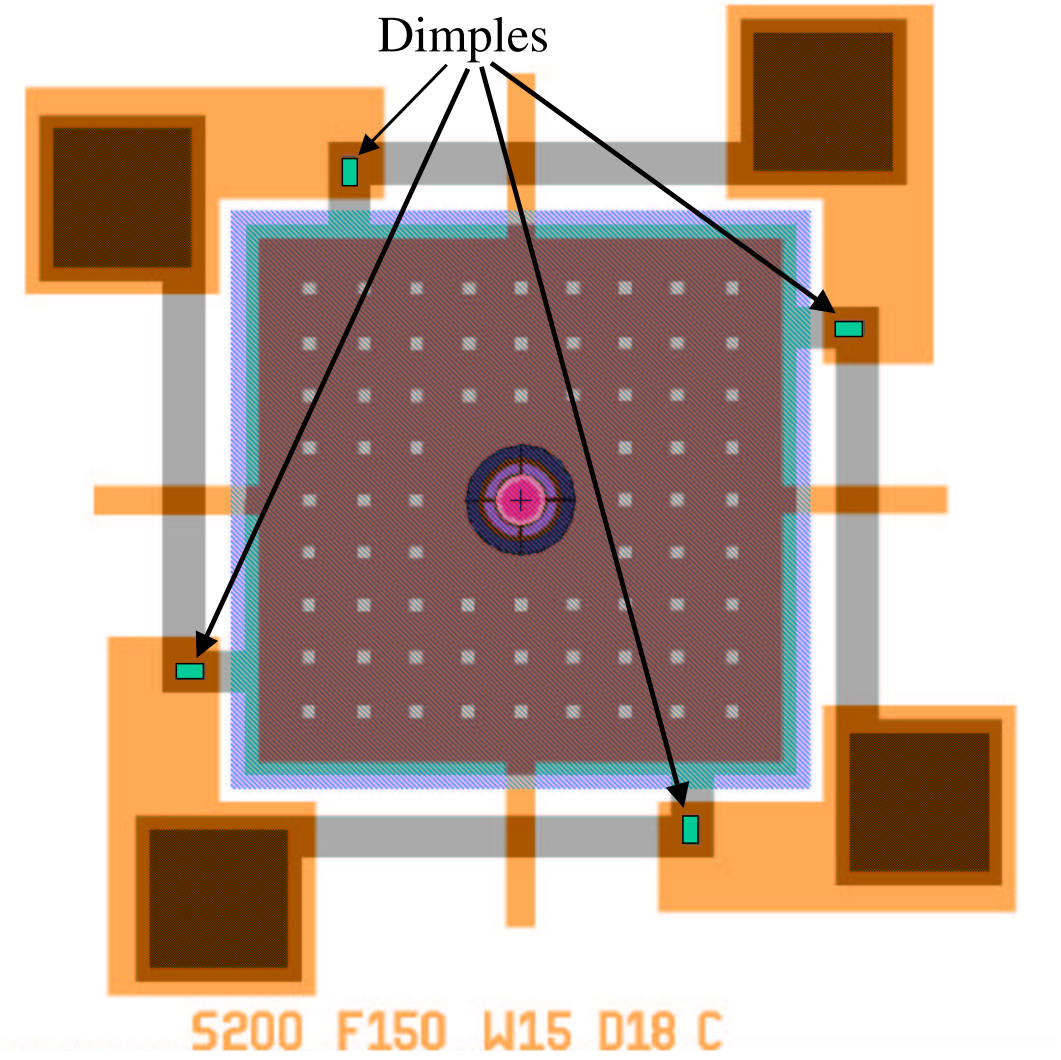


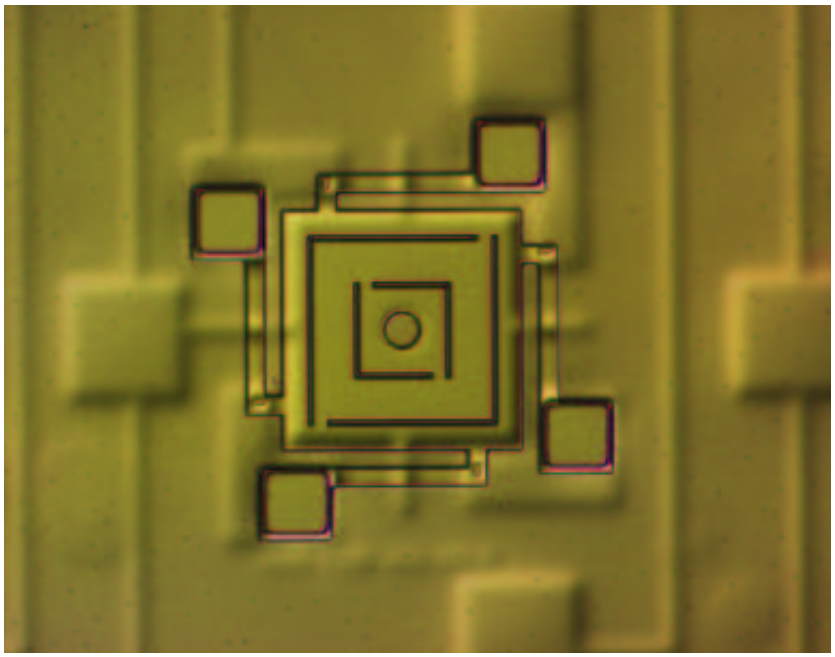
Figure 4.13 Schematic top view of device highlighting dimples.

The dimple fabrication process is very similar to the anchor post-hole removal. As with the anchor step, 1813 is spun-on to the PMGI. Once again, since a very small area of the 1813 will be removed, the dimple mask is darkfield. After exposure and patterning of the photoresist, a 100 sec "partial" DUV is performed which only exposes the PMGI near the surface. Upon development with SAL 101, a shallow dimple approximately 0.75 μm deep is left in the PMGI surface. After deposition and patterning of the gold membrane and flexures, four gold dimples hang down from each device.

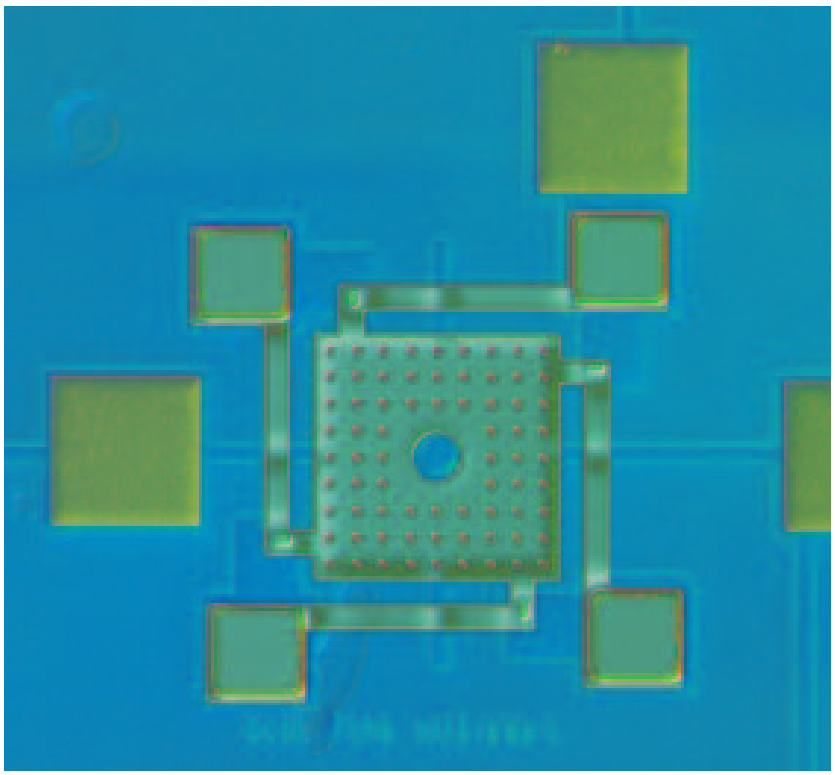
4.7 Membrane Evaporation

The mechanical portion of each MEM device is constructed of a gold membrane either 1 μm or 1.5 μm thick. The processing of this thick metal deposition is similar to the ohmic metal evaporation and lift-off described in section 4.2, but on a larger scale.

Since the evaporated metal is so thick, the lift-off resist (LOR) must be thick as well. A resist known as LOR-10A is spun directly onto the surface of the PMGI, forming a layer approximately 1 μm thick. On top of the LOR-10A a thick layer of 1818 photoresist is applied, with a height of approximately 2 μm. This stack of resist is exposed to UV through mask number 6 and developed using the developer LDD26W. After patterning and development of these layers, the lift-off step height will be 3 μm. If the resulting pattern is sharp, with well defined resist edges, the lift-off of 1 μm or 1.5 μm evaporated gold should proceed with ease (as shown in figure 4.14). If the edges of the resist are fuzzy or ill-defined, there might be problems with the lift-off of smaller features. This is due to the formation of gold stringers on the sloped sidewalls of poorly defined resist patterns (see figure 5.5).



(a)



(b)

Figure 4.14 Microscope image of 1 μm gold evaporation onto PMGI (a) before lift-off of excess gold and (b) after gold lift-off. After lift-off the membrane structure and flexures are clearly defined.

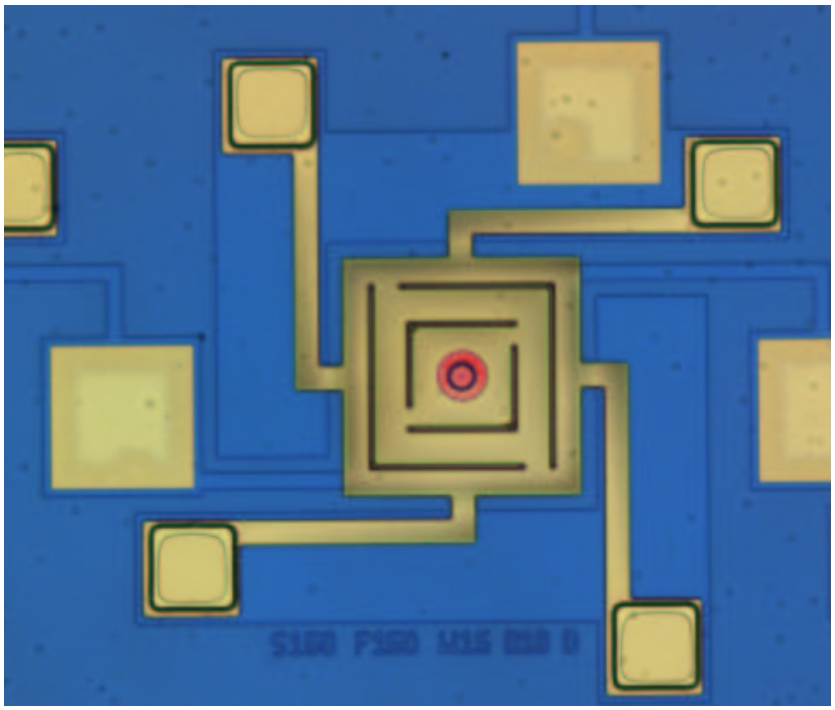
4.8 Dielectric DBR Mirror Deposition

Upon completion of a successful metal lift-off, the device is ready for the final fabrication step. In order to create an optical cavity, a highly reflective DBR mirror stack must be deposited and patterned over the central hole in the gold membrane. Since this stack is composed of quarter-wave layers of Si_3N_4 and SiO_2, is may be deposited either via PECVD or sputtering. One disadvantage of the sputtered Si_3N_4 is it's resistance to the etchant CF-23. Due to this, it must be removed with a more aggressive freon enchant known as CF-14 (CF_4). Unfortunately, as it removes the Si_3N_4 layers, the CF-14 severely undercuts the SiO_2 layers. Therefore, the PECVD system was used to deposit the dielectric DBR mirror stack.

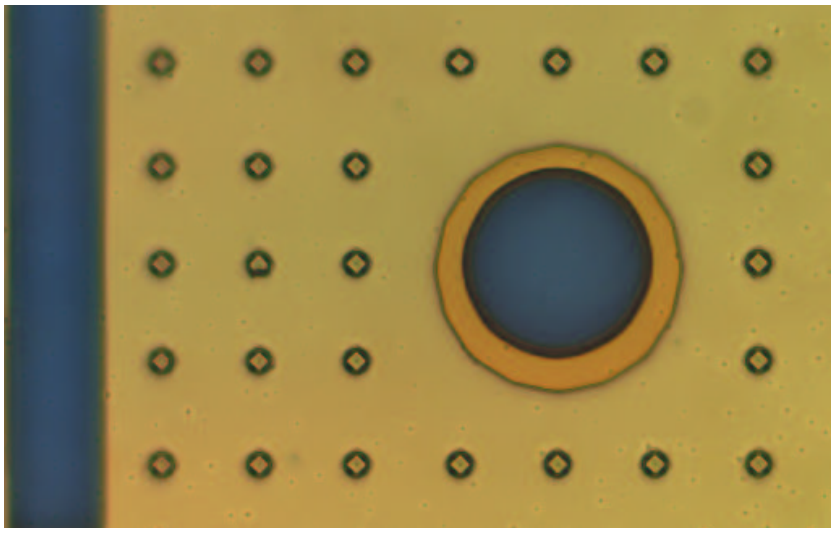
The standard PECVD formula requires a plasma temperature over 250 °C. Since this will cause the PMGI to reflow, a lower temperature process (200 °C) is used. For construction of the Fabry-Perot etalon device, a mirror stack of at least 4.5 pairs Si_3N_4/SiO_2 must be deposited to achieve a reflectance of 93%. When fabricating a VCSEL device, at least 9.5 pairs must be deposited in order for lasing to occur.

Upon completion of the dielectric stack deposition, 1818 photoresist is spun-on and patterned using mask #8. This mask has a clearfield pattern which only leaves the resist covering a circle of dielectric material at the center of the gold membrane. Since quarter-wave layers of Si_3N_4 and SiO_2 have a thickness of 1222 Å and 1667 Å respectively, a stack consisting of 9.5 pairs is 2.72 μm thick. This is a significant amount of dielectric material to pattern, considering a CF-23 etch rate of 100 Å-200 Å per minute. At best it will require 2 1/2 hours in the RIE plasma etcher, and there will be some undercutting of the top layers due to their long exposure time.

Figure 4.15 shows a successful mirror deposition of 3.5 pairs of Si_3N_4 and SiO_2 quarter-wave layers. An SEM image of the completed DBR mirror stack can be seen in figure 5.4.



(a)



(b)

Figure 4.15 Microscope images highlighting dielectric DBR mirror at center of device membrane. This mirror consists of 3.5 pairs Si_3N_4 and SiO_2 quarter-wave layers. (b) is a closeup of a device membrane showing the completed DBR mirror. Note the failure of the metal lift-off to remove small features such as the 4 μm$\times$ 4 μm etch holes.

4.9 Backside Metallization

When constructing a tunable Fabry-Perot device, fabrication is complete after the processing of the top DBR mirror. When a tunable VCSEL is being fabricated, a backside metallization must be performed in order to provide a contact to activate the laser. Since the surface electrode is grounded, a negative voltage must be applied to the backside contact for lasing to occur.

The wafer of interest must first be mounted upside-down onto a sapphire substrate using crystal bond 509. With a Q-tip, the exposed surface of the sapphire wafer is coated with a layer of 1818 photoresist. After a 5 min hot plate bake at 110 °C the wafer is ready for metallization. A standard n-type ohmic contact formula, consisting of 500 Å Au, 400 Å Germanium (Ge), 400 Å Nickel(Ni), and 1000 Å Au, is evaporated onto the exposed wafer backside. After removal from the sapphire substrate and cleaning with acetone, the laser fabrication process is complete.

4.10 Device Packaging

At this time, before the sacrificial PMGI is removed, the wafer die is cut into quarters for future packaging. The complete die is divided into four subcells, each consisting of 63 separate devices. These are designed to fit onto a standard 64 pin package (see figure 4.16). There are 64 outer bond pads (200 μm $\times$ 200 μm) designed for wire bonding to the package casing. Each of these large bond pads are connected to individual devices through wiring defined on the surface by the RIE etch discussed in section 4.3.

4.11 Removal of Sacrificial PMGI

Now that the fabrication is complete, the sacrificial PMGI must be removed from the wafer. This last critical step releases the airgap between the gold membrane and the wafer surface, allowing actuation of the tunable device. This step can lead to the destruction of the delicate gold structures if not handled properly [3].

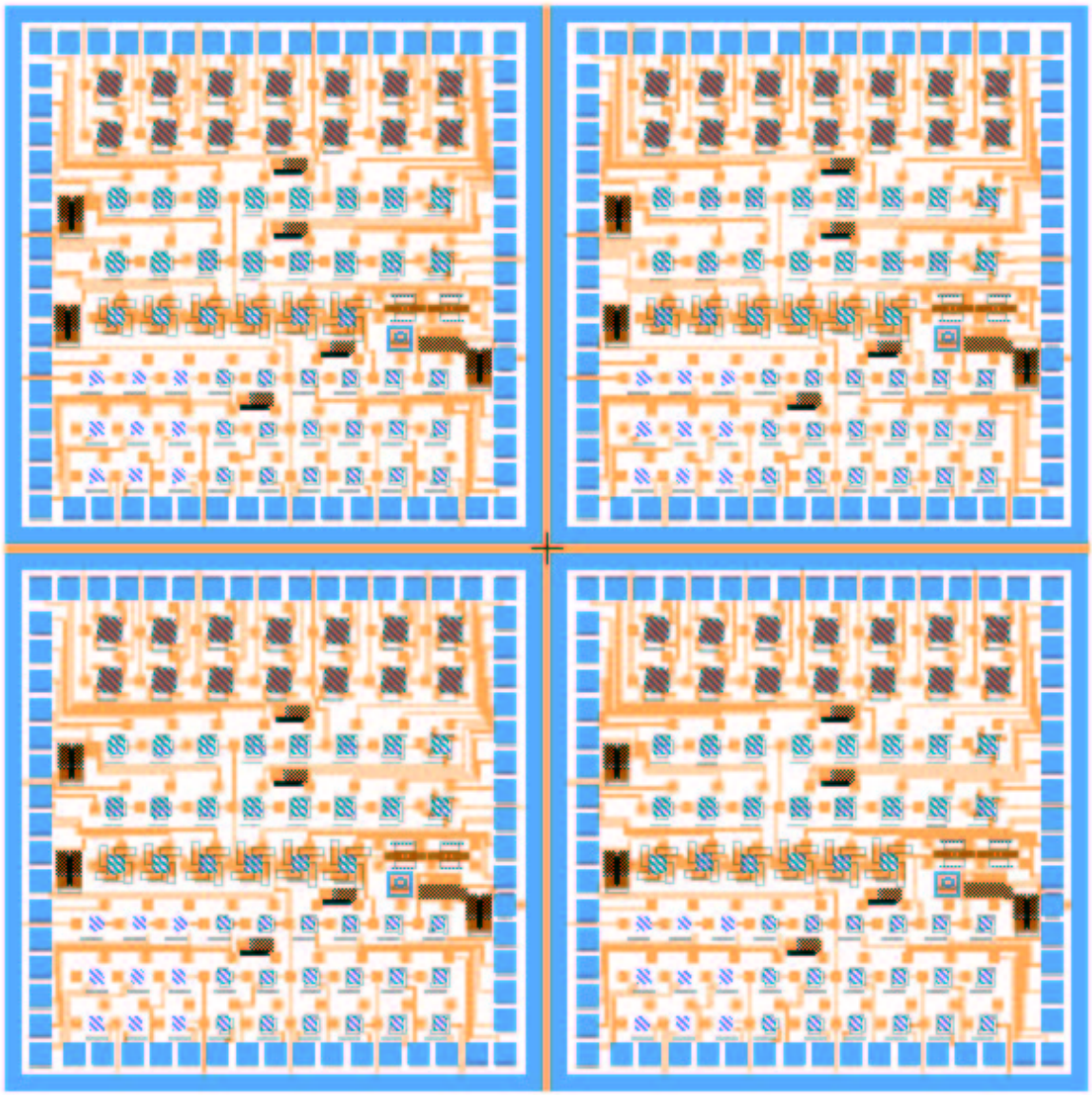


Figure 4.16 Schematic top view of complete wafer die. The die is composed of four separate quarters, each designed to fit into a standard 64 pin package. One ground pin, and one connection pin for each of the 63 devices. Use of packaging should greatly improved the ability to test devices.

A chemical solvent known as 1165 is used to strip the PMGI. The 1165 is heated to 90 °C on a hotplate, and the wafer is submerged for 30 min. After 30min the PMGI is completely removed from the wafer. The released wafer must be transferred immediately to a deionized water (DIW) bath before the 1165 has a chance

to evaporate. After one minute submerged in the DIW, the wafer is transferred to a sealed container filled with methanol, where it is safe to transport to the CO_2 dryer.

After placing the individual wafer quarters into the CO_2 dryer (one piece at a time), the methanol surrounding the devices is safely removed without introducing damaging stress or stiction. Figure 4.17 is an SEM showing completely released devices upon removal from the CO_2 dryer.

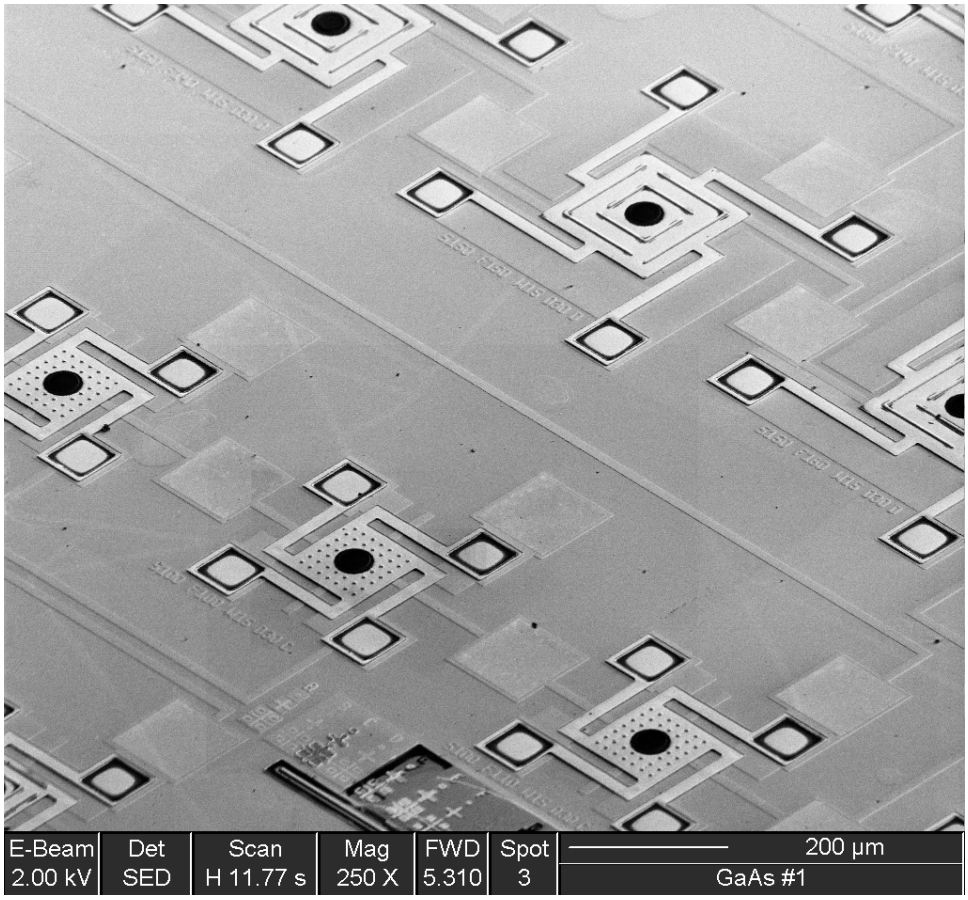


Figure 4.17 SEM image of released devices.

4.12 Conclusion

In this chapter I discussed the processing required to construct an electrically actuated Fabry-Perot etalon and MTV device. For specific details of the lab procedures, see the process followers I prepared for use in the cleanroom (Appendix A).

Details of the eight layer mask design were only briefly discussed. As shown in figure 4.16, the complete mask layout is very complex and contains a wide variety of devices. Each quarter of the mask layout contains 63 unique MEM designs. Every device consists of a distinct combination of membrane area, flexure length, etch hole type, and central mirror radius. All told, between the four die subcells, there are 252 one of a kind devices available for testing. The introduction of such a wide variety was an attempt to reduce the risk present in this research project.

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V. Results and Analysis

5.1 Chapter Overview

In this chapter I present the results of my research. Four device fabrication runs have been attempted with varying degrees of success. A fifth run is in progress, but results may not be available in time to publish in this document.

An initial fabrication run on a bare substrate is described in detail in chapter IV. This resulted in a completed device, including the top DBR mirrors. Unfortunately, no bottom epitaxial mirror stack was present.

A second fabrication run was started on an intrinsic substrate with 15 pairs of p-doped quarter-wave layers (wafer G2-2752). Device fabrication proceeded as planned, and a 1.5 μm gold membrane was evaporated over the PMGI sacrificial layer. At this point, the gold lift-off process partially failed. Although the mechanical structures are intact, it was not possible to deposit the top DBR mirror. The third and fourth fabrication attempts were thwarted by equipment failure, and an unforeseen chemical interaction.

This chapter looks at the results of electrical actuation testing, and discusses design and fabrication issues which must be resolved before a fully functional device can be fabricated. At the time of this writing, a fifth fabrication run is underway, incorporating lessons learned from previous attempts. Hopefully, this will result in a fully functional optical device.

5.2 Fabrication Issues

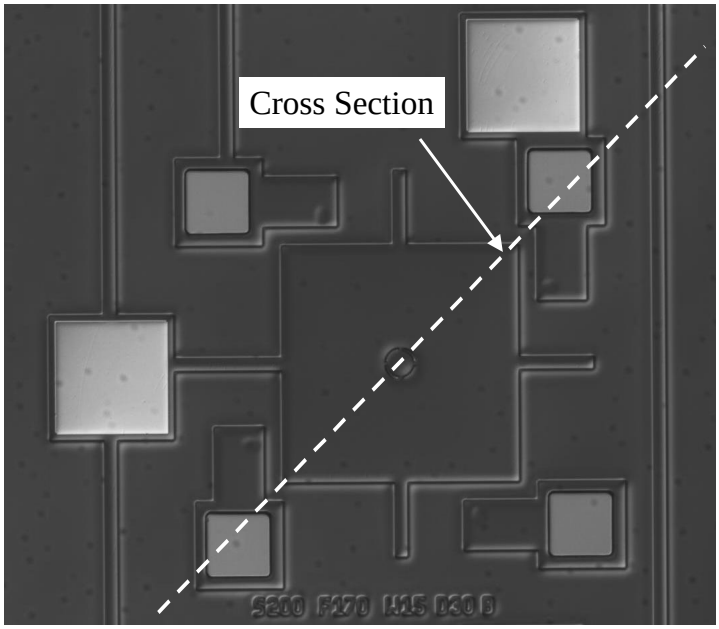
5.2.1 PMGI Behavior. PMGI was originally selected as the sacrificial layer due to its ease of application and it's use in an existing AFRL/SN MEMS fabrication process. However, use of this spin-on polymer has caused difficulties

with device fabrication due to it's conformal nature and the curvature of what were expected to be flat regions.

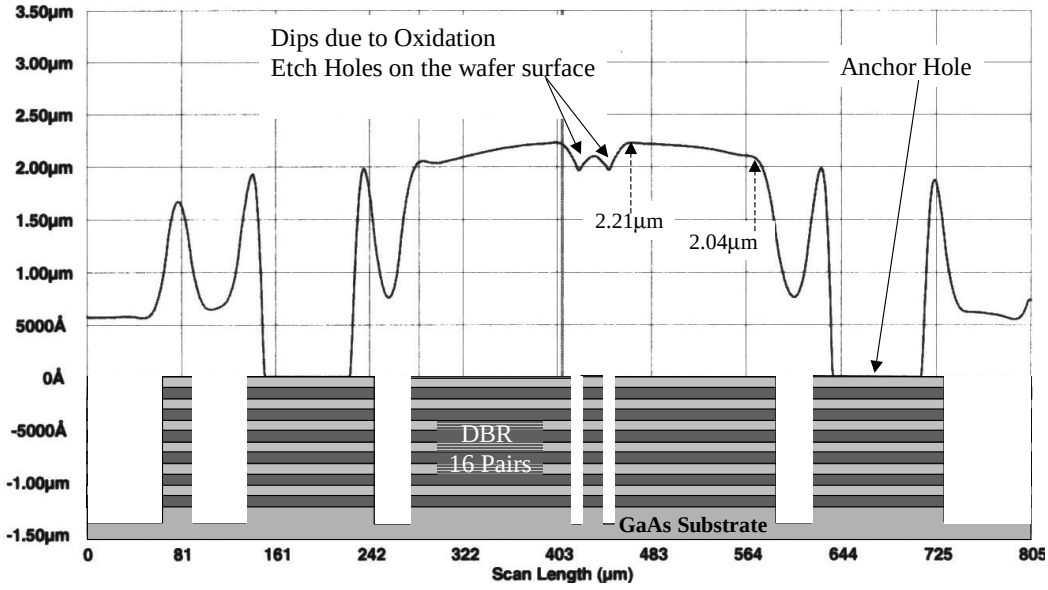
Upon initial spin-on, the surface of the SF-11 PMGI is conformal to the patterned wafer underneath. The design of the Fabry-Perot etalon requires a deep RIE etch of the wafer surface, all the way through the DBR mirror stack to the intrinsic GaAs substrate below. This provides electrical isolation to the wires and structures on the surface. This RIE etch measured 2.5 μm for the second fabrication run (epitaxial growth G2-2752) and 3.6 μm for runs three and four (G2-2545).

After spinning on the PMGI, five major processing steps still remain. The problem is the non-planar surface makes photolithographic processing difficult. Photoresist which is spun onto the surface over the PMGI will add an additional layer of variation to the wafer surface. This causes difficulties when attempting to align and expose the resist to UV for patterning. During alignment under the microscope, portions of the surface may be in focus, while others are not. Before exposure to UV, the wafer is lifted into contact with the lithography mask. Due to the surface height variations, only a portion of the wafer is actually in contact. Other areas may be several microns distant. This results in poorly defined photolithography and causes misalignment of the MEM structures and a general 'fuzziness' of device features.

Section 4.5 describes the fabrication of the anchor holes required to fasten the structure to the wafer surface. The final step of this fabrication sequence is a process known as reflow. Since the PMGI is a liquid polymer, it begins to flow as it is heated above 250°C. While this is useful for creating angled anchor hole sidewalls, it also causes the surface of the PMGI to bow. Figure 5.1b shows a surface profile measurement across the center of a device after the reflow step. It clearly shows the curvature of the surface. Since the gold membrane is evaporated directly onto this curved PMGI, an undesirable flex is introduced into the final device. In addition, as discussed above, this curvature makes photolithography difficult, and results in problems with the gold lift-off step.



(a)



(b)

Figure 5.1 Surface profile measurement showing the conformal nature of the PMGI sacrificial layer. The curvature of the PMGI is due to the reflow processing step (see section 4.5) conducted before evaporation of the membrane metal. A representation of the underlying RIE patterned wafer surface has been added.

5.2.2 PMGI Process Improvements. Fabrication run number five (incomplete) is based on a laser epitaxial growth. In order to provide electrical isolation to the surface features and allow access to the $Al_{0.98}Ga_{0.02}As$ layers for oxidation, an RIE etch must be at least 5200 Å deep. This is significantly shallower than the 2.5 μm to 3 μm etch required when fabricating the Fabry-Perot structure. The shallow depth of the resulting surface features mean better planarization of the PMGI and photoresist. Hopefully, this will result in more precise photolithography and fewer problems with the metal lift-off.

In order to eliminate the curvature of the PMGI as shown in figure 5.1, the PMGI reflow step has been removed from the fabrication process for run number five. Since the sidewalls of the anchor etch holes are nearly vertical (see figure 4.12) before the reflow, it will be necessary to perform two metallization steps. A first step consisting of approximately 1.5 μm of gold will fill the anchor holes and connect the membrane structure to the wafer surface. A second 1.5 μm deposition will form the device membrane and flexures as shown in figure 5.2. While a two step process requires twice the fabrication time and consumes twice the gold, the increase in device yield should make it worthwhile.

5.2.3 Metal Lift-off. The number one problem impacting device operation is the failure of the membrane metal lift-off step. Although the majority of the evaporated metal is removed during processing, as shown in figure 5.3, small features such as the etch holes and the central opening in the top membrane remain attached. The removal of the etch holes should not have a detrimental impact on device operation, but the central opening must be clear of gold to allow for the deposition of the dielectric DBR top mirror stack.

For the first test fabrication run, only 1 μm of gold was evaporated onto the top membrane. While the lift-off was not complete, several of the large central holes successfully cleared out, allowing 3.5 pairs of Si_3N_4/SiO_2 quarter-wave layers to be

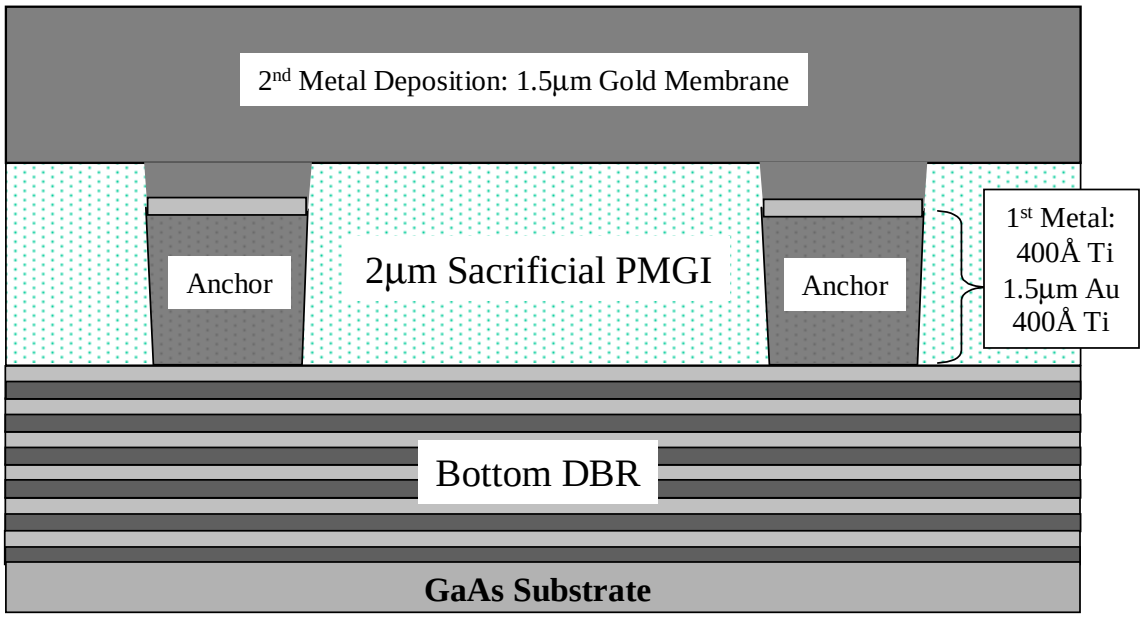


Figure 5.2 Modified anchor process using two metal deposition steps. The first deposition consists of 400 Å Ti/1.5 μm Au/400 Å Ti, and nearly fills the 2 μm deep anchor hole. A second metal deposition of 1.5 μm gold completes the connection to the wafer surface and forms the top device membrane and flexures.

deposited via PECVD. The deposition and RIE etching of the dielectric mirror stack proves that a complete MEM device can be successfully fabricated. Unfortunately, this test run was constructed on a bare GaAs wafer, meaning the optical and electrical characteristics of the devices cannot be explored.

Figure 5.4 is an SEM image of one such device membrane with the dielectric DBR deposited at the center. While the large central disk has lifted-off, the smaller etch holes remain attached. Figure 5.5 is a closeup of an etch bar (hole) showing the stringers of gold holding this feature on the surface. As discussed in section 5.2.1, the problem lies with poor lift-off photolithography, due in part to the unevenness of the PMGI sacrificial layer.

For the second fabrication run, the thickness of the membrane layer was increased to 1.5 μm. This was an attempt to reduce the curvature of the released gold membrane due to tensile stress. As shown in figure 5.6, the measured curvature of

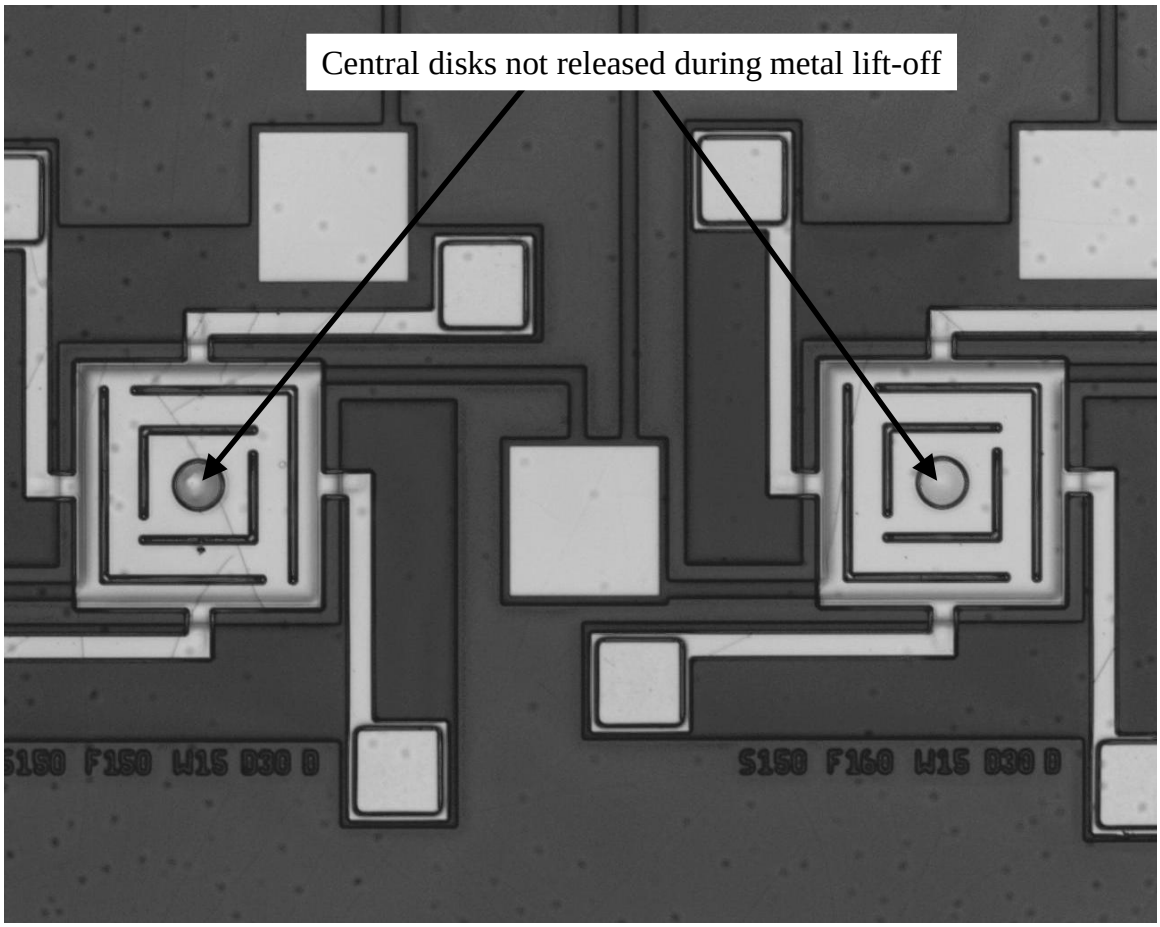


Figure 5.3 On this run (G2-2752C), the gold lift-off failed to remove the etch holes or the central disk. Without the central hole in the membrane, no top DBR mirror can be deposited, and this wafer has been processed as completely as possible. The sacrificial layer was removed, and the electrostatic properties were investigated (section 5.3). This gold membrane is 1.5 μm thick.

a 1 μm thick membrane device with an area of 200 μm $\times$ 200 μm gives an initial airgap height of 2.7 μm. The same device with a 1.5 μm membrane has an initial airgap of 2.12 μm (see figure 5.14). Note from figure 5.6a, the curvature of the membrane causes its corners to deflect towards the surface. Since the flexures are attached to the membrane at it's corners, the flexures are also deflected downward.

Although an increase in the membrane thickness helps to reduce the curvature of the device, it also reduces the possibility of a clean metal lift-off. If the attempt to

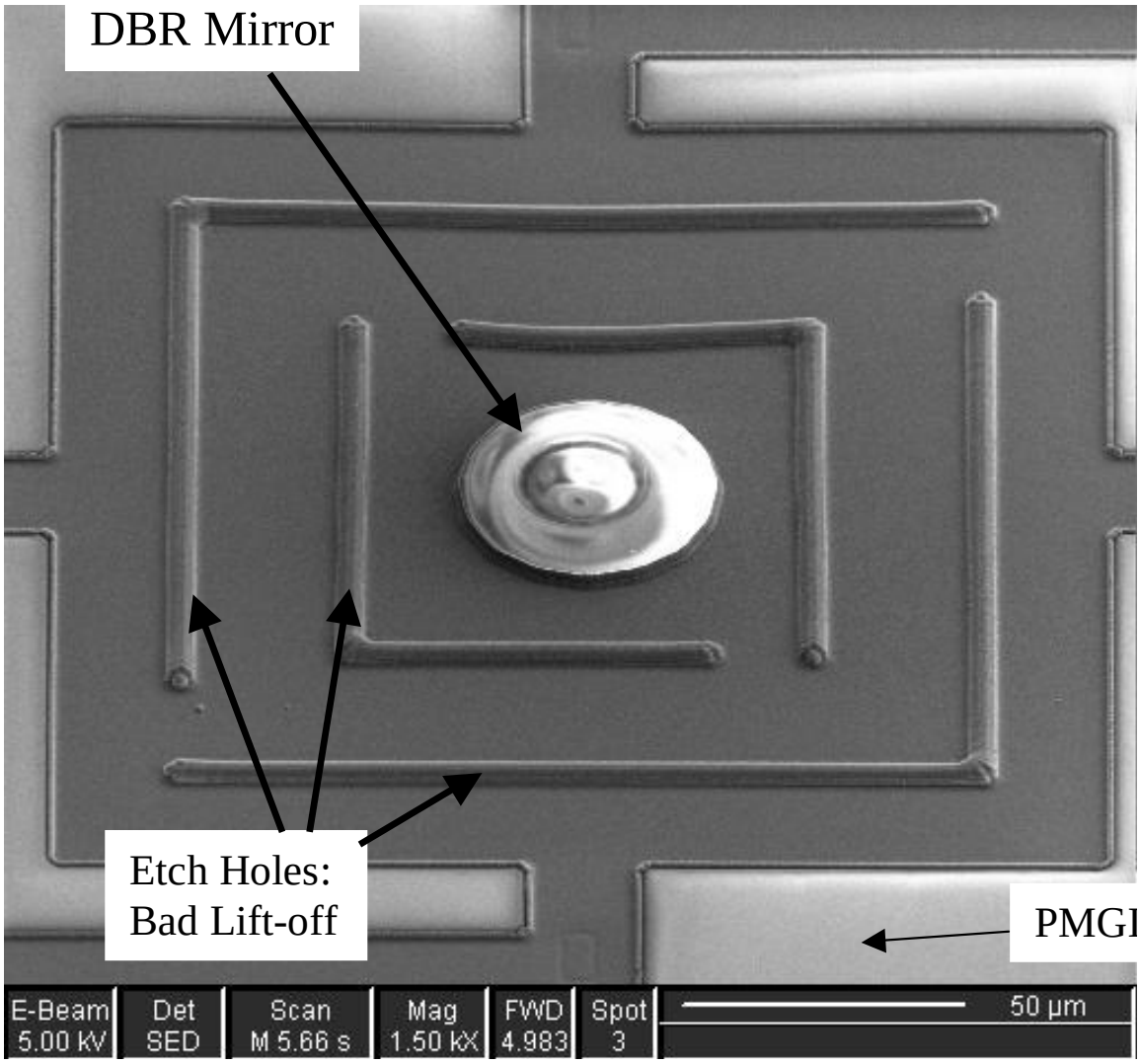


Figure 5.4 SEM image of a completed device before release of the PMGI sacrificial layer. The 1 μm thick gold membrane didn't lift off cleanly - smaller features, such as etch holes, are still attached.

increase the planarization of the PMGI is successful, the clarity of the photolithography will increase, and it should be possible to perform a clean lift-off of a 1.5 μm membrane.

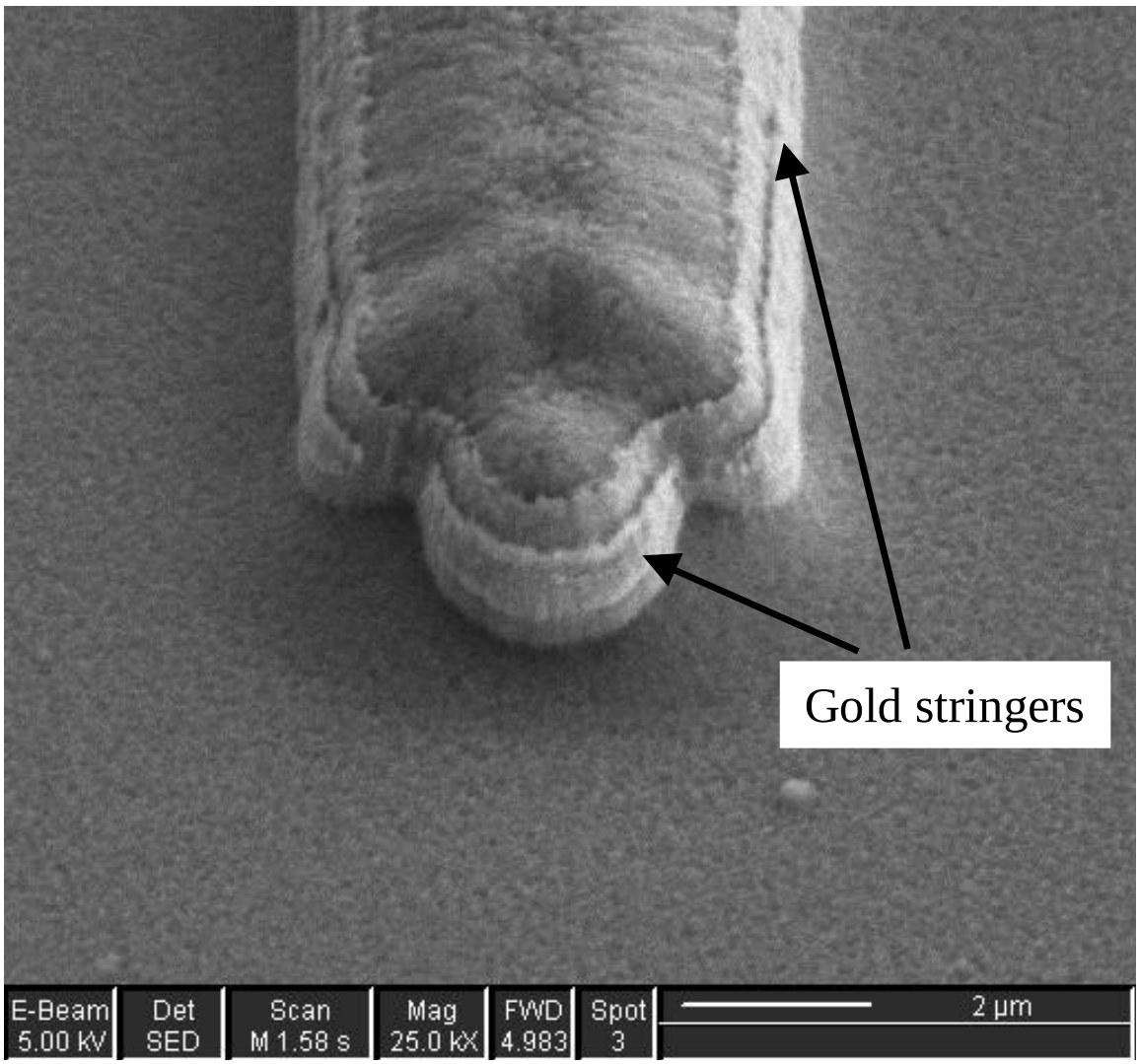
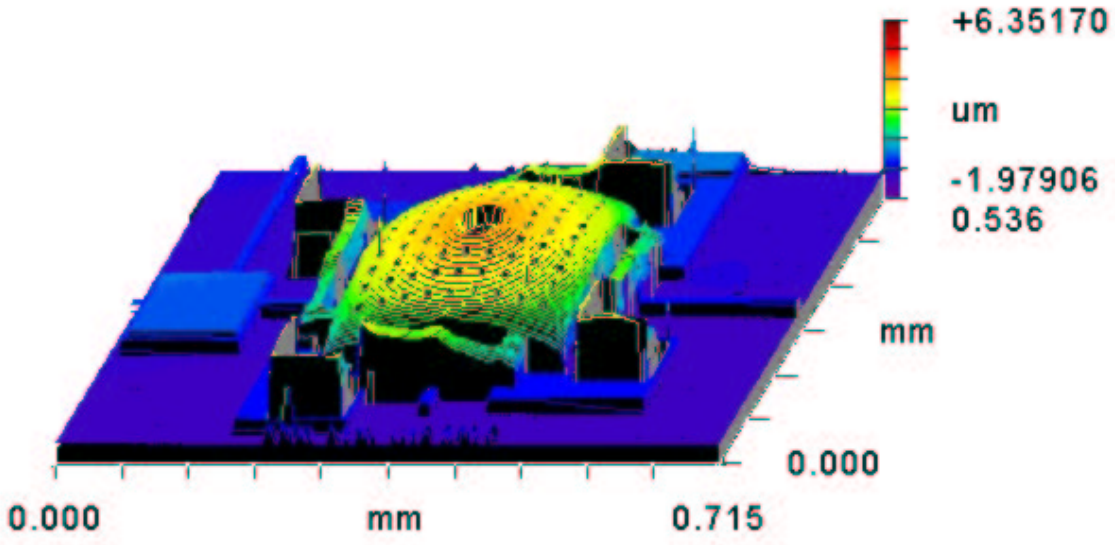


Figure 5.5 SEM image showing unreleased etch bar. The gold lift-off failed due to stringers of gold attaching the bar to the 1 μm thick gold membrane. These stringers are a result of poorly defined photolithography in the lift-off process.



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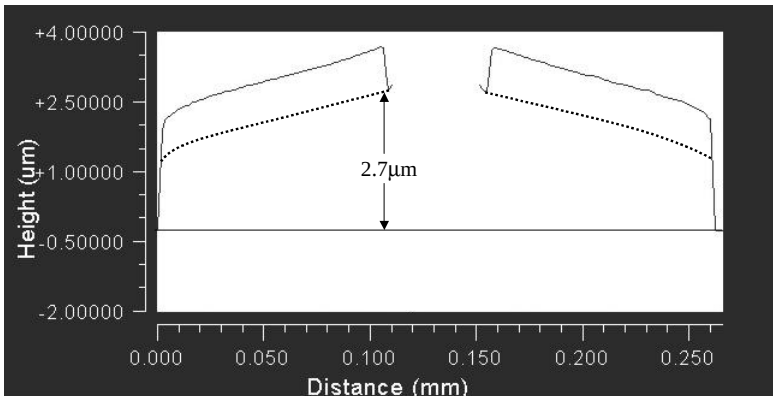


(b)

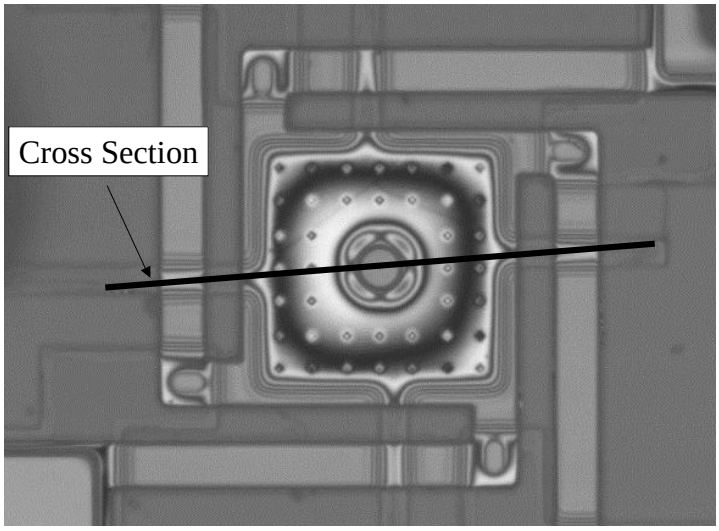
Figure 5.6 (a) This is a 3-dimensional microscope interferometer measurement of 1 μm thick MEM device with membrane area of 200 μm $\times$ 200 μm, and (b) a cross section measurement across the center of the device. Due to the curvature of the membrane there is an initial airgap thickness of 2.7 μm. The flex of the gold membrane may be due to a combination of the underlying curvature of the PMGI sacrificial layer and tensile stress in the evaporated gold.

5.3 Electrostatic Actuation Measurements

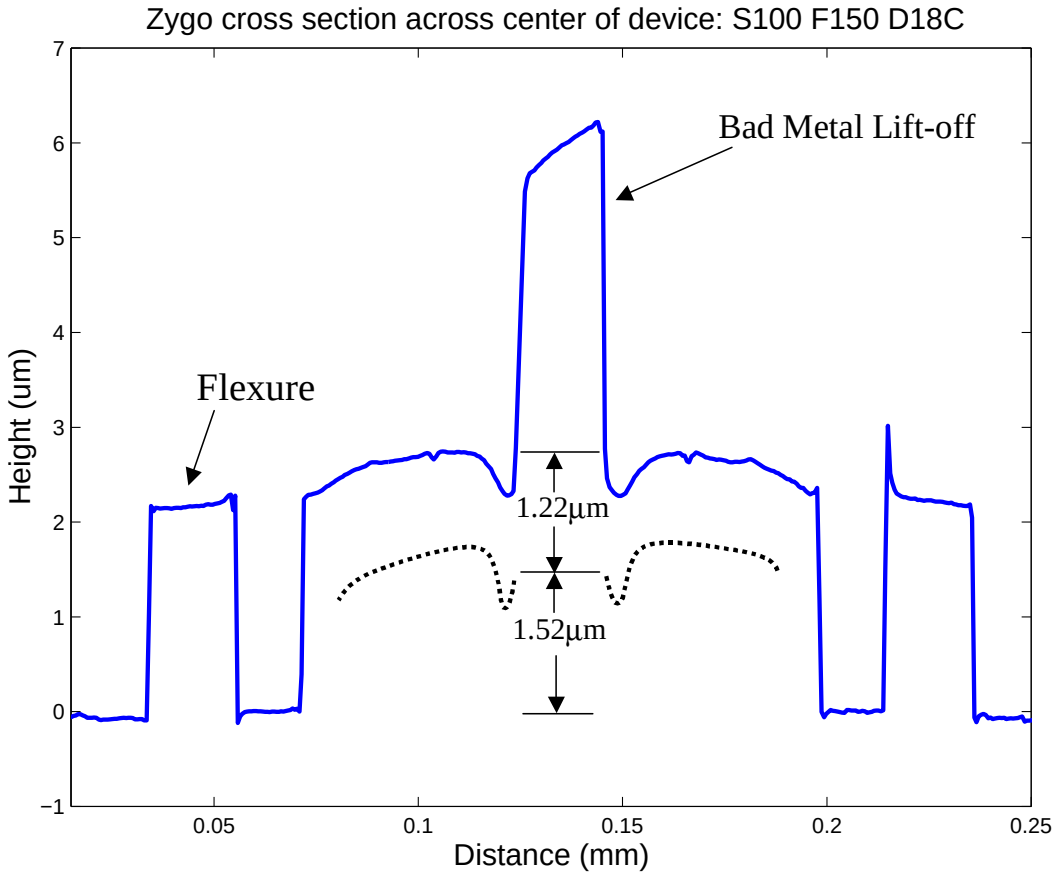
Due to the failed membrane metal lift-off it wasn't possible to deposit the dielectric top DBR mirror and finish the optical fabrication of run number 2. Instead, the devices were released as they were by stripping away the sacrificial PMGI layer. Although unable to check the optical properties of the complete devices, the electrostatic response of the mechanical structures were tested.

In order to test the applied electrical voltage vs. membrane displacement, the released structures were analyzed using a Zygo interferometer microscope (IFM). The wafer was placed on the IFM test platform and two probes were used to apply a voltage potential. One probe was grounded and placed in contact with the highly p-doped ($4 \times 10^{19}\ cm^{-3}$) surface electrode contact pad. The other probe was placed in contact with the gold membrane and flexures through the conducting anchor connection. A positive voltage between 0V and 50V was then placed on the second probe. This resulted in the downward deflection of the top membrane due to electrostatic force, as described in section 2.3.

A total of 12 devices, of various surface and flexure geometry, were analyzed to determine the actuation characteristics and snap-down voltage. Figure 5.7 through figure 5.13 highlight the analysis of three devices. The first device has a membrane area of 100 μm $\times$ 100 μm, and a flexure length of 150 μm. Before application of a voltage potential, the contour of the membrane surface and the device flexures were analyzed with the IFM. Figure 5.7 shows a cross section measurement over the center of the MEM device. The initial curvature of the gold membrane is clearly visible, as is the large central gold disk which didn't release. The bottom surface of the membrane has a measured starting airgap of 1.52 μm, which is 0.5 μm lower than expected.



(a)



(b)

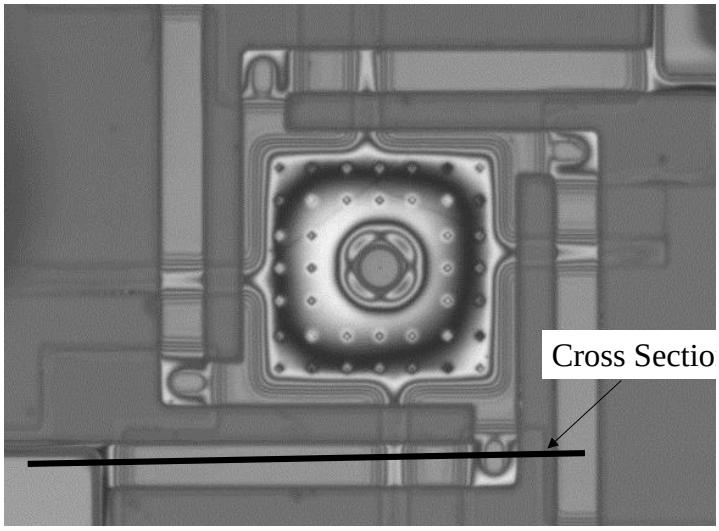
Figure 5.7 IFM cross section measurement across center of MEM device. The flex of the gold membrane may be due to a combination of the underlying curvature of the PMGI sacrificial layer and tensile stress in the evaporated gold.

Of more interest is the surface geometry of the device flexure, as shown in figure 5.8. Since the flexure extends across an area of the wafer which was RIE etched 2.5 μm, it has significant height variations across it's length. Ideally, the flexure should be straight and flat from the anchor to the membrane. But as the deposition of the PMGI and gold membrane are conformal, the flexure takes on the shape of the wafer surface. Perhaps due to the extremes of the flexure shape, the dimple located near the tip of the flexure is resting on the wafer surface instead of floating suspended.

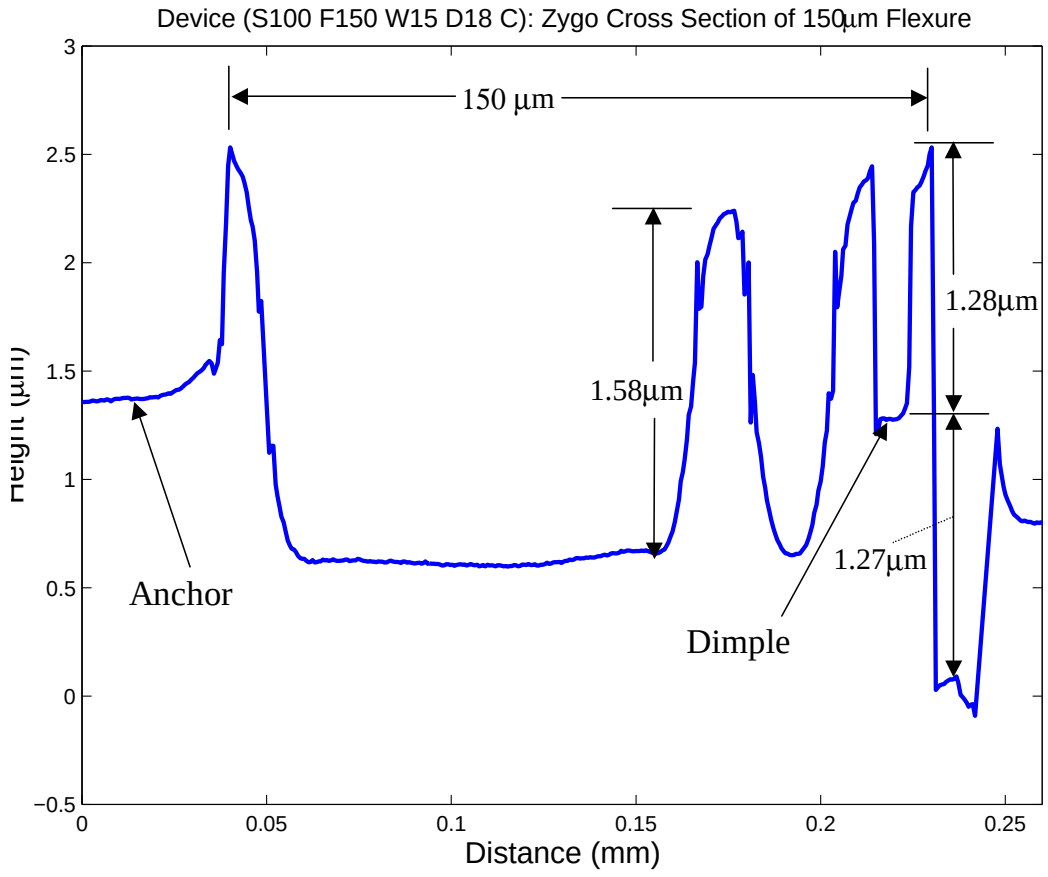
This device is not operating as intended, and all previous voltage vs. deflection measurements are invalid for this structure. Since all four dimples are resting on the surface, the flexures are no longer acting as springs. The membrane is still suspended above the wafer surface, but since the flexures cannot deflect any further the deflection vs. voltage relationship is now due solely to the bending of the membrane as the electrostatic force increases. The electrostatic force required to bend the membrane is larger than the force required to deflect the flexures. Therefore the calculated snap-down occurs at a much lower voltage than the measured snap-down.

Figure 5.9 shows the visible changes in the IFM fringe lines as the membrane is deflected towards the surface and eventually goes through snap-down at 34 V. As the voltage is reduced, the device stays in snap-down until 22 V is reached, where it is released from the surface. Figure 5.10 is the measured hysteresis curve of the applied voltage vs. airgap height.

Analysis of 12 separate devices reveals that all dimples are in contact with the surface. Figure 5.11 through Figure 5.13 show the cross section, IFM deflection images, and airgap vs. voltage measurements for a 150 μm $\times$ 150 μm membrane device. Figure 5.14 through figure 5.16 show the same for a 200 μm $\times$ 200 μm device. A comparison of the calculated snap-down voltage vs the measured snap-down voltage for these 12 devices is shown in table 5.1.

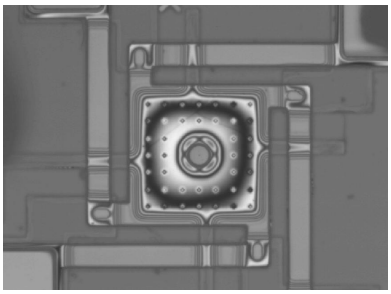


(a)

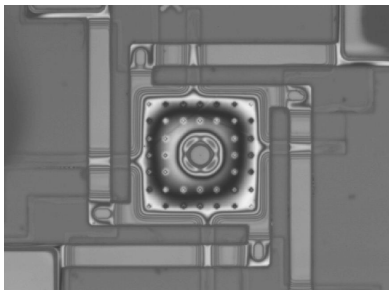


(b)

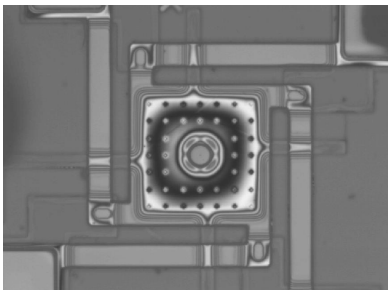
Figure 5.8 IFM cross section measurement of a 150 μm device flexure. Due to the geometry of the underlying wafer surface, the device flexures experience large curvature.



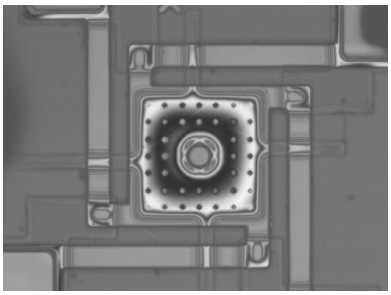
0 V: Airgap 1.54 μm



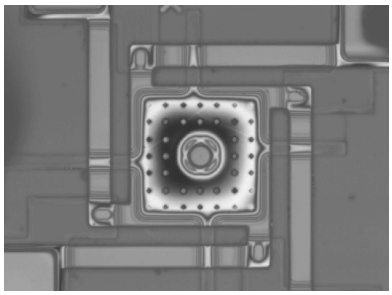
5 V: Airgap 1.48 μm



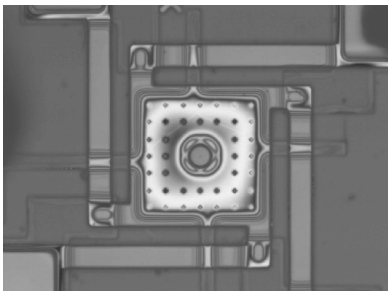
10 V: Airgap 1.44 μm



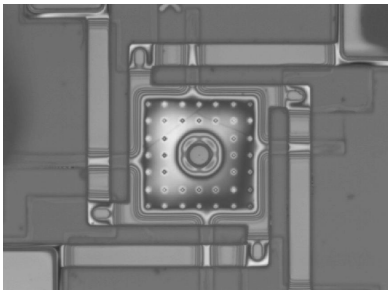
15 V: Airgap 1.43 μm



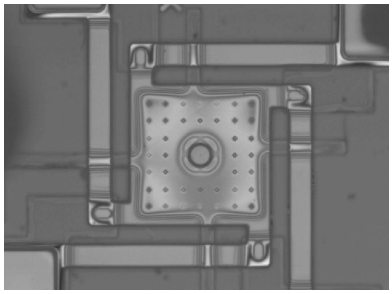
20 V: Airgap 1.42 μm



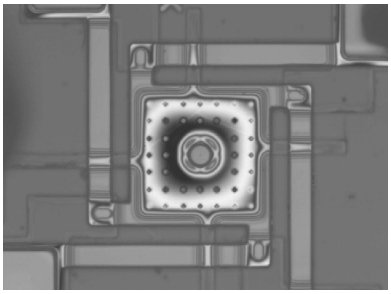
25 V: Airgap 1.35 μm



30 V: Airgap 1.31 μm



34 V: Snap-down



22 V: Release-Airgap 1.40 μm

Figure 5.9 Series of IFM images showing downward deflection of the membrane as the applied voltage is increased. Movement is indicated by the shift in fringe lines. This device has a top membrane area of 100 μm $\times$ 100 μm, and flexure length of 150 μm. The snap-down voltage was measured at 34 V, and the device released from snap-down at 22 V.

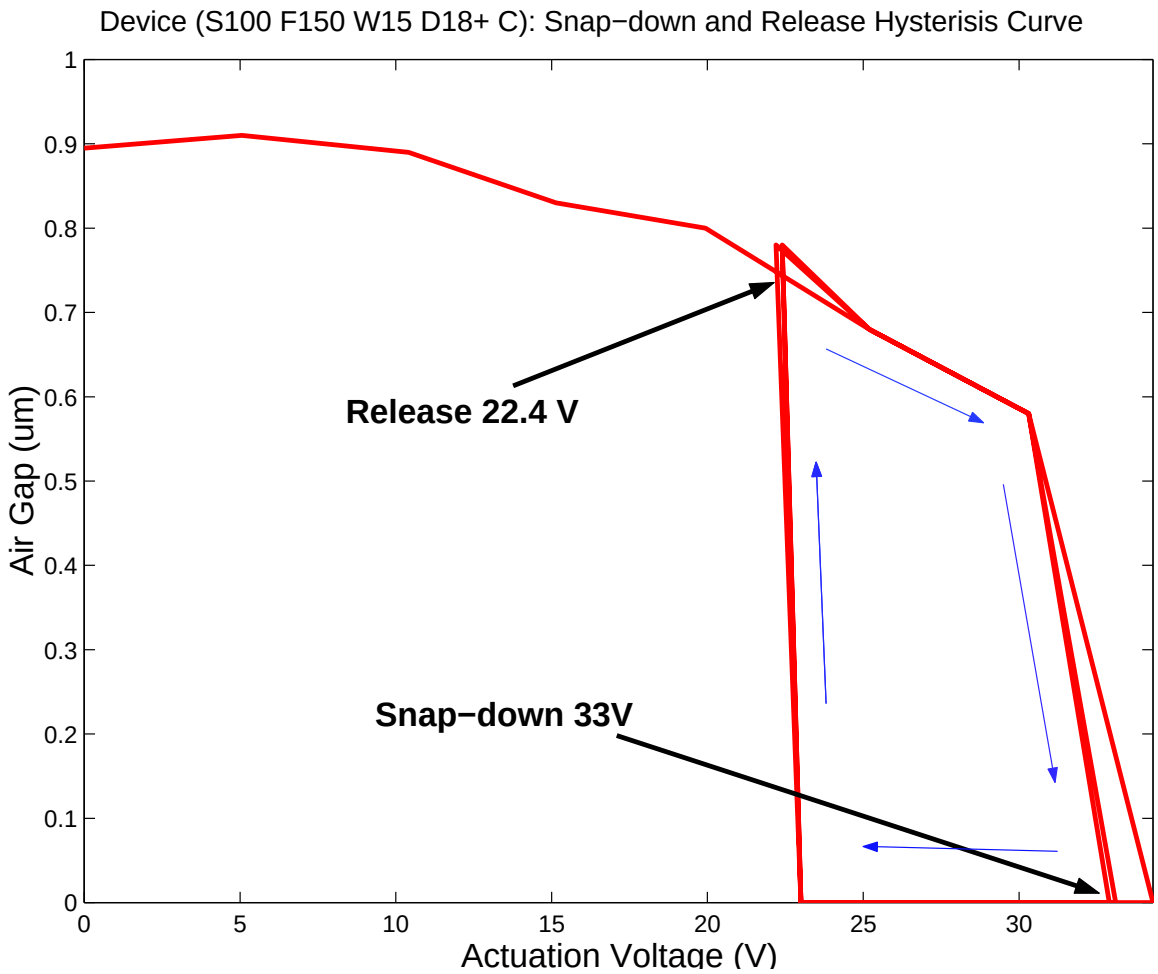
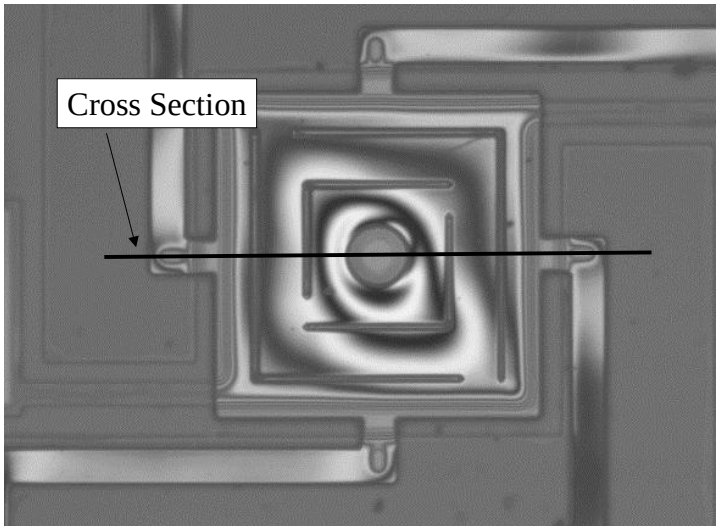
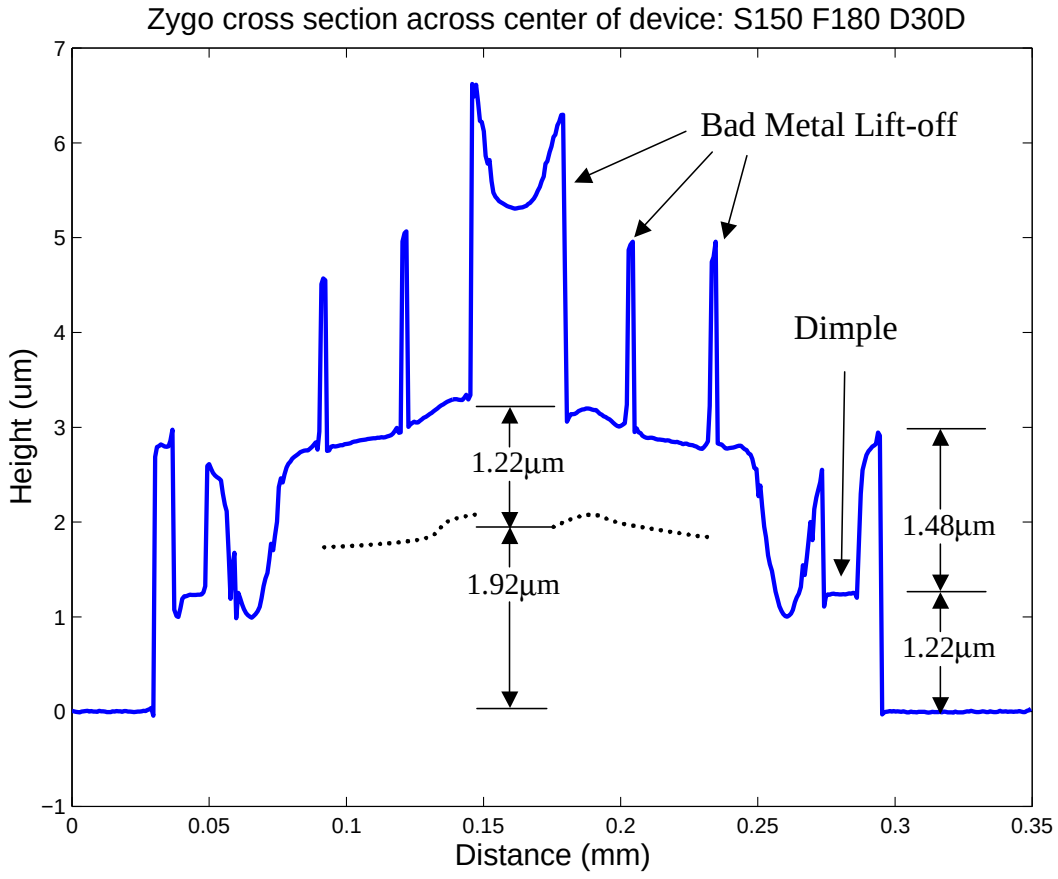


Figure 5.10 Measured hysteresis of device snap-down and release. This structure has a membrane area of 100 μm $\times$ 100 μm, and flexure length of 150 μm. This is the only tested device which exhibited this type of response. All other devices where destroyed by 'stiction' or a short circuit.



(a)



(b)

Figure 5.11 IFM cross section measurement across center of MEM device. The flex of the gold membrane may be due to a combination of the underlying curvature of the PMGI sacrificial layer and tensile stress in the evaporated gold.

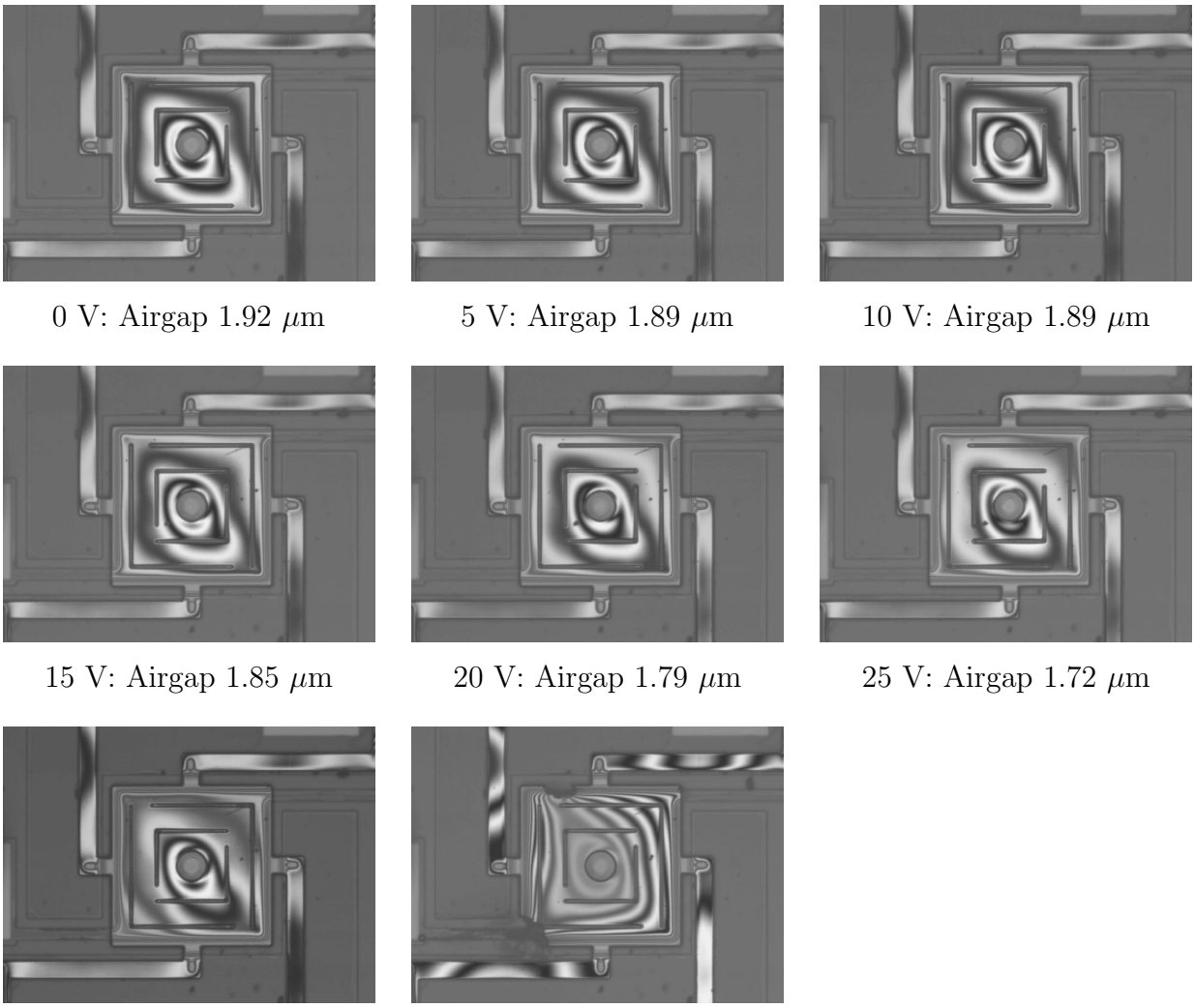


Figure 5.12 Series of IFM images showing downward deflection of the membrane as the applied voltage is increased. Movement is indicated by the shift in fringe lines. This device has a top membrane area of 150 μm $\times$ 150 μm, and flexure length of 180 μm. The snap-down voltage was measured at 34 V. During snap-down a portion of the device made contact with the bottom electrode, and the resulting short circuit caused the destruction of the membrane.

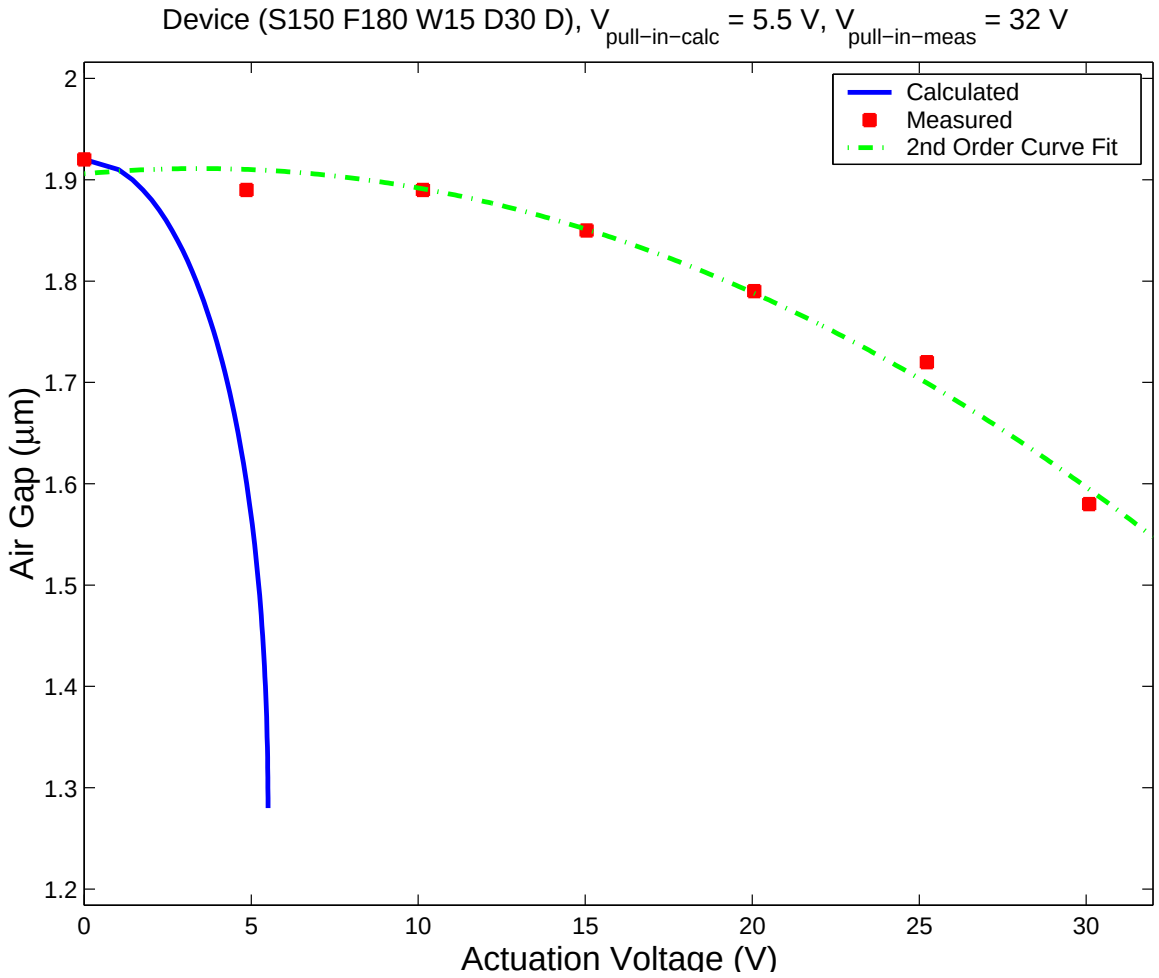
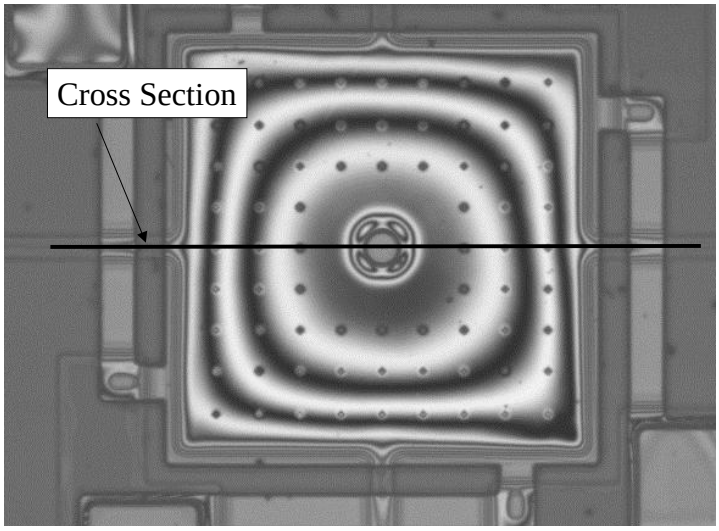
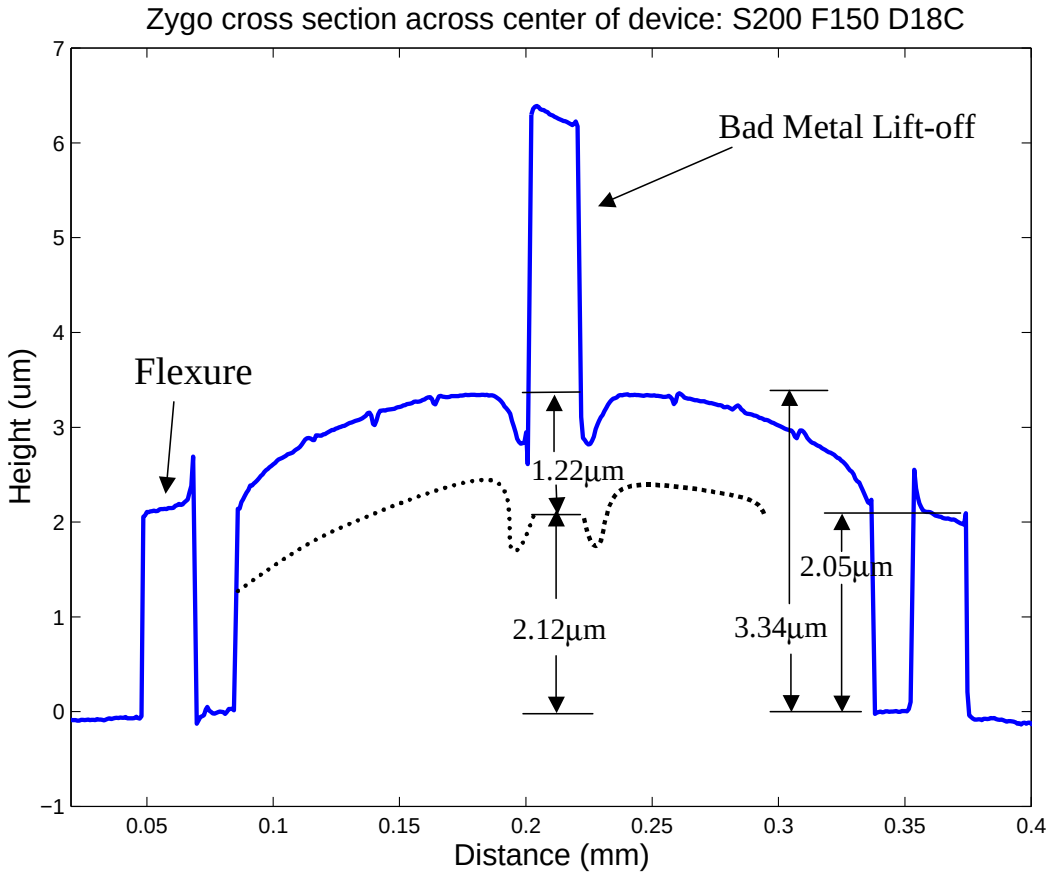


Figure 5.13 Comparison of calculated pull-in voltage vs. measured pull-in. This device is not operating as designed since the flexures are deflected downwards and the dimples are resting on the surface. As the flexures cannot deflect any further, the deflection vs. voltage relationship is now due solely to the bending of the membrane as the electrostatic force increases. The electrostatic force required to bend the membrane is larger than the force required to deflect the flexures. Therefore the calculated actuation curve occurs at a much lower voltage than the measured curve. This structure has a membrane area of 150 μm $\times$ 150 μm, and flexure length of 180 μm.

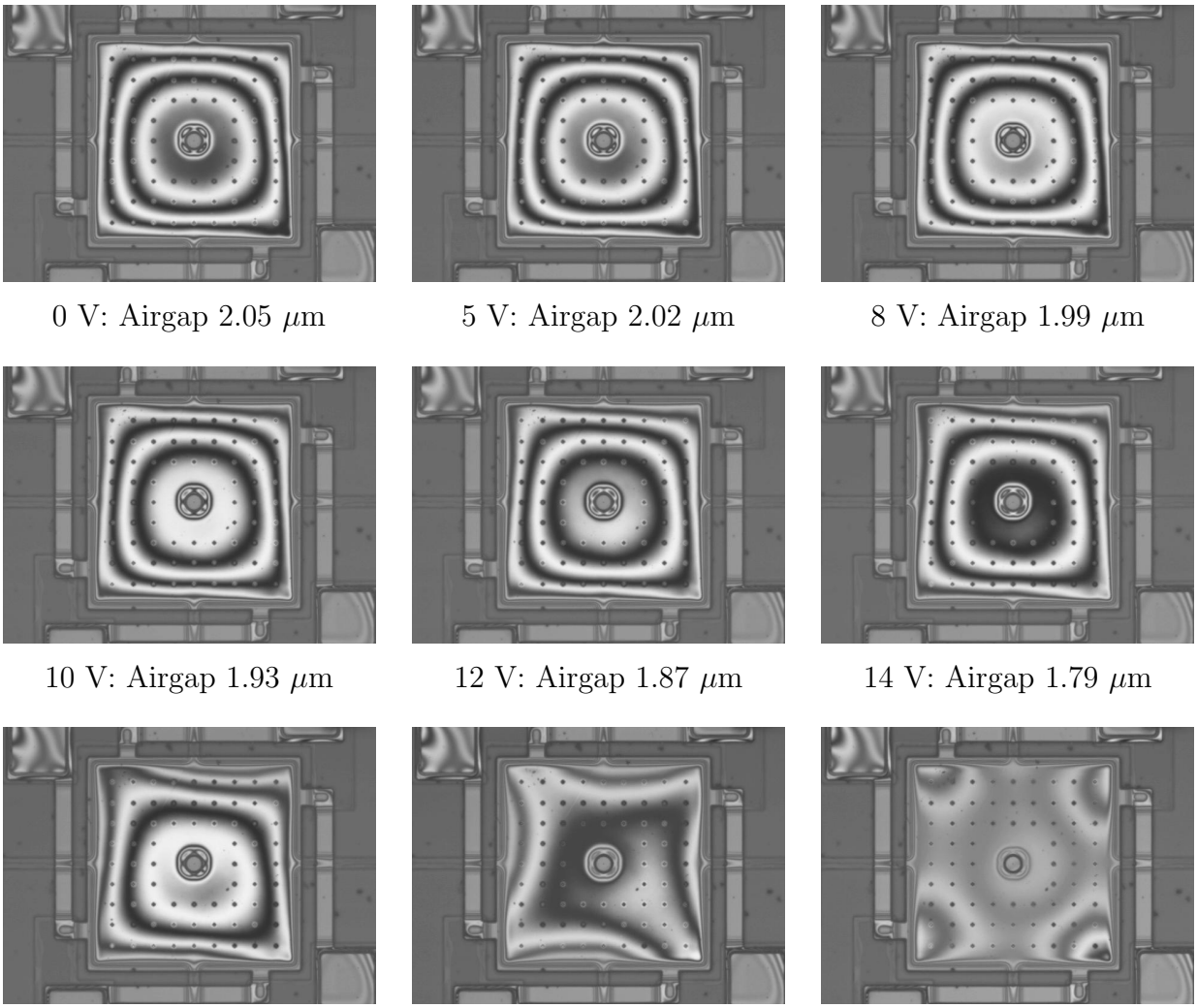


(a)



(b)

Figure 5.14 IFM cross section measurement across center of MEM device. The flex of the gold membrane may be due to a combination of the underlying curvature of the PMGI sacrificial layer and tensile stress in the evaporated gold.



0 V: Airgap 2.05 μm | 5 V: Airgap 2.02 μm | 8 V: Airgap 1.99 μm

10 V: Airgap 1.93 μm | 12 V: Airgap 1.87 μm | 14 V: Airgap 1.79 μm

16 V: Airgap 1.67 μm | 18 V: Partial Snap-down | 18.4 V: Snap-down

Figure 5.15 Series of IFM images showing downward deflection of the membrane as the applied voltage is increased. Movement is indicated by the shift in fringe lines. This device has a top membrane area of 200 μm $\times$ 200 μm, and flexure length of 150 μm. The snap-down voltage was measured at 18 V.

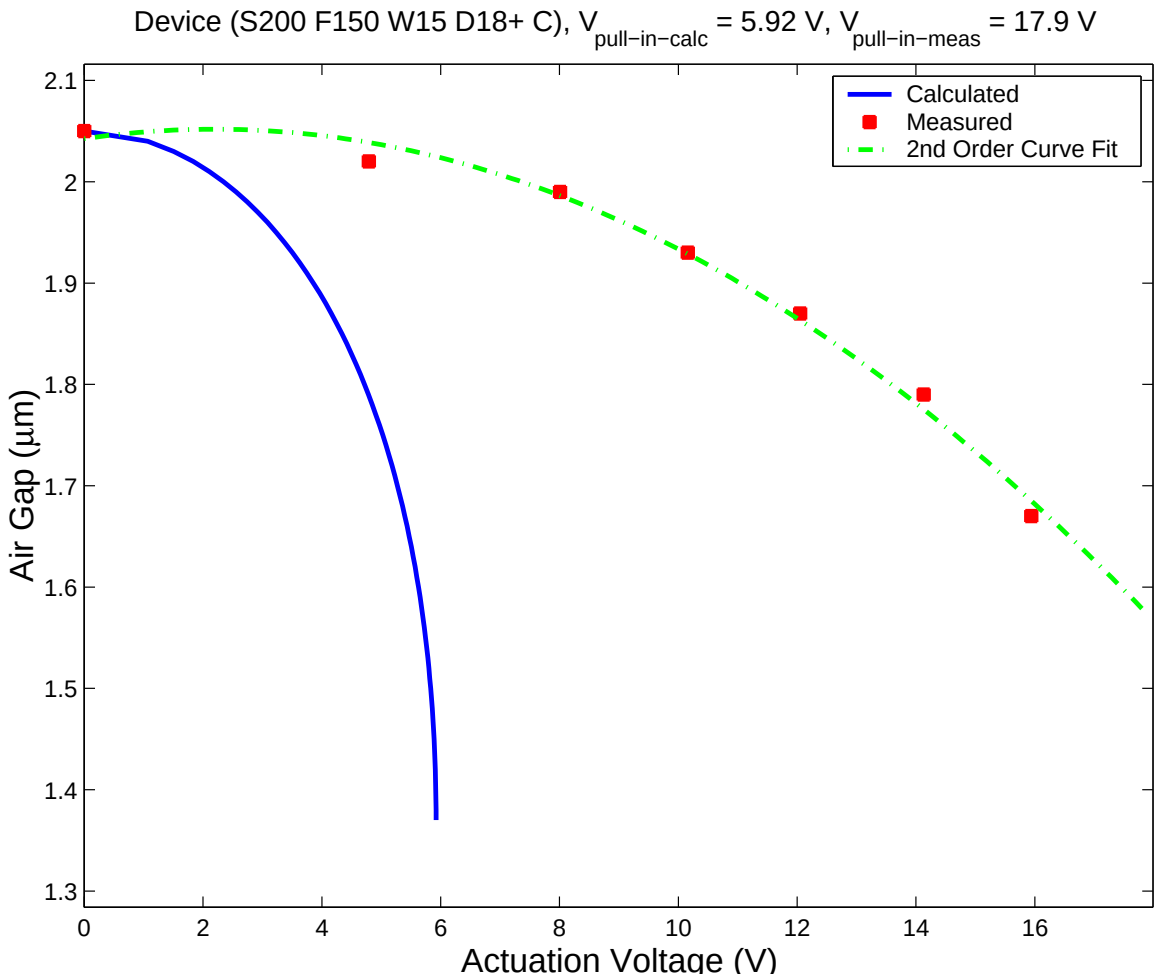


Figure 5.16 Comparison of calculated pull-in voltage vs. measured pull-in. This device is not operating as designed since the flexures are deflected downwards and the dimples are resting on the surface. As the flexures cannot deflect any further, the deflection vs. voltage relationship is now due solely to the bending of the membrane as the electrostatic force increases. The electrostatic force required to bend the membrane is larger than the force required to deflect the flexures. Therefore the calculated actuation curve occurs at a much lower voltage than the measured curve. This structure has a membrane area of 200 μm $\times$ 200 μm, and flexure length of 150 μm.

Table 5.1 Measured snap-down voltages for selected device configurations with gold flexure thickness of 1.5 μm. Note that flexure length has no bearing on the snap-down voltage, only membrane area has a significant impact

Device Number	**Top Membrane Area**	**Flexure Length**	**Calculated Snap-down Voltage)**	**Measured Snap-down Voltage**
S100F70W15D18A	100 μm × 100 μm	70 μm	37.3 V	**40.2 V**
S100F100W15D18C	100 μm × 100 μm	100 μm	21.9 V	**37 V**
S100F130W15D10C	100 μm × 100 μm	130 μm	14.7 V	**32.7 V**
S100F150W15D18+C	100 μm × 100 μm	150 μm	11.9 V	**34.3 V**
S150F120W15D30C	150 μm × 150 μm	120 μm	11.7 V	**25.4 V**
S150F140W15D30C	150 μm × 150 μm	140 μm	9.3 V	**24.5 V**
S150F170W15D10C	150 μm × 150 μm	170 μm	6.9 V	**22 V**
S150F180W15D30D	150 μm × 150 μm	180 μm	6.4 V	**32 V**
S150F190W15D30C	150 μm × 150 μm	190 μm	5.86 V	**22 V**
S200F120W15D30C	200 μm × 200 μm	120 μm	8.6 V	**18.79 V**
S200F150W15D18+C	200 μm × 200 μm	150 μm	6.2 V	**17.95 V**
S200F180W15D30C	200 μm × 200 μm	180 μm	4.7 V	**18.96 V**

As noted previously, the devices are not operating as intended and all theoretical voltage vs deflection calculations are invalid for these structures. The deflection vs voltage relationship is now due solely to the bending of the membrane as the electrostatic force increases. The governing differential equations describing the membrane movement are discussed in section 2.3.1, but have not been calculated due to time constraints.

5.4 Alternate Fabrication Technique

In an attempt to overcome the difficulties encountered in fabrication run one and two, runs number three and four utilized a different membrane material. Si_3N_4 was used to fabricate the top membrane and flexure structures instead of gold. Figure 5.17 shows a simplified schematic of the device fabrication.

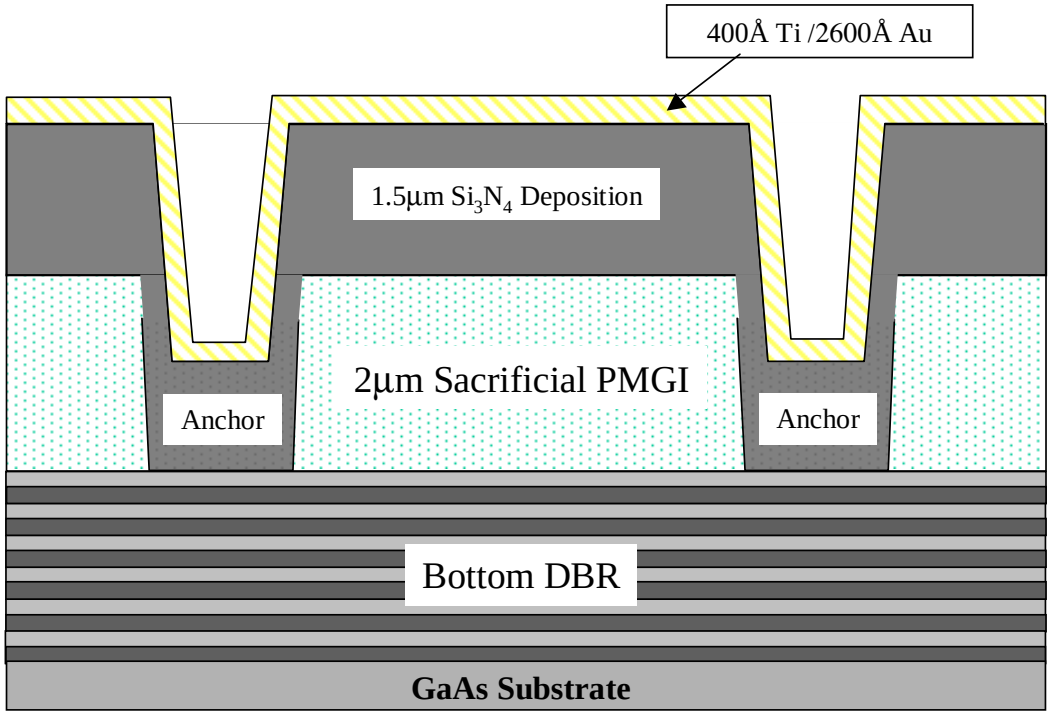


Figure 5.17 Simplified schematic of a fabrication process using Si_3N_4as the membrane and flexure mechanical material. A thin gold layer is used to mask the Si_3N_4 while RIE etching.

The process to fabricate this device is identical to that described in chapter IV, up until the deposition of the membrane metal. Instead of gold, 1.5 μm-thick Si_3N_4 is deposited directly onto the surface of the PMGI via PECVD. In order to pattern the Si_3N_4 into the required membranes and flexures, it is necessary to perform an RIE etch. A thin (2200 Å) layer of gold is evaporated and patterned over the nitride. This gold film is used as a mask for the RIE etch step. Due to the thickness of the Si_3N_4 layer, the RIE etch (using CF-23) is accomplished in three separate steps, each lasting 30 min. Upon completion, nitride is removed wherever there is an opening in the gold mask.

Since the nitride membrane is a dielectric material, the gold mask layer is the conductor upon which electrostatic force is applied. Due to the thickness of the nitride layer, the gap between the top and bottom electrodes has been increased to

3.5 μm. This in turn will significantly increase the actuation voltage of the devices. In addition, the Young's modulus of PECVD deposited Si_3N_4 has been measured at E=146 GPa [2]. This is nearly twice the Young's modulus of gold, meaning the flexures will be stiffer and require a greater downward force to cause actuation.

With the top membrane and flexures intact, the next step is to deposit the top DBR mirror stack consisting of 4.5 pairs of Si_3N_4/SiO_2 quarter-wave layers.

During deposition of the 1.5 μm Si_3N_4 membrane, a boundary layer was formed between the PMGI and the Si_3N_4. The material composition of this layer is unknown, but it has been hypothesized that it was formed during nitride deposition by an interaction between the helium/nitrogen plasma of the PECVD system and the PMGI [1].

This layer is extremely resilient, and prevents the complete removal of the Si_3N_4 deposition. Figure 5.18 is a microscope view showing this unknown material over the sacrificial PMGI layer. Attempts were made to remove the material with a freon CF-23 RIE etch, an O_2 plasma etch, acetone, methanol, and DI water. None of these were successful, and it was necessary to scrap the fabrication of runs three and four.

5.5 Conclusion

In this chapter I presented the results of my research. Four device fabrication runs have been attempted with varying degrees of success. The first run produced a complete MEMS wafer as presented in Chapter IV, but the devices were unusable since the starting wafer was a bare substrate. The second fabrication run was an attempt to construct a MEM tunable Fabry-Perot etalon. The initial wafer was an epitaxially grown semiconductor DBR with 15 pairs $GaAs/Al_{0.9}Ga_{0.1}As$ quarter-wave layers. This run proceeded as expected until trouble with the metal lift-off halted fabrication. Although no top DBR mirror was deposited, a complete set of devices was released and the actuation voltage vs deflection characteristics were

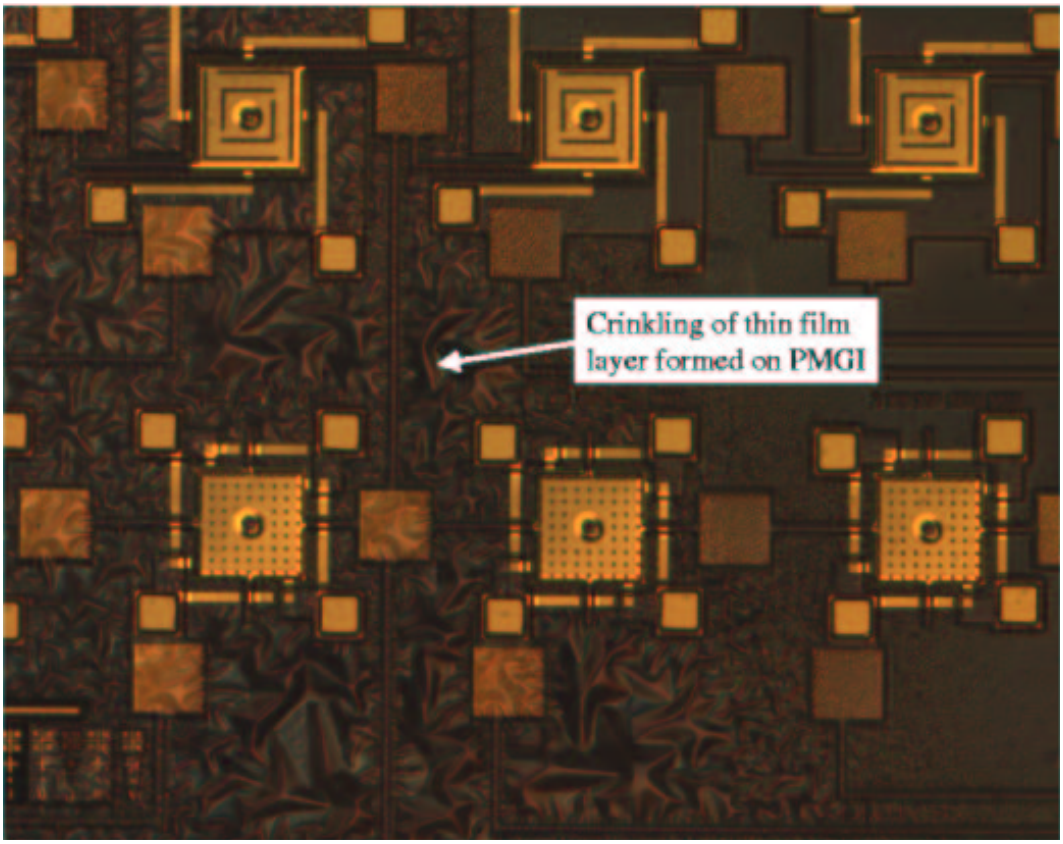


Figure 5.18 Microscope image showing unknown material (ripples) on top of PMGI sacrificial layer.

analyzed. In an attempt to overcome the problems encountered during metal lift-off, runs three and four utilized Si_3N_4 instead of gold as the membrane and flexure mechanical material. Fabrication of these devices was thwarted by an unknown chemical reaction which left a residue covering the wafers.

In addition to my analysis, I have presented process improvements (section 5.2.2) and alternative fabrication techniques (section 5.4) to be implemented in future processing runs.

Bibliography

1. Ebel, J., "Private Communication." Ph. D. , Air Force Research Labs, Sensors Directorate, Devices Branch, Wright-Patterson AFB, OH. 15 February 2002.
2. Kovacs, G. T. *Micromachined Transducers Sourcebook*. Boston: McGraw-Hill, 1998.

VI. Conclusions, Recommendations, and Future Work

6.1 Summary

Although I was unable to reach my goal of demonstrating a tunable optical device, the research I have presented in this thesis shows that complex surface micromachined MEM structures can be fabricated and integrated with III-V semiconductor micro-optical devices. This technology may be used for military systems requiring robust network and communication hardware capable of operating in extreme conditions. Future WDM systems will incorporate thousands of such devices with dynamically reconfigurable topologies. This technology will vastly increase the available bandwidth for voice, imagery, and RF data streams.

In order to achieve my research goals, I conducted in-depth modeling of MEM tunable Fabry-Perot and VCSEL designs by composing a mathematical computer software toolset. From my analysis I demonstrated tunable devices compatible with conventional silicon 5 V integrated circuit technology. My design for a Fabry-Perot etalon has a theoretical tuning range of $\Delta\lambda = 200\ nm$, and my VCSEL design has a tuning range of $\Delta\lambda = 44\ nm$, both achieved with actuation voltages as low as 4 V. Utilizing my theoretical device designs I planned a new microelectronics fabrication process to realize a set of prototype MEM-tunable devices with a peak central emission wavelength at $\lambda_o = 980\ nm$. I then designed a mask set consisting of 8 mask levels and 252 distinct device designs, all within a die size of one square centimeter. My unique fabrication process utilizes a gold MEM flexure with an Si_3N_4/SiO_2 dielectric distributed Bragg reflector (DBR) mirror, grown on an all-semiconductor VCSEL or Fabry-Perot substrate. I then successfully fabricated a complete set of MEM-tunable test structures using the cleanroom laboratory facilities at the Air Force Institute of Technology (AFIT) and the Air Force Research Laboratory (AFRL). I characterized the structures by optical interferometry measurements with nanometer scale resolution. The initial prototype devices display minimum electrostatic actuation voltages

as low as 18 V, which is comparable to existing MEM tunable VCSEL designs. In order to enhance device performance, I developed improvements to my laboratory process for incorporation in future fabrication runs.

6.2 Recommendations and Future Work

The process I utilized to construct the initial MEM prototype devices is flawed due to problems with the PMGI sacrificial layer and the large variation on the surface of the wafer. I have presented alternate fabrication techniques to solve these issues, including the elimination of the PMGI reflow process and the separation of the membrane metal evaporation into two metal lift-off steps. In addition, the RIE etch of the wafer surface must be as shallow as possible in order to reduce vertical contours across the surface of the PMGI. This can be accomplished by carefully designing the epitaxial growth of the semiconductor material. For a Fabry-Perot DBR structure, only the top quarter-wave layers needs p-doping. All other layers should be grown intrinsically to increase the stack resistance. In order to isolate an area or wire defined on the top surface, an RIE etchant must remove wafer material until the intrinsic layer is exposed. If only the top two layers are p-doped, 3000 Å of material must to be removed. This shallow depth will help to eliminate problems associated with difficult mask alignment or "fuzziness" of the photoresist after exposure. This in turn will increase the likelihood of a clean metal lift-off when depositing the gold membrane and flexures.

Gold (Au) is not the most ideal material for fabricating complex MEM devices. The low Young's modulus and the amount of tensile stress present in evaporated thin film gold makes device processing difficult. I have attempted to use Si_3N_4 as a mechanical layer, but my efforts were thwarted by an undetermined chemical reaction at the boundary between the PMGI and Si_3N_4 (see figure 5.18). It is hypothesized that this reaction occurred during the PECVD deposition of the bottom Si_3N_4 layer onto the PMGI sacrificial layer. Therefore, it might be possible to sputter Si_3N_4 onto

the PMGI surface without forming the unwanted boundary layer. After applying a thin Si_3N_4 layer via sputtering, the remainder of the Si_3N_4 mechanical layer can be deposited by the PECVD system. This will ensure that the majority of the mechanical material can be anisotropically RIE etched using CF-23 (sputtered Si_3N_4 is resistant to CF-23).

In addition to Si_3N_4, it might be possible to reduce the stress, and thus the curvature of the top membrane, by using an alternating stack of dielectric quarter-wave pairs as the top mechanical layer of the MEM device. In addition, this would eliminate the need to deposit and pattern a separate top DBR mirror stack.

Finally, improvements to the photolithographic mask set would ease the fabrication and ability to test the optical characteristics of the MEM tunable devices. Specifically, all of the surface wires and bottom electrodes should consist of ohmic metal evaporated onto the top semiconductor layer. This would greatly lower the resistance of the electrical connections, and would eliminate the need grow p-doped Fabry-Perot mirror stacks. Without the need to RIE etch through the top mirror layers, the problems associated with height variations across the wafer surface would be eliminated. In addition, the diameter of the top dielectric DBR mirror stack should be increased to accommodate the power reflectance test bench setup at AFRL/SN. A minimum diameter of 60 μm would help to facilitate reflectance dip measurements for a tunable device.

In the months following the presentation of this thesis document, I intend to continue development of my fabrication process with the goal of demonstrating an operational MEM tunable VCSEL. This research is an important part of the Air Force's effort to maintain information superiority, both on and off the battlefield. My results form the fundamental basis for advanced development of manufacturable MEM-tunable optical emitting and detecting device arrays. Such arrays might be used to vastly increase the bandwidth of existing fiber-optic communication systems through the application of wavelength division multiplexing (WDM). Increases in

data transmission throughput means those aerospace systems utilizing wavelength-division multiplexing (WDM) techniques will have access to vastly increased bandwidth for voice, imagery, and RF data.

Appendix A. Fabrication Process

This appendix contains the process followers (checklists) used throughout the fabrication process. These followers detail every step of the MEM manufacturing.

MEM Tunable VCSEL – Ohmic Metal (Mask #1)			
17 February, 2002		**Piece ID:**	
Init.	**Process Step**	**Notes**	**Date Time**
	INSPECT WAFER: ❑ Note any defects	**Start Date** **Start Time**	
	SOLVENT CLEAN: ❑ 20 sec acetone rinse at 500 rpm ❑ 20 sec isopropyl rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	OXIDE REMOVAL: ❑ 30 sec dip (1:10) HCl:DI Water ❑ 3x DI Water bucket rinse ❑ Dry wafer with nitrogen on clean texwipes		
	DEHYDRATION BAKE: ❑ 1 min 110 ° C Hot plate bake		
	XP LOR 3A Coat: ❑ Set spinner ramp rate = 200 ; spin 4000 rpm ❑ Coat sample with XP LOR 3A ❑ Spin 30 sec at 4,000 rpm, ramp=200 ❑ Use EBR to clean backside ❑ 2 minute HPB at 170° C ; cool		
	1805 COAT: ❑ Flood wafer with 1805 ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑ 75 sec 110° C hot plate bake ❑ Use acetone to remove 1813 on backside		
	Edge Bead Removal : ❑ Flood expose edge bead mask for 2 min (2mw/cm^2) ❑ Develop for 30 seconds using LDD26W developer ❑ DI rinse, N2 dry		
	EXPOSE 1805 with DC ELECTRODE MASK: ❑ Align to Bottom Metal alignment mark ❑ 17.5 sec Exposure		
	1805 DEVELOP: ❑ 75 sec develop with LDD26W at 1000 rpm ❑ 30 sec DI Water rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes ❑ Clean mask using acetone wipe and N_2 dry		
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	ASHER DESCUM ❑ 4 min, 200 W, 400 sccm O_2, LFE Barrel Asher		
	PRE-METAL DIP: ❑ 30 sec Dip (1:7) BOE:DI Water ❑ 3x DI Water bucket rinse ❑ Dry wafer with nitrogen on clean texwipes		
	DC ELECTRODE METAL DEPOSITION: ❑ Evaporate 400 Å Ti / 2200Å Au (Titanium/Gold)		

MEM Tunable VCSEL – Ohmic Metal (Mask #1)			
17 February, 2002		**Piece ID:**	
	LIFT-OFF DC ELECTRODE METAL: ❑ 20 sec spray with acetone gun at 1000 rpm (pressurized @ 40 psi) ❑ 20 sec spray with acetone bottle at 500 rpm ❑ 30 sec spray with isopropyl alcohol at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	1165 STRIP XPLORE 3A: ❑ 5 min 90 ° C 1165 remover ❑ 3x DI water bucket rinse ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT WAFER: ❑ Inspect for resist removal under microscope	**Finish Date**	
	DEKTAK DC ELECTRODE HEIGHT: ❑ Measure DC electrode step height using Dektak box Record height measurements: _____ _____ _____	**Finish Time**	

MEM Tunable VCSEL – Oxidation Etch (Mask #2)			
17 February, 2002		**Piece ID:**	
Init.	**Process Step**	**Notes**	**Date Time**
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	1813 COAT: ❑ Flood wafer with 1813 ❑ 30 sec spin at 4000 rpm, ramp=200 ❑ 75 sec 110 ° C hot plate bake ❑ Use acetone to remove 1813 on backside	**Start Time**	
	1813 Edge Bead Removal: ❑ Flood expose edge bead mask for 2 min (2mw/cm^2) ❑ Develop for 30 seconds using 351 developer ❑ DI rinse 30 sec, N2 dry ❑ Remove Edge Bead stragglers with q-tip and Acetone	Use foil EBR mask	
	INSPECT Edge Bead: ❑ Check to ensure 1813 Edge Bead Removal		
	EXPOSE 1813 with Oxidation Etch MASK: ❑ Align to Bottom Metal alignment mark ❑ 40 sec Exposure		
	1813 DEVELOP: ❑ 30ec develop with 351:DI (1:5) at 500 rpm ❑ 30 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	RIE Etch ❑ Set up reflectance monitoring equipment on ICP etcher ❑ PC – double click on RIE Reflectance ❑ Change time interval to .1 (seconds) ❑ Mount sample on sapphire holder using diffusion pump oil (*use a SMALL amount of oil, otherwise it will contaminate wafer surface!)* ❑ Etch through microcav and bottom AlAs layer ❑ Clean wafer and sapphire holder using isopropanol swabs	-anisotropic etch down to oxidation layer below microcav	
	INSPECT WAFER: ❑ Inspect for GaAs etch		
	STRIP 1813 ❑ 20 sec acetone gun at 1000 rpm ❑ 20 sec acetone rinse at 500 rpm ❑ 30 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes		
	INSPECT RESIST: ❑ Inspect photoresist for 1813 removal		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	DEKTAK POST HEIGHT: ❑ Measure resist step height in three locations Top _____ Middle _____ Bottom _____		

MEM Tunable VCSEL – Oxidation Etch (Mask #2)			
17 February, 2002		**Piece ID:**	
	Set up oxidation system ❑ Ensure water bottle is full of fresh DIW ❑ Set for oxidation at desired temperature (400 °C preliminarily) ❑ Set flow parameters according to operating instruction ❑ Place sample on heated chuck ❑ Note time when water vapor flow is begun		
	Observe Oxidation ❑ Position microscope objective over "lapped" area of sample with structures ❑ Note times when each size of each structure type is "pinched off"		
	Halt Oxidation ❑ When the desired oxidation progress has been achieved ❑ Shut-off water vapor valve ❑ Shut down system according to instructions—don't forget to turn off the Nitrogen Dewar ❑ Remove sample from chamber after it has cooled below 100 °C		
	Remove Oxide ❑ Dip sample in BOE:DIW 1:1 for 30 seconds ❑ Rinse 3, 30 second cycles in DIW rinse tank ❑ N_2 blow dry	**Finish Date**	
	Observe Lateral Etching Using Optical Microscope and SEM ❑ Measure selectivity ❑ Measure lateral of top structure vs. lateral of sacrificial GaAs ❑ Measure vertical of exposed bottom DBR vs. lateral of sacrificial GaAs ❑ Measure vertical into bottom of top DBR vs. lateral of sacrificial GaAs ❑ Check for viability of release process ❑ Look for effects of residual stress due to growth and/or oxidation	**Finish Time**	

MEM Tunable VCSEL – SiN (Mask #3)			
17 February, 2002		**Piece ID:**	
Init.	**Process Step**	**Notes**	**Date Time**
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	PRE-NITRIDE DIP: ❑ 30 sec BOE:DI (1:7) dip ❑ 3X DI water bucket rinse ❑ Dry with nitrogen on clean texwipes		
	NITRIDE DEPOSITION: ❑ Deposit 3667 Å of silicon nitride ❑ PECVD: ___ min, 17 sccm 5% Silane in N_2, 25 sccm N_2, 10 sccm NH_4, 20W, 850 mTorr, 200 ° C (Process7) **NOTE: Temp < 200C** **OR:** ❑ Sputtered: ___ min, ___ sccm Silane, ___ sccm N_2, ____W, 850 mTorr ❑ Measure nitride thickness on silicon with ellipsometer Thickness_____ Index of refraction_____		
	INSPECT NITRIDE: ❑ Inspect wafer under microscope and look for ❑ Uniform color ❑ Pin holes ❑ Cracks around metal		
	1813 COAT: ❑ Flood wafer with 1813 ❑ 30 sec spin at 4000 rpm, ramp=200 ❑ 75 sec 110 ° C hot plate bake ❑ Use acetone to remove 1813 on backside		
	EXPOSE 1813 with SiN MASK: ❑ Align to Bottom Metal alignment mark ❑ 40 sec Exposure		
	1813 DEVELOP: ❑ 30ec develop with 351:DI (1:5) at 500 rpm ❑ 30 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	NITRIDE ETCH DIP: ❑ 30 sec BOEI:DI (1:10) dip ❑ 3X DI water bucket rinse ❑ Dry with nitrogen on clean texwipes **OR** **RIE ETCH NITRIDE:** ❑ 10 min dry etch in double barrel RIE using Freon CF-23 etchant ❑ Inspect under microscope to ensure Si3N4 removal in Anchor holes		
	INSPECT WAFER: ❑ Inspect for nitride removal		

MEM Tunable VCSEL – SiN (Mask #3)			
17 February, 2002		**Piece ID:**	
	STRIP 1813 ❑ 20 sec acetone gun at 1000 rpm ❑ 20 sec acetone rinse at 500 rpm ❑ 30 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes		
	INSPECT RESIST: ❑ Inspect photoresist for 1813 removal		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE	**Finish Date**	
	DEKTAK POST HEIGHT: ❑ Measure SiN step height in three locations Top _____ Middle _____ Bottom _____	**Finish Time**	

MEM Tunable VCSEL – Dimple Etch (Mask #5)

17 February, 2002 **Piece ID:**

Init.	Process Step	Notes	Date Time
	DEHYDRATION BAKE: ❑ 1 min 110° C Hot plate bake	**Start Date**	
	PMGI COAT #1: ❑ Flood wafer with SF-11 PMGI ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑ Use edge bead remover (EBR) to remove PMGI on backside (1 min @ 20° C) ❑ 1 min 270 ° C hot plate bake	**Start Time**	
	PMGI COAT #2 (USE FOR 2 µm MEMBRANE HEIGHT): ❑ Flood wafer with SF-11 PMGI ❑ 30 sec spin at 4,000 rpm, ramp=200 ❑ Use edge bead remover (EBR) to remove PMGI on backside (1 min @ 20° C) ❑ 1 min 270 ° C hot plate bake		
	1813 COAT: ❑ Flood wafer with 1813 ❑ 30 sec spin at 4000 rpm, ramp=200 ❑ 75 sec 110 ° C hot plate bake ❑ Use acetone to remove 1813 on backside		
	1813 Edge Bead Removal: ❑ Flood expose edge bead mask for 2 min (2mw/cm^2) ❑ Develop for 30 seconds using 351 developer ❑ DI rinse 30 sec, N2 dry ❑ Remove Edge Bead stragglers with q-tip and Acetone	Use foil EBR mask	
	Edge Bead Removal: ❑ 200 sec Deep UV exposure @ 35mW/cm2, 254 nm ❑ 60 sec SAL 101 spin develop at 500 rpm ❑ 30 sec DI water rinse at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes ❑ Repeat DUV and Develop 2nd Time ❑ Repeat DUV and Develop 3rd Time	-Continue to use foil EBR mask for all three DUV steps. Otherwise 1818 resist will be ruined -Repeat 3 times due to thickness at corners	
	INSPECT Edge Bead: ❑ Check to ensure 1813 & PMGI Edge Bead Removal		
	EXPOSE 1813 with DIMPLE MASK: ❑ Align to Bottom Metal alignment mark ❑ 40 sec Exposure		
	1813 DEVELOP: ❑ 30 sec develop with 351:DI (1:5) at 500 rpm ❑ 30 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	TENCOR MEASURE: ❑ Measure resist step height in three locations Top _____ Middle _____ Bottom _____		
	PARTIAL DUV CYCLE (~0.75µm / cycle) ❑ 100 sec Deep UV exposure @ 35 mW/cm^2, 254 nm		
	PMGI DEVELOP: ❑ 60 sec SAL 101 spin develop at 500 rpm ❑ 30 sec DI water rinse at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		

MEM Tunable VCSEL – Dimple Etch (Mask #5)			
17 February, 2002		**Piece ID:**	
	TENCOR MEASURE ❑ Measure resist step height in three locations Top _____ Middle _____ Bottom _____		
	STRIP 1813: ❑ 20 sec acetone gun at 1000 rpm ❑ 20 sec acetone bottle at 500 rpm ❑ 20 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes		
	INSPECT RESIST: ❑ Inspect photoresist for 1813 removal		
	TENCOR MEASURE: ❑ Measure dimple step height in three locations Top _____ Middle _____ Bottom _____	**Finish Date** **Finish Time**	

MEM Tunable VCSEL – Anchor (Mask #4)

17 February, 2002 **Piece ID:**

Init.	Process Step	Notes	Date Time
	DEHYDRATION BAKE: ❑ 1 min 110° C Hot plate bake	**Start Date**	
	1813 COAT: ❑ Flood wafer with 1813 ❑ 30 sec spin at 4000 rpm, ramp=200 ❑ 75 sec 110 ° C hot plate bake ❑ Use acetone to remove 1813 on backside	**Start Time**	
	EXPOSE 1813 with ANCHOR MASK: ❑ Align to Bottom Metal alignment mark ❑ 40 sec Exposure		
	1813 DEVELOP: ❑ 30 sec develop with 351:DI (1:5) at 500 rpm ❑ 30 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	1ST DUV CYCLE (~1.5µm / cycle) ❑ 200 sec Deep UV exposure @ 35 mW/cm^2, 254 nm		
	PMGI DEVELOP: ❑ 60 sec SAL 101 spin develop at 500 rpm ❑ 30 sec DI water rinse at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT RESIST: ❑ Inspect photoresist		
	2ND DUV CYCLE ❑ 200 sec Deep UV exposure @ 35 mW/cm^2, 254 nm		
	PMGI DEVELOP ❑ 60 sec SAL 101 spin develop at 500 rpm ❑ 30 sec DI water rinse at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT RESIST: ❑ Inspect photresist		
	STRIP 1813: ❑ 20 sec acetone gun at 1000 rpm ❑ 20 sec acetone rinse at 500 rpm ❑ 30 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes		
	INSPECT RESIST: ❑ Inspect photoresist for 1813 removal		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	DEKTAK POST HEIGHT: ❑ Measure resist step height in three locations Top _____ Middle _____ Bottom _____		

MEM Tunable VCSEL – Anchor (Mask #4)		
17 February, 2002		**Piece ID:**
	POST REFLOW & INSPECT WAFER: ❑ 120 sec 250 ° C hot air oven bake **USE OVEN TRAY** Start timer after door is closed ❑ Inspect for resist reflow. Reflow again if necessary	**Reflow Time:**
	TENCOR MEASURE: ❑ Measure resist step height in center and save Tencor profile. Resist Height: _____	**Finish Date**
	HARD BAKE: ❑ Place in 90 ° C hot air oven 60 min before bridge lithography	**Finish Time**

MEM Tunable VCSEL – Evap Bridge Metal (Mask #6)

17 February, 2002 **Piece ID:**

Init.	Process Step	Notes	Date Time
	PREPARATIONS: ❑ Check metal schedule: 500 Å Ti / 10000Å Au / 500 Å Ti (Titanium/Gold/Titanium) **OR** 500 Å Mo / 8000Å Au / 500 Å Mo (Molybdenum/Gold/Molybdenum)	**Start Date** **Start Time**	
	HARD BAKE: ❑ Place in 90 ° C hot air oven 60 min before bridge lithography **IF** Post Lithography was not immediately performed previously, otherwise: **DEHYDRATION BAKE:** ❑ 60 sec 110° C Hot plate bake		
	LOR10 COAT: ❑ Flood wafer with LOR10 ❑ 30 sec Spin at 4000 RPM, Ramp=200 ❑ 2 min 170 ° C Hot Plate Bake ❑ Cool Wafer		
	1818 COAT: ❑ Flood wafer with 1818 ❑ 30 sec Spin at 4,000 RPM, Ramp=200 ❑ 75 sec 110° C Hot Plate Bake ❑ Check cleanliness of wafer backside		
	Edge Bead Removal : ❑ Flood expose edge bead mask for 2 min (2mw/cm^2) ❑ Develop for 60 seconds using LDD26W developer ❑ DI rinse, N2 dry		
	EXPOSE 1818 TO BRIDGE MASK: ❑ Align to Bottom Metal alignment mark ❑ 60 sec Exposure		
	1818 DEVELOP: ❑ 45 sec develop with 351:DI Water (1:5) at 500 rpm ❑ 30 sec DI Water rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	LOR10 DEVELOP: ❑ 90 sec LDD 26W spin at 500 rpm ❑ 30 sec DI H_2O rinse at 500 rpm ❑ Dry with N_2 on clean Texwipes		
	INSPECT RESIST: ❑ Inspect photoresist using yellow filter		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	PRE-METAL DIP: ❑ 30 sec BOE : DI water (1:7) ❑ 3x bucket DI water rinse ❑ Dry wafer on clean texwipes with Nitrogen		
A. **B.**	**BRIDGE METAL DEPOSITION:** ❑ Evaporate 500 Å Ti / 15000Å Au / 500 Å Ti (Titanium/Gold/Titanium) **OR** ❑ Evaporate 500 Å Mo / 15000Å Au / 500 Å Mo (Molybdenum/Gold/Molybdenum)		

MEM Tunable VCSEL – Evap Bridge Metal (Mask #6)			
17 February, 2002		**Piece ID:**	
	STRIP 1818: ❑ Use acetone soak to gently lift off metal ❑ Visually inspect for metal removal ❑ 20 sec acetone rinse at 500 rpm ❑ 20 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes	**WARNING:** Acetone gun may strip gold structure from substrate	
	INSPECT WAFER: ❑ Inspect for resist removal	**Finish Date**	
	DEKTAK BRIDGE HEIGHT: ❑ Measure bridge step height using Dektak box Record height measurements: _____ _____ _____	**Finish Time**	

MEM Tunable VCSEL – Dielectric DBR (Mask #8)			
17 February, 2002		**Piece ID:**	
Init.	**Process Step**	**Notes**	**Date Time**
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	PRE DIP: ❑ 30 sec BOE:DI (1:7) dip ❑ 3X DI water bucket rinse ❑ Dry with nitrogen on clean texwipes		
	SiO2 DEPOSITION: ❑ Deposit 1667 Å of silicon oxide ❑ PECVD: ___ min, 17 sccm 5% Silane in N_2, 25 sccm N_2, 10 sccm NH_4, 20W, 850 mTorr, 200 ° C (Process 7) **NOTE: Temp < 200C** **OR:** ❑ Sputtered: ___ min, ___ sccm Silane, ___ sccm N_2, ____W, 850 mTorr ❑ Measure thickness on silicon with ellipsometer Thickness_____ Index of refraction_____		
	NITRIDE DEPOSITION: ❑ Deposit 1222 Å of silicon nitride ❑ PECVD: ___ min, 17 sccm 5% Silane in N_2, 25 sccm N_2, 10 sccm NH_4, 20W, 850 mTorr, 200 ° C (Process 7) **NOTE: Temp < 200C** **OR:** ❑ Sputtered: ___ min, ___ sccm Silane, ___ sccm N_2, ____W, 850 mTorr ❑ Measure nitride thickness on silicon with ellipsometer Thickness_____ Index of refraction_____		
	Repeat SiO2 & NITRIDE DEPOSITION ❑ Deposit SiO2/Si3N4 Pairs until stack is complete ❑ Number of Pairs_____ Calculated Thickness_____		
	INSPECT NITRIDE: ❑ Inspect wafer under microscope and look for ❑ Uniform color ❑ Pin holes ❑ Cracks around metal		
	1818 COAT: ❑ Flood wafer with 1818 ❑ 30 sec spin at 4000 rpm, ramp=200 ❑ 75 sec 110 ° C hot plate bake ❑ Use acetone to remove 1818 on backside		
	1818 Edge Bead Removal: ❑ Flood expose edge bead mask for 2 min (2mw/cm^2) ❑ Develop for 30 seconds using 351 developer ❑ DI rinse 30 sec, N2 dry ❑ Remove Edge Bead stragglers with q-tip and Acetone	Use foil EBR mask	
	INSPECT Edge Bead: ❑ Check to ensure 1813 & PMGI Edge Bead Removal		
	EXPOSE 1818 with DBR MASK: ❑ Align to Bottom Metal alignment mark ❑ 60 sec Exposure		
	1818 DEVELOP: ❑ 45 sec develop with 351:DI (1:5) at 500 rpm ❑ 30 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with nitrogen on clean texwipes		

MEM Tunable VCSEL – Dielectric DBR (Mask #8)			
17 February, 2002		**Piece ID:**	
	INSPECT LITHOGRAPHY: ❑ Place wafer flat towards top of microscope ❑ Inspect wafer alignment with yellow filter on microscope ❑ Check Lithography : ❑ Open ❑ Clean ❑ Sharp Definition		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	NITRIDE ETCH DIP: ❑ 30 sec BOEI:DI (1:10) dip ❑ 3X DI water bucket rinse ❑ Dry with nitrogen on clean texwipes **OR** **RIE ETCH NITRIDE:** ❑ 30 min dry etch in double barrel RIE using Freon CF-23 etchant ❑ Inspect under microscope to ensure Si3N4 removal in Anchor holes	-isotropic etch -anisotropic etch	
	INSPECT WAFER: ❑ Inspect for nitride removal		
	STRIP 1818 ❑ 20 sec acetone gun at 1000 rpm ❑ 20 sec acetone rinse at 500 rpm ❑ 30 sec Isopropanol rinse at 500 rpm ❑ 10 sec DI rinse at 500 rpm ❑ Dry with nitrogen at 500 rpm ❑ Dry wafer with Nitrogen on clean texwipes	**WARNING:** acetone gun may damage gold mechanicals -use 10min soak instead	
	INSPECT RESIST: ❑ Inspect photoresist for 1818 removal		
	ASHER: ❑ 4 min, 200 W, 400 sccm O_2, LFE		
	TENCOR MEASURE: ❑ Measure resist step height in center and save Tencor profile. Resist Height: _____	**Finish Date**	

MEM Tunable VCSEL – Backside Metal			
17 February, 2002		**Piece ID:**	
Init.	**Process Step**	**Notes**	**Date Time**
	Backside Metalization ❏ Mount sample to sapphire substrate using Crystal Bond 509 -- *Heat hotplate to 130° C* -- *Place sapphire substrate on hotplate* -- *Place sample UPSIDEDOWN on melted crystal bond (ensure all air bubbles have been removed)* ❏ Acetone rinse to remove excess crystal bond ❏ Methanol, Isopropanol rinse, N_2 dry ❏ Coat edges of sample and exposed sapphire surface with 1818 resist ❏ 5 min HPB @ 110°C ❏ 30 sec BOE (7:1) dip ❏ DI rinse, N_2 dry (ensuring all water has been removed ~ decreases pumpdown time) Standard SND n-Ohmic metalization (200 Å Ti, 2500 Å Au)		
	Remove Wafer from Sapphire Substrate ❏ Score metal (on Sapphire Substrate – NOT on wafer) w/ tweezers ❏ Soak wafer and substrate in Acetone bath for 5 min ❏ Rinse wafer with Acetone spray ❏ Swab edges of sample with Acetone ❏ Heat hotplate to 130ºC ❏ Heat substrate and remove sample once Crystal Bond 509 melts ❏ Remove Crystal bond from sample		
	Clean Wafer ❏ Spin clean wafer with acetone, methanol, isopropyl alcohol, and DIW 30 seconds each @ 500 rpm ❏ N_2 blow dry		

Appendix B. Molecular Beam Epitaxy Growth Sheets

This appendix contains the growth sheets maintained by the MBE Gen II crystal grower for the three epitaxial growths used for this research.

MBE# G2- 2545 Orgn. SNDD POC Feld Date 26 Jul 99

Device & Use VCSEL n+ mirror to check oven drift and resistivity

Substrate 3" SI AXT G078K264102 #8 Orient. 2°<100> Holder A

OVENS (mv, bfp)

Si 22.8 Time 0935 RT: 70.9 °F RH: 42%

As 6.7, 908, 1.5, 7.8E-6 Cracker

Al na, 21.60,>3.0E-7, .93 >use as .9 Ox. Desorb. (°V) 580

Ga 1100, 16.59(16.53), ~6.9E-7 , 1.01 Rotate (rpm) 30

In na, 10 Source Flg. Temp 42 °C WW -18 °C

Be 10 GC pump cur. 3.6 µA Aux 14.4 µA

Layer (starting at substrate)				Angst.	Sec.	Repeats	Temp. (°V, volt, amp)
GaAs		Si		696.023	243.5		600, 30.1, 5.3
4E18				812.685	287.17	/--- 30 ---	
Al Ga2As	x=.9	Si	4E18	696.023	243.5	----------/	
GaAs		Si					
4E18							

Comment

Fits for mirroor indicate AlGaAs layer thin by ~3% so set Al higher to try and compensate.

Reflectivity fit has the AlGaAs layer .5% thin

MBE# G2- 2752 Orgn. SNDD/AFIT POC Nelson/Harvey Date 11 Feb 02

Device & Use p-mirror for dielectric tunable filter

Substrate 3" SI AXT Go78K264102 #37 Orient. 2°<100> Holder Z

OVENS (mv, bfp)

Si	800	Time 1050	RT: 68.1 °F RH: 24%
As	3.84, 900, .05, 6.7e-6	Cracker	
Al	1088, 1148, , .87 (.92 after run)	Ox. Desorb. (°V)	700
Ga	1010, 820, 5.8e-8, .1	Rotate (rpm)	30
In	na, 500	Source Flg. Temp	36 °C WW -13 °C
Be	68	GC pump cur.	3.8 µA Aux 12.8 µA

Layer (starting at substrate)			**Angst.**	**Sec.**	**Repeats**	**Temp.** (°V, volt, amp)
Ga2As	C	1e19	696	248.86	/ -- 15 --	690
AlGa1As	C	1e19	812.65	296.57	----------/	
As	>C			150		
Ga2As	C	4e19	696	248.86		

Comment

new holder

Appendix C. Fabrication Techniques

C.1 Introduction

This chapter provides a general overview of the fabrication techniques and equipement I utilized to construct MEMS devices. For a step by step account of device processing, see appendix A.

C.2 Thin Film Deposition

Surface micromachined MEMS devices are constructed entirely using successive layers of thin film material, deposited and patterned one by one. This section covers the thin film deposition methods utilized for MEMS fabrication.

C.2.1 Spin-on Thin Films. Spin coating is the most practical method of applying thins films such as photoresist to wafer surfaces. The film material is applied as a solvent mixture to the wafer, which is mounted on a rotating vacuum chuck. As the wafer material is spun at a rotational velocity of several thousand revolutions per minute, the film is spread evenly across the surface due to the centrifugal force. The factors determining applied film thickness are the rotation speed and the film material properties. Applied film thickness varies anywhere from 0.1 μm to 50 μm , depending on the application.

C.2.2 Sputter Deposition. The sputter deposition process utilizes inert ions (such as Ar+), which are accelerated using a DC or RF potential. The accelerated ions bombard a target material, causing clusters of the target material to be vaporized from the surface. These vaporized ions are then redeposited on the surface of a substrate located near the target. Nearly any material may be deposited by sputtering if a sufficiently high-energy plasma of vaporized ions can be generated [1]. Figure C.1 details the difference between the two prevalent deposition techniques, DC and RF sputtering. DC sputter deposition requires a conductive target to close

the path for the electrical current between the power supply and the plasma, which acts as a resistor [1]. This allows a direct current to flow between the power supply and the resistive plasma. On the other hand, if the target material is non-conductive, no electrical circuit can be formed using a DC circuit. In this case the target may be considered a capacitor, and will require an RF power supply for current to flow. This adds an extra layer of complexity to the sputtering system design. The sputter deposition of dielectric thin-films such as SiO_2, Si_3N_4, and TiO_2 requires an RF configuration.

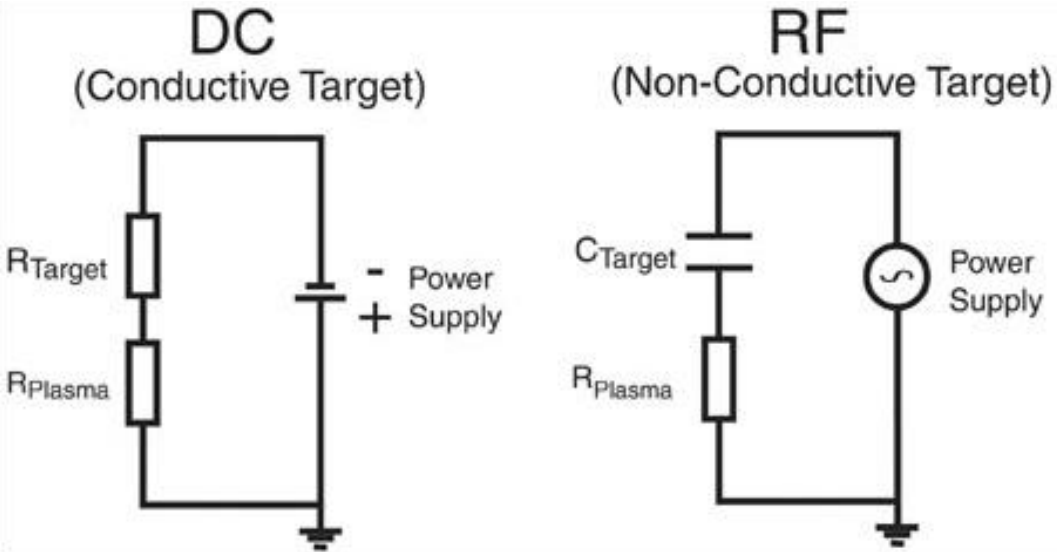


Figure C.1 Simplified electrical circuit diagrams for sputtering of a conductive and non-conductive target. If the target is non-conductive a direct current can not flow, since the circuit is interrupted. Instead an RF power supplier must be employed [1].

A primary concern when depositing a thin-film, whether by evaporation or by sputtering, is the stress gradient formed in the deposited material. Stress in thin-films can be either compressive or tensile, depending on numerous factors such as the flux and energy of the particles striking the film. Studies indicate [7] that the normalized momentum

$$P = g \cdot (M \cdot E)^{\frac{1}{2}} \tag{C.1}$$

where g is the energetic particle/atom flux ration, M the bombarding particle mass, and E its energy, may be an appropriate stress scaling factor. An idealized stress-momentum curve is shown in figure C.2. By applying a DC bias during RF sputter deposition, it is possible to alter the momentum of the target particles and to nearly eliminate stress in the material deposition.

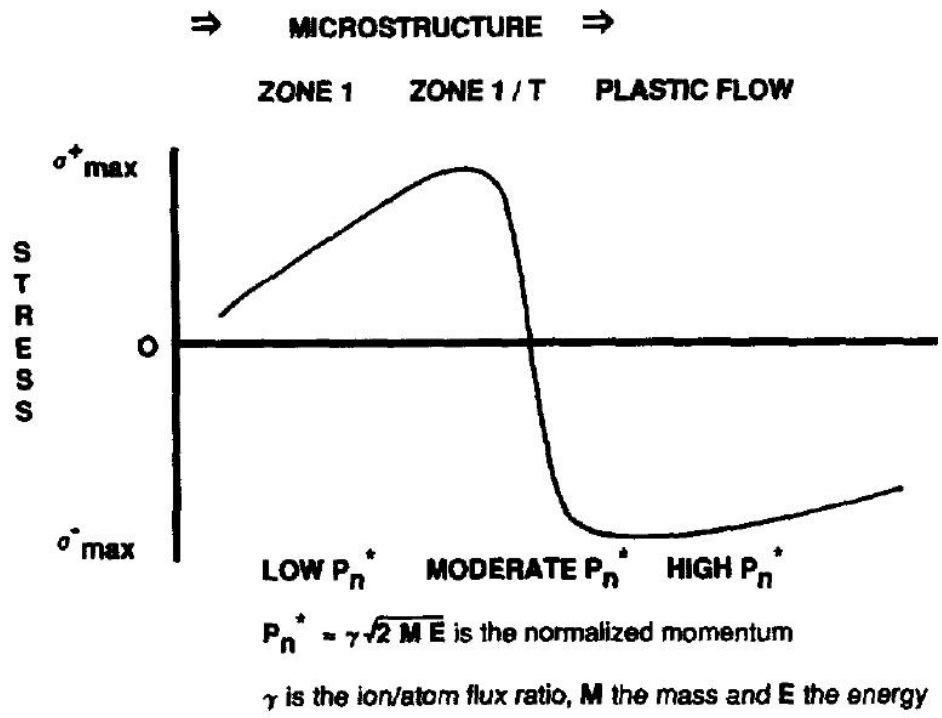


Figure C.2 Idealized stress-normalized momentum curve for sputtered films [7].

C.2.3 Evaporation. A common technique for depositing thin film materials is evaporation from a heated source. A typical evaporation system, as shown in figure C.3, utilizes a vacuum chamber to remove the atmosphere down 10^{-6} or 10^{-7} Torr. A crucible containing the material is then heated, causing the material to evaporate. As a shutter is opened and closed, the evaporated material condenses onto a sample (ie. the wafer or substrate). The thickness of the applied material is controlled by the amount of time the shutter is open and the vapor pressure of the evaporated material. Evaporated material travels in a straight path from the

crucible to the sample, and thus tends to suffer from shadowing effects that yield non-uniform thickness and poor step coverage [3]. This is very useful for a metal lift-off process, as the metal cannot overcoat steep or undercut steps.

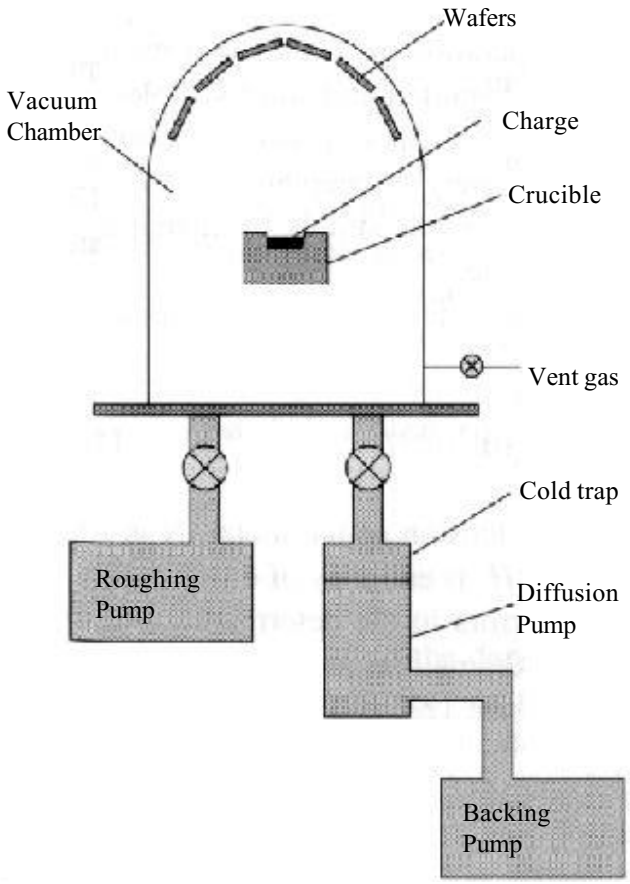


Figure C.3 A typical metal evaporation system.

C.2.4 Plasma Enhanced Chemical Vapor Deposition. Chemical vapor deposition (CVD) is a process for depositing a materials onto a wafer surface. The CVD process works by heating a gas until it breaks into it's component materials. Some of these particles make their way to the wafer surface where they attach and grow as a solid film. The CVD process introduces potentially damaging stress into deposited layers. This stress and other mechanical properties can be controlled to some degree by the deposition conditions and subsequent annealing steps [6]. In ad-

dition, the typical CVD process involves temperatures from $700°C$ to $1,100°C$. This is far to hot for materials used in MEMS fabrication, such as gold (Au), aluminum, or polyimide. Structures that are micromachined from these materials would be destroyed by the intense heat.

Plasma enhanced chemical vapor deposition, or PECVD, relies on plasma induced decomposition of gaseous compounds instead of thermal reactions. This means the process temperature is a comparatively low $200°C$. This is low enough to leave previously fabricated MEMS structures undamaged. For the purposes of this research, only silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) are deposited by PECVD with the following simplified plasma reactions:

$$SiH_4 + O_2 \longrightarrow SiO_2 + 2H_2 \tag{C.2}$$

$$2SiH_4 + N_2 \longrightarrow 2SiNH + 3H_2 \tag{C.3}$$

where SiH_4 is the gas silane.

One problem with PECVD deposited nitrides is their lack of stoichiometry (Si_xN_y) and their incorporation of hydrogen, which may effect etchant resistance [3]. The stoichiometry and stress of deposited nitride is significantly affected by changes in the plasma drive frequency of the PECVD system. A frequency of 13.56 MHz yields approximately 400 MPa of tensile stress, while a frequency of 50 kHz yields approximately 200 MPa of compressive stress [3]. Modern PECVD systems use rapid modulation between different frequencies to obtain nearly stress free film deposition.

C.3 Photolithography

An essential part of MEMS device fabrication is the photolithography process, involving the application and removal of light sensitive thin films known as photoresist. There are numerous photoresists available, each appropriate for a specific application. A common characteristic of all types of photoresist is their sensitivity

to ultra-violet light (UV). The application of UV breaks down or strengthens the chemical bonds of the resist where it is exposed. UV applied to a positive resist will break down the chemical bonds, while UV applied to a negative resist will strengthen the bonds. After exposure, the resist can be placed in a developer solution, which dissolves the weakened chemical bonds and leaves the strong bonds intact. Typically, UV light is shone through a patterned quartz mask and focused onto the photoresist film. The photoresist which has been exposed to light is removed by the developer solution. After removal of the unwanted resist from the wafer surface, any number of process steps can be accomplished, including the deposition of new material or the etch removal of old material in specific locations.

A similar material known as polymethylglutarimide (PMGI) is a polymer positive resist ideally suited for lift-off processing applications or as a sacrificial layer for airbridge or membrane fabrication. PMGI resists will not intermix when used in combination with imaging resists, eliminating the need for plasma descum steps [5], and is spin coatable to a wide variety of film thicknesses. In addition, it planarizes very easily under controlled bake conditions, making it ideal as a sacrificial layer for micro-electromechanical structures. PMGI can be patterned and removed easily by using standard photoresist lithography techniques.

C.3.1 Mask Fabrication. The patterned quartz masks utilized during photolithography are designed by engineers using commercially available CAD layout tools. The layout pattern is broken down into small rectangular regions (typically 50 nm to 500 nm on a side, as determined by mask design restrictions) and transferred to the mask making system. A glass plate is coated with a thin film of light blocking chromium and a photoresist layer. The photoresist is then exposed to UV light rectangle by rectangle according to the design layout. Depending on the design, this process may be repeated hundreds of thousands of times to completely expose the mask surface. Upon completion, the photoresist is developed and the unwanted chromium is etched from the glass surface.

When an engineer designs a mask, he or she must determine whether it will be a clearfield or darkfield mask based on a number of design options. The definition of a clearfield, or positive mask, is that all the open space on the layout design is transparent. A darkfield, or negative mask, is the opposite, and all the open space of the design layout is opaque (see figure C.4). Table C.1 lists the possible mask and photoresist combinations needed to perform a subtractive (etch) or additive (lift-off) processing step. Clearly, it is imperative the device fabrication process be carefully considered before submitting a mask design.

Table C.1 Mask Polarities and Orientation [4]

Desired Feature Polarity	**Resist Type**	**Pattern Processing**	**Mask Polarity Required**
Positive	Positive	Subtractive (Etch)	Clearfield
Positive	Positive	Additive (lift-off)	Darkfield
Positive	Negative	Subtractive (Etch)	Darkfield
Positive	Negative	Additive (lift-off)	Clearfield
Negative	Positive	Subtractive (Etch)	Darkfield
Negative	Positive	Additive (lift-off)	Clearfield
Negative	Negative	Subtractive (Etch)	Clearfield
Negative	Negative	Additive (lift-off)	Darkfield

C.3.2 Aligning multiple photolithography steps. Most device fabrication processes require multiple thin film layers to be deposited and patterned. Each layer typically requires a unique mask layout with completely different features. In order to ensure each mask step is correctly aligned before UV exposure, special features known as alignment marks are placed onto each mask. These marks are orientated with marks already in place on the wafer surface from previous mask exposure steps.

Ideally, an automatic step alignment system is used to expose each individual mask set, since this eliminates error introduced by manual alignment procedures. For this research project, manual alignment of each mask layer was required, making it difficult to perfectly align each process step. Mask alignment marks are designed to help the operator correctly and precisely align the masks before exposure.

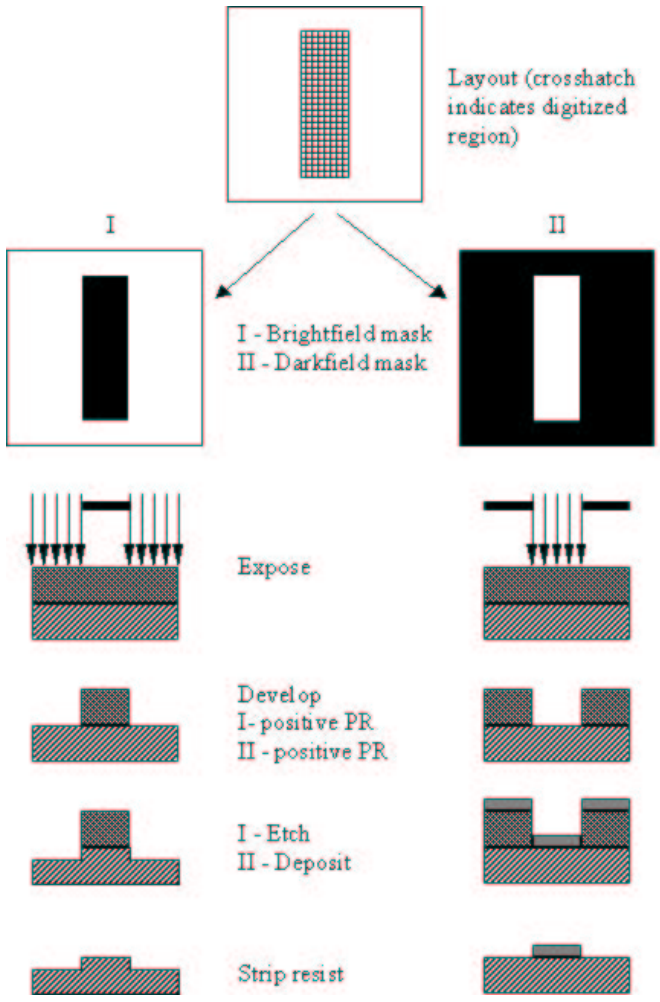


Figure C.4 Clearfield and Darkfield Mask Patterns [4]

C.4 Wafer Patterning

After a spun-on photoresist layer has been patterned by UV exposure and developed, the wafer surface is ready for material deposition and lift-off, or an etch step to remove unwanted material.

C.4.1 Lift-off. Lift-off processing is a common technique for depositing sputtered or evaporated materials onto the wafer. A layer of sacrificial photoresist or polyimide is spun onto the surface and patterned using photolithography as discussed above. Typically a 'negative' or 'dark field' mask is used to expose the photoresist,

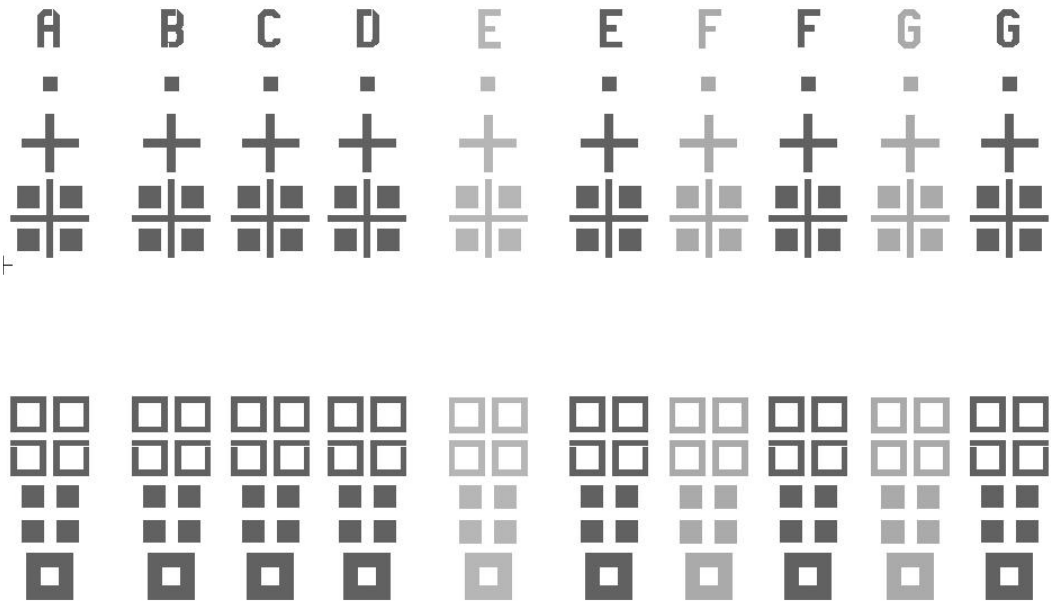


Figure C.5 Surface alignment marks patterned onto the wafer.

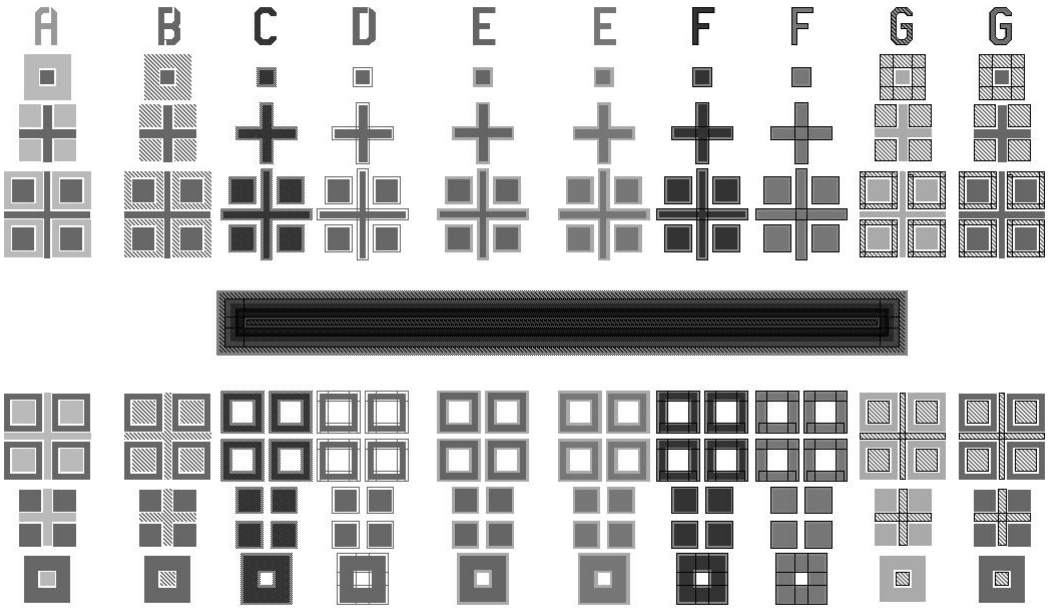


Figure C.6 Complete set of overlayed mask alignment marks.

since the features of interest will be deposited wherever photoresist has been removed. After development and removal of unwanted resist, material may be sputtered or evaporated onto the surface. The lift-off process takes advantage of the fact that

step coverage of sputtering and evaporation deposition methods is very limited, so the metal cannot overcoat steep or undercut steps [3]. The unwanted material is then lifted off by the removal of the sacrificial layer, leaving only the patterned deposited film.

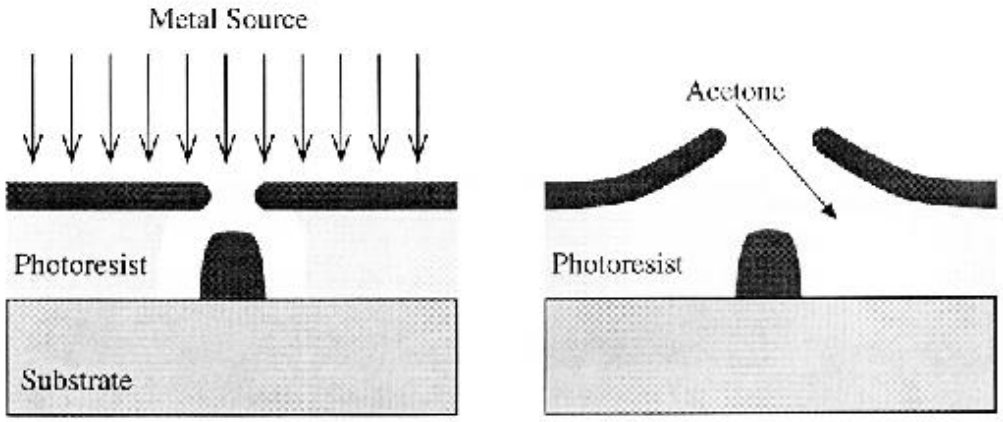


Figure C.7 Photoresist based lift-off metal deposition process used to fabricated metallization patterns. Metal is deposited by evaporation and adheres to the substrate where photoresist was exposed and developed away. After evaporation, the photoresist is dissolved in acetone, lifting off the undesired metal [3].

C.4.2 Reactive Ion Etching. Reactive Ion Etching, or RIE, involves the use of reactive etchants in a gaseous state. This etch process is also referred to as 'dry etching', since no wet chemicals are utilized. The etching takes place in a sealed chamber, pumped down to a pressure between 10 mTorr and 1 Torr [6]. The wafer sample is placed in the chamber between two electrodes, and an RF potential is applied. RF energy accelerates stray electrons, increasing their kinetic energy until they can break the chemical bonds of the reactant gases, forming ions and additional electrons [3]. This creates a plasma which reacts with the solid material of the wafer surface. Since energetic ions supply the necessary energy for reactions to occur, RIE systems can operate at temperatures between $150°C$ and $250°C$, and some can even be run at room temperature. In addition, the dry etch process can

achieve remarkable anisotropy where perpendicular bombardment of the surface by ions drives the etchant reaction [3].

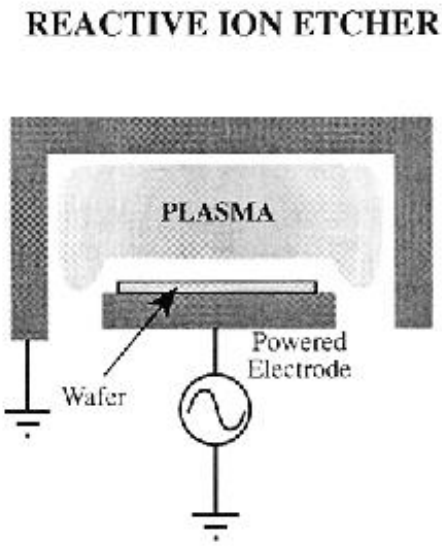


Figure C.8 Schematic diagram of Reactive Ion Etcher (RIE) [3].

A common RIE etchant is SF_6 Freon (C_2CIF_5), which is used to anisotropically etch silicon and other thin films. Dissociation reactions release fluorine free radicals, which perform most of the etching action [3].

$$e^- + SF_6 \longrightarrow SF_5 + F + e^- \tag{C.4}$$

This etchant is fairly aggressive compared with other RIE reactants. It is used during my research for the removal of unwanted $Si_3N_4$with mixed results. It successfully removes Si_3N_4, but it undercuts more than desired. In my research I preferred using more benign etch chemistries which provided sharper sidewalls.

The RIE etchant I used to pattern PECVD deposited Si_3N_4 and SiO_2 is the freon based CF-23 (CHF_3). For etching $Al_xGa_{1-x}As$ epitaxial materials and GaAs substrates, I utilized the RIE etchants BCL_3 and Cl_2.

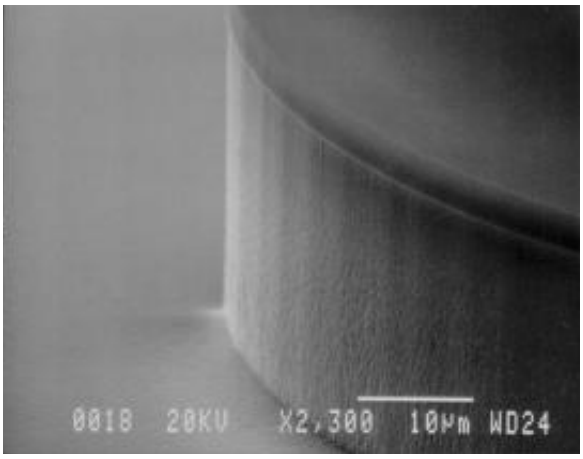


Figure C.9 RIE etch exhibiting extreme crystal plane selectivity.

Dry etch RIE processes are effected by factors such as the amount of exposed substrate in a given area and the geometries of the etched features. Variations in the consumption of reactants at the surface may cause unexpected changes in etch rate across the substrate [3].

C.5 Ellipsometry

Ellipsometry is a nondestructive technique used to measure the index of refraction and thickness of surfaces and very thin films. Elliptically polarized light is utilized to used to take measurements of films from one angstrom up to several microns thick. No other measuring technique is as direct or precise as ellipsometry [2]. It is considered to be superior to other thin film measurement techniques since two parameters (δ and ψ) are independently determined at each measurement point. Reflectometry calculates intensity at each data point, and therefore is limited to thickness measurements only. Ellipsometry is insensitive to intensity fluctuations of the source, and surface roughness. The substrate surface beneath the film can be a semiconductor, dielectric, or metal. The film itself can be transparent or absorbing, and the measuring polarized light can range from UV to IR. For the purpose of the this study, ellipsometry measurements were taken of SiO_2 and Si_3N_4 deposited

via sputtering and PECVD, between the wavelengths of 550 nm to 1100 nm. By carefully measuring the index of refraction values of the deposited dielectrics, it was possible to accurately deposit the alternating stacks needed to create the DBR top mirror.

Ellipsometry makes it's calculations based on the polarization change of light reflected from a film coated surface. In order to accurately describe the polarization of an elliptical beam, the amplitude ratio (ψ), and the phase difference (δ) must be determined. A mathematical relationship between the thickness of the film and the optical constants of the substrate material can be describes as follows:

$$tan\Psi e^{\Delta} = \frac{(r_{p01} + r_{p12}e^{2i\Delta})(1 + r_{01}r_{12}e^{2i\Delta})}{(1 + r_{p01}r_{p12}e^{-2ix})(r_{01} + r_{s01}e^{-2ix})} \tag{C.5}$$

where

$$x = \frac{2\pi}{\lambda} d(n_1^2 - n_0^2 sin\phi^2)^{\frac{1}{2}} \tag{C.6}$$

and

r_{01} = Fresnel reflection coefficient for ambient medium-film interface

r_{12} = Fresnel reflection coefficient for the film-substrate interface

Therefore, the real(n) and complex(k) indices of refraction, corresponding to the optical transmittance and absorptance of a given material, may be calculated from equation C.5, by direct measurement of the ψ and Δ values over a wide range of frequencies. This was accomplished at AFRL/SN for various mole ratios of $Al_xGa_{1-x}As$ grown via molecular beam epitaxy (MBE) as shown in Figure C.10. And for the dielectric materials SiO_2 and Si_3N_4 grown by PECVD, as shown in Figure C.11.

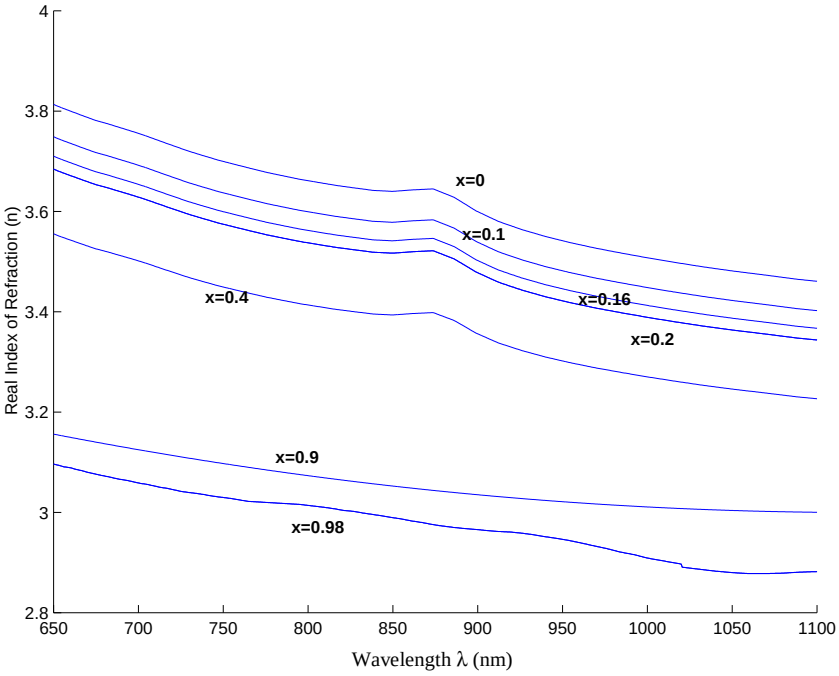


Figure C.10 Measured real index of refraction (n) vs. wavelength for various mole ratios (x) of $Al_xGa_{1-x}As$ grown via MBE.

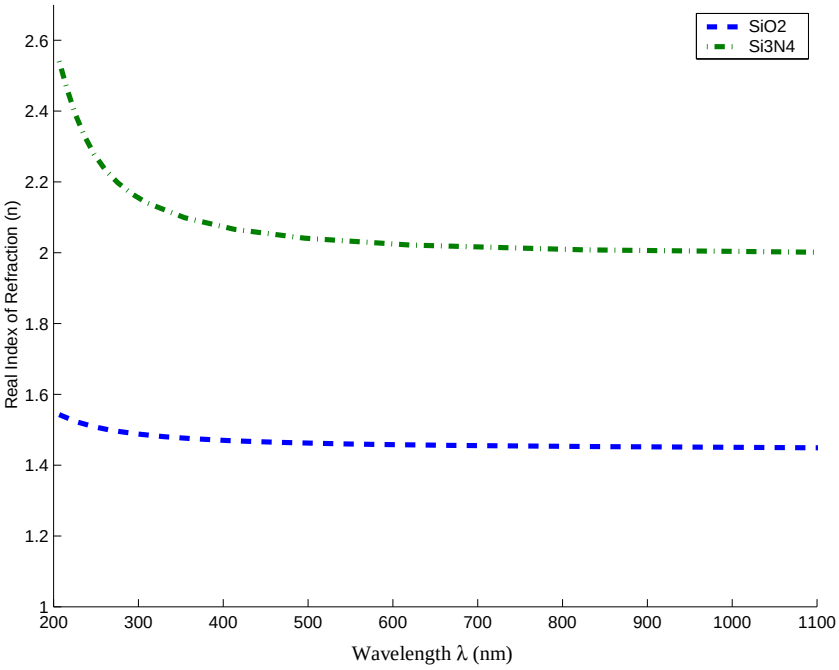


Figure C.11 Measured real index of refraction (n) vs. wavelength for SiO_2 and Si_3N_4 grown by PECVD.

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Appendix D. Laboratory Equipment List

This appendix lists the laboratory equipment I utilized for the fabrication of my MEM devices.

1. Solitec Model 5100 Spinner. The spinner was used throughout fabrication for wafer cleaning, applying photoresist, developing photoresist, and metal lift-off.

Figure D.1 Solitec Model 5100 Spinner.

2. Karl Suss MJB-3 Mask Aligner. Rated intensity of 2 mW/cm^2 at $\lambda = 405\ nm$. Every processing step required the use of the mask aligner to align the lithography mask to the wafer surface and expose the photoresist to UV light for patterning.

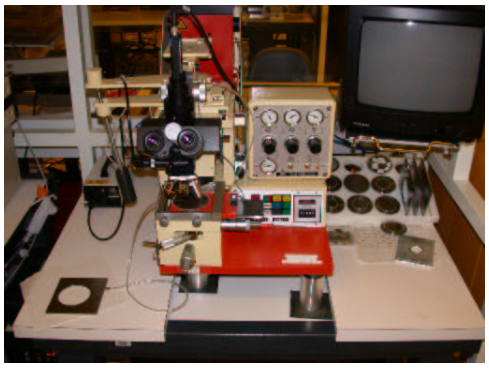

Figure D.2 Karl Suss MJB-3 Mask Aligner.

3. HTG Deep Ultra Violet (DUV) System with xenon arc lamp. Emitts intensity of 16.5 mW/cm^2 at $\lambda = 240\ nm$. The DUV system was required to pattern the photo-sensitive PMGI sacrificial layer

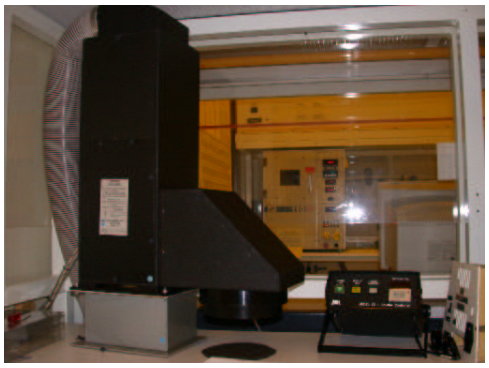

Figure D.3 HTG Deep Ultra Violet (DUV) System.

4. KLA-Tencor P-10 Surface Profiler. This system is used to quickly make step height measurement across a wafer surface or MEM structure.

Figure D.4 KLA-Tencor P-10 Surface Profiler.

5. Plasma Therm 790 Series Plasma Enhanced Chemical Vapor Deposition (PECVD) System. This system was utilized for the deposition of Si_3N_4 and SiO_2 as described in section C.2.4.

Figure D.5 Plasma Therm 790 Series PECVD system.

6. Zygo NewView 5000 Microscope Interferometer. The interferometer microscope was used to measure the 3D surface profile of individual MEM devices. Height measurements were used to determine voltage vs. actuation measurements.

Figure D.6 Zygo NewView 5000 Microscope Interferometer.

7. Temescal BJD-1800 Bell Jar Deposition System for E-beam metallization. All metallization steps were accomplished using this E-beam metallization system.

Figure D.7 Temescal BJD-1800 E-beam metallization system.

8. LFE Plasma Systems 110 Barrel Plasma Oxygen Asher. The plasma oxygen was an essential piece of equipment utilized to clean away resist scum and stringers after photolithography processing.

Figure D.8 LFE Plasma Systems 110 Barrel Plasma Oxygen Asher.

9. Plasma-Therm, Inc 70 Series Dual Chamber RIE System. The dual chamber RIE system was used to anisotropically etch SiO_2 and Si_3N_4 layers using the chemicals CF-23 or CF-14.

Figure D.9 Plasma-Therm, Inc 70 Series Dual Chamber RIE System.

10. Plasma-Therm, Inc SLR Series Inductively Coupled Plasma (ICP) RIE System. This RIE system was utilized to anisotropically dry etch GaAs and $Al_xGa_{1-x}As$ layers with the chemicals boron trichloride (BCL_3) and chlorine gas (CL_2).

Figure D.10 Plasma-Therm, Inc. SLR Series ICP system.

Appendix E. Matlab Application Code

This appendix lists the matlab code written to assist with the design and simulation of MEM tunable VCSELs. In order to use these functions, the MATLAB® toolbox 'oeng775tools' must be installed and in the MATLAB® path.

Example MEM Tunable VCSEL design file for use with VCSEL_TopSim.m function

```
% Sample Design file for epitaxial growth of device with 3 80Ang
Quantum Wells
% Capt Harvey
% 25 Jan 02

% Material  Thick(Å)   n      k   LayerType    MultiLayers

      Air   0        1.000  0.000 Incident       0 0

      Si3N4 1222.38  2.004  0.000 TopDBR         Layer1  9.5
      SiO2  1688.83  1.451  0.000 TopDBR         Layer2  0

       Air  17150.0  1.000  0.000 AirGap         0 0

      GaAs   696.02  3.520  0.000 BufferDBR      0 0
  AlGaAs98   837.75  2.925  0.000 BufferDBR      0 0

      GaAs   527.78  3.520  0.000 MicroCavClad1  0 0
      GaAs   532.78  3.520  0.000 MicroCavClad2  0 0

      GaAs   100.00  3.520  0.000 QW_Low         Layer1  3.5
    InGaAs    80.00  3.711  0.157 QW_High        Layer2  0

      GaAs   532.78  3.520  0.000 MicroCavClad2  0 0
      GaAs   527.78  3.520  0.000 MicroCavClad1  0 0

  AlGaAs98   837.75  2.925  0.000 BottomDBR      0 0

      GaAs   696.02  3.520  0.000 BottomDBR      Layer1  26
  AlGaAs90   812.68  3.015  0.000 BottomDBR      Layer2  0
```

VCSEL_TopSim.m MATLAB FUNCTION

```
function VCSEL_TopSim(fname,RunName,OxideHMat,doCalculations,getInc,...
    getWavelengthSpectrum,getLambdaRange, doRandom, maxError, randomCount,lambdaDesign,...
    lambdaStart,lambdaEnd, lambdaStep, AirGapStart,AirGapStop,AirGapStep,...
    SWaveStart,SWaveStop,SWaveStep,suppressGraphics)
%function VCSEL_TopSim(fname,RunName,OxideHMat,doCalculations,getInc,...
%    getWavelengthSpectrum,getLambdaRange, doRandom, maxError, randomCount,lambdaDesign,...
%    lambdaStart,lambdaEnd, lambdaStep, AirGapStart,AirGapStop,AirGapStep,...
%    SWaveStart,SWaveStop,SWaveStep,suppressGraphics)
%
% This function is composed of a series of subroutines to assist in the design
% and simulation of tunable VCSELs placed onto electrostatically
% actuated micro-electro-mechanical (MEM) flexures.  The central
% emission design wavelength defaults to 980 nm.  The MEM flexure moves vertically,
% thus increasing or decreasing the aip gap.  The initial airgap defaults to 2um.
%
% To use this program, make a directory to store files and cd (change directory) to it.
% Make sure the directories: memtools, datafiles, and oeng775tools are in the path statement.
% Make sure the 'Design_spec' file is in the path or the current directory.  If the openFig
% variable is used, all Figures will be left open.  This may be as many as 60 figures,
% depending on settings - Figures will also be stored as eps files.
%
% Capt Michael Harvey
% 6 Sep 01

close all;

% Options
TRUE=1;
FALSE=0;

% if no arguments are given use these values to begin calulations
if ~exist('fname') fname='Design_spec.txt'; end
if ~exist('RunName') RunName='SiO2/SiN'; end
if ~exist('doCalculations') doCalculations = FALSE; end
if ~exist('getInc') getInc = FALSE; end
if ~exist('getWavelengthSpectrum') getWavelengthSpectrum = FALSE; end
if ~exist('getLambdaRange') getLambdaRange = FALSE; end
if ~exist('doRandom') doRandom=FALSE; end
if ~exist('maxError') maxError=5; end
if ~exist('randomCount') randomCount=10; end
if ~exist('OxideHMat') OxideHMat='Si3N4'; end
if ~exist('suppressGraphics') suppressGraphics=TRUE; end


% Default Design settings
if ~exist('lambdaDesign') lambdaDesign = 9800; end% Angstroms
if ~exist('lambdaStart') lambdaStart = 8500; end
if ~exist('lambdaEnd') lambdaEnd = 11000; end
if ~exist('lambdaStep') lambdaStep = 1; end

% Desired min VCSEL mirror reflectivities
RminDBR1 = .95;   %Top Oxide DBR
RminDBR2 = .999;   %Bottom Semiconductor DBR

% Material Data is loaded into memory in order to increase data access speed.
%  There is a tenfold+ increase in speed by loading the data sets only once,
%  and doing the interpolation whenever needed

GaAs_data = load('GaAs.dat');
AlAs_data = load('AlAs.dat');
AlGaAs90_data = load('Al(0.90)Ga(0.10)As.dat');
AlGaAs98_data = load('Al(0.98)Ga(0.02)As.dat');
InGaAs_data = load('InGaAs.dat');
TiO2_data = load('TiO2.dat');
SiO2_data = load('SiO2.dat');
Si3N4_data = load('si3n4.dat');

% Design index of refraction for each layer
NLAir = 1;
```

```
NLowMat = ['AlGaAs90'];
NLow = getIndxr(AlGaAs90_data, lambdaDesign)
NLowReal = real(NLow);

NHighMat = ['GaAs'];
NHigh = getIndxr(GaAs_data, lambdaDesign)
NHighReal = real(NHigh);

NIncident = NLAir;
NSubstrate = getIndxr(GaAs_data, lambdaDesign);

NAlAs = getIndxr(AlAs_data, lambdaDesign);

if strcmp(OxideHMat,'Si3N4')
    OxideH = getIndxr(Si3N4_data, lambdaDesign)
elseif strcmp(OxideHMat,'TiO2')
    OxideH = getIndxr(TiO2_data, lambdaDesign)
end

OxideLMat = ['SiO2'];
OxideL = getIndxr(SiO2_data, lambdaDesign)

% Cladding Design: Thickness will be automatically adjusted
Clad1Material = ['GaAs'];  %GaAs
Clad1IndxDesign = getIndxr(GaAs_data, lambdaDesign);
Clad1IndxDesignReal = real(Clad1IndxDesign);

Clad2Material = ['GaAs'];  %GaAs
Clad2IndxDesign = getIndxr(GaAs_data, lambdaDesign);
Clad2IndxDesignReal = real(Clad2IndxDesign);

QWLMaterial = ['GaAs'];
QWLIndxDesign = getIndxr(GaAs_data, lambdaDesign);
QWLIndxDesignReal = real(QWLIndxDesign);

QWHMaterial = ['InGaAs'];
QWHIndxDesign = getIndxr(InGaAs_data, lambdaDesign)
QWHIndxDesignReal = real(QWHIndxDesign);

% Default tool settings
typeSP = 0;
y = 1;

if doCalculations == TRUE  % Calculate complete MEM tunable VCSEL structure
% =========== calculations begin ==============

CavityLength = (1.0); % half-lambda cavity
inc = -5.2;
AirGap = 17150;       %thickness of 2-layers SF11 Polyimide is approx 2um
%AirGap = 17150;
NpQW=3.5
NpDBRB=1; %Currently not in use, but must still be defined or script will crash
VariableQW = FALSE;

QWLThick = 100;
QWHThick = 80;
QWHThick_1 = 100;
QWHThick_2 = 80;
QWHThick_3 = 65;

% QW Design: each QW 1/45 of cavity length (to simplify design settings...)
%QWHThick = CavityLength*lambdaDesign/(45*QWHIndxDesignReal);
%QWLThick = CavityLength*lambdaDesign/(45*QWLIndxDesignReal);

% Assemble NpQW periods of QW L-H Pairs
[QWIndx,QWThk]=Pairs([QWLIndxDesign QWHIndxDesign],[QWLThick QWHThick],NpQW);

if VariableQW == TRUE
    QWThk = [QWLThick QWHThick_1 QWLThick QWHThick_2 QWLThick QWHThick_3 QWLThick];
end
```

```
% Assemble NpQW periods of QW Material Pairs
QWMaterial=SinglePair({QWLMaterial QWHMaterial}, NpQW);

LambdaThickQWL=lambdaDesign/((QWLThick*(NpQW + .5))*QWLIndxDesignReal);
LambdaThickQWH=lambdaDesign/((QWHThick*(NpQW - .5))*QWHIndxDesignReal);
LambdaThickQW = 1/LambdaThickQWL + 1/LambdaThickQWH
Delta=(CavityLength - LambdaThickQW)/2

% Calculate cladding thickness
if getInc==TRUE
  j=1;
  for inc = -300:1:300

    [IndxStack, ThickStack] = ...
        VCSEL_Stack(lambdaDesign,RminDBR1,RminDBR2,NLow,NHigh,NIncident,NSubstrate, OxideH, OxideL,
...
       CavityLength, NpQW, NpDBRB, Clad1IndxDesign,Clad2IndxDesign,LambdaThickQW,Delta,NLowMat,
NHighMat, NAlAs, ...
       OxideHMat, OxideLMat, Clad1Material, Clad2Material, QWMaterial, QWThk,QWIndx, NLAir, AirGap,
inc, typeSP, y);

    % code originally used to find amount to subtract from Clad1Thick to obtain resonance
    [EoPlusV,EoMinusV,IntensityV] = ...
      EoEvaluateQuick(NSubstrate,IndxStack,ThickStack,NIncident,lambdaDesign);
      %EoEvaluateQuick(NIncident,IndxStack,ThickStack,NSubstrate,lambdaDesign);
    Ivec(j,:) = [inc IntensityV(1:2)];
    j=j+1;
    inc
  end
  figure;plot(Ivec(:,1),Ivec(:,2));
  goodinc = Ivec(find(min(Ivec(:,2))==Ivec(:,2)),1)
  inc=goodinc;
  %return
end

[IndxStack, ThickStack, MaterialStack, DBR1Thick, NpDBR1, DBRBThick, NpDBRB, DBR2Thick, NpDBR2,
Clad1Thick,Clad2Thick,LabelStack] = ...
       VCSEL_Stack(lambdaDesign,RminDBR1,RminDBR2,NLow,NHigh,NIncident,NSubstrate, OxideH, OxideL,
...
       CavityLength, NpQW, NpDBRB, Clad1IndxDesign,Clad2IndxDesign,LambdaThickQW,Delta,NLowMat,
NHighMat, NAlAs, ...
       OxideHMat, OxideLMat, Clad1Material, Clad2Material, QWMaterial, QWThk,QWIndx, NLAir, AirGap,
inc, typeSP, y);


% Save Design Characteristics in ASCII format
save Design_spec.mat
fid = fopen(fname,'wt');
for i = length(MaterialStack):-1:1
  fprintf(fid,'%10s  %6.2f  %1.3f  %1.3f %s\n', ...
      char(MaterialStack(i)), ThickStack(i), real(IndxStack(i)), imag(IndxStack(i)),
char(LabelStack(i)));
end
fclose(fid);

%*********************************************************************
else
% Load Design File using matlab style comments to block unwanted lines
[MaterialStacktemp,ThickStacktemp,IndxStackReal,IndxStackImag,LabelStacktemp, Layer, NpLayer] = ...
    textread(fname,'%s  %f  %f %f %s %s %f','commentstyle','matlab')

% Search for Layer Stacks from input file and expand
% ie... parse the input file and build the Stacks
MaterialStack=[]; ThickStack=[]; IndxStack=[]; LabelStack=[];
i=1;
while i <= length(Layer)
    if strcmp(Layer(i),'Layer1')
        Nptemp = NpLayer(i);
        LayerNum=1;
        Indxtemp=[]; Thicktemp=[]; Materialtemp=[]; Labeltemp=[];
```

```
        if strcmp(LabelStacktemp(i),'BottomDBR')
            NpDBR2=NpLayer(i)
        elseif strcmp(LabelStacktemp(i),'TopDBR')
            NpDBR1=NpLayer(i)
        end
        while 1   %continue until break function
            LayerNext = strcat('Layer',num2str(LayerNum));
            if strcmp(Layer(i), LayerNext)
                Indxtemp = [Indxtemp complex(IndxStackReal(i),IndxStackImag(i))];
                Thicktemp = [Thicktemp ThickStacktemp(i)];
                Materialtemp = [Materialtemp MaterialStacktemp(i)];
                Labeltemp = [Labeltemp LabelStacktemp(i)];
            else
                break;
            end
            i=i+1
            if i > length(Layer) break; end
            LayerNum=LayerNum+1;
        end %while loop

        %replicate temp stack Nptemp times and add to end of main stack
        MaterialStack = [MaterialStack SinglePair(Materialtemp,Nptemp)]
        ThickStack = [ThickStack SinglePair(Thicktemp,Nptemp)];
        IndxStack = [IndxStack SinglePair(Indxtemp,Nptemp)];
        LabelStack = [LabelStack SinglePair(Labeltemp,Nptemp)];
    %Determine Incident and Substrate Index
    elseif strcmp(LabelStacktemp(i),'Incident')
        NIncident=complex(IndxStackReal(i),IndxStackImag(i));
        i=i+1;
    elseif strcmp(LabelStacktemp(i),'Substrate')
        NSubstrate=complex(IndxStackReal(i),IndxStackImag(i));
       i=i+1;
    else
    MaterialStack = [MaterialStack MaterialStacktemp(i)];
    ThickStack = [ThickStack ThickStacktemp(i)];
    IndxStack = [IndxStack complex(IndxStackReal(i),IndxStackImag(i))];
    LabelStack = [LabelStack LabelStacktemp(i)];
    i=i+1;
    end
end

% Since file is backwards, flip each array - arrays must be in column format (or won't work)
IndxStack = fliplr(IndxStack);
ThickStack = fliplr(ThickStack);
MaterialStack = fliplr(MaterialStack)
LabelStack = fliplr(LabelStack);

end %end Calculations section
%*************************************************************
% calculate random thickness variations for TopDBR mirror
% The value maxError defines the +/- percentage of error
% possible for each layer of the stack
ThickStackOrig=ThickStack;

if doRandom == TRUE
    for k=1:randomCount
        for i=1:length(ThickStack)
            if strcmp(LabelStack(i),'BottomDBR')
                randomError=2*(rand - 0.5)*(maxError/100)*ThickStackOrig(i);
                ThickStack(i) = ThickStackOrig(i) + randomError;
            end
        end

        %lambdaDelta = lambdaDesign * 0.05;
        lambdaDelta = 1; %use 0.5 when calculating for VCSEL and 1 for FP
        lambdaDeltaSpec = 0.25;
        lambdaBegin = lambdaDesign - 100;
        lambdaFinish = lambdaDesign + 100;
        j=1;
        for lambdatest = lambdaBegin:lambdaDelta:lambdaFinish
        % code originally used to find amount to subtract from Clad1Thick to obtain resonance
```

```
        [EoPlusV,EoMinusV,IntensityV] = ...
            EoEvaluateQuick(NSubstrate,IndxStack,ThickStack,NIncident,lambdatest);
        Ivec(j,:) = [lambdatest IntensityV(1:2)];
        j=j+1;
        end
       iteration=k
    goodinc(k) = Ivec(find(min(Ivec(:,2))==Ivec(:,2)),1);
%    IndxStackTemp = IndxStack(find(min(Ivec(:,2))==Ivec(:,2)),:);
end
figure;hist(goodinc,20)
N=hist(goodinc,20);
Mn=mean(goodinc);
stdev=std(goodinc);
X=(max(goodinc) - min(goodinc))*(7/10) + min(goodinc);
Y=max(N)-(1/10)*max(N);
title([sprintf('%s \n Calculated Frequecy Distribution due to random Layer Thickness
Variation',RunName)])
xlabel('Resonant Frequency \lambda (Ang)');
ylabel('# Results per frequency bin');
text(X,Y,['Design \lambda: ' int2str(lambdaDesign) sprintf('\n')...
        'Max Error(+/-): ' sprintf('%.1f',maxError) '%' sprintf('\n')...
        'Mean: ' sprintf('%.2f \n',Mn)...
        'Standard Dev: ' sprintf('%.2f',stdev)])
save histdata.mat  goodinc
end

%************************************************************

% Calculate reflectance of Bottom DBR and Top DBR from Microcavity
BC1 = substrate(0,IndxStack(1),NSubstrate,y,typeSP);
BC2 = substrate(0,IndxStack(length(IndxStack)),NIncident,y,typeSP);
for i = 1:length(LabelStack)
        switch LabelStack{i}
        case 'BottomDBR'
           Mtemp = CharMatrix(IndxStack(i),ThickStack(i),0,lambdaDesign,typeSP,y);
           BC1 = Mtemp*BC1;
        %end
    end
end

RBottom = Reval(BC1,NSubstrate,y)

for i = length(LabelStack):-1:1
        switch LabelStack{i}
        case 'TopDBR'
            Mtemp = CharMatrix(IndxStack(i),ThickStack(i),0,lambdaDesign,typeSP,y);
            BC2 = Mtemp*BC2;
        case 'BufferDBR'
            Mtemp = CharMatrix(IndxStack(i),ThickStack(i),0,lambdaDesign,typeSP,y);
            BC2 = Mtemp*BC2;
        case 'AirGap'
            Mtemp = CharMatrix(IndxStack(i),ThickStack(i),0,lambdaDesign,typeSP,y);
            BC2 = Mtemp*BC2;
        %end
     end
 end

RTop = Reval(BC2,NIncident,y)

% Standing Wave through Stack at Resonance=Design Wavelength
StandWave(NSubstrate,IndxStack,ThickStack,NIncident,lambdaDesign,1);

%place text on Standing Wave Plot
AxValues=axis;
x1=(AxValues(2)-AxValues(1))*5/8;
y1=(AxValues(4)-AxValues(3))*3/4;
x2=(AxValues(2)-AxValues(1))*1/50;
y2=(AxValues(4)-AxValues(3))*1/2;
text(x1,y1,sprintf('NpDBR1=%1.1f\nR_TopDBR=%0.4f',NpDBR1,RTop))
text(x2,y2,sprintf('NpDBR2=%1.1f\nR_BottomDBR=%0.4f',NpDBR2,RBottom))
```

```
if getWavelengthSpectrum==TRUE

  %  ========= R & Rphase vs. wavelength at normal incidence
   VCSEL_Spectrum(lambdaDesign, lambdaStart, lambdaEnd, lambdaStep, MaterialStack, ...
       ThickStack, NIncident, NSubstrate, NpDBR1, NpDBR2, y, typeSP, RunName);

end


if getLambdaRange==TRUE
  tic

if ~exist('AirGapStart')  AirGapStart = 0; end
if ~exist('AirGapStop')  AirGapStop = 40000; end
if ~exist('AirGapStep')  AirGapStep = 50; end

if ~exist('SWaveStart') SWaveStart = 14600; end
if ~exist('SWaveStop')  SWaveStop = 19600; end
if ~exist('SWaveStep')  SWaveStep = 300; end

  skipcount = floor(SWaveStep/AirGapStep);

  i=1;
  count=1;
  for AirGaptest = AirGapStart:AirGapStep:AirGapStop


    %lambdaDelta = lambdaDesign * 0.05;
    lambdaDelta = 1;
    lambdaDeltaSpec = 1;
    lambdaBegin = lambdaDesign - 500;
    lambdaFinish = lambdaDesign + 500;

    j=1;
    for lambdatest = lambdaBegin:lambdaDelta:lambdaFinish

       TiO2 = (getIndxr(TiO2_data, lambdatest));
       SiO2 = (getIndxr(SiO2_data, lambdatest));
       Si3N4 = (getIndxr(Si3N4_data, lambdatest));
       GaAs = (getIndxr(GaAs_data, lambdatest));
       AlGaAs90 = (getIndxr(AlGaAs90_data, lambdatest));
       %AlGaAs92 = real(getIndxr(AlGaAs92_data, lambdatest));
       AlGaAs98 = real(getIndxr(AlGaAs98_data, lambdatest));
       AlAs = (getIndxr(AlAs_data, lambdatest));
       InGaAs = (getIndxr(InGaAs_data, lambdatest));

       Air = 1;
       NSubstrate = GaAs;
       NIncident = Air;

    % Determine Characteristic Matrix for entire stack
    for k = 1:length(MaterialStack)
        switch MaterialStack{k}
        case 'Air'
           IndxStackVar(j,k) = Air;
           ThickStack(k)= AirGaptest;
        case 'GaAs'
            IndxStackVar(j,k) = GaAs;
        case 'AlGaAs90'
            IndxStackVar(j,k) = AlGaAs90;
        case 'AlGaAs92'
            IndxStackVar(j,k) = AlGaAs92;
        case 'AlGaAs98'
           IndxStackVar(j,k) = AlGaAs98;
        case 'AlAs'
           IndxStackVar(j,k) = AlAs;
        case 'InGaAs'
            IndxStackVar(j,k) = InGaAs;
        case 'TiO2'
            IndxStackVar(j,k) = TiO2;
        case 'SiO2'
```

```
            IndxStackVar(j,k) = SiO2;
         case 'Si3N4'
            IndxStackVar(j,k) = Si3N4;
         otherwise
             disp('Invalid Material Type:')
             MaterialStack{k}
             return;
          end
       end

         % code originally used to find amount to subtract from Clad1Thick to obtain resonance
         [EoPlusV,EoMinusV,IntensityV] = ...
            EoEvaluateQuick(NSubstrate,IndxStackVar(j,:),ThickStack,NIncident,lambdatest);
            Ivec(j,:) = [lambdatest IntensityV(1:2)];
            j=j+1;
    end

    goodinc(i) = Ivec(find(min(Ivec(:,2))==Ivec(:,2)),1);
    IndxStackTemp = IndxStackVar(find(min(Ivec(:,2))==Ivec(:,2)),:);
    AirGap(i) = AirGaptest;


    % close all; %close all open figures
    % plot Reflectance Spectrum and Standwave for different Air Gaps and tuning frequencies
    if (AirGaptest >= SWaveStart)&(AirGaptest <= SWaveStop)&(count == skipcount)

       VCSEL_Spectrum(goodinc(i), lambdaBegin, lambdaFinish, lambdaDeltaSpec, ...
          MaterialStack, ThickStack, NIncident, NSubstrate, NpDBR1, NpDBR2, y, typeSP, RunName);
       ReflectHandle = gcf;

fname=strcat('VCSEL_reflectance_Lambda',int2str(goodinc(i)),'_AG',int2str(AirGaptest),'_',int2str(i)
);
       print(ReflectHandle, '-depsc2', '-tiff', '-r600 ', fname);
       if (suppressGraphics == TRUE) close(ReflectHandle); end


       StandWave(NSubstrate,IndxStackTemp,ThickStack,NIncident,goodinc(i),1);
       SWaveHandle = gcf;

fname=strcat('VCSEL_SWave_Lambda',int2str(goodinc(i)),'_AG',int2str(AirGaptest),'_',int2str(i));
       print(SWaveHandle, '-depsc2', '-tiff', '-r600 ', fname);
       if (suppressGraphics == TRUE) close(SWaveHandle); end

    end

    skipcount
    if count >= skipcount
       count = 1
    else
       count = count + 1
    end

    i=i+1
    save checkup.mat

  end

  % Print Airgap vs. Resonant Frequency
  fighandle=figure;plot(goodinc, AirGap/10000, '+');
  title([sprintf('Run Name: %s\n',RunName) 'VCSEL Tuning: Resonant Frequency vs. Air Gap']);
  xlabel('Resonant Frequency \lambda (Ang)');
  ylabel('Air Gap Thickness (\mum)');
  fname=strcat('VCSEL_AirGap_vs_Freq_',int2str(AirGapStart),'_',int2str(AirGapStop));
  print(fighandle, '-depsc2', '-tiff', '-r600 ', fname);
  save(fname);
  %return
  toc
end

return;
```

VCSEL_Stack.m MATLAB FUNCTION

```
function [IndxStack, ThickStack, MaterialStack, DBR1Thick, NpDBR1, DBRBThick, NpDBRB, DBR2Thick,
NpDBR2,Clad1Thick,Clad2Thick,LabelStack] = ...
         VCSEL_Stack(lambdaDesign,RminDBR1,RminDBR2,NLow,NHigh,NIncident,NSubstrate, OxideH, OxideL, ...
         CavityLength, NpQW, NpDBRB, Clad1IndxDesign,Clad2IndxDesign,LambdaThickQW, Delta, NLowMat, NHighMat, NAlAs, ...
         OxideHMat, OxideLMat, Clad1Material, Clad2Material, QWMaterial, QWThk, QWIndx, NLAir, AirGap, inc, typeSP, y)

% This function calculates the thickness, index of refraction, and overall structure of a
% MEM tunable VCSEL material stack.  It is called by the matlab function
% VCSEL_TopSim.m

% Author: Capt Michael Harvey
% Date: 6 Sep 01

Clad1Thick = Delta*lambdaDesign/(2*real(Clad1IndxDesign)) + inc; % THE TRICK TO GET RESONANCE @
lambdaDesign!
Clad2Thick = Delta*lambdaDesign/(2*real(Clad2IndxDesign));

Lambdatest = LambdaThickQW + 2*((Clad1Thick*real(Clad1IndxDesign)) +
(Clad2Thick*real(Clad2IndxDesign)))/lambdaDesign;

% uCavity: 2 layers cladding & NpQW QW Pairs in middle
uCIndxDesign = [Clad1IndxDesign Clad2IndxDesign QWIndx Clad2IndxDesign Clad1IndxDesign];
uCThick = [Clad1Thick Clad2Thick QWThk Clad2Thick Clad1Thick];
uCMaterial = [{Clad1Material} {Clad2Material} QWMaterial {Clad2Material} {Clad1Material}];
QWLabel = SinglePair({'QW_Low' 'QW_High'}, NpQW);
uCLabel = [{'MicroCavClad1'} {'MicroCavClad2'} QWLabel {'MicroCavClad2'} {'MicroCavClad1'}];

% Coupling Stack Buffer Layers

%NAlAs = filmIndxr('AlAs.dat', lambdaDesign);
IndxDBRB = [NHigh NLow NHigh NAlAs];
IndxDBRBreal = real(IndxDBRB);
ThickDBRB =  lambdaDesign./(4*IndxDBRBreal); %make sure these are correct
MaterialDBRB = {'GaAs' 'AlGaAs90' 'GaAs' 'AlGaAs98'};
LabelDBRB = {'BufferDBR' 'BufferDBR' 'BufferDBR' 'BufferDBR'};
DBRBIndxDesign = IndxDBRB(1:2);
DBRBThick = ThickDBRB(1:2);

% DBR1 Design (Top Oxide DBR): xtra-layer needed...
[NpDBR1,RDBR1,RNpDBR1,IndxDBR1,ThickDBR1]=DesignDBR(...
   Clad1IndxDesign, [OxideH OxideL], 1, NSubstrate, lambdaDesign, RminDBR1);
NpDBR1;
RDBR1;
DBR1IndxDesign = (IndxDBR1(1:2));% don't need to fliplr - symmetric looking up or down
DBR1Thick = (ThickDBR1(1:2));  % don't need to fliplr - symmetric looking up or down

MaterialDBR1 = SinglePair({OxideHMat OxideLMat}, NpDBR1);
for i=1:length(MaterialDBR1)
    LabelDBR1(i) = {'TopDBR'};
end

% DBR2 Design (Bottem Semiconductor DBR): no xtra layer needed if (high low)...
[NpDBR2,RDBR2,RNpDBR2,IndxDBR2,ThickDBR2]=DesignDBR(...
   NLAir, [NHigh NLow], 0, NIncident,lambdaDesign, RminDBR2);
NpDBR2;
RDBR2;
DBR2IndxDesign = IndxDBR2(1:2);
DBR2Thick = ThickDBR2(1:2);

MaterialDBR2=SinglePair({NHighMat NLowMat}, NpDBR2);
for i=1:length(MaterialDBR2)
    LabelDBR2(i) = {'BottomDBR'};
end

%Matrix for Air to use in Standing Wave Calculations
IndxAir = [NLAir];
ThickAir = [AirGap];
MaterialAir = {'Air'};
LabelAir = {'AirGap'};
```

```
%Additional AlAs layer on bottom side of DBR
IndxAlAs = [NAlAs];
IndxAlAsreal = real(IndxAlAs);
ThickAlAs =  lambdaDesign./(4*IndxAlAsreal); %make sure these are correct
MaterialAlAs = {'AlGaAs98'};
LabelAlAs = {'BottomDBR'};

% Since plotting with substrate on left, flip stack accordingly...
% StandWave prep: looking up from substrate to incident (air)
IndxStack = fliplr([IndxDBR1 IndxAir IndxDBRB uCIndxDesign IndxAlAs IndxDBR2]);
ThickStack = fliplr([ThickDBR1 ThickAir ThickDBRB uCThick ThickAlAs ThickDBR2]);
MaterialStack = fliplr([MaterialDBR1 MaterialAir MaterialDBRB uCMaterial MaterialAlAs
MaterialDBR2]);
LabelStack = fliplr([LabelDBR1 LabelAir LabelDBRB uCLabel LabelAlAs LabelDBR2]);
```

VCSEL_Spectrum.m MATLAB FUNCTION

```
function VCSEL_Spectrum(lambdaDesign, lambdaStart, lambdaEnd, lambdaStep, ...
              MaterialStack, ThickStack, NIncident, NSubstrate, NpDBR1, NpDBR2, y, typeSP, RunName)


% This function calculates the spectral power reflectance, transmission, absorption,
% and reflectivity phase for a given material stack.  It is called by the matlab function
% VCSEL_TopSim.m

% Author: Capt Michael Harvey
% Date: 6 Sep 01

 %  ========= R & Rphase vs. wavelength at normal incidence


% Load index of refraction data into memory
GaAs_data = load('GaAs.dat');
AlAs_data = load('AlAs.dat');
AlGaAs90_data = load('Al(0.90)Ga(0.10)As.dat');
AlGaAs98_data = load('Al(0.98)Ga(0.02)As.dat');
InGaAs_data = load('InGaAs.dat');
TiO2_data = load('TiO2.dat');
SiO2_data = load('SiO2.dat');
Si3N4_data = load('Si3N4.dat');

 n=1;
 for lambda=lambdaStart:lambdaStep:lambdaEnd

    lambda

    TiO2 = real(getIndxr(TiO2_data, lambda));
    SiO2 = real(getIndxr(SiO2_data, lambda));
    Si3N4 = real(getIndxr(Si3N4_data, lambda));
    GaAs = real(getIndxr(GaAs_data, lambda));
    AlGaAs90 = real(getIndxr(AlGaAs90_data, lambda));
    %AlGaAs92 = real(getIndxr(AlGaAs92_data, lambda));
    AlGaAs98 = real(getIndxr(AlGaAs98_data, lambda));
    AlAs = real(getIndxr(AlAs_data, lambda));
    InGaAs = real(getIndxr(InGaAs_data, lambda));

    Air = 1;

    for i = 1:length(MaterialStack)
        switch MaterialStack{i}
        case 'Air'
           IndxStackVar(i) = Air;
        case 'GaAs'
            IndxStackVar(i) = GaAs;
        case 'AlGaAs90'
            IndxStackVar(i) = AlGaAs90;
        case 'AlGaAs92'
            IndxStackVar(i) = AlGaAs92;
        case 'AlGaAs98'
           IndxStackVar(i) = AlGaAs98;
        case 'AlAs'
           IndxStackVar(i) = AlAs;
        case 'InGaAs'
            IndxStackVar(i) = InGaAs;
        case 'TiO2'
            IndxStackVar(i) = TiO2;
        case 'SiO2'
           IndxStackVar(i) = SiO2;
        case 'Si3N4'
           IndxStackVar(i) = Si3N4;
        otherwise
            disp('Invalid Material Type:')
            MaterialStack{i}
            return;
        end
        if i == 1
```

```
            BC = substrate(0,IndxStackVar(1),NSubstrate,y,typeSP);
        end
        Mtemp = CharMatrix(IndxStackVar(i),ThickStack(i),0,lambda,typeSP,y);
        BC = Mtemp*BC;
     end1

   % Power Reflectance, Reflectivity Phase
   [R(n),Rphase(n)] = Reval(BC,NIncident,y);
   [Absorptance(n),Transmittance(n)] = ATeval(BC,NIncident,y,NSubstrate,0,typeSP); % incident is
air...
   lambdav(n)=lambda;

   n=n+1;

 end

 % Plot Power Reflectance Figure
 plotR(lambdav,lambdaStart,lambdaEnd,R,Rphase)
 subplot(2,1,1)
 title([...
      sprintf('Run Name: %s ',RunName) ...
      'R(' int2str(lambdaDesign) ' Ang)=' ...
      sprintf('%.4f',R(find(lambdav==lambdaDesign))) ...
      ', Np_1=' sprintf('%.1f',NpDBR1) ...
      ', Np_2=' sprintf('%.1f',NpDBR2)])
 hold on
 plot(lambdav,Absorptance,'k:')
 plot(lambdav,Transmittance,'r--')
 legend('Power Reflectance', 'Absorptance', 'Transmittance')
 subplot(2,1,2)
 title([...
      'R Phase(' int2str(lambdaDesign) ' Ang)=' ...
      sprintf('%.5f \pi',Rphase(find(lambdav==lambdaDesign))/pi) ...
      ' (\phi/\pi)'])
```

getIndxr.m MATLAB FUNCTION

```
function [index] = getIndxr(fdata, lambdaDesign)
%
% function [index] = getIndxr(fdata,lambdaDesign)
%
% -Thin film data must have wavelength in nm as column 1, n values for column 2, and k
%  values for column 3
% -Wavelength must be entered in Angstroms, but raw data stores wavelength in nm, so
%  it must be converted.  Most film wizard data files are between 200nm and 1300nm
% -Any data file may be used so long as it has 3 tab seperated
%  columns [wavelength(nm), n, k].
%
%  Author:  Capt Michael Harvey
%  Date:    07 Dec 01


lambdaDesign=lambdaDesign/10;

    rindx = interp1(fdata(:,1),fdata(:,2),lambdaDesign);
    cindx = interp1(fdata(:,1),fdata(:,3),lambdaDesign);

index=rindx + i*cindx;
```

Vita

Captain Michael C. Harvey received his BSEE from Northern Arizona University and was commissioned a 2d Lt in the United States Air force in December 1994. From February 1995 to June 1996 he served as a Electronic Intelligence (ELINT) Technical Analyst in the ELINT branch of the 20th Intelligence Squadron, Offutt Air Force Base, Nebraska. From July 1996 to August 1998 he served as Senior ELINT Engineer at the 97th Intelligence Squadron, Offutt AFB, Nebraska. From August 1998 to August 2000, Capt Harvey served as Deputy Chief of Maintenance for the Misawa Cryptologic Operations Center, 301st Intelligence Squadron, Misawa AFB, Japan. Capt Harvey is currently assigned to the Air Force Institute of Technology (AFIT), Wright-Patterson AFB, Ohio, where he is pursuing an MS in Electrical Engineering, specializing in electro-optics and micro-electromechanical devices.

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14. ABSTRACT

Tunable micro-optical devices are expected to be vital for future military optical communication systems. In this research I seek to optimize the design of a microelectromechanical (MEM) structure integrated with a III-V semiconductor micro-optical device. The resonant frequency of an integrated optical device, consisting of a Fabry-Perot etalon or vertical cavity surface emitting laser (VCSEL), may be tuned by applying an actuation voltage to the MEM flexure, thereby altering the device's optical cavity length. From my analysis I demonstrate tunable devices compatible with conventional silicon 5V integrated circuit technology. My design for a Fabry-Perot etalon has a theoretical tuning range of 200 *nm*, and my VCSEL design has a tuning range of 44 *nm*, both achieved with actuation voltages as low as 4 V. Utilizing my theoretical device designs I planned a new microelectronics fabrication process to realize a set of prototype MEM-tunable devices with a peak central emission wavelength at 980 nm. I designed a mask set consisting of 8 mask levels and 252 distinct device designs, all within a die size of one square centimeter. My unique fabrication process utilizes a gold MEM flexure with a Si3N4/SiO2 dielectric distributed Bragg reflector (DBR) mirror, grown on an all-semiconductor VCSEL or Fabry-Perot substrate. I successfully fabricated a complete set of MEM-tunable test structures using the cleanroom laboratory facilities at the Air Force Institute of Technology (AFIT) and the Air Force Research Laboratory (AFRL). The initial devices display minimum electrostatic actuation voltages as low as 18 V, which is comparable to existing MEM tunable VCSEL designs. In order to enhance device performance, I developed improvements to my laboratory process for incorporation in future fabrication runs. These results form the fundamental basis for advanced development of manufacturable MEM-tunable optical emitting and detecting arrays.

15. SUBJECT TERMS

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