Chapter

Fault Tolerance in Carbon Nanotube Transistors Based Multi Valued Logic

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Abstract

This Chapter presents a solution for fault-tolerance in Multi-Valued Logic (MVL) circuits comprised of Carbon Nano-Tube Field Effect Transistors (CNTFET). This chapter reviews basic primitives of MVL and describes ternary implementations of CNTFET circuits. Finally, this chapter describes a method for error correction called Restorative Feedback (RFB). The RFB method is a variant of Triple-Modular Redundancy (TMR) that utilizes the fault masking capabilities of the Muller C element to provide added protection against noisy transient faults. Fault tolerant properties of Muller C element is discussed and error correction capability of RFB method is demonstrated in detail.

Keywords: CNTFET, Multi-Valued Logic, Fault Tolerance, TMR

1. Introduction

Moore's law along with the Dennard scaling has been the key driving factor that has enabled steady progress in the semiconductor industry over the last three decades. However, continuous scaling of Complementary Metal Oxide Semiconductor (CMOS) transistor into the sub-nanometer regime faces severe challenges due to short channel effects, exponentially rising leakage currents and increased variations in manufacturing process. To combat these challenges, numerous approaches have been explored. One of the promising approaches is to look for alternatives transistor structures that could potentially overcome these challenges. In this regard, Quantum-dot Cellular Automata (QCA), Carbon Nano-Tube Field Effect Transistor (CNTFET) and Single Electron Transistor (SET) are proposed to replace or supplement CMOS technology [1, 2].

From circuits and systems design perspective, several approaches are explored to reduce die area and lower energy consumption. One of the approaches is to use Multi-Valued Logic (MVL) design. MVL circuit design has been explored in CMOS technology for last few decades using circuit styles like voltage-mode CMOS logic (VMCL), I^2L logic and current-mode CMOS logic (CMCL) [3, 4]. Binary logic packs two logic values between available voltage levels, whereas MVL packs more than two logic values between the available voltage levels. Ternary logic is simplest form of MVL. Due to reduced noise margins, MVL logic design is less reliable and more prone to defects. Significant efforts have been directed towards defect and fault tolerance for binary logic and less effort has been directed towards defect and fault tolerant techniques for MVL.

In digital design, transistor is used as switch that transitions between logic states. The switch that controls this transition is the threshold voltage of the transistor. Threshold voltage is a manufacturing process parameter that is set to a unique value during manufacturing. To realize CMOS MVL circuits, multi-threshold transistors are deployed. In CMOS, multi-threshold transistors are realized by applying body bias voltages that exploit body effect to alter threshold voltages [5]. However, CNTFETs are fundamentally different that they allow realization of multi-threshold transistors by tuning a few process parameters. This property has been effectively exploited to realize various forms of ternary logic circuits using CNTFET [6, 7].

Despite several advantages, there are significant issues with the reliable realization of CNTFET circuits. There are fundamental limitations that are specific to Carbon Nanotubes (CNT) that pose major challenges [8]. CNTs are graphene sheets rolled into tubes [9]. Multiple CNTs are deployed in the channel region to provide the required drive currents needed for reliable operation [10]. These CNTs can be either metallic or semiconducting depending on the arrangement of the carbon atoms in the tube. Metallic tubes can result in circuit malfunctioning due to source-drain shorts [8]. It is also not possible to guarantee perfect positioning and alignment of these CNTs in large CNTFET circuits [8]. To harness the potential benefits of CNTFET technology, variation aware defect and fault tolerant techniques are needed for reliable operation of CNTFET MVL circuits.

In this chapter, we present MVL realization of CNTFET circuits and discuss techniques for defect and fault tolerance in MVL CNTFET circuits. The rest of this chapter is organized as follows: Section 2 discusses basic logic primitives that are needed for understanding MVL. Section 3 describes the CNTFET transistor and its operation. Section 4 provides a detail description of various circuit styles that have been proposed to realize MVL CNTFET circuits. Section 5 describes variation in CNTFET devices. Section 6 describes a technique for fault tolerance in MVL CNTFET circuits.

2. MVL basics

Raychowdhury et al. detail and discuss the logic primitives that are needed for understanding MVL [6]. Let us consider an r-valued n-variable function $f(X)$, where $X = x_1, x_2, x_3, \ldots x_n$ and each x_i can take up values from $R = 0, 1, 2, \ldots, r-1$.

The mapping of $f(X)$ is $f : R^n -> R$. There are r^{r^n} different functions that are possible in set f. Ternary logic gates that implement each of these functions would be called primitive gates. There are three main primitives that are useful for understanding MVL: complement, min and tsum. Complement operator is equivalent to a ternary inverter. Min operator is equivalent to a ternary and gate. The complement of the min operator is equivalent to ternary nand gate. Tsum operator is equivalent to a ternary or gate and the complement of tsum operator is a ternary nor gate. Complement of a logic value l is defined as:

$$\hat{l} = (r-1) - l. \tag{1}$$

Consider r = 3. The complement set is given by **Table 1** [9]. A min operator is defined as

$$\min(a_1, a_2, a_3, \ldots a_n) = a_1 \cdot a_2 \cdot a_3 \cdot \ldots a_n \tag{2}$$

Input l	Output $\hat{l}$
0	2
1	1
2	0

Table 1.
Truth table for complement operator [9].

Input a	Input b	Output c_{nand}	Output c_{nor}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

Table 2.
Ternary gates truth table [7].

Ternary nand operator can be defined as

$$c_{nand} = \overline{\min(a_1, a_2, a_3, \ldots a_n)} = \overline{a_1 \cdot a_2 \cdot a_3 \cdot \ldots a_n} \tag{3}$$

Here is an example of min operator: $min\,(1,2,3) = 1$. A tsum operator is defined as

$$\text{tsum}(a_1, a_2, a_3, \ldots a_n) = a_1 \oplus a_2 \oplus a_3 \ldots a_n \tag{4}$$

$$\text{tsum}(a_1, a_2, a_3, \ldots a_n) = \min(a_1 + a_2 + a_3 + \cdots + a_n, r-1) \tag{5}$$

Ternary nor operator can be defined as:

$$c_{nor} = \overline{\text{tsum}(a_1, a_2, a_3, \ldots a_n)} = \overline{\min(a_1 + a_2 + a_3 + \cdots + a_n, r-1)} \tag{6}$$

where belongs to the set R. Consider $r = 3$, $tsum(1,1,0) = min\,(1+1+0,2) = 2$. **Table 2** describes the truth table for ternary nand and ternary nor [7].

3. CNTFET transistor

Figure 1 shows the cross-section of a CNTFET transistor. Similar to MOSFETs, CNTFETs have four terminals: drain, gate, source and substrate [11]. CNTFET transistors are constructed by replacing the silicon channel in CMOS with carbon nanotubes (CNT). CNTs are sheets of Graphene rolled into tubes. Depending on the direction in which the sheets are rolled in the channel, CNTs can be either metallic or semi-conducting. This property of CNT being metallic or non-metallic depending on their rolled direction is termed as chirality [7]. In CMOS transistors, drive current depends on the channel width [5]. However, in the case of CNTFET the drive currents during conduction state depends on the number of CNTs in the

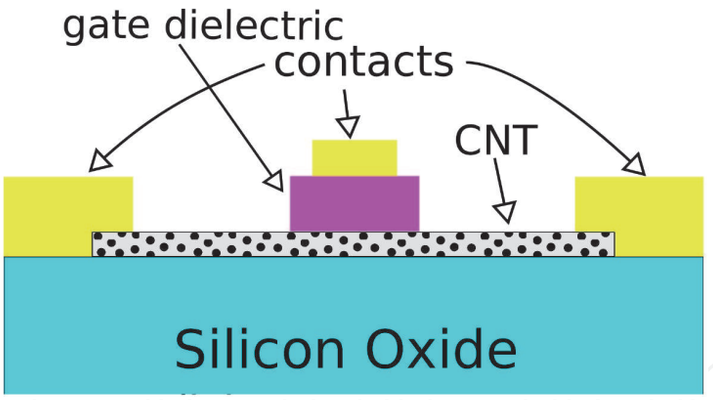

Figure 1.
Side view of a CNTFET transistor.

channel along with gate length, chirality and pitch distance [12]. The V_{th} of the intrinsic CNT channel is given by

$$V_{\text{th}} \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{\text{CNT}}} \tag{7}$$

where $a = 2.49 \times 10^{-10}$, m is the carbon to carbon atom distance, $V_{\pi} = 3.033\ \ ev$ is the carbon $\pi - \pi$ bond energy in the tight bonding model, e is the unit electron charge and D_{CNT} is the tube diameter [13]. D_{CNT} is calculated using the following Equation [13].

$$D_{\text{CNT}} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{8}$$

where a_0 = 0.142 nm is the inter-atomic distance between each carbon atom and its neighbor and (n,m) is called the chirality vector that describes the structure of a carbon nanotube, n is the number of non-metallic tubes and m is the number of metallic tubes present in the channel. The diameter D_{CNT} used in the Stanford CNTFET model is $1.487nm$ [10]. The model assumes that the CNT synthesis process yields zero metallic tubes. The value of n from equation (8) amounts to 19. This corresponds to a chirality vector of (19, 0) and threshold voltage of $0.293V$ based on equation (7). Combination of equations (7) and (8), provides the following insight: Threshold voltage of the CNTFET can be modified by changing the number of non-metallic tubes assuming that CNT synthesis process yields zero metallic tubes. The ratio of threshold voltages of two CNTFETs is inversely proportional to the number of non-metallic tubes present in the CNTFET.

$$\frac{V_{\text{th1}}}{V_{\text{th2}}} = \frac{D_{\text{CNT2}}}{D_{\text{CNT1}}} = \frac{n_2}{n_1}. \tag{9}$$

This property has been effectively exploited to design MVL circuits using CNTFET. In practice, multi-diameter CNTFET is realized by CNT synthesis techniques that can fabricate CNTs with desired chirality [14]. Also, post-processing techniques for adjusting the threshold voltage of multiple tube CNTFET have also been demonstrated [15].

4. Circuit realizations of ternary logic gates

This section discusses two circuit implementations of CNTFET ternary inverters along with a circuit implementation of a CNTFET ternary Muller C element. First

circuit is a resistor based ternary inverter that was proposed by Raychowdhury et al. [9]. Second circuit is a ternary inverter using static complementary circuit style that was proposed by Lin et al. [7]. We will also discuss the circuit implementation and operation of a ternary Muller C element proposed by Sundararajan et al. [16].

4.1 Resistive load ternary inverter

Figure 2 shows the circuit diagram of a resistive load ternary inverter. The circuit consists of two N-channel transistors and two resistors. CNTFET with two different diameters are deployed in this circuit. Transistor T_{LN1} is a low threshold CNTFET and has a diameter of $(19, 0)$ and transistor T_{HN2} is high threshold CNTFET and has a diameter of $(10, 0)$. T_{LN1} and T_{HN2} have threshold voltages of $0.29\ V$ and $0.59\ V$ respectively. The resistors used in this circuit are both $100\ K\Omega$. The circuit is operated at voltage of $V_{DD} = 0.9V$. **Table 3** details the chirality vector, diameter and the threshold voltage of all transistors in **Figure 2**. If the input signal a is below $300\ mV$, none of the transistors are on and the value at output $\hat{a}$ is

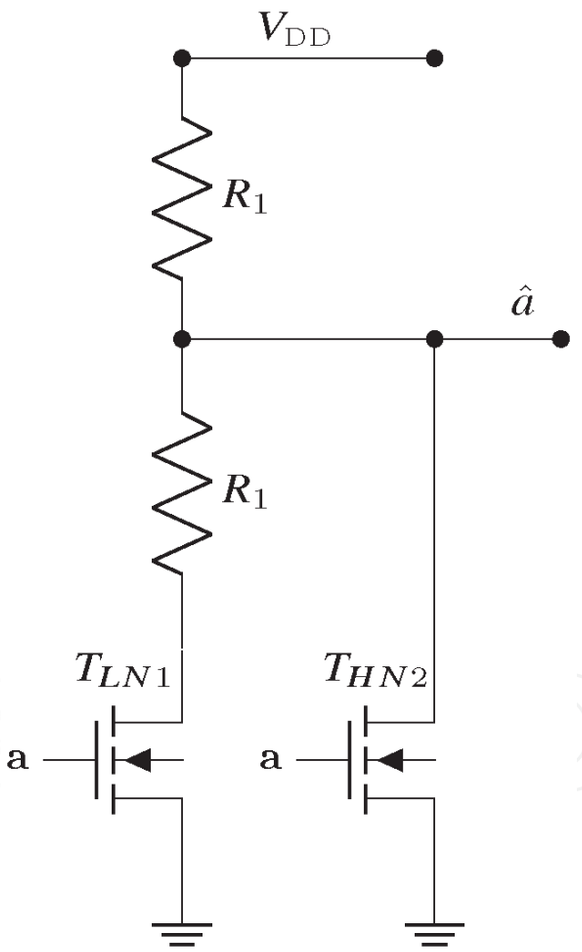

Figure 2.
Resistive CNTFET ternary inverter [6]. Value of R_1 is 100 KΩ.

Transistor	Chirality Vector (n,m)	Diameter(nm)	V_{th}(V)
T_{LN1}	(19,0)	1.487	0.29
T_{HN2}	(10,0)	0.783	0.56

Table 3.
CNTFET chirality, V_{th} and threshold voltages for resistive ternary inverter [7].

0.9 V. If a is operated between 300 mV and 600 mV transistor T_{LN1} turns on, T_{HN2} is off and the circuit operates as a voltage divider and $\hat{a}$ is exactly at half of V_{DD} which is 0.45 V. When a is operated above 600 mV, then the pull down network consisting of both the N channel CNTFETs is on and voltage at $\hat{a}$ is 0 V.

4.2 Static complementary ternary inverter

The problem with the resistive load ternary inverter is that resistors are large, bulky and are prone to noise. Also, static resistors draw leakage currents from the supply and are not suitable for implementation in large scale CNTFET circuits. As an alternative to resistive load ternary inverter, Lin et al. proposed a static complementary version of ternary inverter that employs P-channel and N-channel CNTFETs as shown in **Figure 3**. The resistor in pull up network of the circuit in **Figure 2** is replaced with the two P-Channel CNTFET with varying diameters and the voltage divider resistor is replaced with two diode connected complementary CNTFET. The diode connected transistors have a nominal threshold voltage (V_{th})

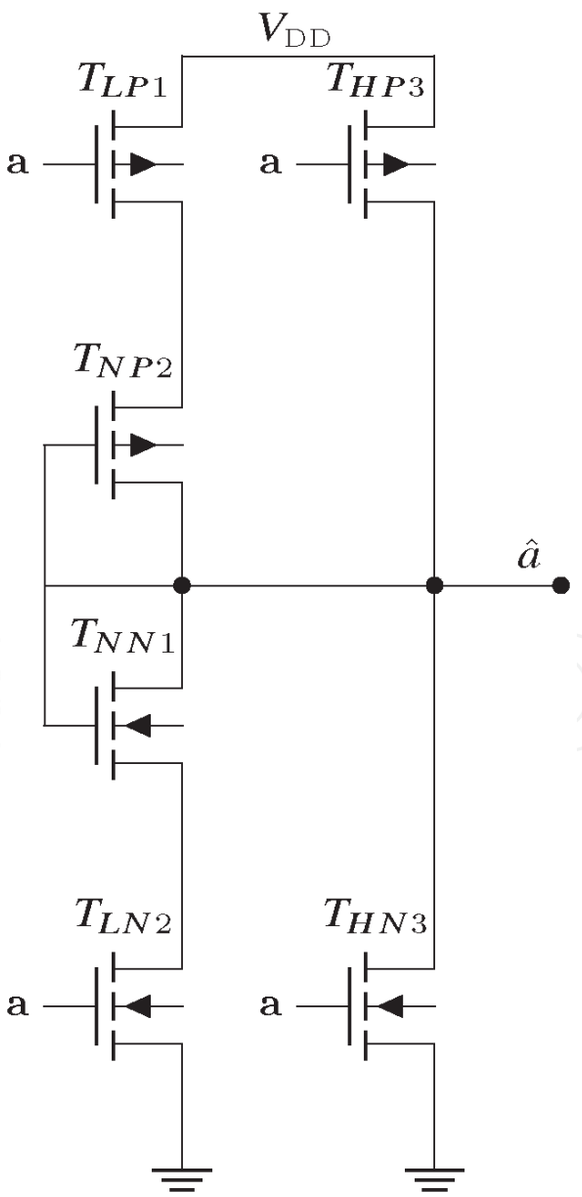

Figure 3.
Static complementary CNTFET ternary inverter [7].

Transistor	Chirality Vector (n,m)	Diameter(nm)	V_{th}(V)
T_{NN1}, T_{NP2}	(13,0)	1.018	0.43
T_{LN2}, T_{LP1}	(19,0)	1.487	0.29
T_{HN3}, T_{HP3}	(10,0)	0.783	0.56

Table 4.
CNTFET chirality, V_{th} and threshold voltages for static ternary inverter [7].

of 0.43 V. **Table 4** describes the chirality values, diameter and threshold voltages of all the transistors in **Figure 3**. If the input signal a is operated below 300 mV, T_{LP1} and T_{HP3} are on and transistors T_{LN2} and T_{HN3} are off. The voltage at $\hat{a}$ is 0.9 V. When input signal a is operated between 300 mV and 600 mV, T_{HP3} is off and diode connected transistors (T_{NP2} and T_{NN1}) are turned on along with T_{LP1} and T_{LN2}. This circuit configuration operates as a voltage divider and produces a voltage drop of 0.45 V at $\hat{a}$. When input signal a is operated above 600 mV, pullup network consisting of all the P-channel transistors is off and all the N-channel transistors are on pulling down voltage at $\hat{a}$ to 0 V.

4.3 Ternary Muller C element

In this section, we will review the circuit implementation of ternary Muller C element described by Sundararajan et al. [16]. Muller C element is a common logic gate that is deployed in asynchronous logic [17, 18]. **Figure 4** shows a circuit schematic and a logic representation of the Muller C element [19]. The basic operation of the C element can be described as follows: When the logic values of inputs a and b are the same, the output c is transparent and input value is latched. Otherwise, output c will retain its previous value. The logic equation describing the behavior of the Muller C element is described as follows [20].

$$c = \hat{c} \cdot (a + b) + a \cdot b \tag{10}$$

where a, b are the two inputs and $\hat{c}$ denotes the previous state of the output c. C element consists of two parts: C-not and S-gates [21]. The C-not part consists of two pmos and two nmos transistors connected in series. The S-gates consists of two cross coupled inverters employing weak feedback and is a widely used implementation proposed by Martin et al. [18]. The ternary Muller C element is similar to its binary counterpart except that the inputs and the output could take three logic values. **Table 5** shows the truth table of ternary Muller C element. **Figure 5** shows the circuit schematic of ternary Muller C element. The C-not portion of the Muller C consists of five P-CNTFETs and five N-CNTFETs. In this design, three kinds of CNTFET transistors having three different chirality vectors are used to realize three different threshold voltages. The chirality vectors used, their corresponding diameters and the resulting threshold voltages are the same as static complementary ternary inverter. The values are listed in **Table 4**. "S" gates consist of the ternary inverters connected in a feedback. To enable correct operation, feedback inverter is a weak inverter with less number of tubes. To realize weak feedback, the number of tubes in all CNTFET transistors in the C-not part and in the strong inverter $I1$ is 12. The number of tubes in weak inverter $I2$ is 3. The inverters are based on a static complementary style discussed in Section 4.2. The operation of the circuit is as follows: When the inputs a and b are below 300 mV P-CNTFET transistors T_{LP1}, T_{LP2}, T_{HP4} and T_{HP5} are on as shown in **Figure 5**. The node C_{out} is pulled to logic 2

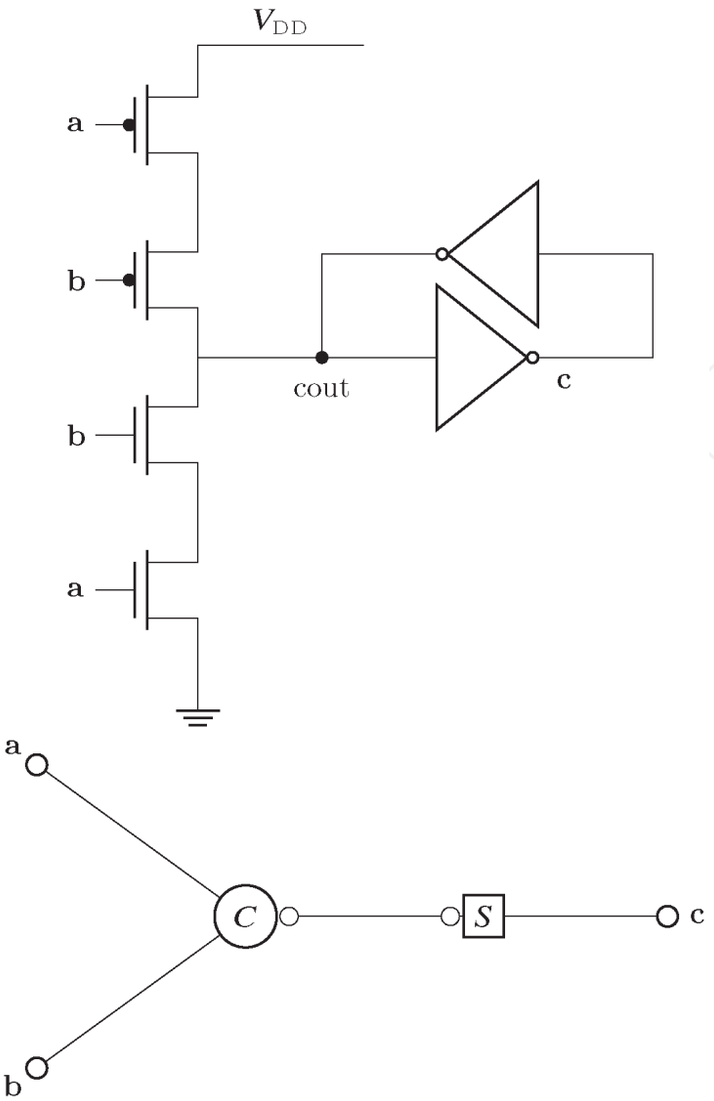

Figure 4.
Binary CMOS Muller C element: Circuit schematic and its logic representation. It has two inputs a, b and an output c. the C element consists of "C-not" and "S" gates [16].

Input a	Input b	Output c
0	0	0
0	1	*S*
0	2	*S*
1	0	*S*
1	1	1
1	2	*S*
2	0	*S*
2	1	*S*
2	2	2

Table 5.
Ternary Muller C-element truth table. S indicates previous state.

and node *c* is pulled to a low value (logic 0). When the input voltages are raised above 300 mV, transistors T_{HP4}, T_{HP5}, T_{HN4} and T_{HN5} are off as shown in **Figure 6**. Combination of transistors T_{LP1}, T_{LP2}, T_{LN2}, T_{LN3} along with the diode connected

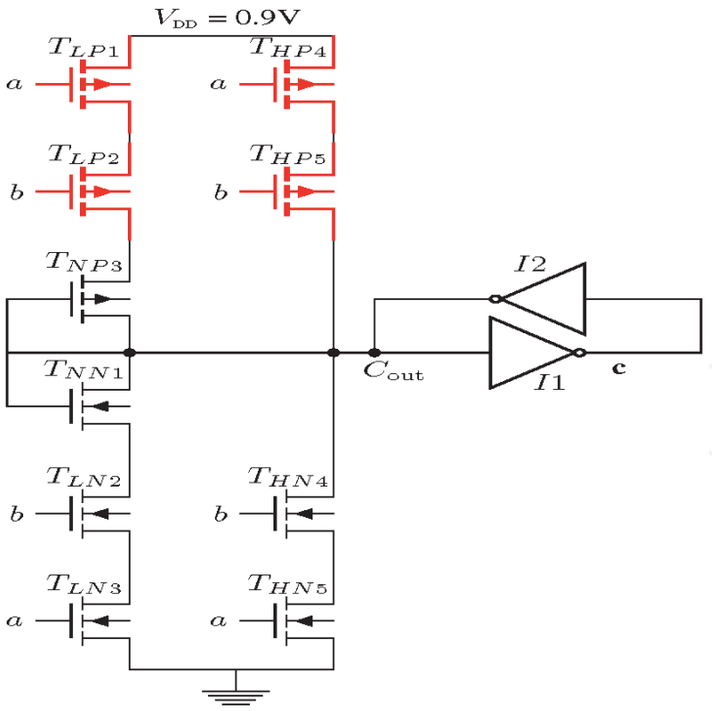

Figure 5.
Schematic for all inputs at logic 0.

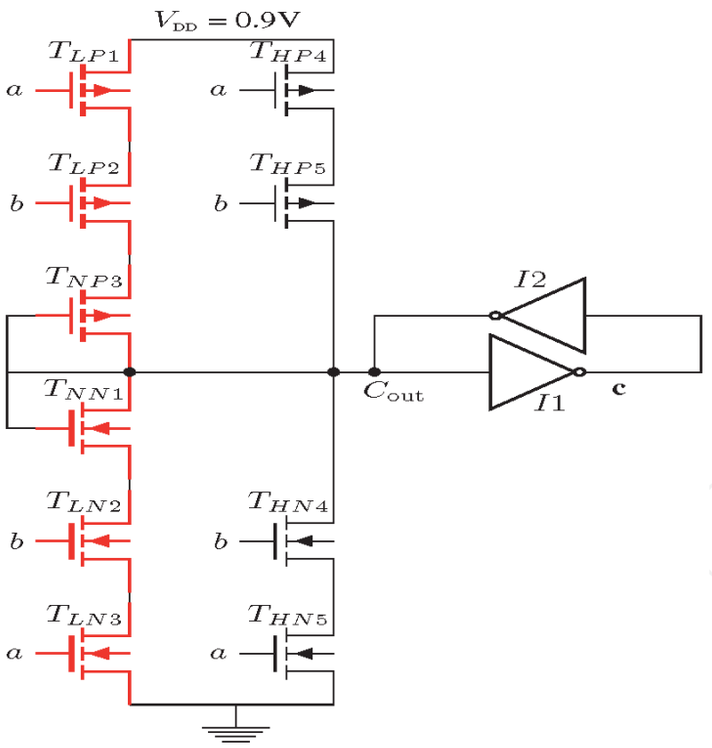

Figure 6.
Schematic for all inputs at logic 1.

transistors T_{NP3} and T_{NN1}, produces a voltage drop of 0.45 V (logic 1) at node C_{out}. This intermediate logic value is fed to the inverter latch, producing a voltage drop of 0.45 V or logic 1 at the output *c*. As the input voltages are raised above 600 mV, transistors T_{HP5} and T_{HP4} are off and transistors T_{HN4} and T_{HN5} are on as shown in **Figure 7** which pull the node C_{out} to a logic low value and drive node *c* to a high value (logic 2). The ternary C element was built and evaluated using Synopsys HSPICE circuit simulator. The design was simulated using CNTFET parameter

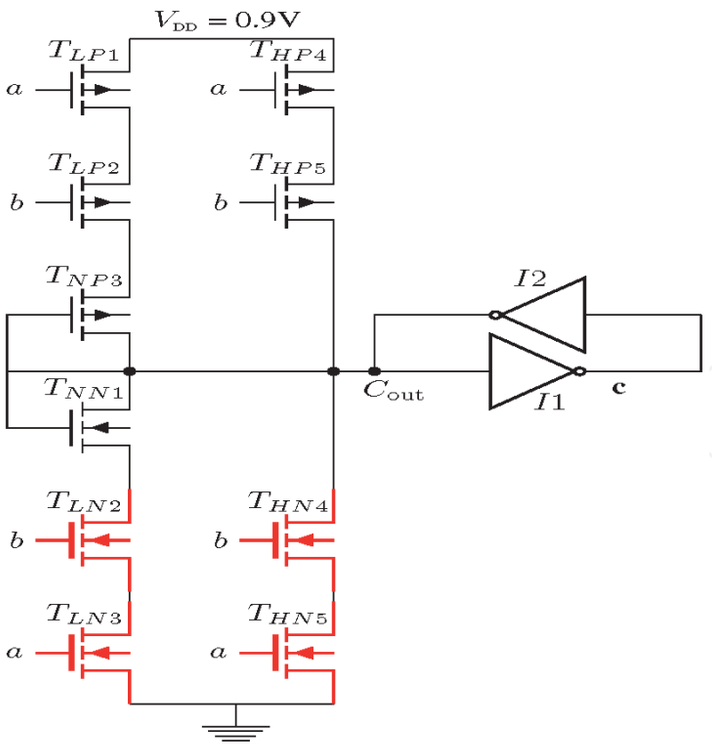

Figure 7.
Schematic for all inputs at logic 2.

models provided by Stanford Nano-electronics Group in the 32 *nm* technology node [22]. The operating supply voltage was 0.9 *V* and the temperature was 27°C. **Figure 8** shows the transient simulation result [16]. In this simulation, input *a* is held at a steady state and input *b* is swept from logic low to a high value. The output changes state when the two inputs are at the same level of logic. When inputs *a* and *b* are at a different logic level, the output holds the previously latched logic value. The inputs are swept from logic low to logic high and then changed to logic low in constant steps and output is observed for a full low to high and a high to low transition. The propagation delay is the average of four terms: the delay from logic 0

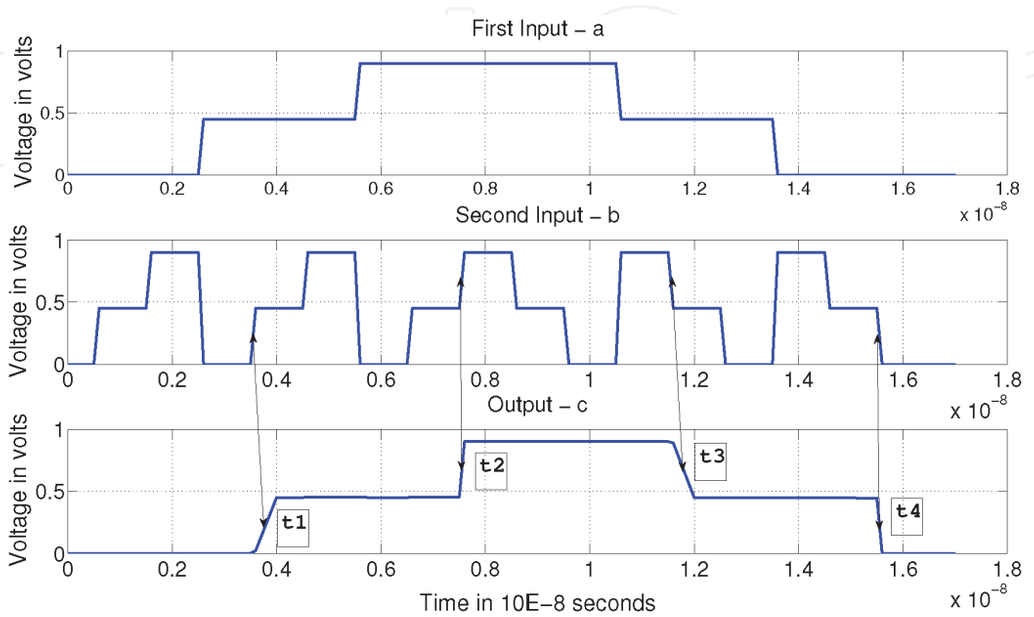

Figure 8.
Transient results of static complementary Muller C [16].

to logic 1 ($t1$), the delay from logic 1 to logic 2 ($t2$), the delay from logic 2 to logic 1 ($t3$), and the delay from logic 1 to logic 0 ($t4$).

5. Variations in CNTFET devices

This section describes the process variation in CNTFET technology. Process variation (PV), an artifact of aggressive technology scaling, causes uncertainty in integrated circuit characteristics. Imperfect lithography, doping fluctuations and imperfect planarization are some of the causes of variation that strongly affect the channel length, oxide thickness, width and eventually the threshold voltage of CMOS transistors. Such variation leads to unpredictable circuit behavior. Due to the random nature of manufacturing process, various effects such as ion implantation, diffusion and thermal annealing have induced significant fluctuations of the electrical characteristics in nanoscale CMOS [23]. CNTFETs are also affected by manufacturing variation caused by imperfect fabrication. CNTFETs not only suffer from traditional process variations, which are in common with the CMOS technologies but they also have their unique source of variations. Paul et al. showed that the CNTFET devices are significantly less sensitive to stochastic variations such as process-induced variations due to their inherent device structures and geometric properties [24]. In addition, CNTFETs are subject to CNT specific variation sources including: CNT type variations, CNT density variations, CNT diameter variations, CNT alignment variations and CNT doping variations [25]. **Figure 9** shows the contributions of each of the aforementioned sources of variations to the on-state current I_{on} in 32 nm technology. To provide sufficient drive current comparable to CMOS, multiple CNTs are deployed in the channel of a single CNTFET. Due to statistical averaging, the impact of the CNT diameter, doping and alignment variations on the on current is significantly reduced for CNTFET with multiple CNTs in the channel [26]. Hence, significant on state current variations are caused by metallic CNT induced count variations and CNT density variations. To overcome the effects of count variations due to metallic CNTs a technique called VLSI-compatible Metallic CNT Removal (VMR) has

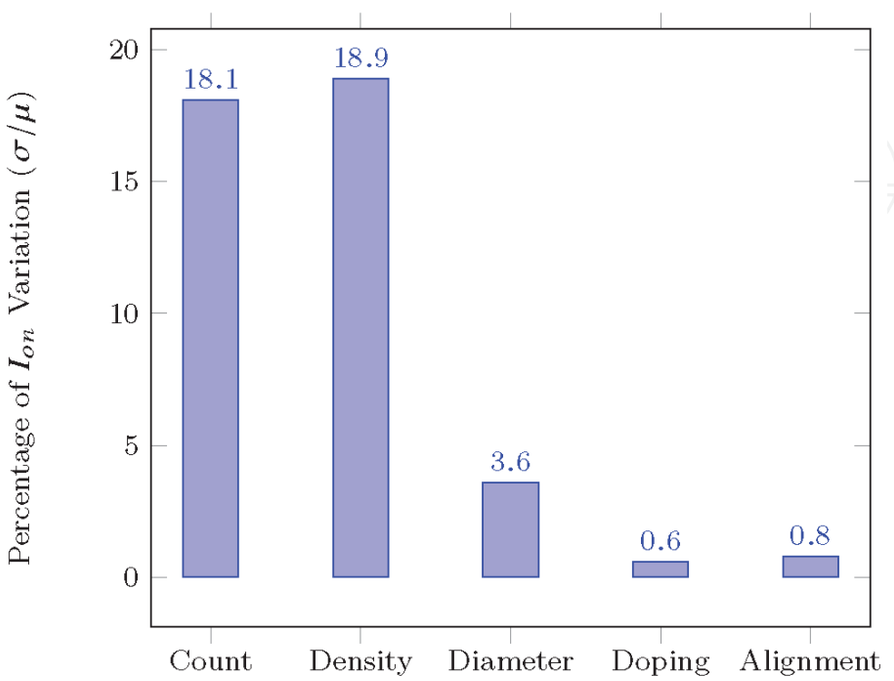

Figure 9.
Contributions of various CNT specific variation sources [25].

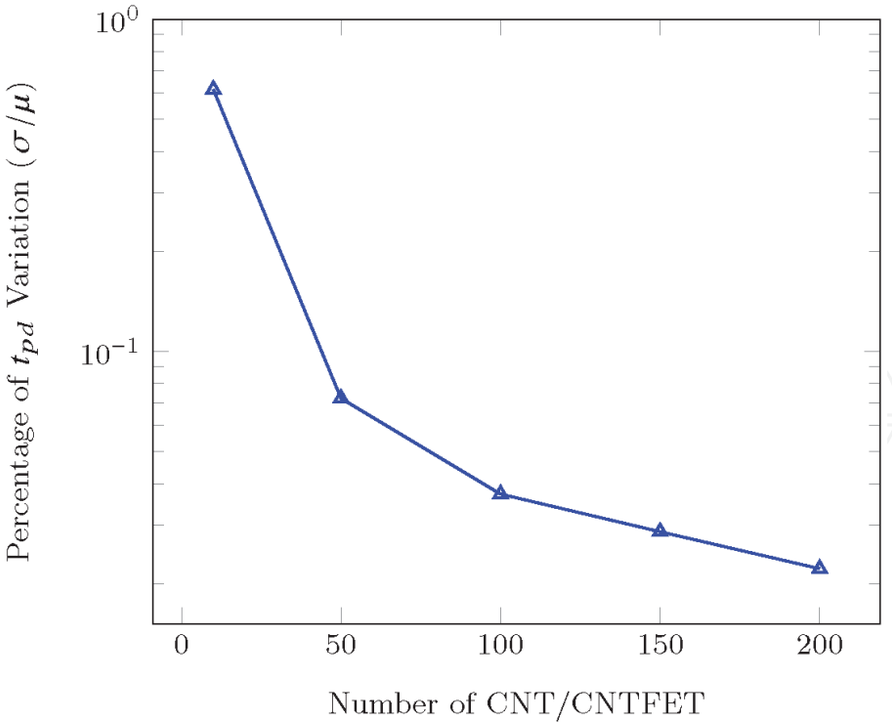

Figure 10.
Percentage of t_{pd} variation for the ternary Muller C element.

been proposed that combines new CNTFET circuit design techniques with the processing [27]. Asymmetrically-Correlated CNTs (ACCNT) is another imperfection immune design technique to tolerate the metallic CNTs [28]. Therefore, CNT density variation is the dominant source of variation in CNTFETs.

5.1 Analysis of process variations

As discussed in Section 5, CNT density is the critical parameter that needs to be accounted for variation aware design. CNT density variation manifests itself as varying amounts of CNT under the gate of every CNTFET transistor. CNT density variation follows a normal distribution with mean $\mu = N$ and the variance $\sigma = \sqrt{(N/2)}$ where N is the expected number of CNTs under the gate of each CNTFET [29]. To assess the impact of CNT density variation on the transient delay, 1000 sample Monte Carlo simulations were performed on the proposed ternary C element. **Figure 10** shows the percentage variation of transient delay with the variation in the number of CNTs per CNTFET.

The C element was driving a capacitance of $25\,fF$. From the plot, we see that when number of CNT in CNTFET is lower, the delay variation is higher and as we increase the number of CNT in the CNTFET, the delay variation goes down. The variation percentage is 0.6 when the number of tubes in a single CNTFET is 10 and it drops $30X$ lower to 0.02 when number of tubes in a single CNTFET is increased to 200.

6. Defect and fault tolerance in CNTFET MVL logic

This section will review a method for fault tolerance in CNTFET Multi-valued logic that was proposed by Sundararajan et al. [16]. The method called Restorative FeedBack (RFB), provides fault resilience against Single Event Upset (SEU) [19]. Triple Modular Redundancy (TMR) is one of the mostly commonly used method

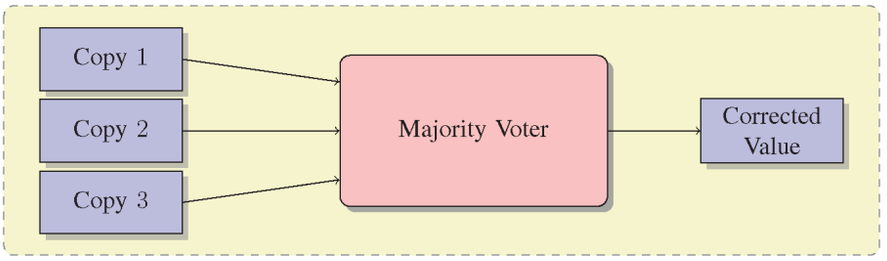

Figure 11.
Triple modular redundancy (TMR).

for fault tolerance in computer systems [30]. In TMR, a logic circuit is replicated three times and a majority vote is taken on the combined outputs. **Figure 11** shows the TMR method, where three copies of a logic circuit are made and a majority vote is taken on those combined copies to obtain a fault free logic value. TMR provides resilience against single error faults. The main drawback of TMR is that logic overhead is high due to replication and and a fault in majority voter can render the technique inefficient. Also, simultaneous error in two copies of the logic value can result in propagation of the error value in the downstream logic. From a MVL perspective, TMR cannot be applied to MVL as it is ambiguous for MVL. As an alternative to TMR, Winstead et al. proposed RFB method, which is an improved version of TMR [19]. RFB method can correct single error faults and CMOS implementations were shown for both binary and ternary logic [19]. RFB method replaces the majority gate in TMR with Muller C elements. The idea of RFB method is based on the inherent fault correcting capabilities of the Muller C element. RFB method is based on two key ideas related to the Muller C element:

- If the C element output is connected back to one of C element's input, then noise in other C element's input will be suppressed every time the C element evaluates.

- Muller C element has inherent fault correcting properties. C element only changes its output state when all inputs have the same logic value. This property can be exploited for fault masking.

Figure 12 shows an example of how a noisy input signal will be rendered less noisy, each time the signal passes through the C element. Suppose ε_a is the error probability associated with input signal a. Then the corresponding Log Likelihood Ratio (LLR), l_a, is defined as [21].

$$l_a = \ln(1-\varepsilon_a)/\varepsilon_a. \tag{11}$$

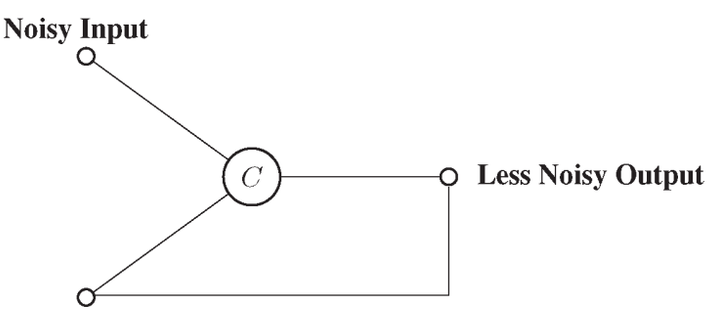

Figure 12.
Muller C element with feedback.

The magnitude of l_a is the confidence that signal a is correct. If, at any given time t, the error events appearing at the C-element's inputs are independent from each other, and also independent from the C-element's internal state, then the output LLR is

$$l_c = l_a + l_b \tag{12}$$

From Eq. (12), we notice that as $l_b \rightarrow l_c$, $l_a \rightarrow 0$. If the C element's output is connected back to the C-element's input then other input that is noisy is rendered less noisy every time the C-element evaluates the output [19]. **Figure 13** shows the schematic implementation of the RFB method where the C -element's output is connected in a feedback fashion to the adjacent C element's input. The other input to the C element is the logic that is replicated thrice (x_1, x_2 and x_3). To fully realize the fault correcting capabilities of the C element, the RFB circuit is operated in two phases: setup phase and restoration phase. There are three inputs signals x_1, x_2 and x_3. Lets asume that the signal x_3 is corrupted and has an incorrect logic value of 1 while x_1 and x_2 are at logic 2. The RFB operation involves two phases and phase switching is accomplished by using a 2-input multiplexer. The select signal ϕ is at logic 0 during the setup phase. The operation in the setup phase is shown in **Figure 14**. During this phase, inputs are barrel shifted to the adjacent C element's output. The error value in x_3 is shifted to y_2. **Figure 15** shows the operation in restoration phase. During this phase, ϕ is at logic 1. The feedback is deactivated and C-not gate's output is transferred to the actual output. The first C element has its inputs held at logic 2 and that causes y_2 to change its state from logic 1 to logic 2. The transient simulation results are shown in **Figure 16** for all possible combinations of error values [16]. The signal of interest is y_2. The setup and the restoration phases corresponding to y_2 are clearly marked and annotated in **Figure 16**. From the plot, we observe that in the setup phase, the error value in x_3 is transferred to signal y_2 and is then corrected in restoration phase, thereby showing the effectiveness of the RFB technique.

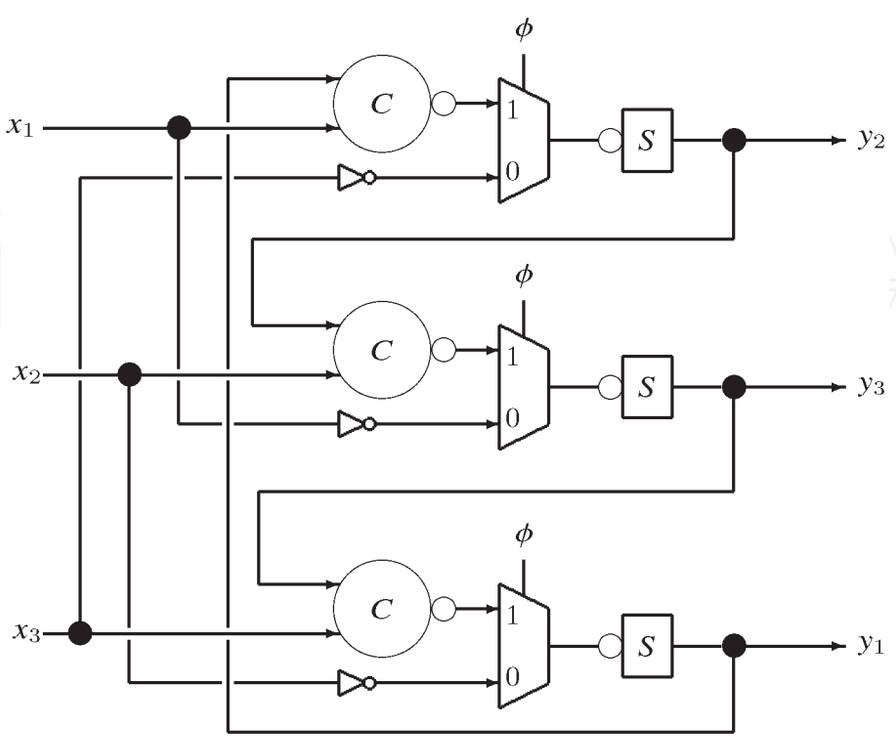

Figure 13.
The RFB circuit based on Muller C-element gates. The S gate is a storage element [21].

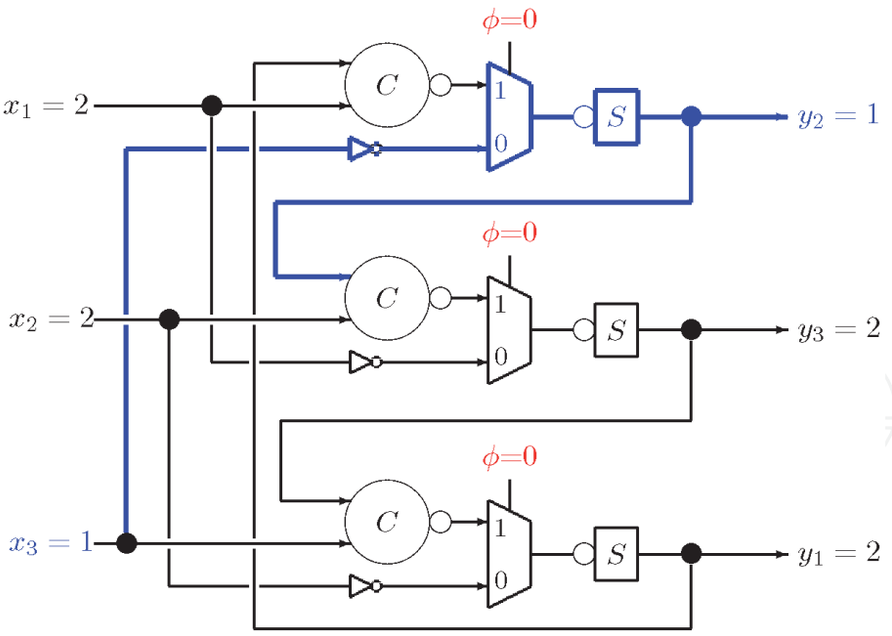

Figure 14.
RFB setup phase.

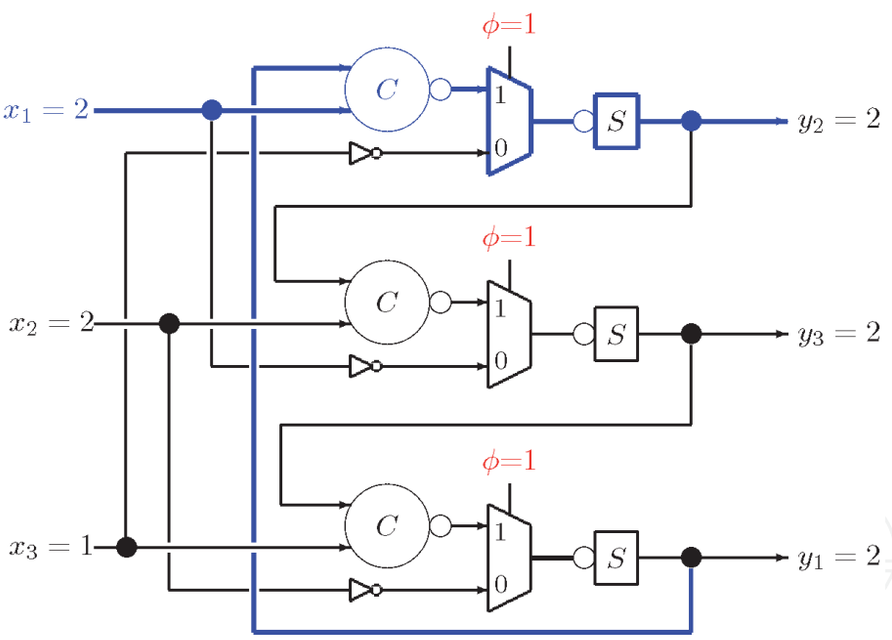

Figure 15.
RFB restoration phase.

7. Conclusion

This chapter discussed a technique for fault tolerance in MVL CNTFET logic. The described technique leverages the error suppression capability of Muller C element to correct single bit error in CNFTET MVL. To realize the technique, a ternary Muller C element is needed. This chapter also discussed the basics of MVL, provided an overview of CNTFET and also discussed the process variation in CNTFET.

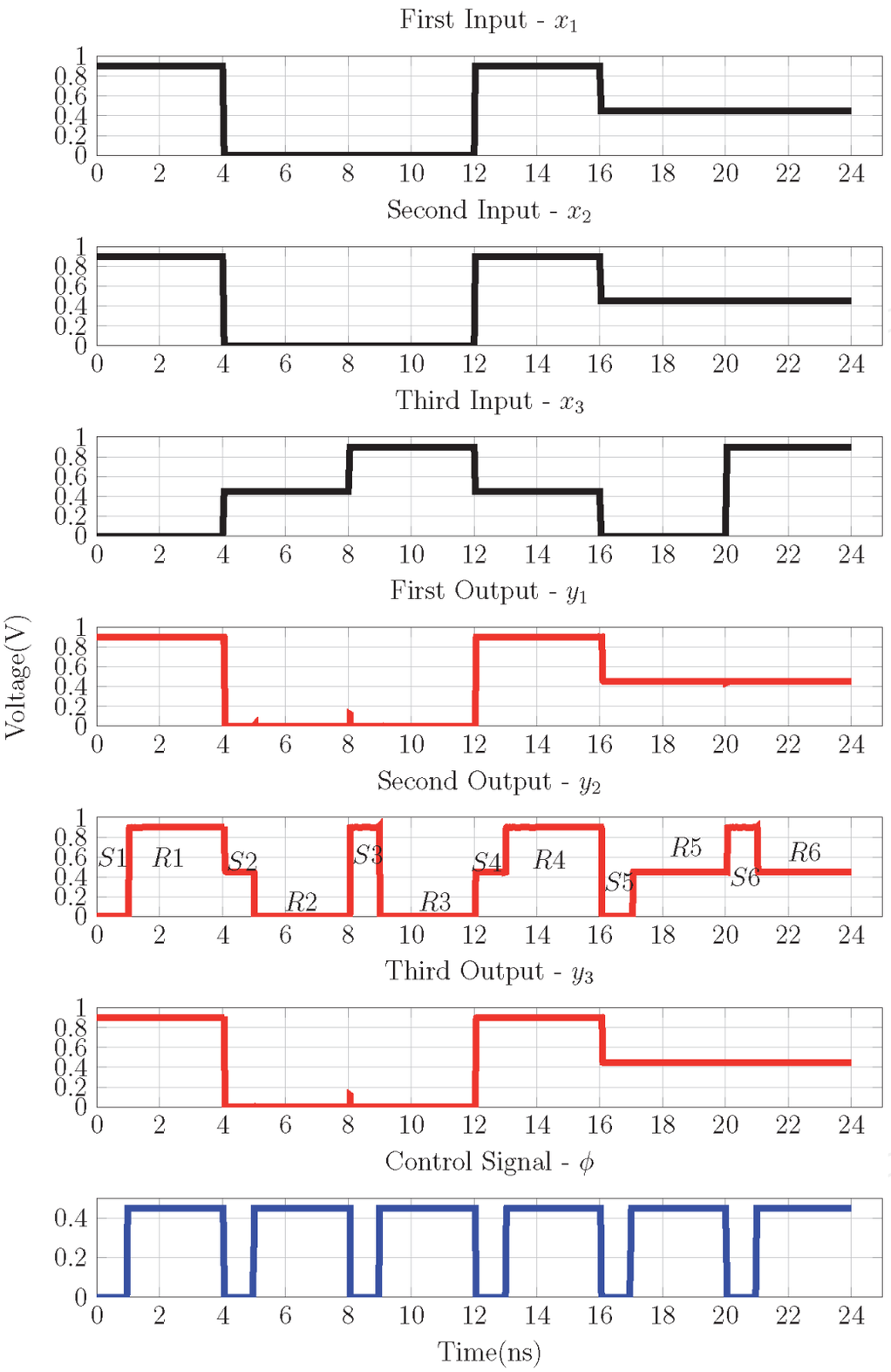

Figure 16.
Transient results of ternary CNTFET RFB method. The input sequence includes the six possible single error patterns. Signals x_1 and x_2 are correct, while x_3 is an error. The error is transferred to y_2 in the set-up phase and is corrected in the restoration phase [16].

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