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SHIPBOARD VOLTAGE SOURCE INVERTER CONTROL SYSTEM TO MEET MIL-STD-1399-300 LIMITS FOR PULSED POWER LOADS

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NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

SHIPBOARD VOLTAGE SOURCE INVERTER CONTROL SYSTEM TO MEET MIL-STD-1399-300 LIMITS FOR PULSED POWER LOADS

by

Daniel P. DeToma

December 2020

Thesis Advisor: Giovanna Oriti
Co-Advisors: Di Zhang
Alexander Julian, Consultant

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13. ABSTRACT (maximum 200 words)

Microgrids are increasingly being adopted throughout the Department of Defense due to their ability to increase energy security. Though each microgrid is unique, one commonality is that each contains loads that could strain the distributed generators on the grid during starting transients. This is especially important in shipboard applications or Marine Corps forward operating bases, where generator droop characteristics could result in unfavorable effects on running machinery during a transient from a newly started load. This thesis research explores a novel controller design for a three-phase voltage source inverter (VSI) that limits the transients on a microgrid while simultaneously correcting the grid power factor to unity. Specifically, transients produced by pulsed power loads as specified in MIL-STD-1399 section 300 are addressed and controlled. The novel controller allows the VSI to use distributed energy resources, such as batteries, renewables, or supercapacitors, to power the initial transient created by large loads. Using stored energy allows the generator to respond to step load changes more slowly while simultaneously reducing the size of the machine required due to reactive power control.

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SHIPBOARD VOLTAGE SOURCE INVERTER CONTROL SYSTEM TO MEET MIL-STD-1399-300 LIMITS FOR PULSED POWER LOADS

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 2020

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Microgrids are increasingly being adopted throughout the Department of Defense due to their ability to increase energy security. Though each microgrid is unique, one commonality is that each contains loads that could strain the distributed generators on the grid during starting transients. This is especially important in shipboard applications or Marine Corps forward operating bases, where generator droop characteristics could result in unfavorable effects on running machinery during a transient from a newly started load. This thesis research explores a novel controller design for a three-phase voltage source inverter (VSI) that limits the transients on a microgrid while simultaneously correcting the grid power factor to unity. Specifically, transients produced by pulsed power loads as specified in MIL-STD-1399 section 300 are addressed and controlled. The novel controller allows the VSI to use distributed energy resources, such as batteries, renewables, or supercapacitors, to power the initial transient created by large loads. Using stored energy allows the generator to respond to step load changes more slowly while simultaneously reducing the size of the machine required due to reactive power control.

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	alternating current
αβ0	alpha-beta-zero (stationary reference frame)
DER	distributed energy resources
DOD	Department of Defense
DOE	Department of Energy
DON	Department of the Navy
FOB	forward operating base
FPGA	field-programmable gate array
FY	fiscal year
HIL	hardware-in-the-loop
I/O	inputs/outputs
LL	line-to-line
LPF	low pass filter
OGM	orthogonal generation methods
PCC	point of common coupling
PG&E	Pacific Gas and Electric
PH	phase
PLL	phase-locked-loop
P-Q	real power-reactive power
PF	power factor
PWM	pulse width modulation
ϕ-N	phase-to-neutral
$qd0^e$	quadrature-direct-zero reference frame, electric (synchronous)
$qd0^s$	quadrature-direct-zero stationary reference frame
RCP	rapid control prototyping
RMS	root mean squared
SS	steady state
SVM	space vector modulation
THD	total harmonic distortion
VSI	voltage source inverter

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I. INTRODUCTION

A. RESEARCH MOTIVATION

The Department of Defense (DOD) has prioritized energy security and energy resilience into its energy policy, where energy resilience is summarized as ensuring energy availability and reliability to guarantee mission readiness by avoiding, preparing for, adapting to, and overcoming anticipated and unanticipated energy disruptions [1]. To meet this end, deploying microgrids across the DOD has become an attractive option. For the Department of the Navy (DON) specifically, despite a utility outage, a microgrid can ensure that moored ships maintain power or an airfield maintains its radars operational. Figure 1 shows that 78% of power outages are unplanned, and thus installations could benefit from alternative power sources provided by a microgrid.

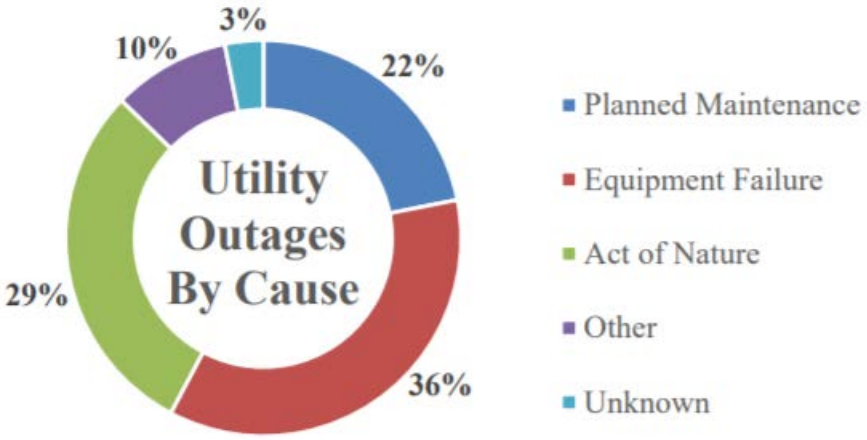

Figure 1. FY18 DOD Utility Outages by Cause. Source: [1].

In addition to a microgrid built to connect to a traditional utility grid, many microgrids, including forward operating bases (FOB) and naval vessels, are purpose-built to be islanded from a utility grid. Naval ships often use gas turbines or steam-powered generators to supply all ship power at the MW scale. Forward operating bases employ a

combination of diesel generators and distributed energy resources (DER) such as batteries and renewables to support all operational requirements such as heating and cooling, lighting, radars, other sensors, and more. These systems typically employ three-phase alternating current as a means for producing and distributing power.

In microgrid applications, it is beneficial to correct the power factor (PF) to unity. As PF is reduced away from one, costs can increase as a result of utility grid charges, or in a shipboard environment, larger generators are required. For example, the Pacific Gas and Electric utility company adjusts billing for customers with peak demand over 400 kW via the power factor at which they operate, which can mean a bill if the power factor is less than 0.85 or credit if the power factor is corrected above 0.85 [2]. With the addition of renewables and other distributed energy resources, often connected through power electronic converters, the power factor at a grid's point of common coupling can be corrected.

Furthermore, as radars, sonars, and weapons systems become more sophisticated, so do the power profiles that are drawn from the grid by these loads. On a grid with a generator employing traditional frequency and voltage droop control, as the real and reactive power (P-Q) increases, frequency and voltage go down, and thus rotor speed and field excitation must be adjusted to compensate, which generally happens over seconds [3]. In a microgrid, as opposed to a traditional utility grid, the combined inertia of rotational generators may not be sufficient to instantaneously support all load changes from a pulsed power or cyclic load without adverse effects on grid parameters such as voltage and frequency [3]. Again, a power electronic converter can quickly react and compensate for these changes relieving the generator of this responsibility.

B. PREVIOUS RESEARCH

The impact of pulsed loads on power systems has been considered in research for over 20 years, with research 20 years ago suggesting that warships did not yet possess pulsed power loads and that development of power supplies for those loads would be required [4]. Research has also suggested that power electronics, combined with stored energy, can be used to correct power quality problems introduced by other systems [5].

The benefits of energy storage systems such as flywheels on ships or hybrid fuel cell/battery power systems on aircraft have been discussed in [6] and [7], respectively. An optimal charging profile for a DC microgrid is presented in [8], which could benefit a Voltage Source Inverter (VSI) supplying a three-phase grid by ensuring DC bus stability for the voltage conversion process.

Additional research has been conducted into P-Q flow control techniques, as they related to microgrids, in [9]. Oriti et al. [9] suggest that an energy management system can be used to control a single phase VSI to power critical loads if a grid fails, control peak power in the case where load exceeds grid capacity, or to shave loading when grid usage prices are highest to facilitate a reduction in cost. Kanavaros et al. [10] expanded on research conducted by Mendoza [11] into Q control in single-phase microgrids by also controlling real power using a mixed frame controller and examining orthogonal generation methods (OGM) to ensure that DERs could be utilized to correct PF to unity while supplying real power needed. A research direction suggested by Kanavaros [12] is to examine methods to perform peak power shaving during large transients. With the majority of industrial microgrids, including shipboard applications, consisting of three-phase power distribution, it is a natural progression to further this research in the three-phase domain.

C. RESEARCH GOAL

Any microgrid that contains traditional generators combined with DERs can benefit from a grid-tied inverter that can control active and reactive power flow to and from the grid. The benefits of power factor correction and ability to rapidly adjust to changes in load provide significant motivation for research into the primary controller of a three-phase VSI. Allowing a VSI to provide all reactive power, while also performing peak power shaving of pulsed loads, gives traditional generators the time needed to respond to changes in load within their mechanical limitations.

This research seeks to develop a P-Q controller for a three-phase voltage source inverter, which can correct the grid power factor to unity, while also minimizing abrupt changes in grid-supplied power coming from a pulsed load. Furthermore, this research

seeks to prove that the controller design can operate within the voltage requirements for Type I power, as defined in [13].

D. THESIS ARRANGEMENT

This thesis is arranged to ensure that the results of the described research are understood and reproducible. In Chapter II, the background for the research is presented, including the definition of terminology important to the remainder of the thesis. Chapters III presents the physics-based model of the system, to include the grid, VSI, loads, and the DC/DC buck/ boost converter. Chapter IV explains the simulations performed and presents the simulation results for the selected scenarios. Chapter V provides the experimental validation of the physics-based model and software simulation using laboratory hardware. Finally, Chapter VI presents conclusions and future work. An appendix contains the code implemented in MATLAB to run the Simulink models and produce plots of data.

II. BACKGROUND

This chapter contains definitions and explanations that help to support the importance of this research to the DOD and lay the groundwork for understanding the simulation and experimental methodologies.

A. MICROGRID

1. Basic Definition and Use

According to the U.S. Department of Energy (DOE), "a microgrid is a group of interconnected loads and distributed energy resources within clearly defined electrical boundaries that act as a single controllable entity with respect to the grid. A microgrid can connect and disconnect from the grid to enable it to operate in both grid-connected or island-mode" [14]. The DOD definition is slightly less rigorous in that it does not require that the microgrid must interface with a utility grid, as may be the case with a FOB. The DOD definition of a microgrid is "an integrated energy system consisting of interconnected loads and energy resources, which, as an integrated system, can island from the local utility grid and function as a stand-alone system" [15]. As soon as a ship disconnects from shore power, it becomes an islanded microgrid, compatible with the DOD definition. Similarly, FOBs are often set up in areas without existing infrastructure and may exclusively operate in islanded mode.

2. The Benefit of Three Phase Microgrid Analysis

Because of benefits such as constant instantaneous power over time and reduced cost of electric distribution due to smaller line sizes, three-phase power is preferred in large industrial applications [16]. As a result, single-phase microgrids, such as those researched in [9], [11], [12], [17] have limited scope in terms of DOD microgrids. While it is true that any three-phase microgrid utilized by personnel has a portion dedicated to single-phase power for loads such as computers, coffee makers, and vacuum cleaners, the majority of power usage comes from larger three-phase loads such as refrigeration, HVAC, sonars, radars, pumps, etc. For example, a home with solar panels and a battery storage system that

interfaces with the grid to provide cost savings or battery backup could be considered a single-phase microgrid that would benefit from previously researched P-Q control. While a single household may enjoy the benefit of reducing their monthly electric bill, the DOD is seeking to reduce tens of thousands of kWh of energy consumption, while prolonging the lifetime of power generation equipment using DERs. It is, therefore, necessary to expand research of P-Q control of DOD microgrids into the three-phase domain.

B. THREE-PHASE REAL AND REACTIVE POWER FLOW

Understanding how electricity is generated and distributed is essential to understanding how to design a controller that controls real and reactive power flow, as well as being able to design the physics-based model of that controller. Three-phase electricity is generated and distributed by major utility companies, at high voltage, to end-users where it is stepped down via transformers and then distributed as single or three-phase electrical power for residential, commercial, or industrial use. This basic premise is shown in Figure 2. In a microgrid, three-phase power may be generated (by diesel generators, steam turbines, gas turbines) at the voltage required for three-phase loads to which they are connected. These microgrids are generally able to interface with the main grid via a switch, such as a breaker or a bus transfer.

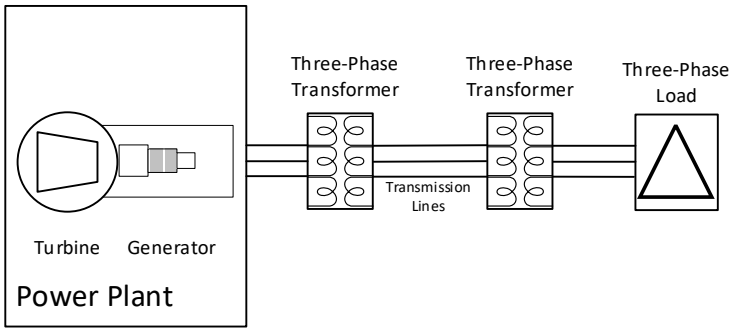

Figure 2. Basic Diagram of Three-Phase Power Generation and Distribution

1. Balanced Three-Phase Power Calculations

Aside from a fault or other system irregularity, three-phase systems are engineered to be balanced. A balanced system allows each phase of the circuit to be analyzed as an

independent single-phase circuit. To perform the calculations correctly, one must note whether sources and loads are “wye-connected” or “delta-connected,” as shown in Figure 3.

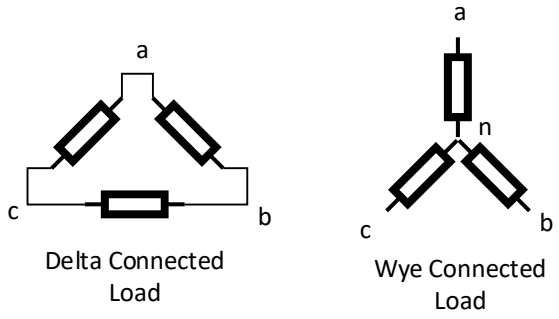

Figure 3. Example of Delta Connected and Wye Connected Loads

In the typical case of a wye connected source, connected to a wye-connected load, the circuit can be simplified, as shown in Figure 4.

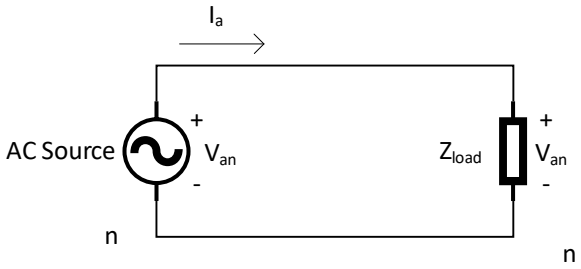

Figure 4. Single-Phase Representation of Wye-Wye Connected Source-Load

Traditionally, phasors are used to represent all quantities in an AC circuit, and within a three-phase circuit, each phase is physically 120° apart, which leads to the representation of source voltage in Equation (1), where V_{pk} is the peak value of the sinusoidal voltage, and the nomenclature “an” represents “phase a to neutral.”

$$\begin{aligned}\mathbf{V_{an}} &= V_{pk}\angle 0° \\ \mathbf{V_{bn}} &= V_{pk}\angle 120° \\ \mathbf{V_{cn}} &= V_{pk}\angle 240°\end{aligned} \tag{1}$$

When analyzing the circuit in Figure 4, the voltage angle, θ_v, is equal to 0°. Because the load impedance, Z_{load}, can represent a combination of resistors, inductors, and capacitors, it is also important to represent this value as a phasor as shown in Equation (2), where θ_z is the impedance angle, R is the resistance, and X_L and X_c are the inductive and capacitive reactances, respectively.

$$\mathbf{Z_{load}} = \left|Z_{load}\right|\angle\theta_z = \sqrt{R^2 + \left|X_L - X_C\right|^2}\angle \tan^{-1}\left(\frac{\left|X_L - X_C\right|}{R}\right) \tag{2}$$

Following Ohm's law, this leaves the current to be calculated as follows in Equation (3).

$$I_{a_{pk}}\angle\theta_i = \frac{V_{pk}\angle\theta_v}{\left|Z_{load}\right|\angle\theta_z} \tag{3}$$

In practical applications, voltage and current are the measured quantities, which requires the conclusion that the impedance angle is the difference of voltage angle and current angle, which can be shown by slightly rearranging Equation (3), or graphically in Figure 5.

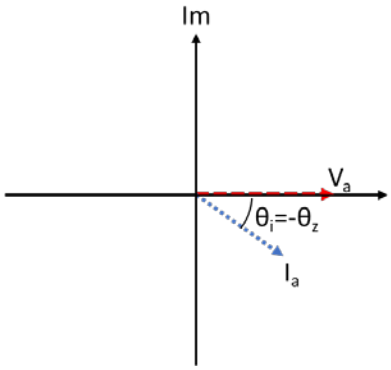

Figure 5. Visual Representation of Impedance Angle

The impedance angle is used to calculate the power factor (PF), per Equation (4). The impedance angle, voltage angle, and current angle are annotated as θ_z, θ_v, and θ_i, respectively. PF is described as either leading or lagging depending on if the current is leading or lagging the voltage. In the case of Figure 5, the power factor is lagging, and the load is inductive.

$$PF = \cos\left(\theta_z\right) = \cos\left(\theta_v - \theta_i\right) \tag{4}$$

Once the vector quantities of the voltage and current are known for the equation of Figure 4, power can be calculated per Equation (5).

$$P_A = \left|V_{an}\right|\left|I_a\right|\cos(\theta_v - \theta_i) = \left|V_{an}\right|\left|I_a\right|PF \tag{5}$$

Since each phase is balanced, the total power of the three-phase system is just three times the power of a single phase. The subscript "*ph*" in Equation (6) represents "phase."

$$\begin{aligned} P_A &= P_B = P_C \\ P_{ABC} &= P_A + P_B + P_C = 3P_A \\ P_{ABC} &= 3V_{ph}I_{ph}PF \end{aligned} \tag{6}$$

Due to the nature of wye and delta connections shown in Figure 3, the phase and line values of voltage and currents are not necessarily equal. For a wye connected circuit, the relationships of Equation (7) apply, and for a delta connected circuit, the relationships of Equation (8) apply [18].

$$\begin{aligned} I_{line} &= I_{ph} \\ V_{line} &= \sqrt{3}V_{ph}\angle 30° \end{aligned} \tag{7}$$

$$\begin{aligned} I_{line} &= \sqrt{3}I_{ph}\angle -30° \\ V_{line} &= V_{ph} \\ Z_{delta} &= 3Z_{wye} \end{aligned} \tag{8}$$

Real power is the power consumed to do actual work, such producing heat or driving a motor. In an AC system, however, capacitance and inductances that are present cause another type of power to be developed, called reactive power. Reactive power does no real work, but represents energy stored and exchanged between magnetic and electric fields. The magnitude of real and reactive power represents a third quantity called apparent power. These quantities, related by the impedance angle, are typically represented in a triangle, as shown in Figure 6.

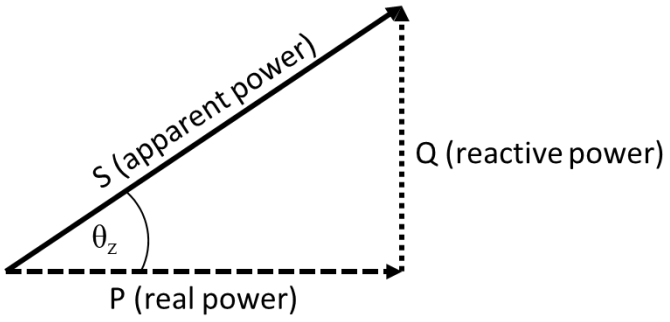

Figure 6. Power Triangle Relationships

In a three-phase circuit, reactive power can be calculated per Equation (9), apparent power per Equation (10), and complex power per Equation (11).

$$Q_{ABC} = 3V_{ph}I_{ph}\sin\left(\theta_z\right) \tag{9}.$$

$$\left|S_{ABC}\right| = 3\left|S_{ph}\right| = 3\sqrt{P^2 + Q^2} \tag{10}$$

$$S = P + jQ \tag{11}$$

2. Inverter Current Control

It was discussed in Section I.A. that reactive power is undesirable in a grid because the apparent power is larger than it would need to be to complete the same amount of real work. In this way, the goal of the controller of an inverter should be to inject a current with a magnitude and angle such that it is actively canceling out the reactive (imaginary) current

of any loads. In this way, θ_z becomes 0, and the PF becomes 1, and the grid is therefore supplying only real power. Additionally, an inverter can be quickly controlled to provide current that supplies not only the reactive current required by a load but also all the current that is required when a step-change in load current occurs.

Figure 7 shows a source, such as a traditional turbine generator or a grid, powering an inductive load. The load current is equal to the source current as the source is supplying all the power. The real and imaginary current components are projected onto their respective axes and are represented in Equation (12).

$$I_{load} = I_{load\_re} + jI_{load\_im} \tag{12}$$

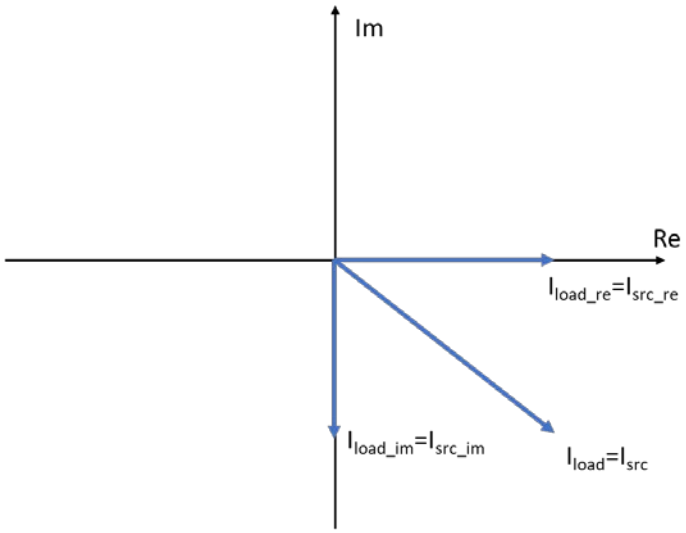

Figure 7. Phasor Diagram of Source Supplying A Load

Once a voltage source inverter is connected to the grid, a current command can be issued to allow the inverter to produce a current which supplies all the reactive load current and corrects the PF to unity. This is shown in Figure 8, and the relationships of Equation (13).

$$I_{load} = I_{inv} + I_{src}$$
$$I_{load\_im} = I_{inv}$$
$$I_{load\_re} = I_{src} \quad (13)$$

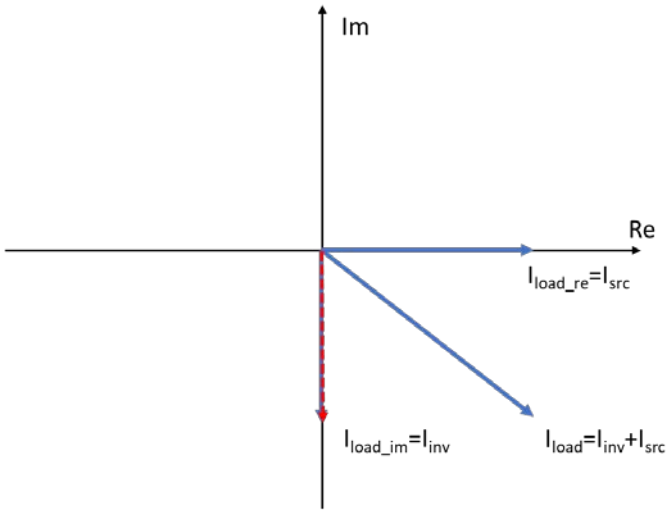

Figure 8. Phasor Diagram with Inverter Current Supplying Reactive Current

Following a step increase in load, given the same power factor, the inverter current is commanded to supply all reactive power, while also providing any additional real power over what the grid is supplying. Allowing grid or generator current to remain initially constant enables the current controller for the inverter to slowly reduce the real current it is supplying, thereby allowing the generator to pick up the additional load more slowly. In Figure 9, it is shown that the inverter is now supplying all reactive current, as well as that portion of real current that was not previously being supplied by the source. This is also represented in Equation (14).

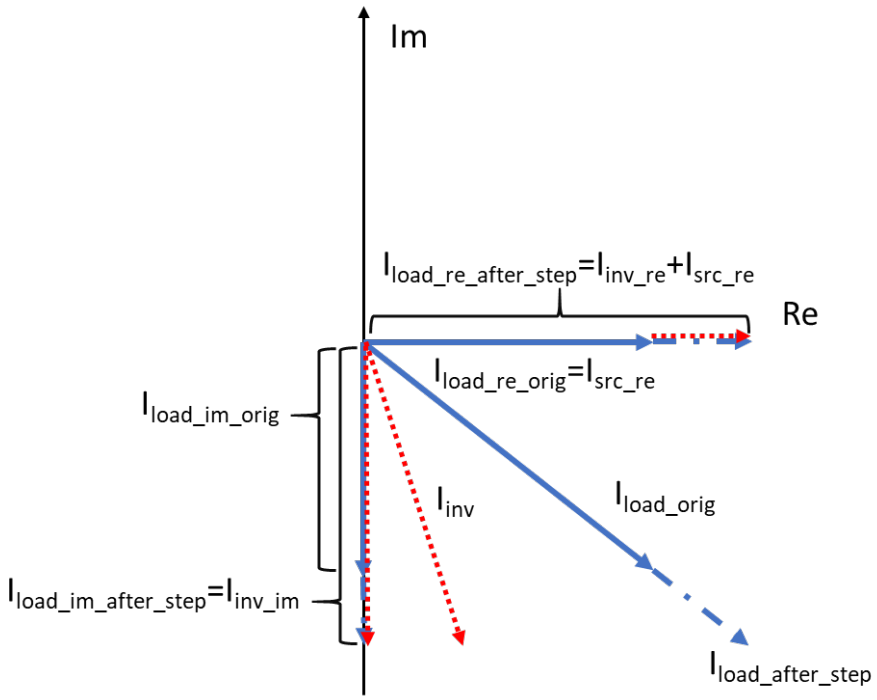

Figure 9. Phasor Diagram of the Instant after a Step Load Increase

$$
\begin{aligned}
I_{load\_after\_step\_up} &= I_{inv} + I_{src} \\
I_{load\_im\_after\_step\_up} &= I_{inv\_im} \\
I_{load\_re\_after\_step\_up} &= I_{src\_before\_step\_up} + I_{inv\_re}
\end{aligned}
\tag{14}
$$

Once the condition is restored similar to that of Figure 8, where the source is supplying all real current, and the inverter is supplying all reactive current, presume a step load reduction occurs, as shown in Figure 10. The current controller adjusts to provide a smaller amount of reactive current and supplies a negative real current. This implies that the grid is now powering the inverter, and that the source of the inverter is being charged, whether it is a battery or supercapacitor. Again, the idea is that the grid, which had previously adjusted to the higher load, sees no immediate impact of the load reduction. The reduction in real grid current can happen slowly as the real inverter current is slowly reduced to zero. Equation (15) represents what is seen in Figure 10.

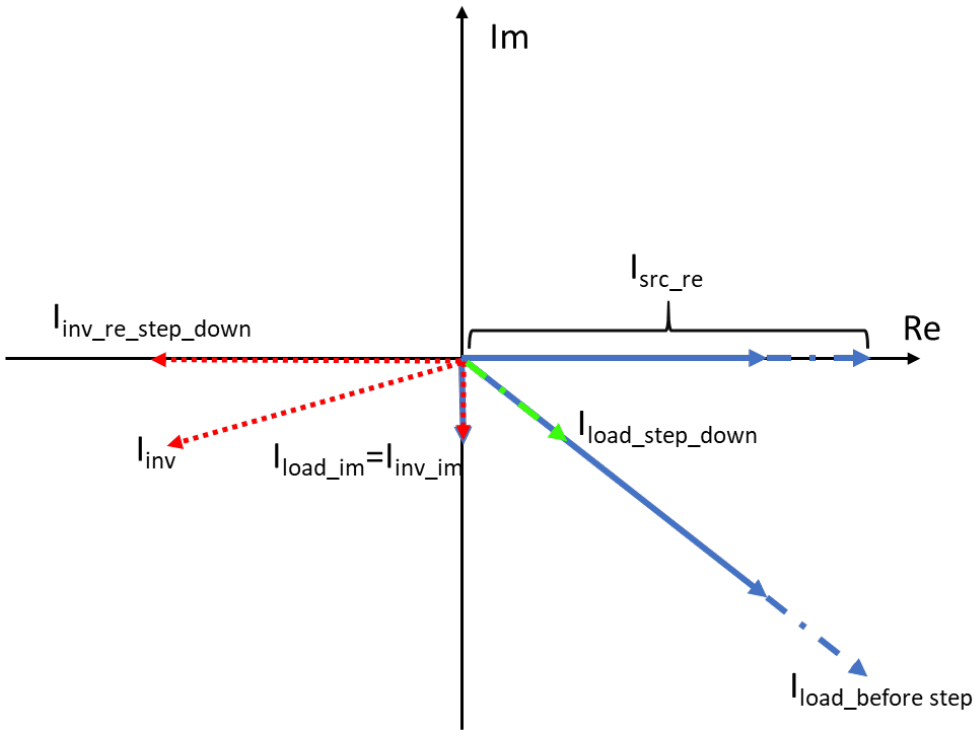

Figure 10. Phasor Diagram of Instant after a Step Load Decrease

$$
\begin{aligned}
I_{load\_after\_step\_down} &= I_{inv} + I_{src} \\
I_{load\_im\_after\_step\_down} &= I_{inv\_im} \\
I_{load\_re\_after\_step\_down} &= I_{src\_before\_step\_down} + I_{inv\_re}
\end{aligned} \tag{15}
$$

The previous description provides a high-level overview of the purpose of this thesis: design a controller for an inverter that can adjust grid power factor to unity and supply real power rapidly to minimize the effect on the grid and any connected rotational generators.

C. MIL-STD-1399-300-1 REQUIREMENTS

1. Type I, 60Hz Power

AC power found onboard naval ships is generally 440V_{rms}, 60Hz, three-phase, ungrounded or high-resistance grounded, and for the purposes of lighting or other user equipment, AC power is 115Vrms, 60Hz, three-phase ungrounded. [13]. Power systems onboard ships must meet the requirements in Table 1.

Table 1. Characteristics of Type I Shipboard Electric Power Systems. Adapted from [13].

Characteristics	Type I
Frequency	
1. Nominal Frequency	60 Hz
2. Frequency Modulation	0.5%
3. Frequency Tolerance	±3% (Submarines: ±5%)
4. Frequency Transient Tolerance	±4%
5. Worst Case Frequency SS and Transient Excursion	±5.5%
6. Recovery Time from Item 4 or 5	2 seconds
Voltage	
7. Designated Nominal User Voltage	440, 115, 115/200 V_{rms}
8. LL Voltage Unbalance	3% (Submarines: 0.5% for 440$V_{rms;}$ 1% for 115V_{rms})
9. Voltage Modulation	2%
10. Average LL Voltage from Nominal Tolerance	±5%
11. Single LL Voltage from Nominal Tolerance	±7% (CVN 78 class: ±10%)
12. Maximum Voltage SS Departure	±8% (CVN 78 class: ±10%)
13. Voltage Transient Tolerance	±16%
14. Worst Case Voltage SS and Transient Excursion	±20%
15. Recovery Time from Item 13 or 14	2 seconds
16. Voltage Spike (± Peak Value)	2.5kV_p/1.0kV_p (440 V_{rms}/115V_{rms} sys)
Waveform (Voltage)	
17. Maximum THD	5%
18. Maximum Single Harmonic	3%
19. Maximum Deviation Factor	5% (Submarines: 3%)

Because Table 1 is sourced from [13], it is therefore approved for use by all departments and agencies of the DOD. As such, when designing a controller that could be used in any DOD power system, it is prudent to ensure the design meets the specifications of [13].

2. Pulsed Loads

As was previously mentioned, in lieu of energy storage to power a pulsed load, a generator must have sufficient inertia to avoid a significant degradation in power quality (voltage or frequency) [3], [13]. The military defines a pulsed load as “user equipment that

demands infrequent of repetitive power input that could be supplemented by energy storage," and goes on to give the examples of a sonar or radar [13].

The increasing prevalence of advanced electronics has allowed engineers to design and implement new types of sensors and other technologies to benefit the DOD. Technological advances such as the railgun, electromagnetic catapult onboard Ford-class aircraft carriers, directed energy weapons, as well as advanced radars and sonars require large amounts of electrical energy to be utilized in a short period of time [8]. In late May 2020, the Navy completed a test of a 150kW laser on USS Portland (LPD-27), successfully disabling an aerial drone [19].

As the complexity of loads increases, so too will the complexity of the power profile drawn by these loads. The military recognized this and updated [13] in 2018 to include pulsed load requirements. The pulsed load requirements apply to loads with a maximum instantaneous power of $\geq$100kW and $\leq$2MW, and are such that the "three-phase pulsed real power deviation from the average real power level…be less than ±50kW over a 1-second interval centered on the event" [13].

Figure 11 is an example pulsed power waveform that is meant to demonstrate both acceptable and unacceptable jumps in power. The gray-shaded areas show the times in which the jump in power is too large, such that it exceeds ±50kW from the 1 second centered rolling average [13]. This power profile provides a good benchmark for an inverter controller to meet, for if it can meet the demands of a power profile that violates the limit, then it inherently meets the standard.

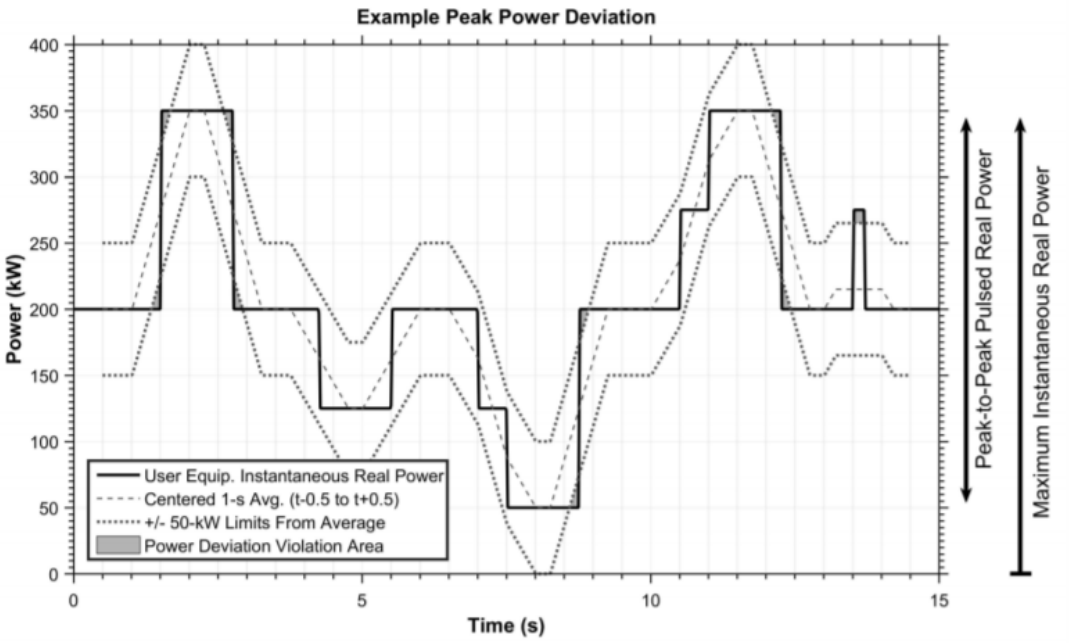

Figure 11. Pulsed Power Waveform and Deviation Example. Source: [13].

D. REFERENCE FRAME THEORY

By changing the frame of reference from which AC power systems parameters (voltage or current) are observed, a simplification can occur where differential equations are simplified, and the control of systems becomes simpler [20]. Figure 12 represents the idea of converting a three-phase signal (f_{abc}) to an arbitrary reference frame (f_{qd0}). Each phasor of f_{abc} can be projected onto the q and d axis, based on the angle, θ. The resulting vectors, f_{qd0}, rotate based on the chosen arbitrary angular velocity, ω. In a balanced three-phase system, f_0 always equals 0.

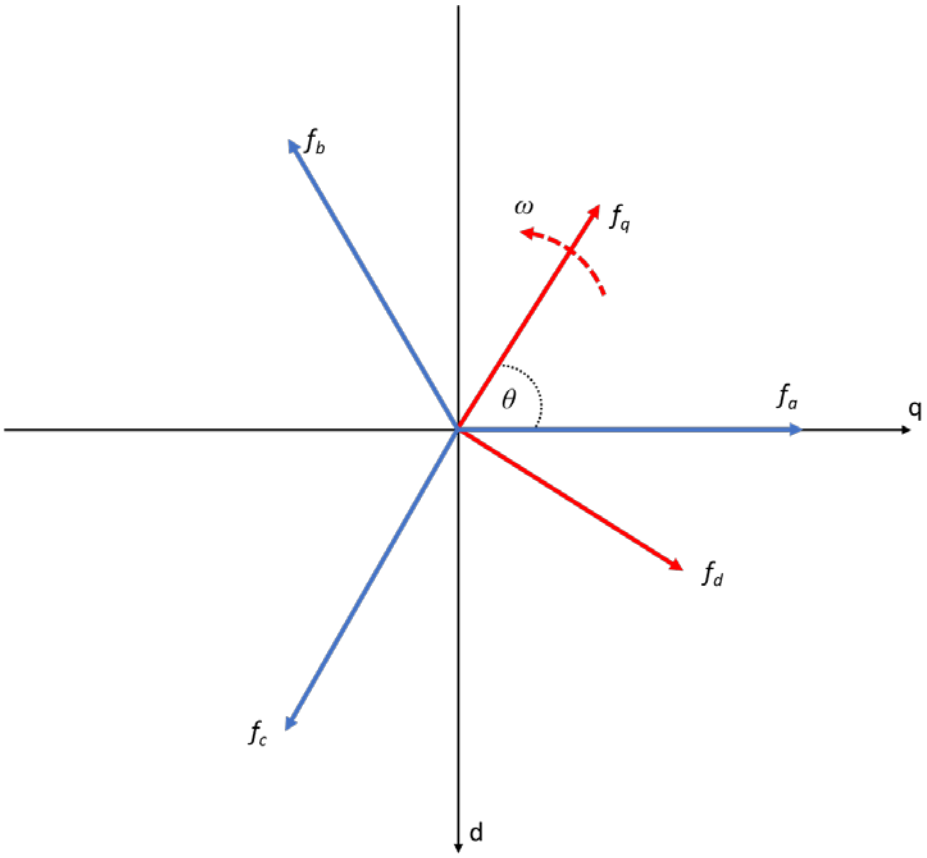

Figure 12. Reference Frame Transform from f_{abc} to f_{qd0}. Adapted from [20].

1. Stationary Reference Frame

The stationary reference frame transformation, also known as the Clarke transformation (f_{abc} to $f_{\alpha\beta 0}$), projects three-phase time-varying signals onto a stationary reference frame, or in other words, a stationary axis. The results, in a balanced system, are vectors f_{α} and $f_{\beta,}$ which oscillate on their α and β axes, respectively. The α and β axes are shown in Figure 13. The resultant vector, shown in red in Figure 13, continues to rotate counter-clockwise at the same frequency as the original f_{abc} vector. For this thesis, the Clarke transformation is also identified as the $qd0^s$ reference frame.

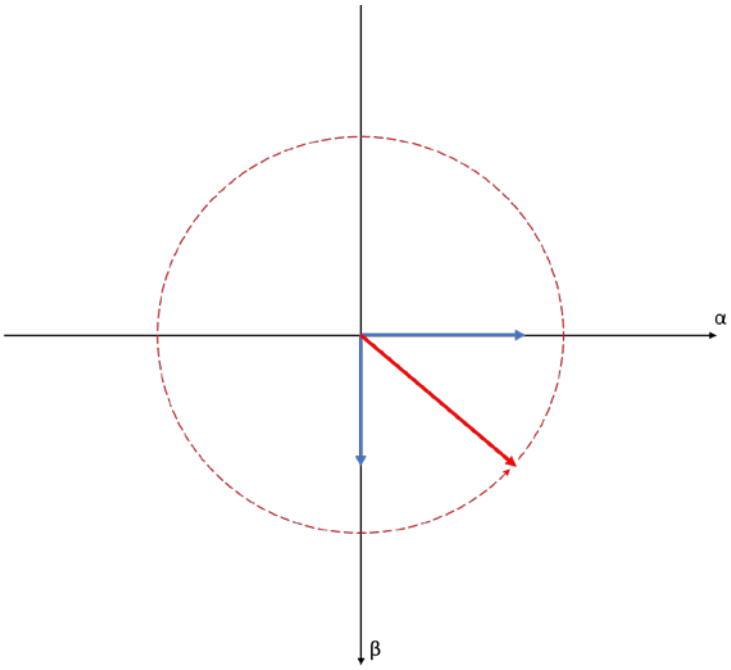

Figure 13. αβ0 Reference Frame

A conversion from f_{abc} to $f_{\alpha\beta 0}$ is performed per Equations (16)-(17) [20].

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} = K_s \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{16}$$

$$K_s = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{17}$$

2. Rotating Reference Frame

The rotating reference frame is also known as the Park transformation (f_{abc} to f_{qd0}). In this transformation, the q and d axes, as labeled in Figure 12, rotate counter-clockwise with an arbitrary angular frequency. The angular frequency can be selected based on the

application to create simplifications as desired. The angular frequency could, for example, equal that of the stator, or that of the rotor, of a machine. The result of the Park transformation is two vectors projected onto the q and d axes, and due to the rotation of the axes, the sum of those vectors equals the resultant vector when summing f_{abc}. For this thesis, the Park transformation is also identified as the $qd0^e$ reference frame, where the e represents the electrical frequency 60Hz. In this case, the magnitudes of the q and d components are constant, allowing the steady-state error of a PI controller to equal 0 [21].

A conversion from f_{abc} to f_{qd0} is performed per Equations (18)-(19) and, once voltage and current are converted to $qd0^e$, three-phase P-Q is calculated per Equations (20)-(21) [20]. Equations (20)-(21) assume that the system is balanced such that f_0 equals 0.

$$\begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} = K_{s_{qd0}} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{18}$$

$$K_{s_{qd0}} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{19}$$

$$P_{qd0} = \frac{3}{2}(v_q i_q + v_d i_d) \tag{20}$$

$$Q_{qd0} = \frac{3}{2}(v_q i_d - v_d i_q) \tag{21}$$

III. CONVERTER AND GRID PHYSICS-BASED MODEL

A. OVERVIEW

The physics-based model used for simulations consists of four main sections: a bidirectional boost/buck DC/DC converter, a three-phase VSI, the grid, and the controllers for both the DC/DC converter and the VSI. Figure 14 shows a general overview of the system. The design of the VSI controller is the focus of this thesis and will, therefore, garner the most attention. When referring to system values, those required for Type I $200V_{rms}$ power are referenced. For Type I $440V_{rms}$ power, parameters are listed in Appendix A.

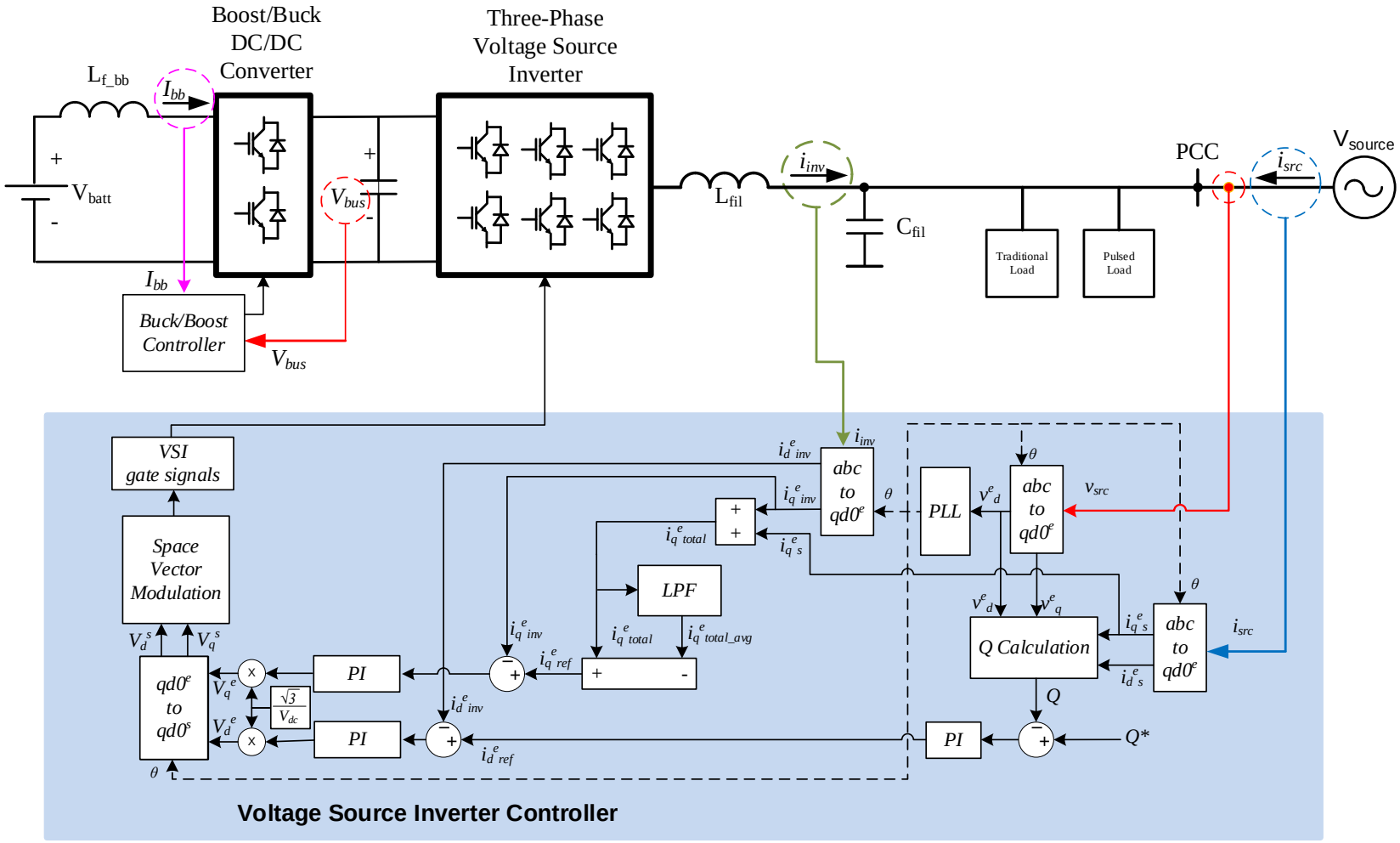

Figure 14. Overview of the Three-Phase VSI Controller and the System Interface

B. GRID/CONVERTER/LOAD CONNECTION

The VSI is coupled, through an LC filter, to the loads and the source. When referring to the source, this represents the traditional grid to which one would connect a three-phase load. As discussed in Sections I.A and C.2, a conventional grid has sufficient capacity such that under most load variations, voltage and frequency are not adversely affected. In a shipboard environment or FOB, the relatively small generators may struggle with large pulsed loads. It is, therefore, necessary to also consider that the "source" could be a smaller shipboard generator or a diesel generator at an FOB, that would benefit from being interfaced with a VSI.

The source is modeled, as shown in Figure 15, as an ideal voltage source. A 0.5mH inductor and a 0.2Ω resistor are placed in series with each phase of the voltage source to simulate the line impedance between the source and the point of common coupling (PCC). *Vref* represents the peak amplitude of the line to neutral voltage. The three-phase source voltage is represented by Equation (22).

$$\begin{aligned} v_a &= Vref\cos\left(2\pi f\_fund\right) \\ v_b &= Vref\cos\left(2\pi f\_fund - \tfrac{2\pi}{3}\right) \\ v_c &= Vref\cos\left(2\pi f\_fund + \tfrac{2\pi}{3}\right) \end{aligned} \tag{22}$$

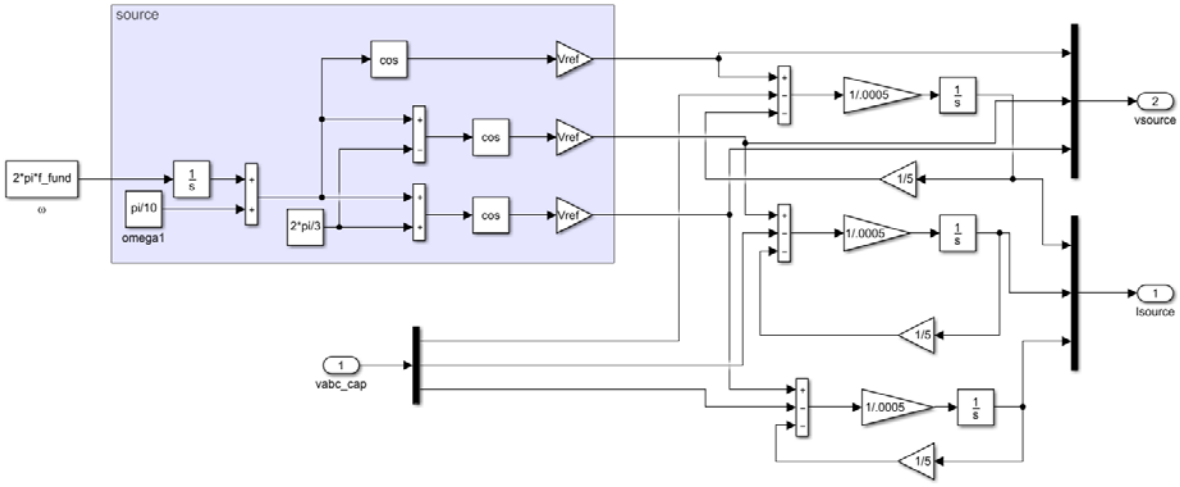

Figure 15. Grid Source Model

As Figure 14 shows, a pulsed load or a traditional load can be connected to the grid. For this model, only a pulsed load is simulated because the P-Q controller is designed such that the source would always carry the "average" loading. In other words, the P-Q controller would maintain any "constant" loads powered by the source; it is, therefore, trivial to simulate additional loading.

The pulsed load simulated is a wye-connected load, designed to maintain near a 0.8 lagging PF through all steps. The 0.8 lagging PF was chosen as most actual loads are inductive, and it was significantly far enough from unity that the effects of Q control could be observed. The load profile of Figure 11 was used to determine times at which it was desired for step changes to occur, and the loads to be simulated. The resistance and inductance were back-calculated from the theory of Section B.1, but with power scaled down by a factor of 100 (3.5kW of load instead of 350kW of load). By adjusting the simulation parameters, $440V_{rms}$ Type I power and loads greater than 50kW are simulated to ensure the controller functions as designed under the actual pulsed power requirements of [13]. Equations (23) - (29) demonstrate how each value for L_o and R_o is calculated.

$$V_{rms_{LL}} = 200V \Rightarrow V_{rms_{ph}} = \frac{200V}{\sqrt{3}} = 115.47V \tag{23}$$

$$|S| = \frac{P_{desired}}{PF_{desired}} = \frac{3500W}{0.8} = 4375VA \tag{24}$$

$$\begin{aligned} S &= P + jQ = |S| PF_{desired} + j|S| \sin\left(\cos^{-1}\left(PF_{desired}\right)\right) \\ S &= (4375VA)(0.8) + j(4375VA)\sin\left(\cos^{-1}(0.8)\right) \\ S &= (3500 + j2625)VA \\ P &= 3500W, Q = 2625VAR \end{aligned} \tag{25}$$

$$I_{rms_{ph}} = \left(\frac{S}{3V_{rms_{ph}}}\right)^* = \left(\frac{(3500 + j2625)VA}{(3)115.47V}\right)^* = (10.10 - j7.58)A \tag{26}$$

$$Z_{ph} = \frac{V_{ph}}{I_{ph}} = \frac{115.47V}{(10.10 - j7.58)A} = R + jX_L = (7.31 + j5.49)\Omega \tag{27}$$

$$R = 7.31\Omega \tag{28}$$

$$L = \frac{X_L}{2\pi f} = \frac{5.49\Omega}{2\pi(60Hz)} = 14.6mH \tag{29}$$

Table 2 shows the values of resistance and inductance that are used to simulate each load step and the time at which each load step occurs. This table represents the power profile at 1/100 of the real power values in Figure 11. To simulate a power profile that is considered pulsed power by [13], with maximum instantaneous real power between 100kW and 2MW, a variable *MIL_STD_LOAD_ENABLE* can be set from 0 to 1. Changing *MIL_STD_LOAD_ENABLE* to 1 divides each value of R_o and L_o by 32 in the model, allowing the model to transition from simulating the power values listed in Table 2 to simulating the power values above 100kW. Such a large power profile requires $440V_{rms}$ Type I power, and other adjustments listed in Appendix A. The SIMULINK implementation of the load profile in Table 2 is shown in Figure 16 and Figure 17.

Table 2. Simulated Multi-Step Load Profile for Type I 200V_{rms} Power

Step Time Start [s]	Step Time End [s]	Real Power (W)	Reactive Power (VAR)	R_o (Ω)	L_o (mH)
0.00	1.50	2000	1500	12.8	25.5
1.50	2.75	3500	2625	7.31	14.6
2.75	4.25	2000	1500	12.8	25.5
4.25	5.50	1250	937.5	20.5	40.7
5.50	7.00	2000	1500	12.8	25.5
7.00	7.50	1250	937.5	20.5	40.7
7.50	8.75	500	375	51.2	101.9
8.75	10.50	2000	1500	12.8	25.5
10.50	11.00	2750	2062.5	9.31	18.5
11.00	12.25	3500	2625	7.31	14.6
12.25	13.50	2000	1500	12.8	25.5
13.50	13.75	2750	2062.5	9.31	18.5
13.75	15.00	2000	1500	12.8	25.5

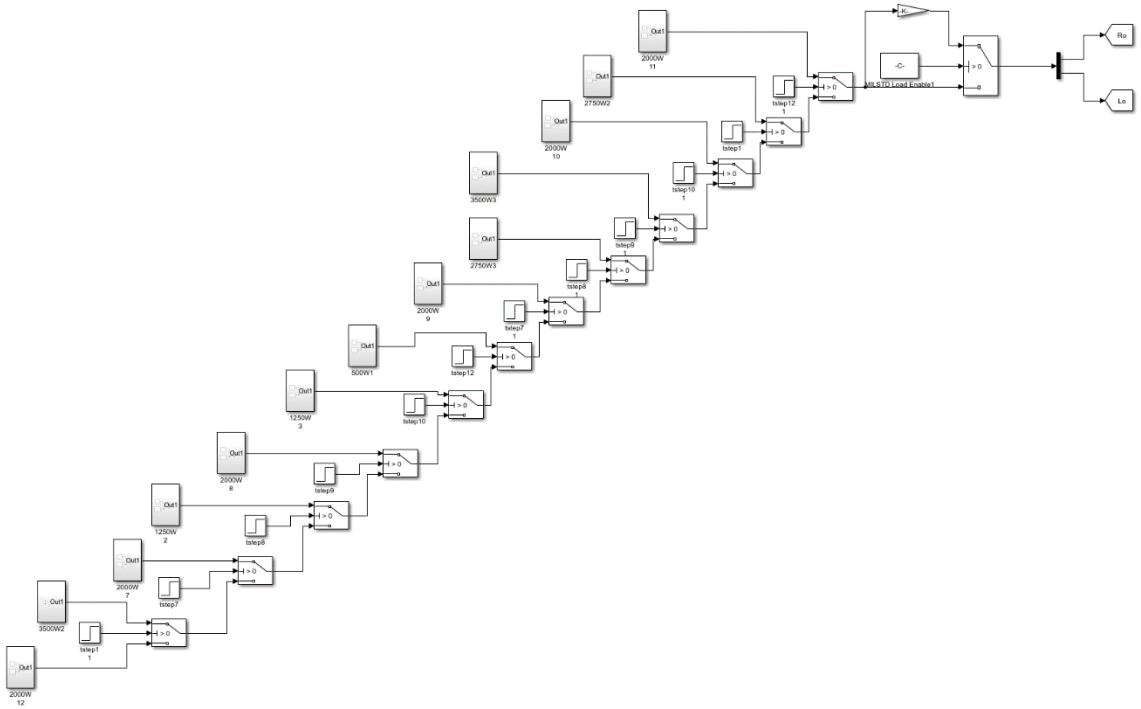

Figure 16. Simulink Implementation of Load Profile

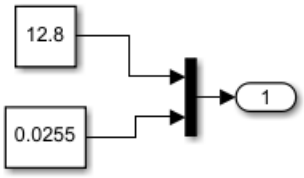

Figure 17. Resistance (Top) and Inductance (Bottom) Inside a Load Block

Another load profile simulated is a pulsed load from 1250W to 3500W, to aid in the understanding of how the controller handles a more severe jump. This profile is shown in Table 3.

Table 3. Simulated Single-Step Load Profile for Type I 200V_{rms} Power

Step Time Start [s]	**Step Time End [s]**	**Real Power (W)**	**Reactive Power (VAR)**	**R_o (Ω)**	**L_o (mH)**
0.00	3	1250	937.5	20.5	40.7
3	6	3500	2625	7.31	14.6
6	9	1250	937.5	20.5	40.7
9	12	3500	2625	7.31	14.6
12	15	1250	937.5	20.5	40.7

As shown in Figure 18, the three-phase VSI is connected to the grid through an LC filter. The physics-based model of the VSI output circuit is derived in the *abc* frame and then transformed into the *qd0* synchronous frame, where the control system is implemented [19], [22]. This transformation is shown in Equations (30) - (33).

$$\begin{bmatrix} v_q^{\,e} \\ v_d^{\,e} \\ v_0^{\,e} \end{bmatrix} = K_{s_{qd0}} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{30}$$

$$\begin{bmatrix} v_{q\,C_f}^{\,e} \\ v_{d\,C_f}^{\,e} \\ v_{0\,C_f}^{\,e} \end{bmatrix} = K_{s_{qd0}} \begin{bmatrix} v_{C_f a} \\ v_{C_f b} \\ v_{C_f c} \end{bmatrix} \tag{31}$$

$$\begin{bmatrix} i_{q\ inv}^{\ e} \\ i_{d\ inv}^{\ e} \\ i_{0\ inv}^{\ e} \end{bmatrix} = K_{s_{qd0}} \begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \end{bmatrix} \tag{32}$$

$$\begin{bmatrix} i_{q\ load}^{\ e} \\ i_{d\ load}^{\ e} \\ i_{0\ load}^{\ e} \end{bmatrix} = K_{s_{qd0}} \begin{bmatrix} i_{load_a} \\ i_{load_b} \\ i_{load_c} \end{bmatrix} \tag{33}$$

$K_{s_{qd0}}$ is the matrix to transform the *abc* variables into the *qd0* synchronous reference frame, as defined in (19). Neglecting the zero axis variables, the physics-based model in the synchronous reference frame of the VSI output network is shown in (34) in matrix format, where *s* is the Laplace transform operator.

$$\begin{bmatrix} 0 & \omega L_f & 1 & 0 & 0 & 0 \\ -\omega L_f & 0 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & \omega C_f & 1 & 0 \\ 0 & -1 & -\omega C_f & 0 & 0 & 1 \\ 0 & 0 & -1 & 0 & R_{load} & \omega L_{load} \\ 0 & 0 & 0 & -1 & -\omega L_{load} & R_{load} \end{bmatrix} \begin{bmatrix} i_{q\ inv}^{\ e} \\ i_{d\ inv}^{\ e} \\ v_{q\ C_f}^{\ e} \\ v_{d\ C_f}^{\ e} \\ i_{q\ load}^{\ e} \\ i_{d\ load}^{\ e} \end{bmatrix}$$
$$+ s \begin{bmatrix} L_f & 0 & 0 & 0 & 0 & 0 \\ 0 & L_f & 0 & 0 & 0 & 0 \\ 0 & 0 & C_f & 0 & 0 & 0 \\ 0 & 0 & 0 & C_f & 0 & 0 \\ 0 & 0 & 0 & 0 & L_{load} & 0 \\ 0 & 0 & 0 & 0 & 0 & L_{load} \end{bmatrix} \begin{bmatrix} i_{q\ inv}^{\ e} \\ i_{d\ inv}^{\ e} \\ v_{q\ C_f}^{\ e} \\ v_{d\ C_f}^{\ e} \\ i_{q\ load}^{\ e} \\ i_{d\ load}^{\ e} \end{bmatrix} - \begin{bmatrix} v_q^{\ e} \\ v_d^{\ e} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = 0 \tag{34}$$

The passive components are labeled as in Figure 18, and L_{load} and R_{load} are the components inside the "pulsed load" boxes in Figure 18.

The model allows simulating the system with an ideal converter as well as a switching PWM converter. In the first case, the reference voltages are sent to the output of the VSI, while in the second case, the reference voltages are input to the space vector

modulation (SVM) algorithm. The variable *ideal_source* set to 1 chooses the ideal converter simulation, and if set to 0, *ideal_source* selects the non-ideal inverter simulation instead. The benefit of using the ideal waveform is that the simulation time step can be increased, thus reducing simulation time for longer horizon simulations. The switching VSI model is necessary when a more detailed simulation is required, for example, for harmonic analysis.

To generate the ideal voltage waveform from the VSI, the voltages $V_q{}^s{}_{ref}$ and $V_d{}^s{}_{ref}$, in the stationary reference frame ($qd0^s$), produced by the current PI controller, are converted as shown in Equation (35). V_{DC} is the nominal voltage on the DC bus, and K_s^{-1} is the inverse of the K_s matrix defined in Equation (17).

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{V_{DC}}{\sqrt{3}} K_s^{-1} \begin{bmatrix} v_q{}^s{}_{ref} \\ v_d{}^s{}_{ref} \\ 0 \end{bmatrix} \tag{35}$$

When *ideal_source* is set to 0, the inverter phase voltages are instead produced by the SVM algorithm of the VSI, which is discussed in Section III.D.1 of this chapter. When the top switch of phase A is on, and the two bottom switches of phases B and C are on, the resulting ϕ-N voltages are computed as in (36) [23]. Thus the ϕ-N voltage is dependent on the switch state for a given phase and half the voltage on the DC bus [24].

$$\begin{aligned} v_{an} &= \frac{V_{bus}}{2} \\ v_{bn} &= -\frac{V_{bus}}{2} \\ v_{cn} &= -\frac{V_{bus}}{2} \end{aligned} \tag{36}$$

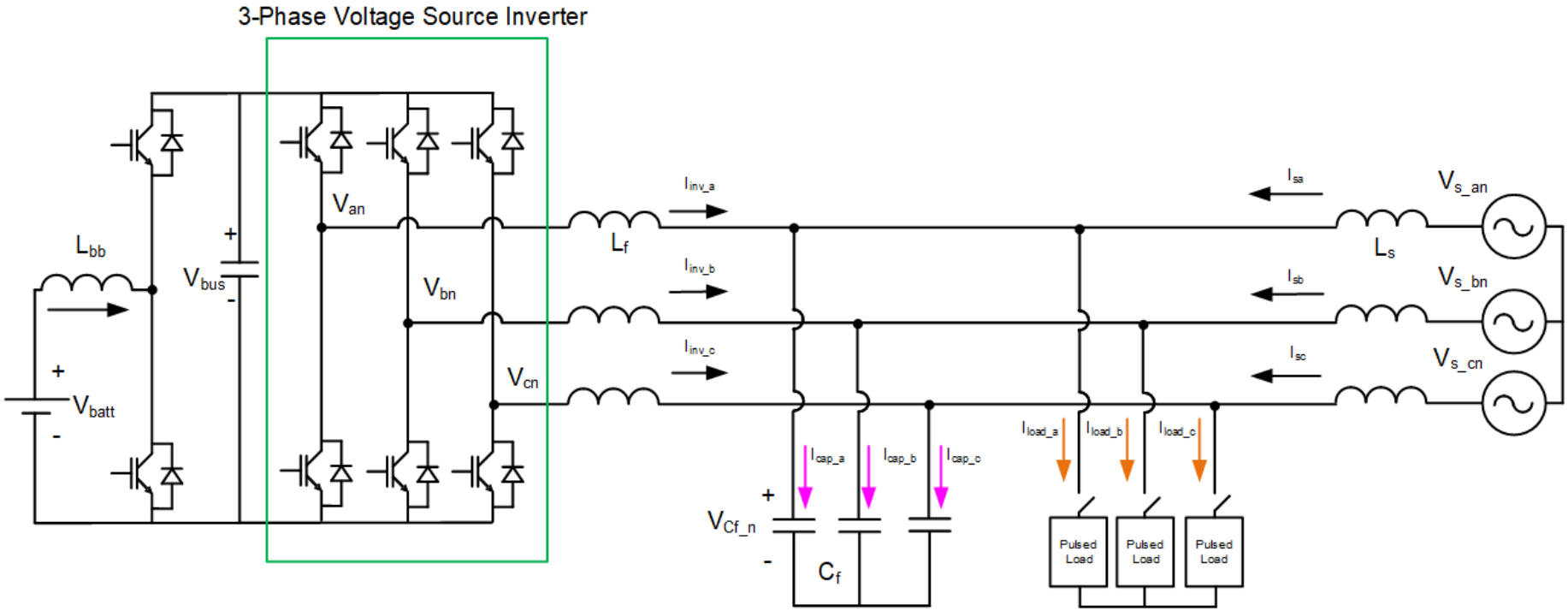

Figure 18. Basic Three-Phase VSI Implementation. Adapted from [24].

The Simulink implementation of the grid, converter, and load connections is shown in Figure 19.

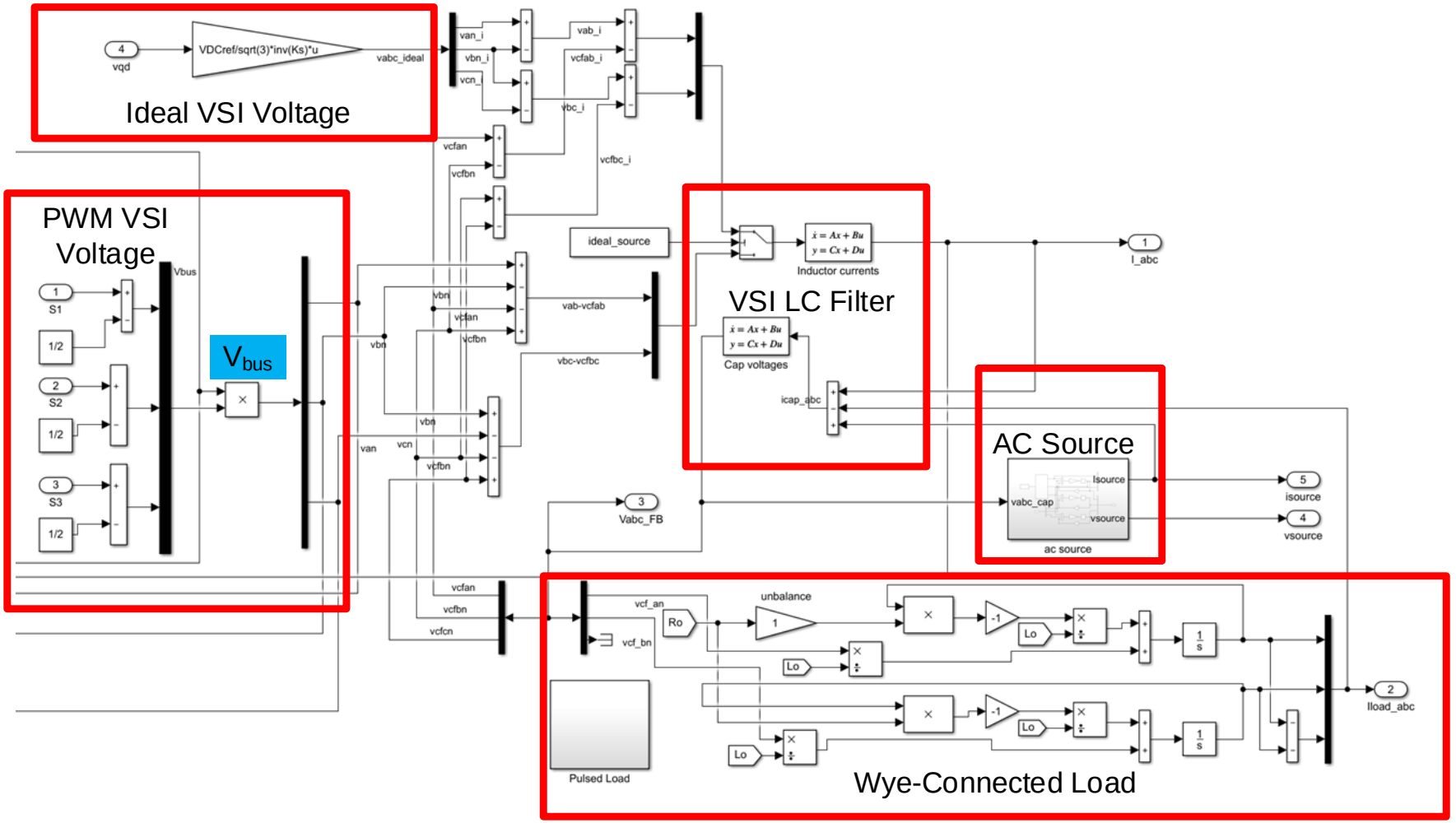

Figure 19. Simulink Model of Inverter, LC Filter, Load, and Source

C. DC-DC BOOST/BUCK CONVERTER

The P-Q controller designed in this thesis can be simulated using an ideal $450V_{dc}$ source at the input of the VSI. In that instance, where V_{bus} is labeled in Figure 19, a constant 450V would be placed instead. In nearly any practical shipboard or FOB application, a voltage that high is created from a DC/DC Boost/Buck converter. A DC/DC converter interfaced with a high voltage DC bus allows lower voltage DERs, such as batteries or supercapacitors, to interface with a higher voltage three-phase AC system. Because a bidirectional converter is being used, the DERs could be charged from the grid, or can supply power to the grid, depending on the current signal commanded to the VSI. The physics-based model, therefore, includes a DC/DC Boost/Buck converter, interfacing a $96V_{DC}$ battery (8 series-connected 12V Pb-Acid Batteries) to a $450V_{DC}$ nominal intermediate bus. Boost/Buck converter topology is well known and is presented in Figure 20 [24].

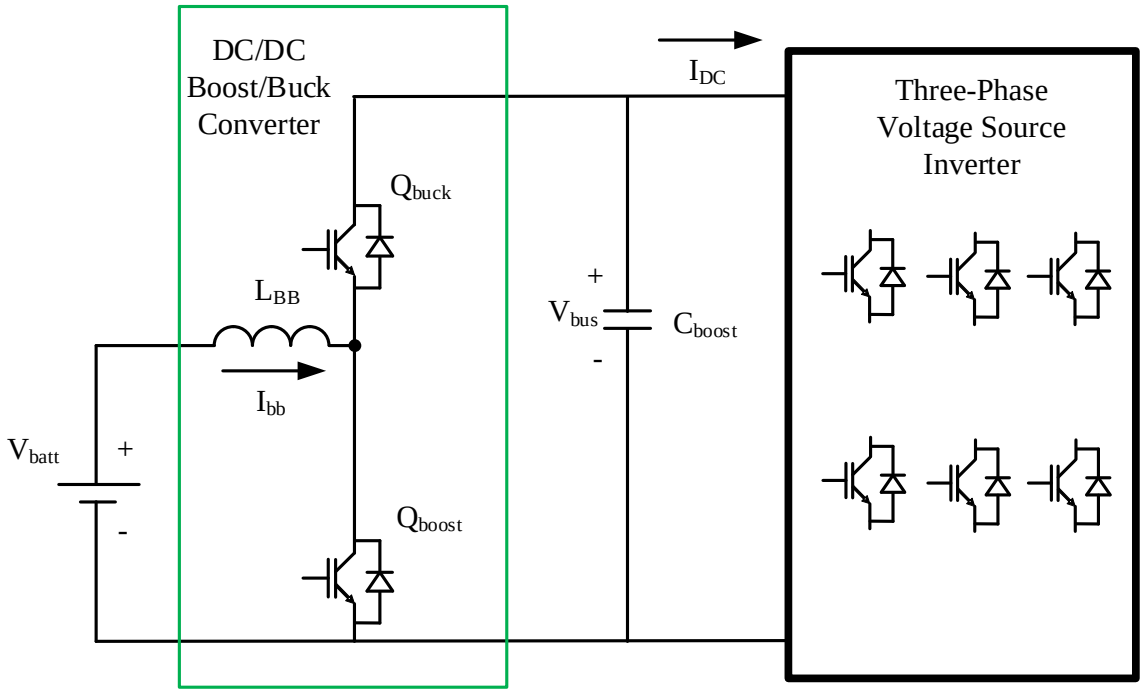

Figure 20. DC/DC Boost/Buck Converter Topology

The controller implementation for the Boost/Buck converter, shown in Figure 21, requires that two converter output parameters are measured, V_{bus} and I_{bb}. The difference between V_{DCref} and V_{bus} is passed through a PI controller and limited to ±0.98; this value is called v_c^*. For stability purposes, I_{bb} is passed through a low pass filter (LPF) and divided by 100, and this is subtracted from v_c^*. Finally, the switching waveform for Q_{buck}/Q_{boost} is determined by comparing the $v_c^*/-v_c^*$ to a sawtooth waveform (between 0 and 1) at the Buck/Boost converter switching frequency, *sw_freqB*.

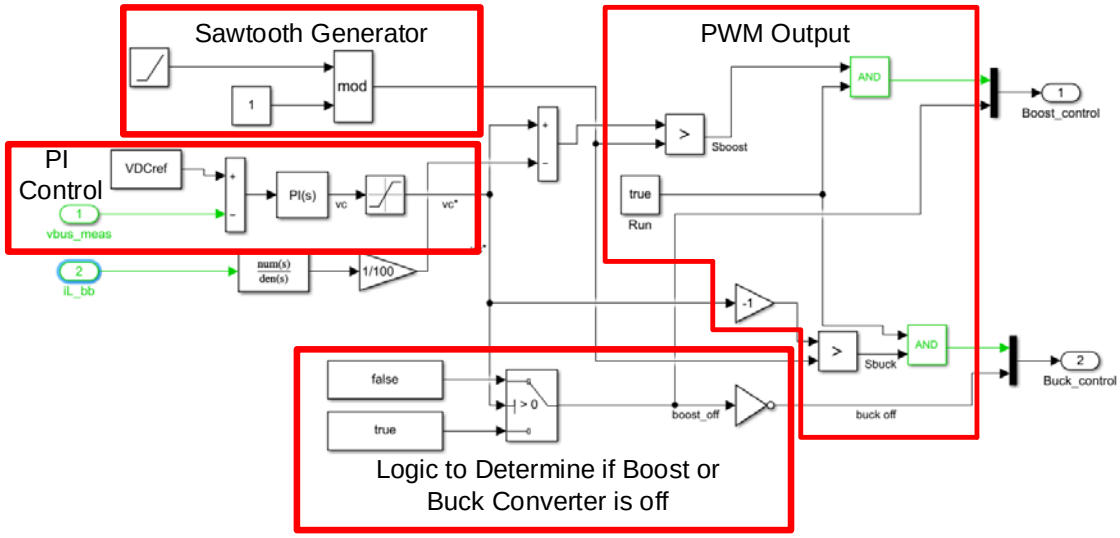

Figure 21. DC/DC Buck/Boost Converter Controller

The DC/DC converter controller interfaces with a mathematical model for the currents and voltages associated with the converter in Figure 20. This general overview is presented in Figure 22. *Boost_control* and *Buck_control* are multiplexed signals of the switching signals for Q_{boost}/Q_{buck} and logic that disables the respective IGBT when the other is in use. I_{BB} is defined in Equation (37). I_{DC} represents the current flowing into the VSI that can be calculated via the power balance shown in Equation (38) [24]. The Buck-current mode block calculates the current, I_{buck_in}, flowing into the battery when Q_{buck} is on, as shown in Equation (39).

$$I_{bb} = I_{L\_Boost} - I_{buck\_in} \tag{37}$$

$$
\begin{aligned}
&P_{DC\_IN} = P_{AC\_OUT} \\
&V_{Bus} I_{DC} = P_{INV_A} + P_{INV_B} + P_{INV_C} \\
&I_{DC} = \frac{v_{AN} i_{INV\_A} + v_{BN} i_{INV\_B} + v_{CN} i_{INV\_C}}{V_{Bus}}
\end{aligned}
\tag{38}
$$

$$
\begin{aligned}
&V_{bus} - V_{batt} = L_{BB} \frac{di_{buck\_in}}{dt} \\
&I_{buck\_in} = \frac{1}{L_{BB}} \int V_{bus} - V_{batt} dt
\end{aligned}
\tag{39}
$$

The Boost-current mode block calculates $V_{bus,}$ as shown in Equation (40).

$$
\begin{aligned}
&I_{BB} - I_{DC} = I_{L\_Boost} - I_{buck\_in} - I_{DC} = C_{boost} \frac{dv_{bus}}{dt} \\
&V_{bus} = \frac{1}{C_{boost}} \int (I_{BB} - I_{DC}) dt
\end{aligned}
\tag{40}
$$

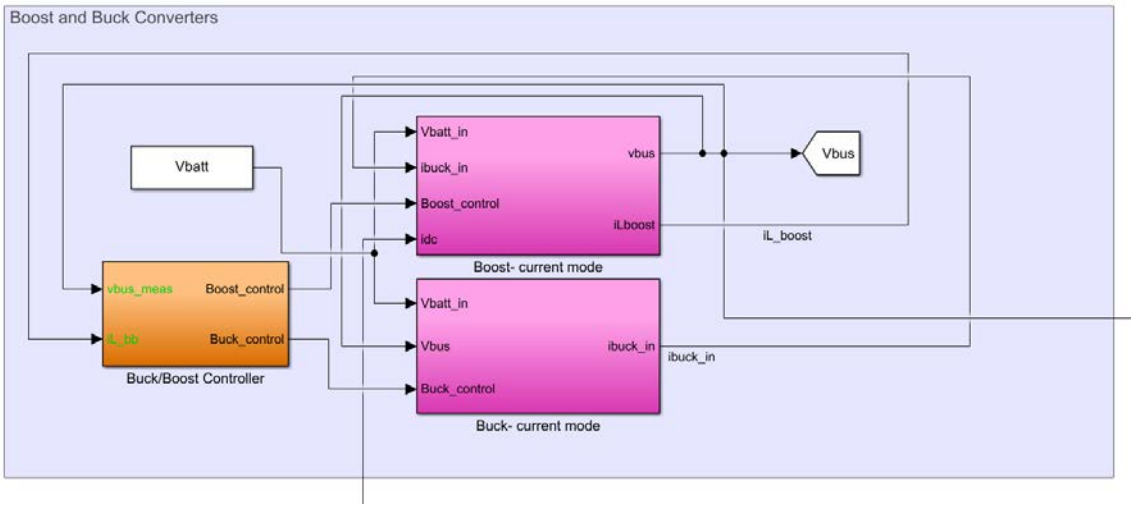

Figure 22. Overview of the Simulink Model for the Buck/Boost Converter

D. THREE-PHASE VSI CONTROL SYSTEM

The control system for the VSI includes the active and reactive power flow controller and the space vector modulation algorithm, which are presented in this section.

1. P-Q Controller

The P-Q controller implemented in the physics-based model is a novel design that seeks to correct the PF of the grid to unity while also allowing the source/generator to slowly adjust to load increases, by commanding the inverter to provide real power in excess of the "moving average" of the real power the generator is supplying. The P-Q controller implemented is presented in Figure 23.

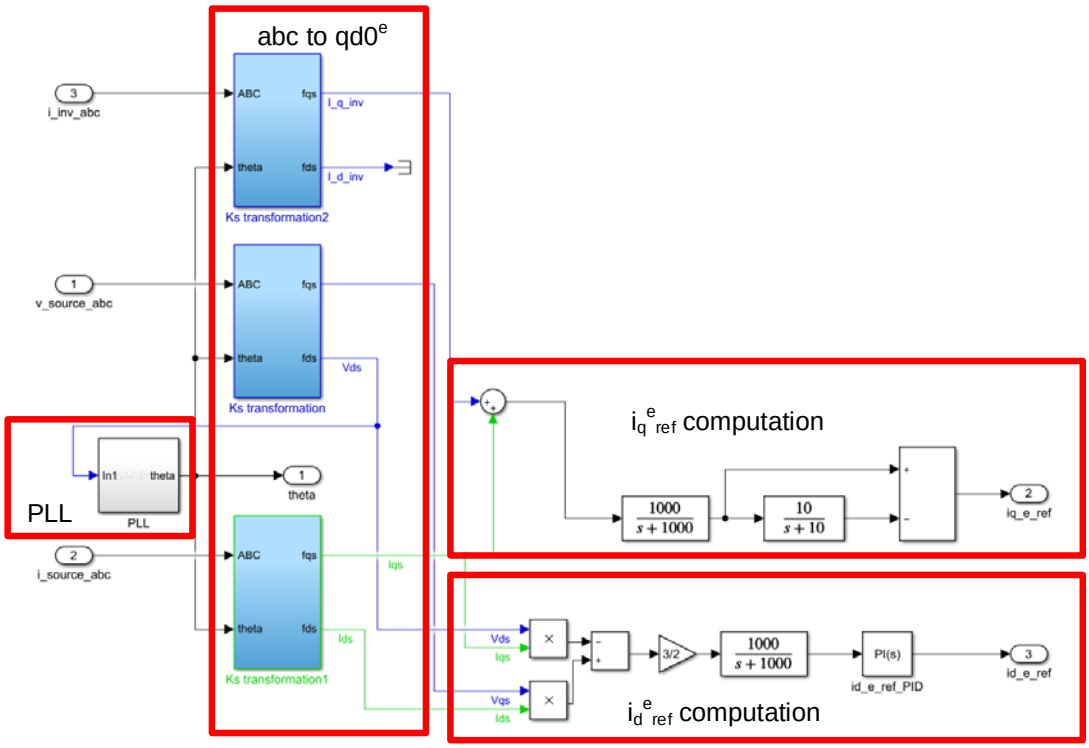

Figure 23. P-Q Controller Implementation in Simulink

The P-Q controller requires that inverter phase currents (*i_inv_abc*), source phase currents (*i_source_abc*), and AC bus phase voltages (in this case, *v_source_abc*) are measured. Once measured, each parameter is converted into the synchronous reference frame, qd0^e, as discussed in Section II.D. A phase-locked-loop (PLL) calculates the angle, θ, per Equation (41), with which the inverter voltage can be synchronized with the grid voltage.

$$\theta = \int \left[(2\pi 60) - V_{d_{source}} (K_p + \frac{K_i}{s}) \right] dt \tag{41}$$

The reactive current command for the inverter, $i_d{}^e{}_{ref}$, is calculated so that the source current is in phase with the source voltage. First, source power is calculated in the $qd0^e$ reference frame by (42). The LPF at 1000 rad/s is present throughout the model to filter out high-frequency components that exist due to noise. The resulting Q_{source} is passed through a PI controller with a reference of 0VAR. The resulting current command $i_d{}^e{}_{ref}$, is adjusted until Q_{source} equals zero.

$$Q_{source} = \frac{3}{2}\left(V_{qs} I_{ds} - V_{ds} I_{qs} \right) \tag{42}$$

The real current command for the inverter, $i_q{}^e{}_{ref}$, is calculated, such that the high-frequency currents are sent to the inverter, thus maintaining the low-frequency components to the source. A similar technique was employed by Oriti et al. [25], when they allowed a supercapacitor to supply the high-frequency current in a single-phase microgrid with multiple DERs (solar panel, battery, and supercapacitors). This controller differs, however, in that the current command is based on the total current flowing from the VSI and the source. Equations (43)-(45) demonstrate how the $i_q{}^e{}_{ref}$ is developed. The low pass filter, centered at 10 rad/s, in Equation (44), can be adjusted higher or lower to tune how quickly the source is allowed to respond. Note that the subscript "s" stands for source

$$i_q{}^e{}_{total} = i_q{}^e{}_{inv} + i_q{}^e{}_s \tag{43}$$

$$i_q{}^e{}_{total\_avg} = i_q{}^e{}_{total} \left[\frac{10}{s+10} \right] \tag{44}$$

$$i_q{}^e{}_{ref} = i_q{}^e{}_{total} - i_q{}^e{}_{total\_avg} \tag{45}$$

2. Space Vector Modulation

To produce the switching signals for the IGBTs in the VSI, space vector modulation is utilized. In SVM, the switching states are determined by the location of a reference

stationary reference frame voltage vector within a hexagon that represents the possible switching states of a VSI. This hexagon is presented in Figure 24, where the switching states are shown in parenthesis. In Figure 24, the reference vector V_{ref} has projections onto the "pnn" state (V_1) and "ppn" state (V_2). A given state, "ppn" for example, refers to the fact that the phase A and B top IGBTs are switched on ($V_{an}=V_{bn}=V_{dc}/2$), connecting them to the positive DC bus, and the bottom IGBT on phase C is switched on, connecting it to the negative DC bus ($V_{cn}=-V_{dc}/2$) [23]. Switching states "ppp" and "nnn" represent the zero states in the center of the hexagon, when all IGBTs are connected to the positive or negative DC bus, respectively. The IGBT location is shown in Figure 18.

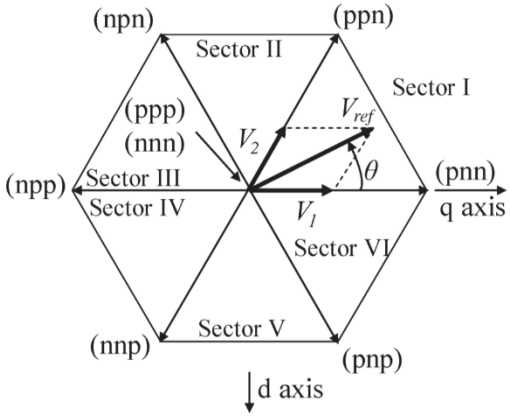

Figure 24. Space Vector Hexagon. Source [23].

The projections of V_{ref} onto the respective switching state positions determine the amount of a switching period is spent in a given state. Equations (46)-(48) show how the times in a given state are calculated [23]. T_x, T_y, and T_0 represent the amount of time spent on the switching states of V_1, V_2, and zero, respectively. Additionally, T_s is the switching period, and the maximum vector length is $2/3V_{DC}$ [23]. The maximum vector would be when V_{ref} lies entirely on a single switching state with a length measured from the origin to the hexagon edge.

$$T_x = \frac{3}{2}\frac{V_1 T_s}{V_{DC}} \tag{46}$$

$$T_y = \frac{3}{2}\frac{V_2 T_s}{V_{DC}} \tag{47}$$

$$T_0 = T_s - T_x - T_y \tag{48}$$

The law of sines produces the relationship in Equation (49), which then modifies Equations (46)-(47) to those shown in Equations (50)-(51) [23].

$$\frac{2V_{ref}}{\sqrt{3}} = \frac{V_1}{\sin(\frac{\pi}{3} - \theta)} = \frac{V_2}{\sin(\theta)} \tag{49}$$

$$T_x = \frac{V_{ref}\sqrt{3}}{V_{DC}} T_s \sin(\tfrac{\pi}{3} - \theta) \tag{50}$$

$$T_y = \frac{V_{ref}\sqrt{3}}{V_{DC}} T_s \sin(\theta) \tag{51}$$

The implementation of SVM for the physics-based model is shown in Figure 25. Determining the time that a given switch must be on requires that the reference voltage vector in the stationary reference frame is calculated. The current PI controller in Figure 25 uses the angle, θ, currents $i_q{}^e{}_{ref}$ and $i_d{}^e{}_{ref}$, and inverter currents i_{abc} to calculate the reference voltage projections onto the q and d axes. Inside the current PI controller, i_{abc} is transformed into the synchronous reference frame via Equation (18). Following that, $v_q{}^e$ and $v_d{}^e$ are calculated, as shown in Equations (52)-(53).

$$v_q{}^e = \left(i_q{}^e{}_{ref} - i_q{}^e\right)\left(K_p + \frac{K_i}{s}\right)\left(\frac{\sqrt{3}}{V_{DC}}\right) \tag{52}$$

$$v_d{}^e = \left(i_d{}^e{}_{ref} - i_d{}^e\right)\left(K_p + \frac{K_i}{s}\right)\left(\frac{\sqrt{3}}{V_{DC}}\right) \tag{53}$$

The variables $v_q{}^e$ and $v_d{}^e$ are next converted to $v_q{}^s$ and $v_d{}^s$ in the stationary reference frame, via the transformation in Equation (54) [20].

$$\begin{bmatrix} v_q^{\ s} \\ v_d^{\ s} \end{bmatrix} = \begin{bmatrix} \cos(\theta^e) & \sin(\theta^e) \\ -\sin(\theta^e) & \cos(\theta^e) \end{bmatrix} \begin{bmatrix} v_q^{\ e} \\ v_d^{\ e} \end{bmatrix} \tag{54}$$

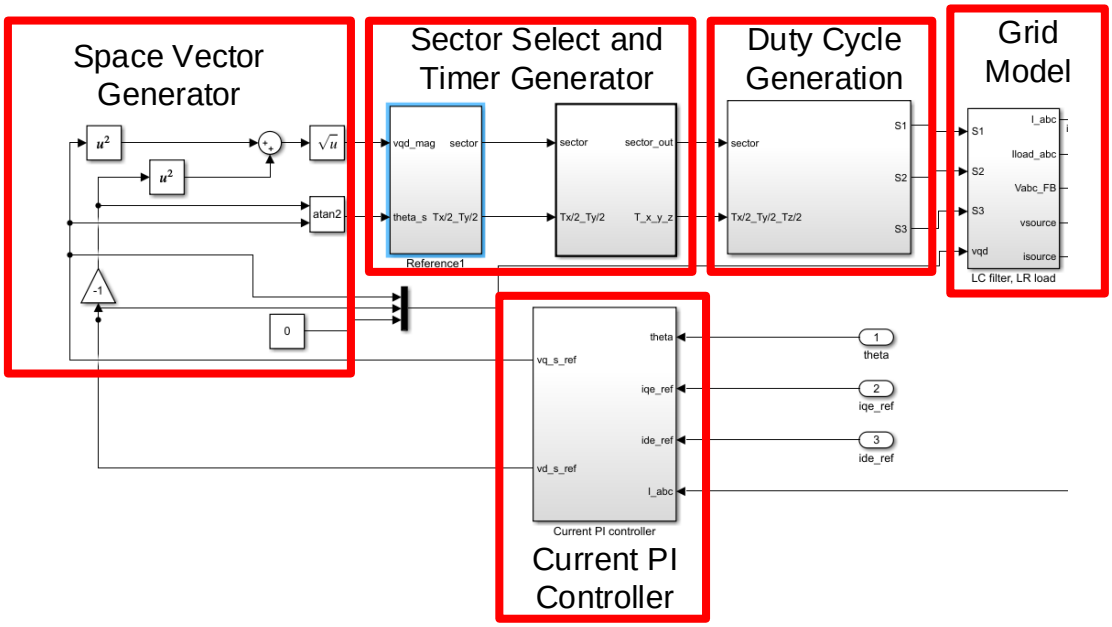

Figure 25. Space Vector Modulation Implementation Overview

Following the current PI controller, the vector V_{ref}, as defined in Figure 24, is calculated per Equation (55).

$$\begin{aligned} V_{ref} &= V_{qd}^{\ s} \\ \left|V_{ref}\right| &= \sqrt{\left(v_q^{\ s}{}_{ref}\right)^2 + \left(-v_d^{\ s}{}_{ref}\right)^2} \\ \theta^s &= \angle V_{ref} = \tan^{-1}\left(\frac{-v_d^{\ s}{}_{ref}}{v_q^{\ s}{}_{ref}}\right) \end{aligned} \tag{55}$$

The model then selects the sector in which V_{ref} lies based on the angle, θ^s, and determines the timers spent in a given state, based on that sector, per Equations (56)-(58).

$$\frac{T_x}{2} = \left|V_{qd}^{\ s}\right| \frac{T_s}{2} \sin\left(\tfrac{\pi}{3} - \theta^s\right) \tag{56}$$

$$\frac{T_y}{2} = \left|V_{qd}{}^s\right| \frac{T_s}{2} \sin(\theta^s) \tag{57}$$

$$\frac{T_0}{2} = \left(\frac{T_s}{2}\right) - \left(\frac{T_x}{2}\right) - \left(\frac{T_y}{2}\right) \tag{58}$$

The half-switching-periods values are calculated due to generating the gate signals per the lookup table in Figure 26, with the only difference that $T_1 = T_x$ and $T_2 = T_y$.

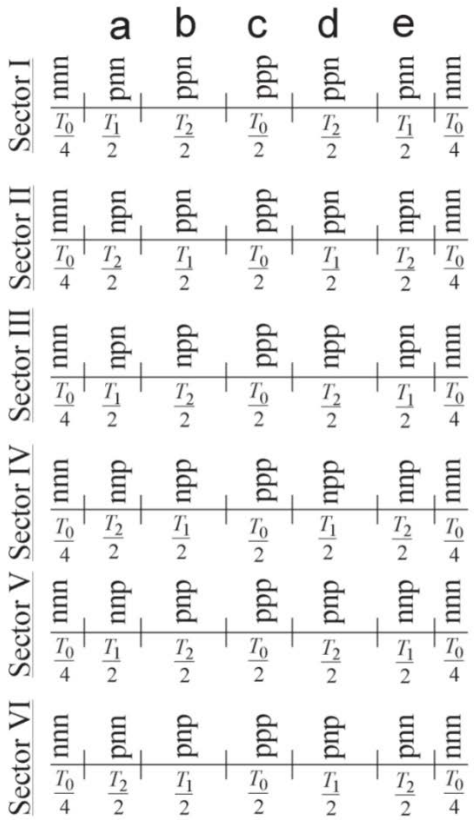

Figure 26. Switching Sequence by Sector. Source: [23].

The duty cycle for a given switch can then be calculated by looking at the sector and determining how long an AC phase is connected to either the positive or negative DC bus. An example of the duty cycle calculation for Sector I, phase A top/bottom switches, is shown in Equation (59).

$$D_{A_{top}} = \frac{1}{T_s}\left(\frac{T_0}{2} + 2\frac{T_x}{2} + 2\frac{T_y}{2}\right)$$
$$D_{A_{bottom}} = \frac{1}{T_s}\left(\frac{T_0}{2}\right) \tag{59}$$

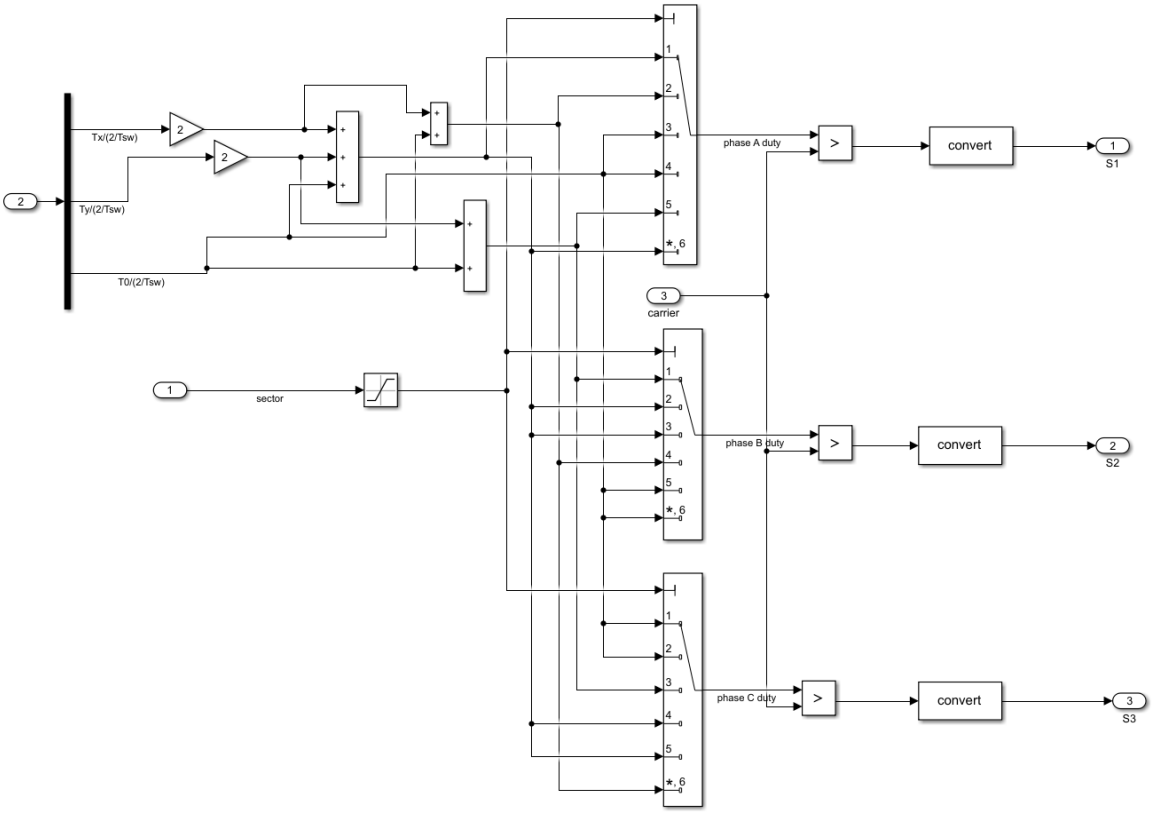

Figure 27. Duty Cycle/Switching Signal Generation

IV. SIMULATION RESULTS

The physics-based model described in Chapter III was used to simulate the performance of the VSI controller in five different scenarios. Type I $200V_{rms}$ power was used for a multi-step load profile, with both the ideal VSI case and the PWM VSI case. Additionally, a multi-step load profile with Type I $440V_{rms}$ power was simulated with an ideal VSI, as it is likely that a Type I $440V_{rms}$ would be used for pulsed load in excess of 50kW. Additionally, for comparison purposes, the effect of the LPF, described in Equation (44), centered at 10rad/s and 1 rad/s and is explored for the Type I $200V_{rms}$ ideal case.

A. MULTI-STEP LOAD PROFILE FOR TYPE I $200V_{RMS}$ POWER

The multi-step load profile simulates a wye-connected load with resistances and inductances, as shown in Table 2. The resulting load pulses are 1% of those in Figure 11 from [13]. This profile was chosen because the load changes, in some instances, exceed the requirements of [13]. As a result, if the proposed controller can perform according to the specification in MIL-STD-1399-300 under these conditions, it can perform well for loads compliant with [13].

1. Ideal VSI, LPF at 10 rad/s

Figure 28 and Figure 29 represent the real and reactive power, respectively, for the ideal VSI case, with the LPF at 10 rad/s. Figure 28 shows that the inverter is taking the initial jump in real power, but that the within 0.5s, the source begins powering the majority of the real power of the load. At each step, the reactive power has a minimal effect on the source, but the inverter is supplying nearly all reactive power through the load profile, as designed.

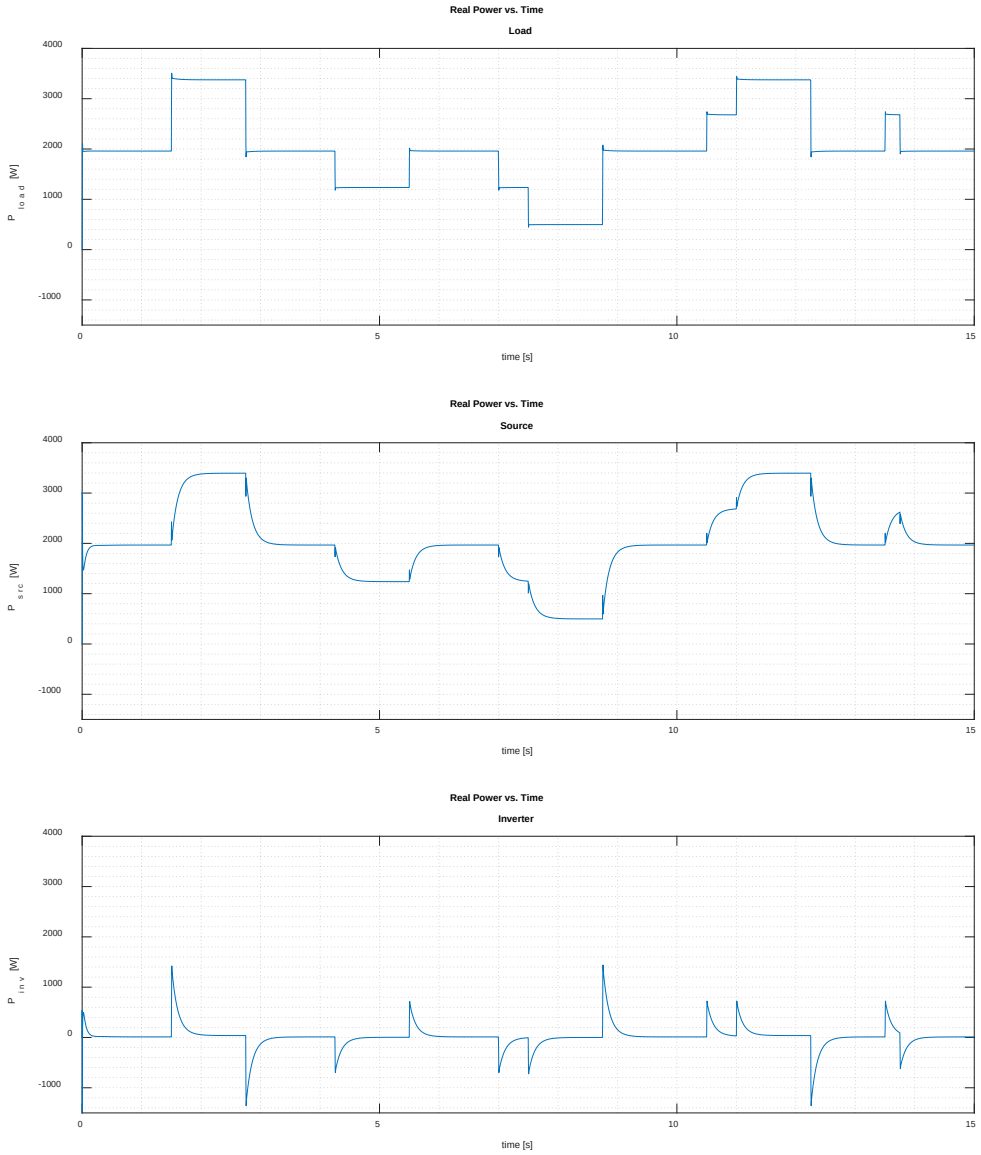

Figure 28. Multi-Step Simulated Real Power versus Time, 200V_{rms}, Ideal VSI

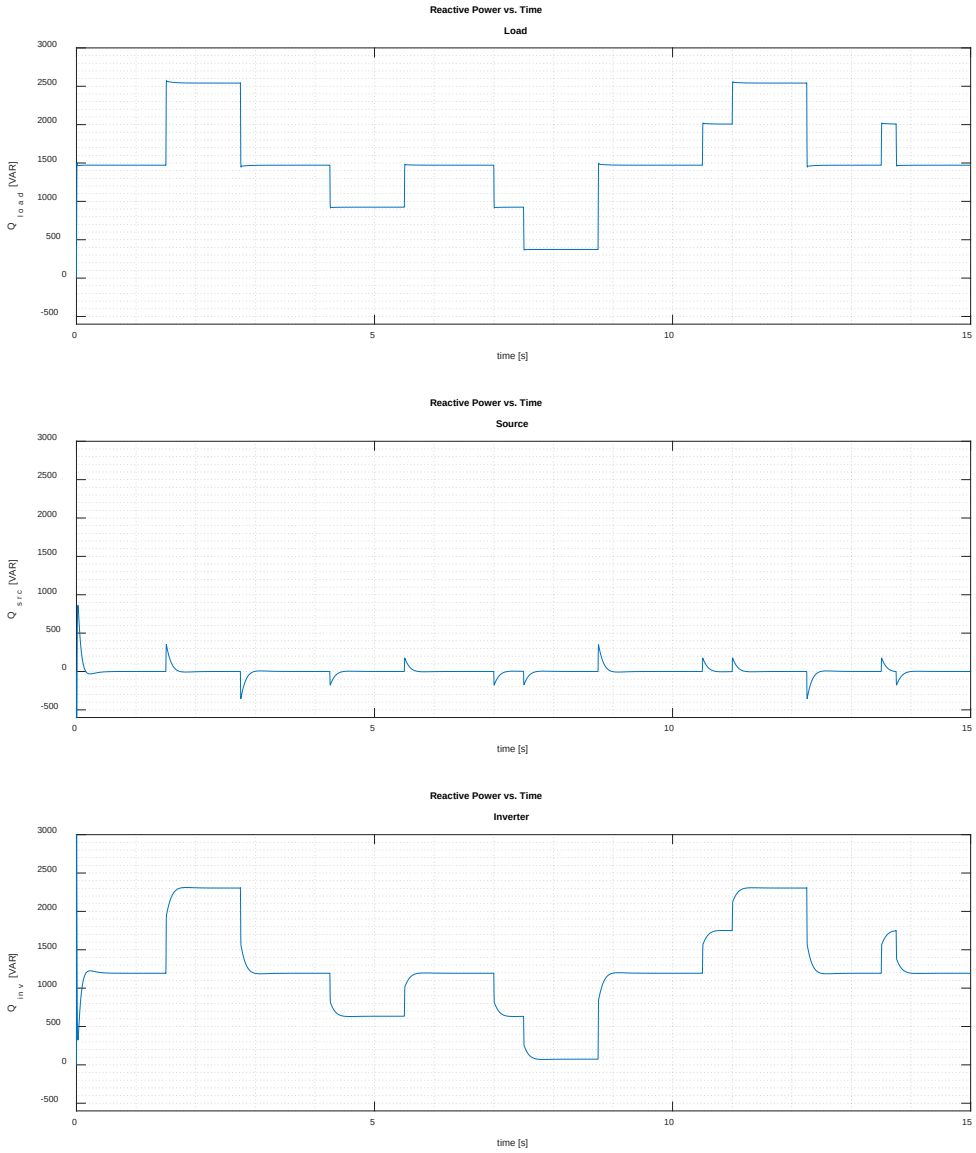

Figure 29. Multi-Step Simulated Reactive Power versus Time, 200V_{rms}, Ideal VSI

Figure 30 and Figure 31 show the load, inverter, and source currents versus time for a step load increase, and a step load decrease, respectively. Of note in each picture, at the step, there is a slight distortion on the source current, but in general, it stays at the same peak-to-peak value, indicating the source power is not immediately changing. Transients

on the source at 1.501s and 1.502s are labeled. The inverter in each case is, however, changing quickly to accommodate the steps in load. Additionally, in Figure 31, the phase marked in yellow for the load at 2.779 seconds is nearly in phase with the source at 2.777 seconds. The same phase on the inverter at 2.775 is nearly 180 degrees out of phase with the source and the load. This indicates that, as expected, current is flowing from the grid to the DC bus (AC/DC conversion through the VSI).

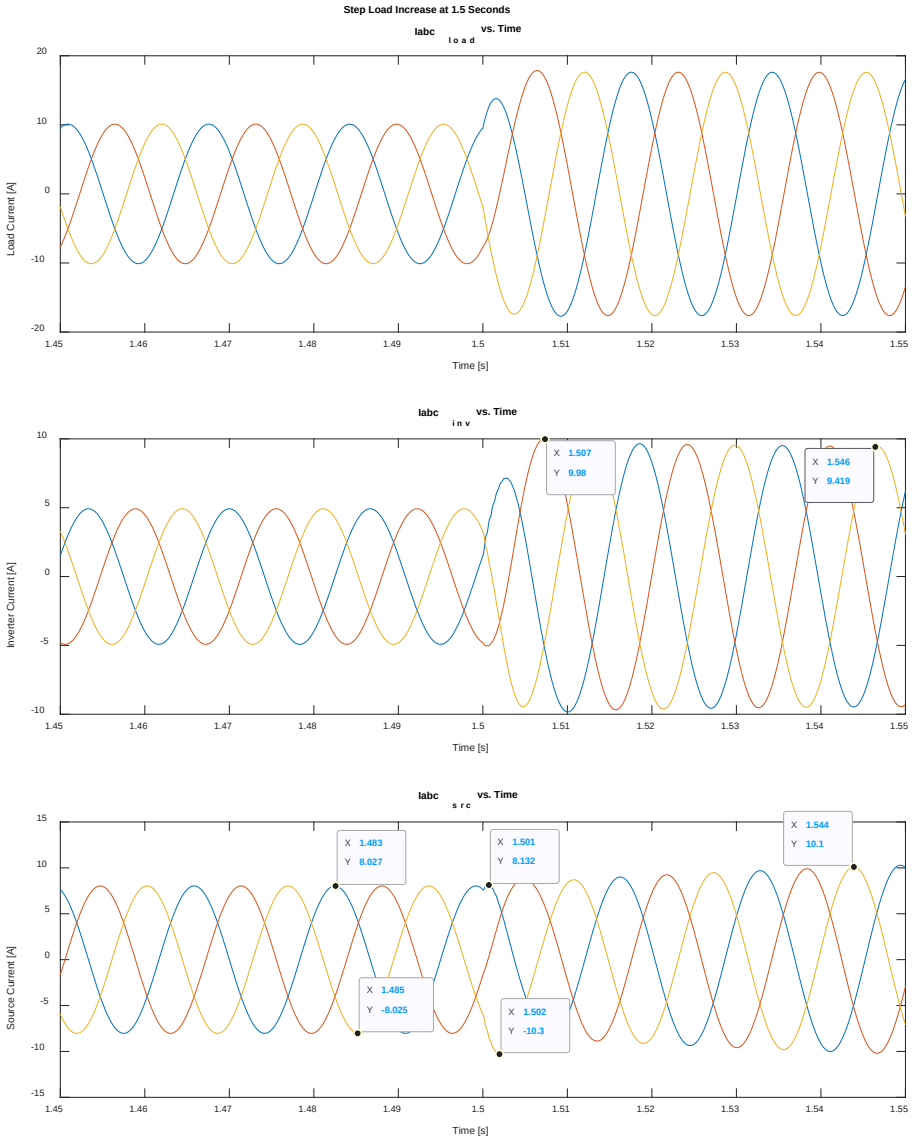

Figure 30. Step Increase at 1.5s - Simulated Current versus Time, 200V_{rms}, Ideal VSI

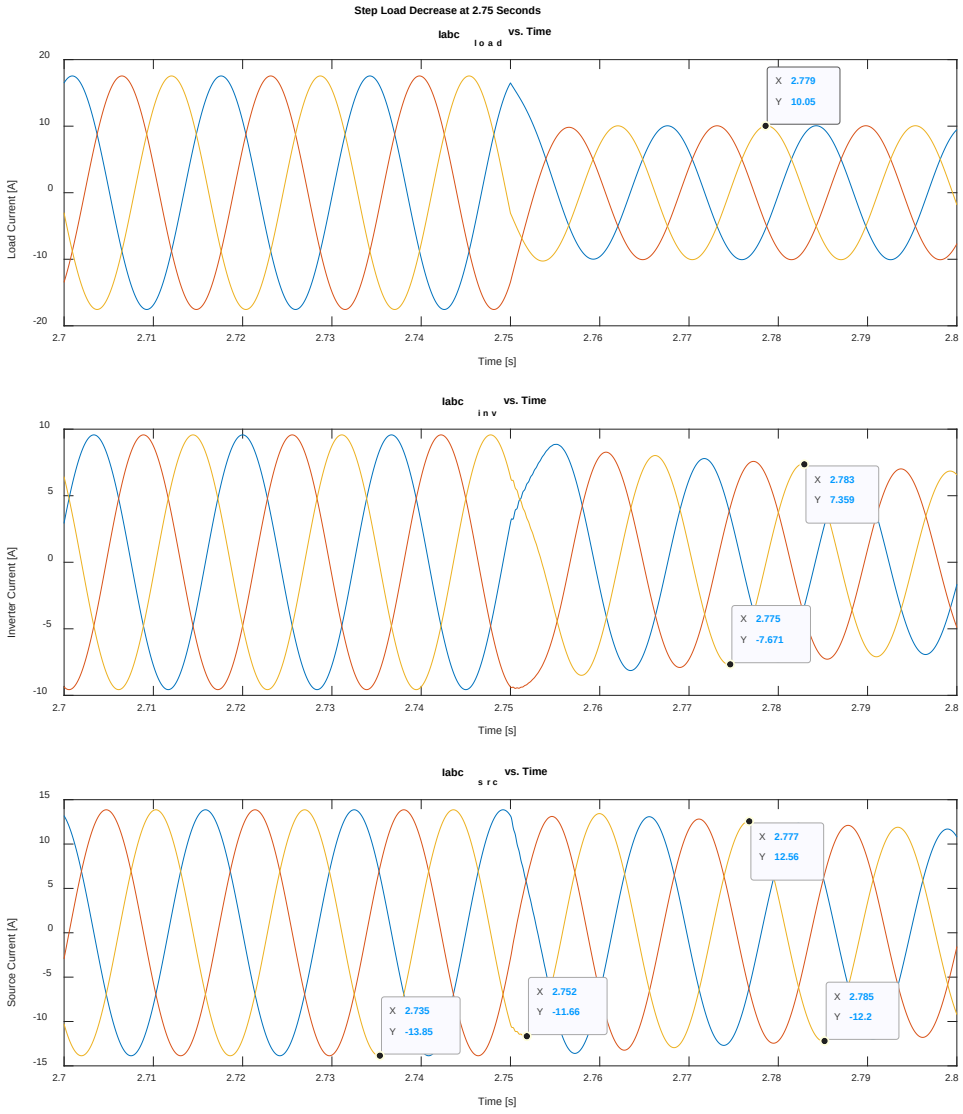

Figure 31. Step Decrease Simulated Currents versus Time, 200V_{rms}, Ideal VSI

Figure 32 demonstrates how PF correction is occurring. Source voltage and current are marked at three distinct times in the first 0.15 seconds of the simulation. In the beginning, the voltage leads the current by 0.00132 seconds. This equates to approximately 28.5 degrees of a cycle or a power factor of 0.88. Seven cycles later, the voltage leads the current by approximately 0.0001 seconds (2.2 degrees), or a power factor of 0.999. In fact,

when a more accurate analysis is done, as shown in the code of Appendix A.1, the displacement power factor (DPF) is calculated to be 1.000. Figure 33 further demonstrates that later in the simulation, despite a step, source voltage and current remain nearly in phase.

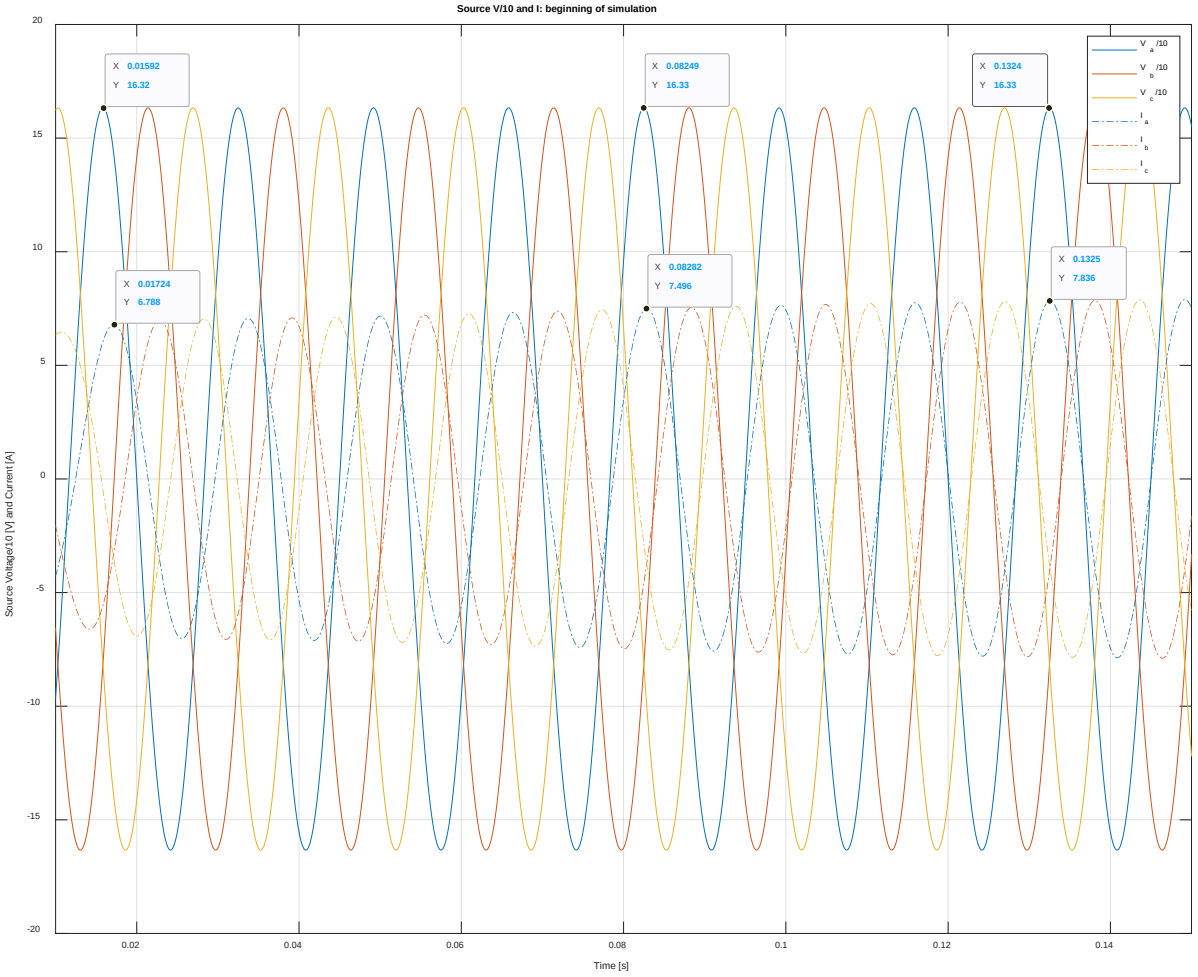

Figure 32. Simulated Source V/10 and Current versus Time, 200V_{rms}, Ideal VSI, Beginning

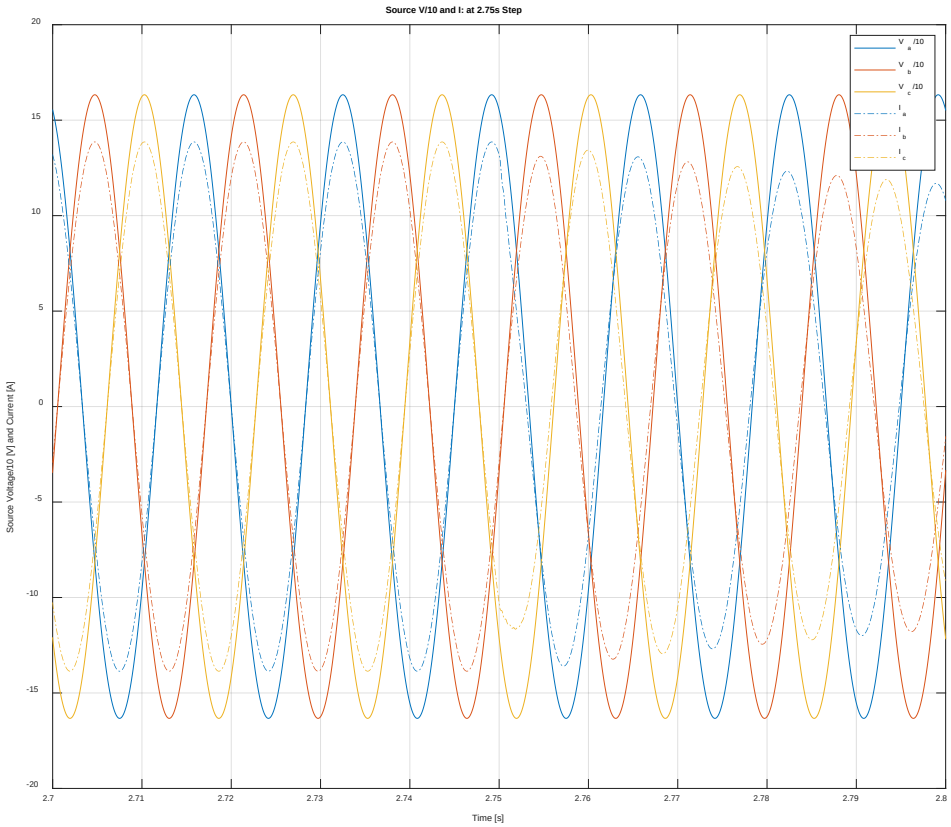

Figure 33. Multi-Step Simulated V/10 and Current versus Time, $200V_{rms}$, Ideal, 2.75s Step

For the final cycle of the simulation, an analysis was done on the voltage and current spectra. The resulting spectra are shown in Figure 34 and Figure 35. As expected for the ideal case, there is no harmonic distortion on the voltage or current waveforms, and the peak value occurs at 60Hz, the fundamental frequency.

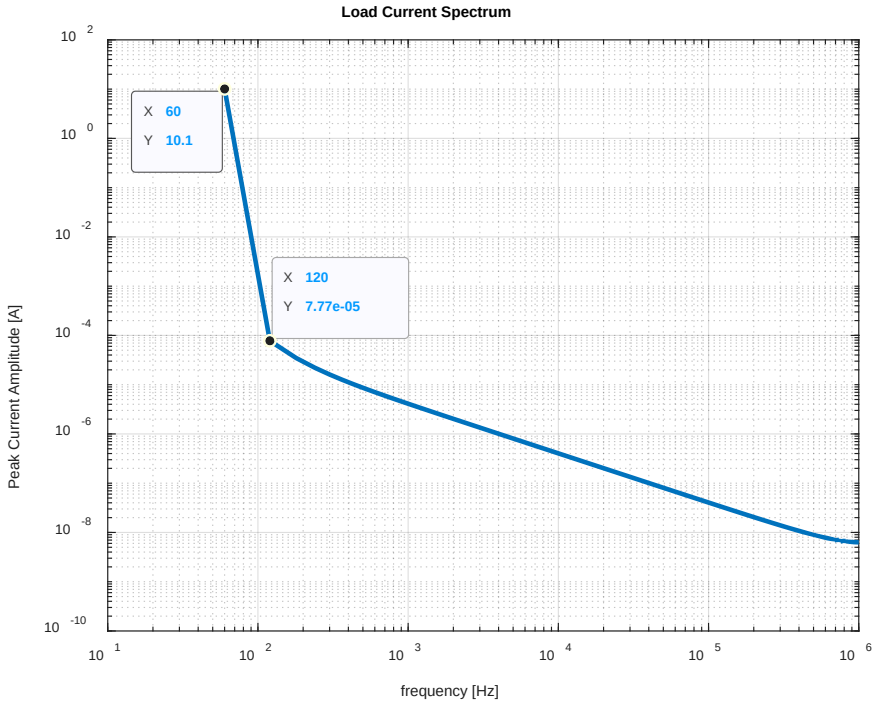

Figure 34. Multi-Step Simulated Load Current Spectrum, 200V_{rms}, Ideal

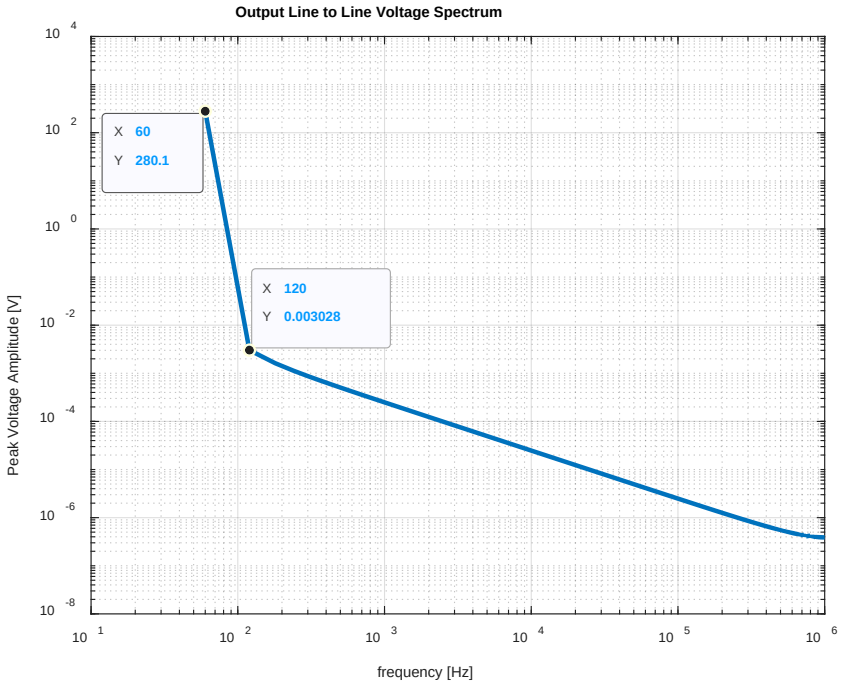

Figure 35. Multi-Step Simulated Load V_{LL} Spectrum, 200V_{rms}, Ideal

Figure 36 demonstrates how DC bus voltage changes throughout the simulation. The DC/DC converter is appropriately sized to maintain nearly 450V_{DC} with minimal ripple.

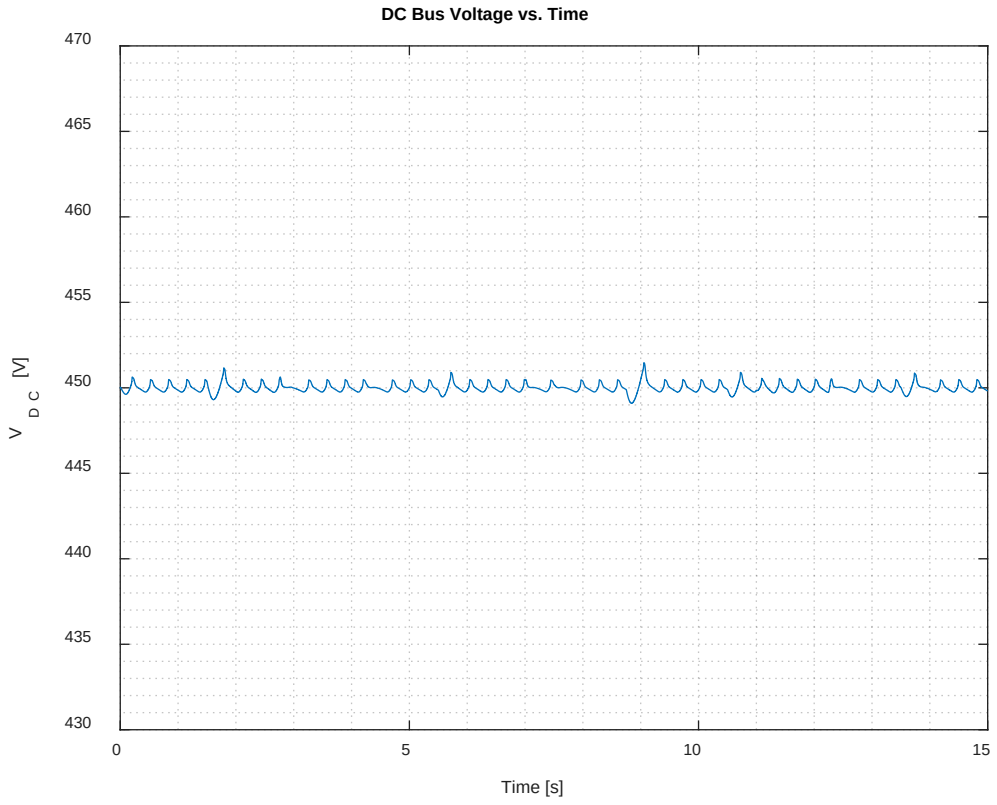

Figure 36. Multi-Step DC Bus Voltage versus Time, Ideal

2. Ideal VSI, LPF at 1 rad/s

Figure 37 and Figure 38 provide a direct comparison to Figure 28 and Figure 29. The only difference is that for Figure 37and Figure 38, the LPF generating $i_q{}^e{}_{total\_avg}$ is centered at 1 rad/s instead of 10 rad/s. At this frequency, the source responds much more slowly to changes in loading. The inverter can successfully power the grid or absorb power from the grid to allow the source to change its load over the course of 1-2 seconds. This demonstrates the with the LPF centered at a lower frequency, a generator would be more easily able to respond within any mechanical limits

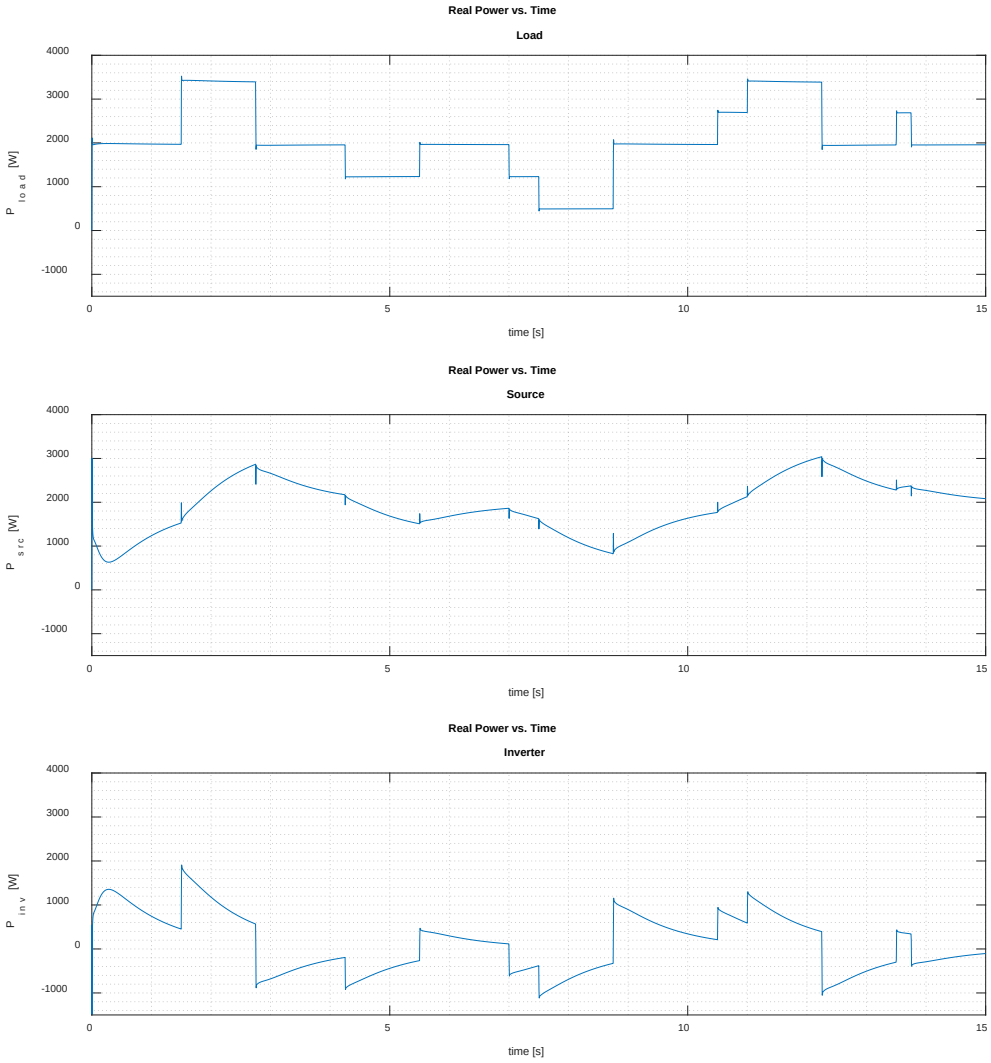

Figure 37. Multi-Step Simulated P versus Time, 200V_{rms}, Ideal, LPF 1rad/s

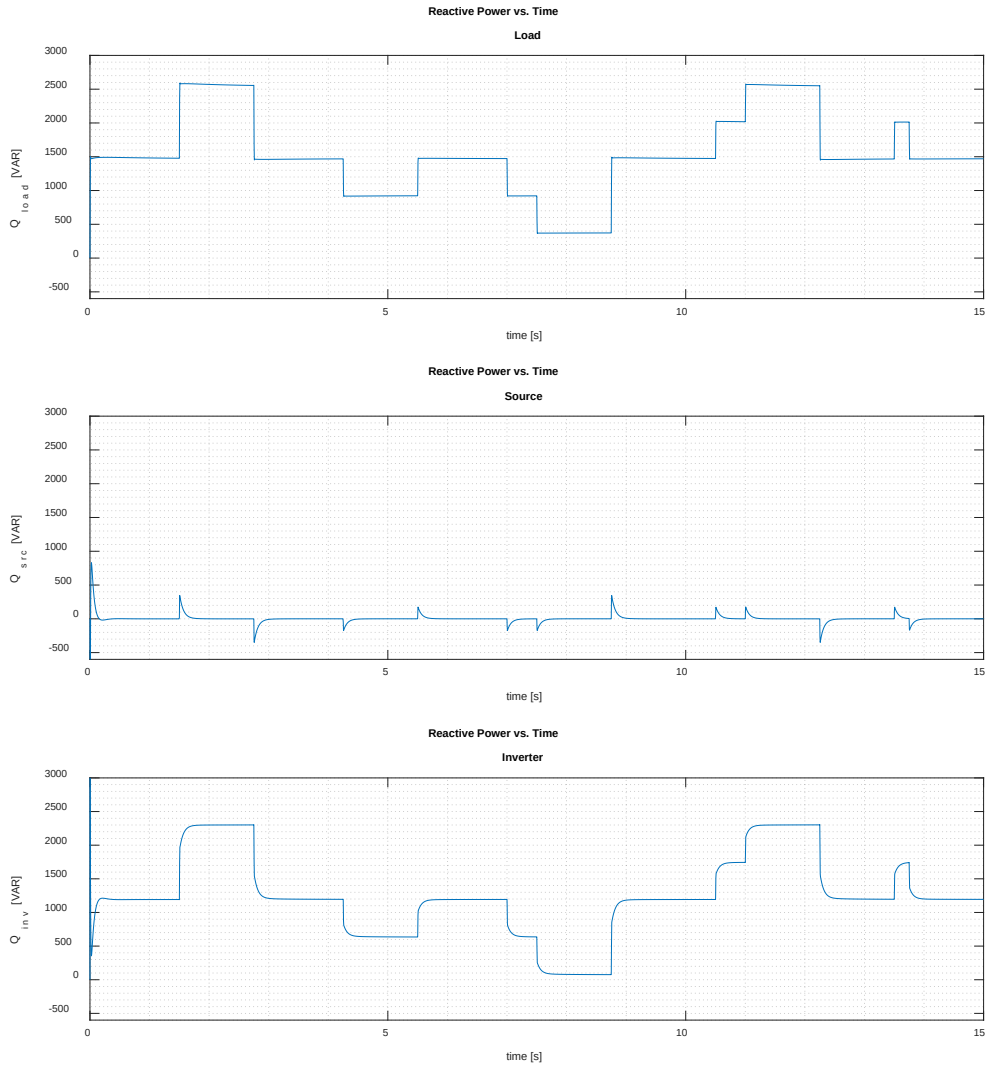

Figure 38. Multi-Step Simulated Q versus Time, 200V_{rms}, Ideal, LPF 1 rad/s

3. PWM VSI

For the simulations with PWM VSI, only the 10 rad/s LPF results are compared. An analysis of the final cycle of the simulation reveals that the total harmonic distortion is 1.35%, and the displacement power factor is again 1.000. The THD is within the limit of [13], and the grid power factor has again been corrected to unity. Figure 39 through Figure

46 can be directly compared and contrasted with Figure 28 through Figure 36. Notable differences between the real and ideal cases are discussed.

Figure 39 shows that due to simulating the switching on the VSI, and the effect of that switching on the DC bus, there are some visible ripples in the real power of the inverter and load. Additionally, some noise can be seen on the reactive power versus time plot, Figure 40.

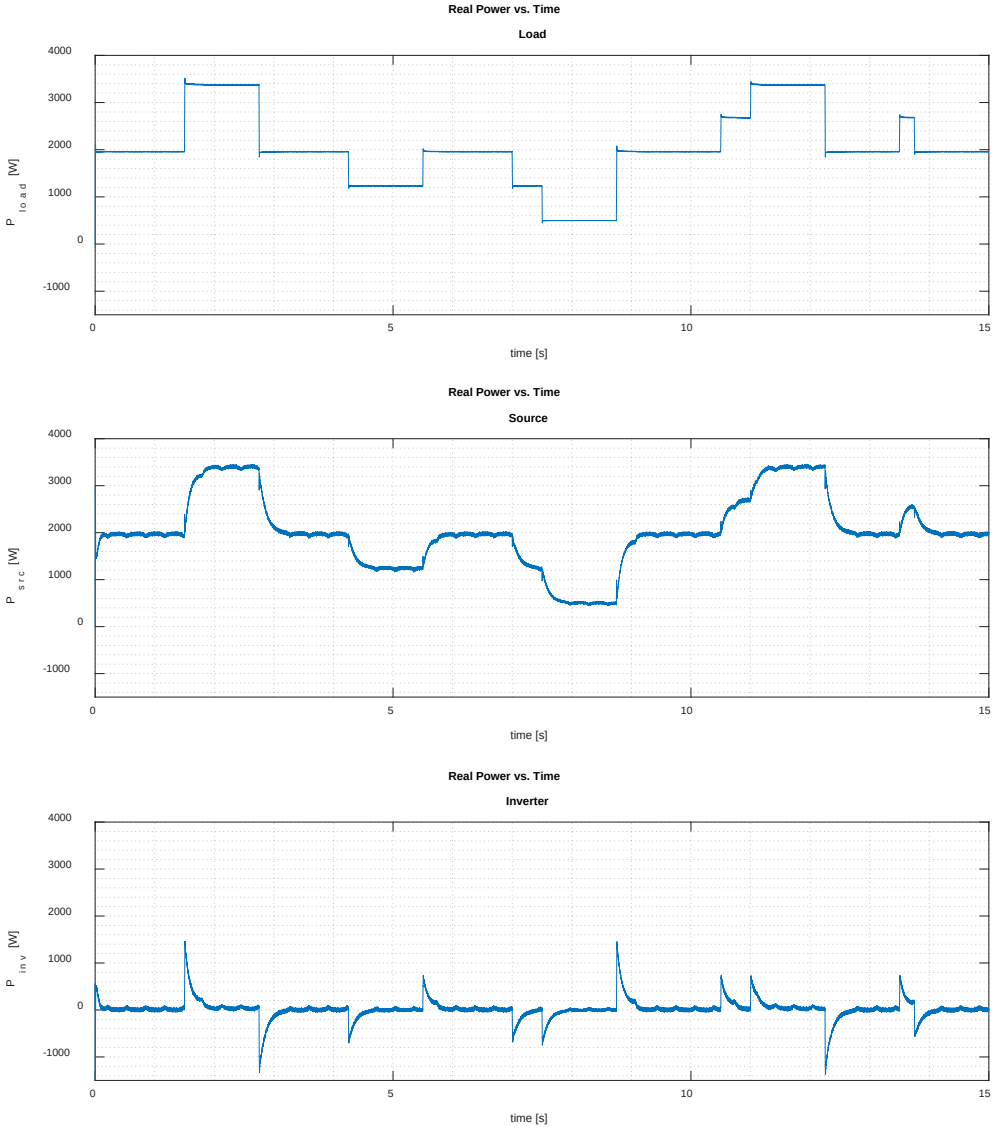

Figure 39. Multi-Step Simulated Real Power versus Time, 200V_{rms}, PWM VSI

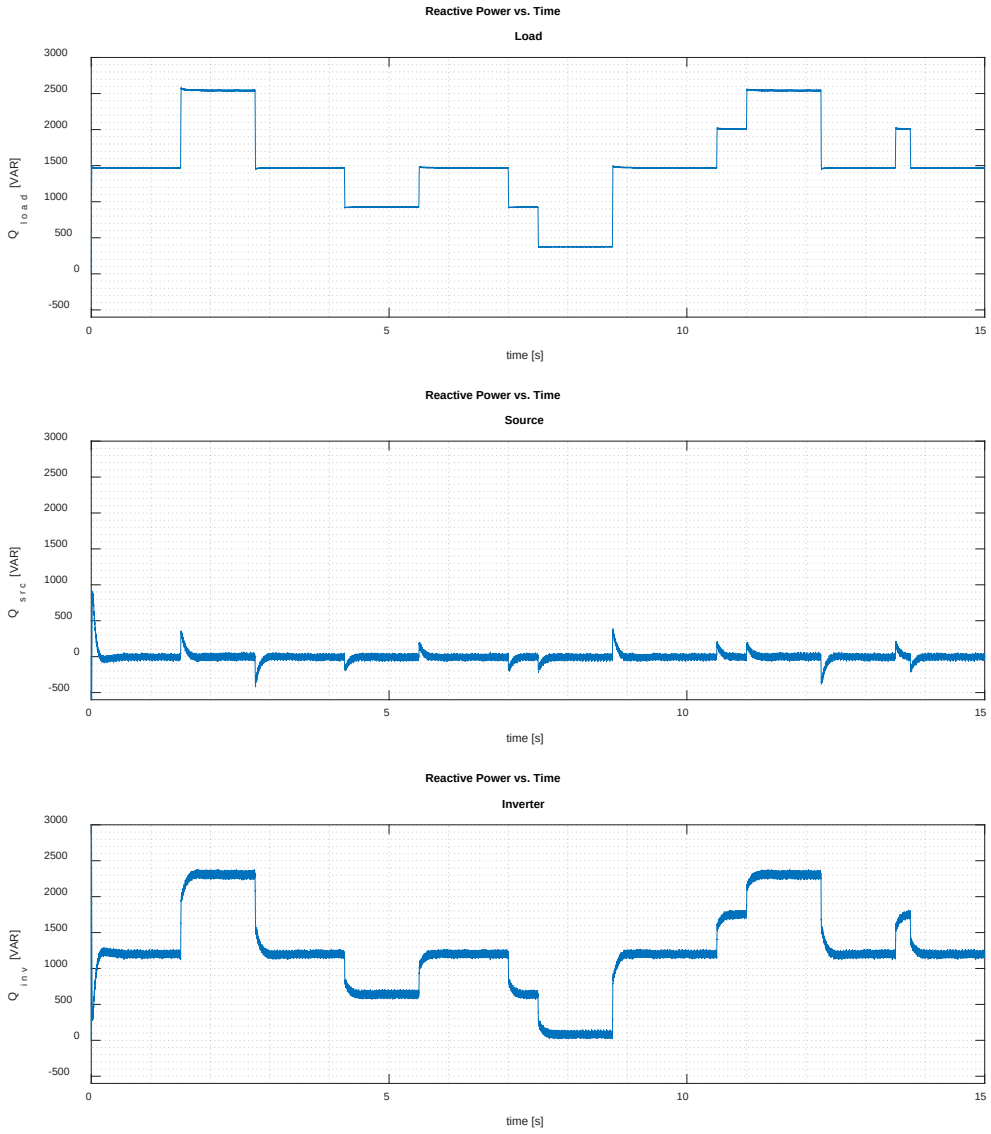

Figure 40. Multi-Step Simulated Reactive Power versus Time, $200V_{rms}$, PWM

Figure 41 demonstrates PF correction, similar to Figure 32. As was previously discussed, the P-Q controller corrected the DPF to unity, just as it did in the ideal case.

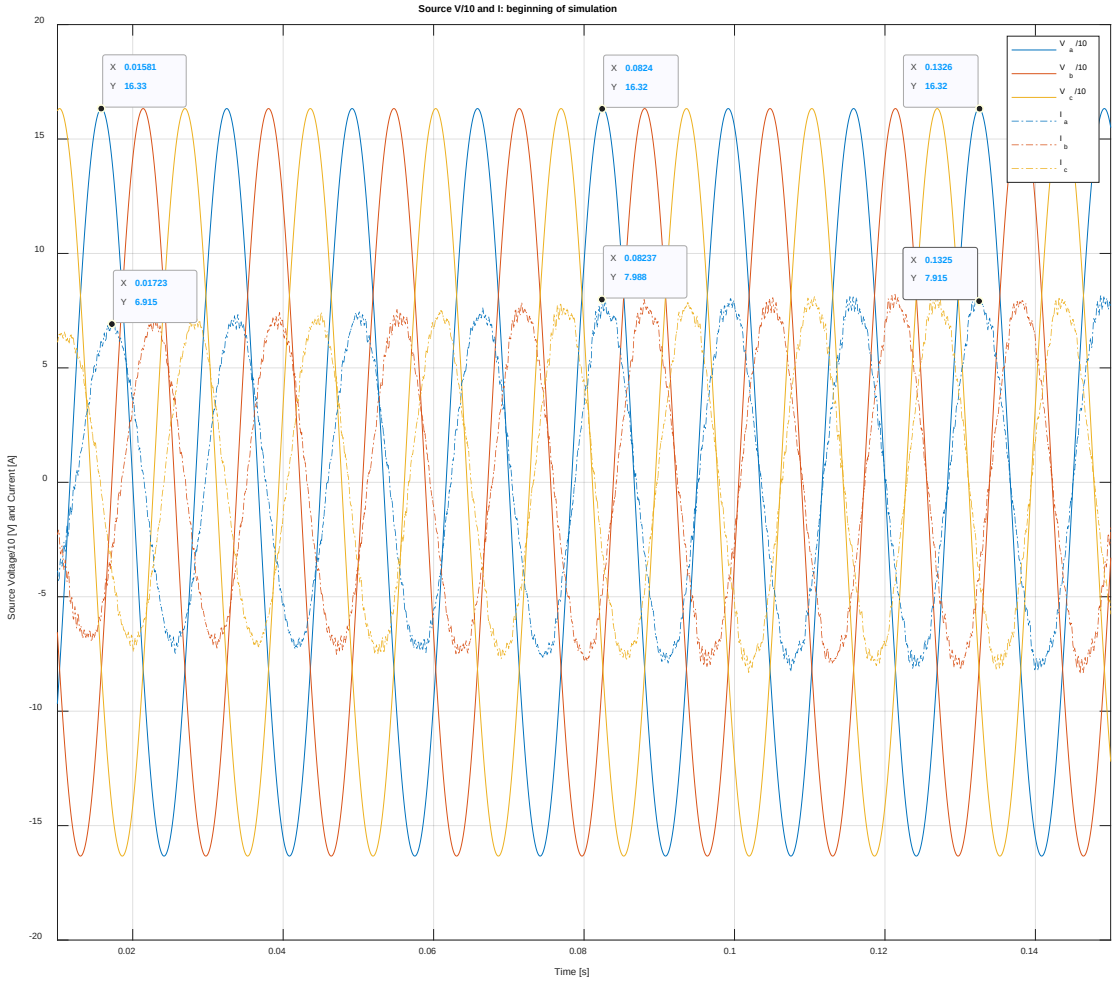

Figure 41. Multi-Step Simulation, V/10 and Current versus Time, 200V_{rms}, PWM, Beginning

Figure 42 and Figure 43 show that there is some harmonic distortion on the phase currents and voltages. At each step listed in the figures, there is again a negligible transient on the phase voltage, meeting the requirement of voltage transient tolerance in [13]

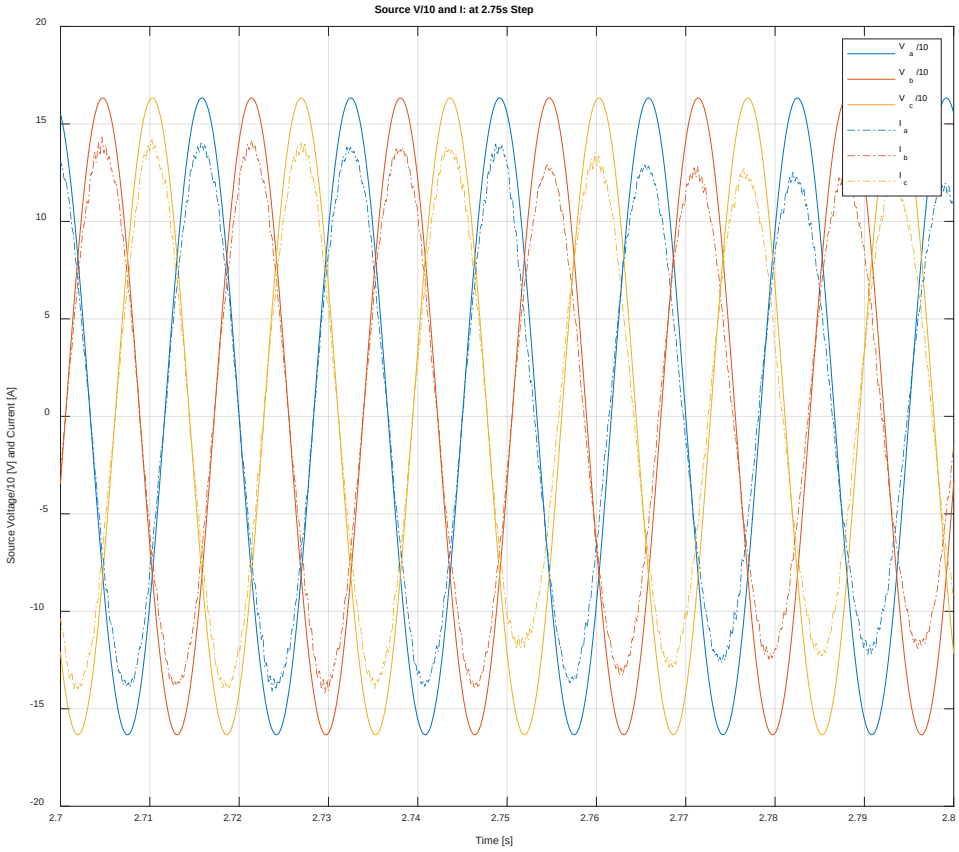

Figure 42. Multi-Step Simulated V/10 and Current versus Time, 200V_{rms}, PWM, 2.75s Step

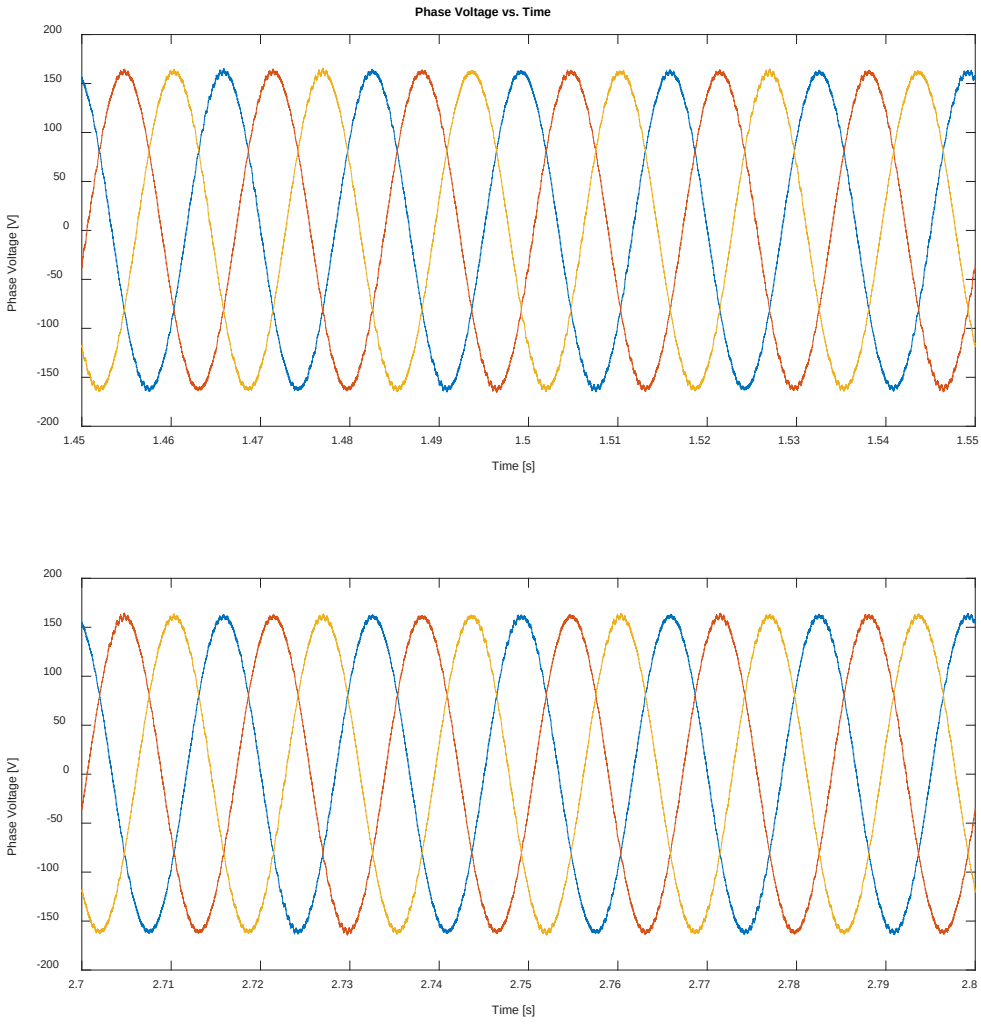

Figure 43. Multi-Step Simulated AC V_{PH} versus Time for First and Second Load Steps, 200V_{rms}, PWM

With real switching, Figure 44 and Figure 45, demonstrate harmonic distortion of the voltage and current waveforms. Voltage THD is 1.35%, with a notable harmonic around the switching frequency (10kHz). Overall, THD is within the specification of 5% maximum THD and no single harmonic THD above 3%, as shown in Table 1.

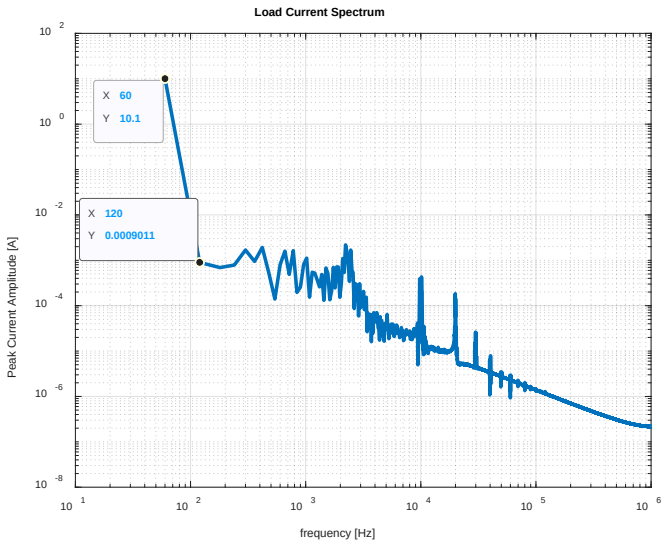

Figure 44. Multi-Step Simulated Load Current Spectrum, 200V_{rms}, PWM

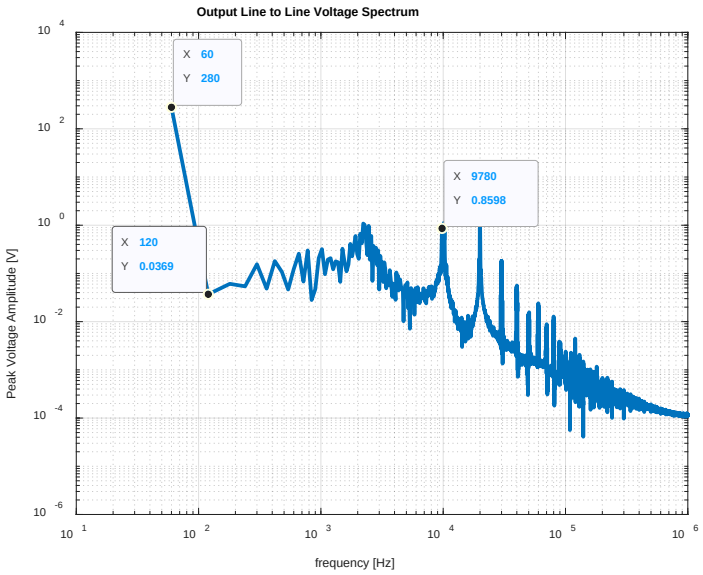

Figure 45. Multi-Step Simulated Load V_{LL} Spectrum, 200V_{rms}, PWM

With the PWM VSI, DC bus voltage remains minimally affected by the multi-step transient, as shown in Figure 46.

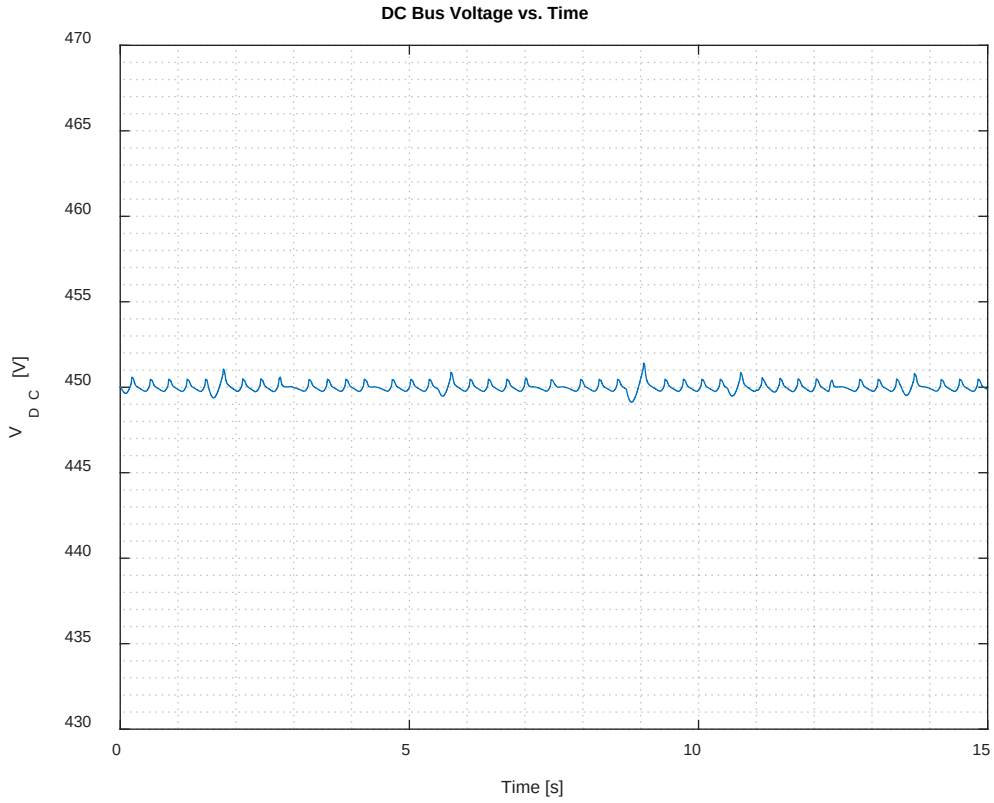

Figure 46. Multi-Step DC Bus Voltage versus Time, PWM

B. MULTI-STEP LOAD PROFILE FOR TYPE I 440V_{RMS} POWER

This section presents simulation results with Type I 440V_{rms} power to demonstrate that the controller design can be adapted to higher voltages supplying power in excess of the pulsed power definition of 50kW-2MW loading.

1. Ideal VSI, LPF at 10 rad/s

Figure 47 and Figure 48 show the real and reactive power versus time for the load, source, and inverter. In each case, similar to what was demonstrated in Figure 28 and Figure 29, the inverter can supply sufficient real power at each step to support a large pulsed load (~200kW average). The reactive power is also supplied from the inverter, allowing source PF to be corrected to unity.

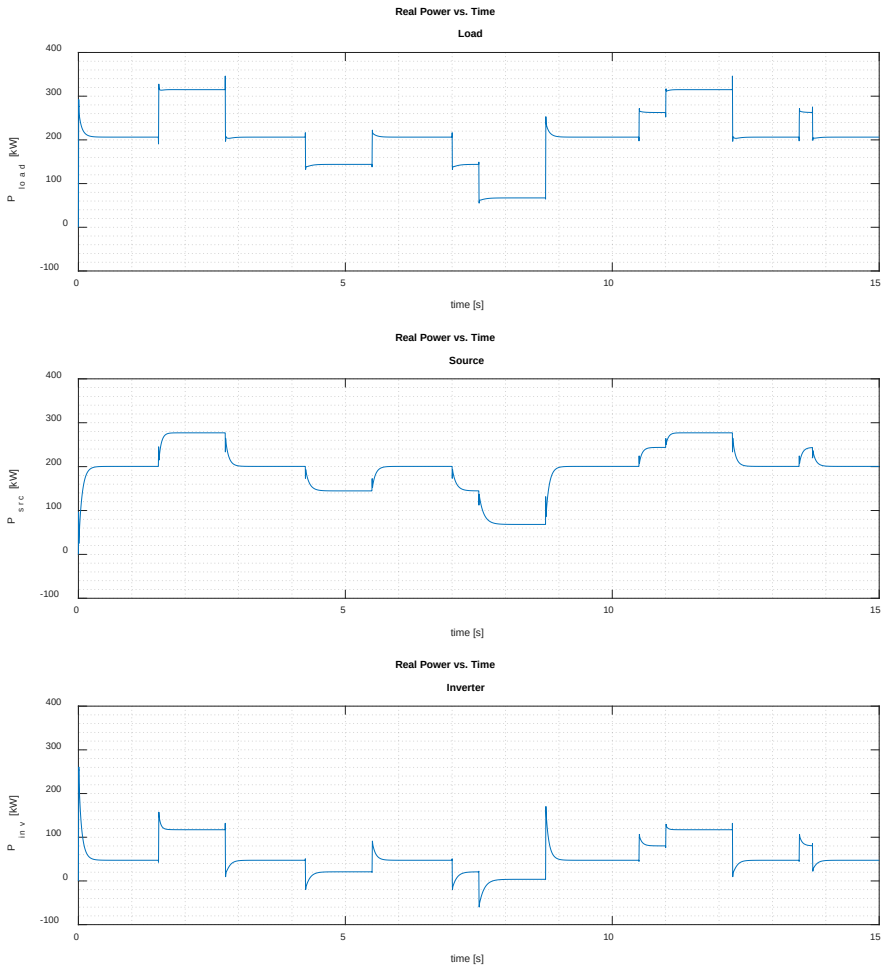

Figure 47. Multi-Step Simulated P versus Time, 440V_{rms}, Ideal VSI, LPF 10rad/s

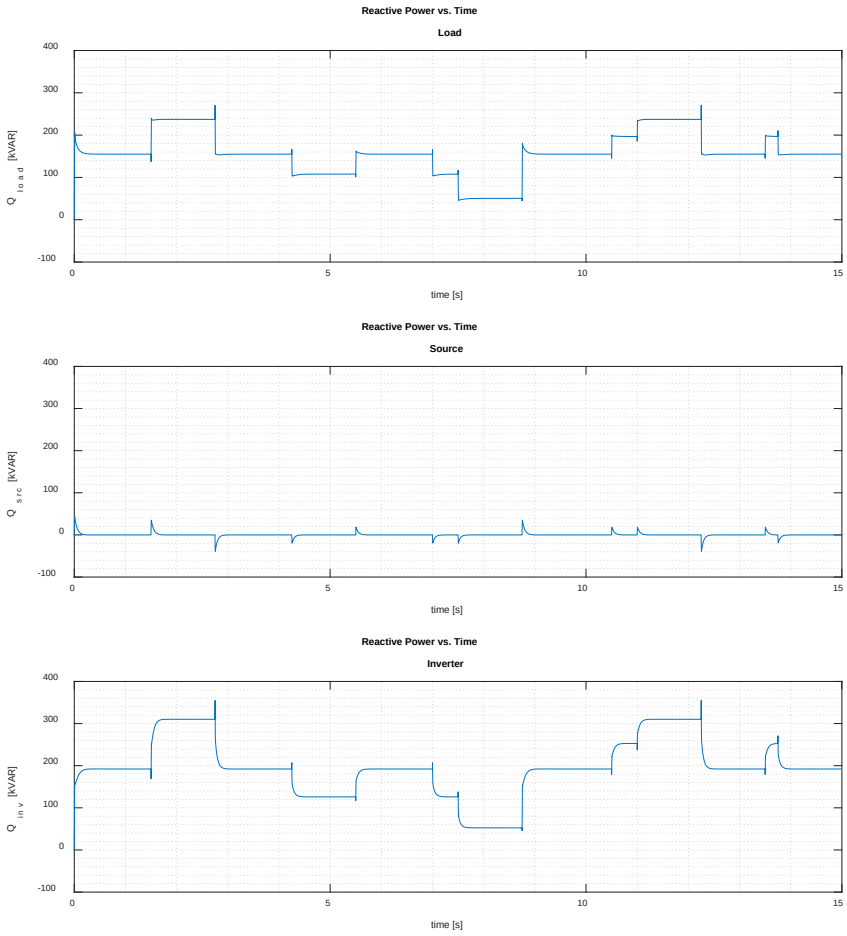

Figure 48. LPF Multi-Step Simulated Q versus Time, 200V_{rms}, Ideal VSI, 10rad/s

2. Ideal VSI, LPF at 1 rad/s

Comparing Figure 49 and Figure 50 to Figure 37 and Figure 38 yields an interesting result. The source PF is still corrected to unity; however, the model presents some instability in how the load responds to steps. Further work is required to adjust the model to work flawlessly with Type I 440V_{rms} power. In general, the inverter supplies or absorbs power through each jump. The result is that the source power raises or lowers slowly enough that a generator could more efficiently respond to these jumps.

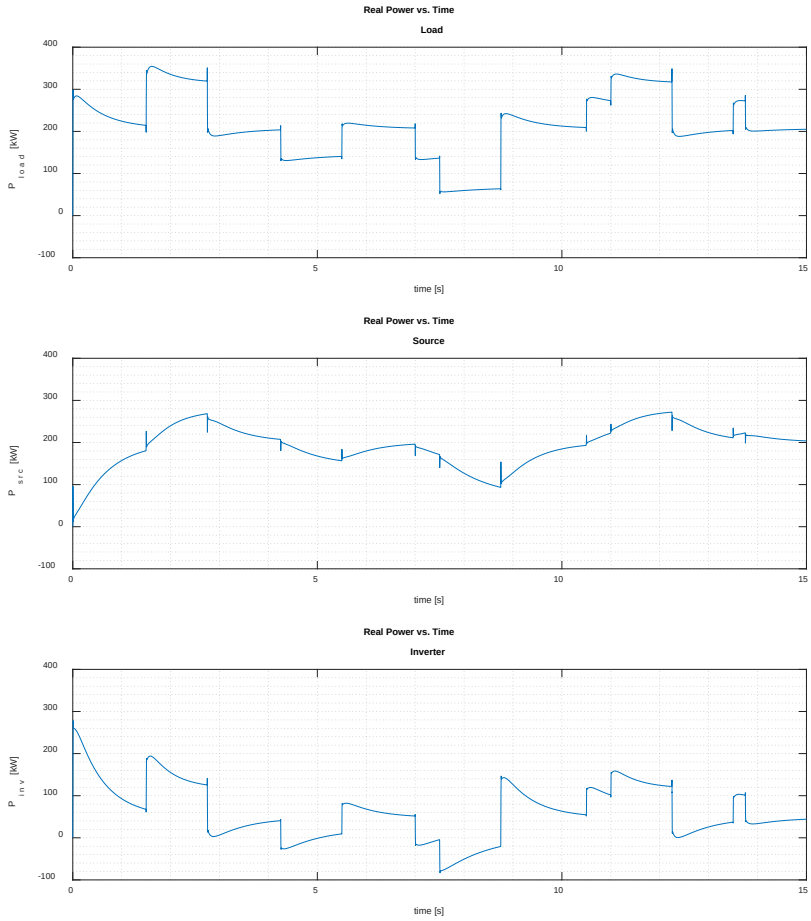

Figure 49. Multi-Step Simulated P versus Time, 440V_{rms}, Ideal VSI, 1rad/s LPF

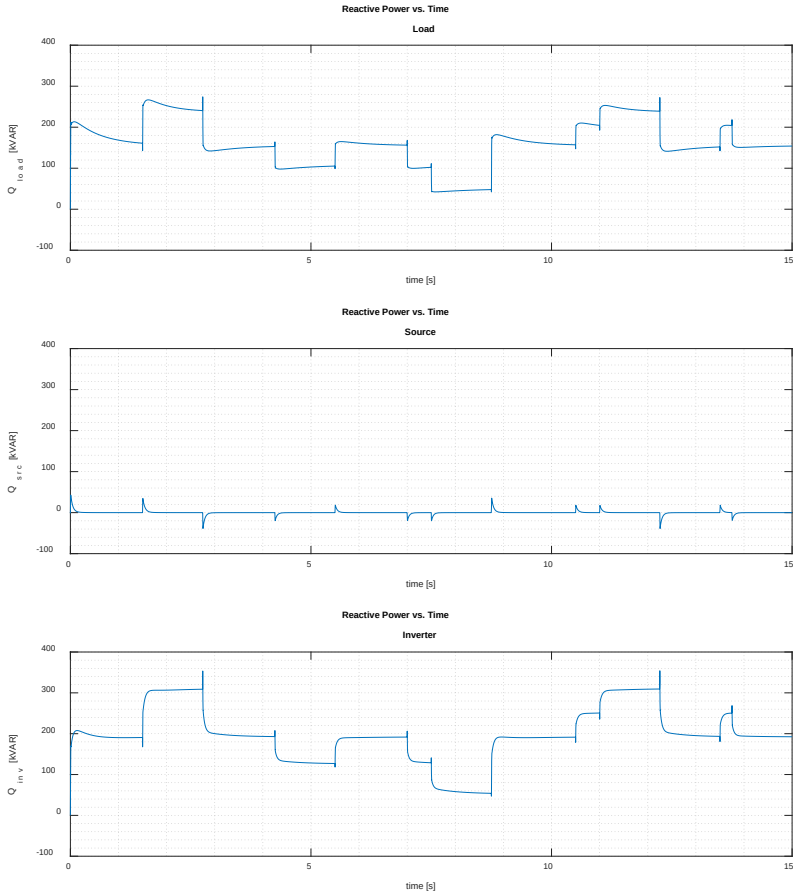

Figure 50. Multi-Step Simulated Q versus Time, 440V_{rms}, Ideal VSI, 1rad/s LPF

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V. EXPERIMENTAL VALIDATION

A. CONTROL SYSTEM IMPLEMENTATION

The controller designed in this thesis is implemented and tested on an OPAL-RT OP4510 RCP/Hardware-in-the-Loop (HIL) control system. The OP4510 system interfaces with MATLAB/SIMULINK via RT-LAB, an OPAL-RT proprietary software. The OP4510 contains a 4-core CPU that interfaces with a Xilinx Kintex-7 K325T Field Programmable Gate Array (FPGA)via a PCI-Express link, running a model with a timestep in the tens of microseconds while allowing the FPGA to execute PWM and other control features in the tens of nanoseconds. The specifications of the OP4510 system are summarized in Table 4.

Table 4. OP4510 Specifications Overview. Adapted from [26], [27].

Processor	Intel Xeon E3 4-core 3.5GHz	7μS minimum time step for model execution
FPGA	Kintex-7 K325T	10nS time resolution and 250nS minimum time step
Inputs	16 Analog	32 Digital
Outputs	16 Analog	32 Digital
Connectivity	Ethernet, RS-232, USB, JTAG, VGA, Keyboard, Mouse	
Memory	2x8GB	

The basic architecture of the OP4510 is shown in Figure 51. The OP4510 contains additional functionality, such as expansion ports for additional inputs/outputs (I/O), fiber optic synchronization, which are unnecessary for the scope of this thesis. The OP4510 is connected to a host PC running RT-LAB for the purposes of generating the model, building the C-code for execution on the OP4510, and displaying a graphical user interface (GUI)

during simulation runs, etc. The model is able to execute on the OP4510 with the step sizes near the specification listed in Table 4 due to the PCI-Express interface between the processor, motherboard, and FPGA. An additional benefit of the RT-LAB software is that it allows various parts of a SIMULINK model to be defined to run in parallel on separate cores of the CPU for faster execution. The ethernet connection between the host PC and the OP4510 is much slower, however, and precludes real-time data collection. The use of a GUI for a small step size model is best reserved for making changes to the model while it is running, such as a PI gain value or a portion of the hardware (buck/boost converter, then VSI, etc.).

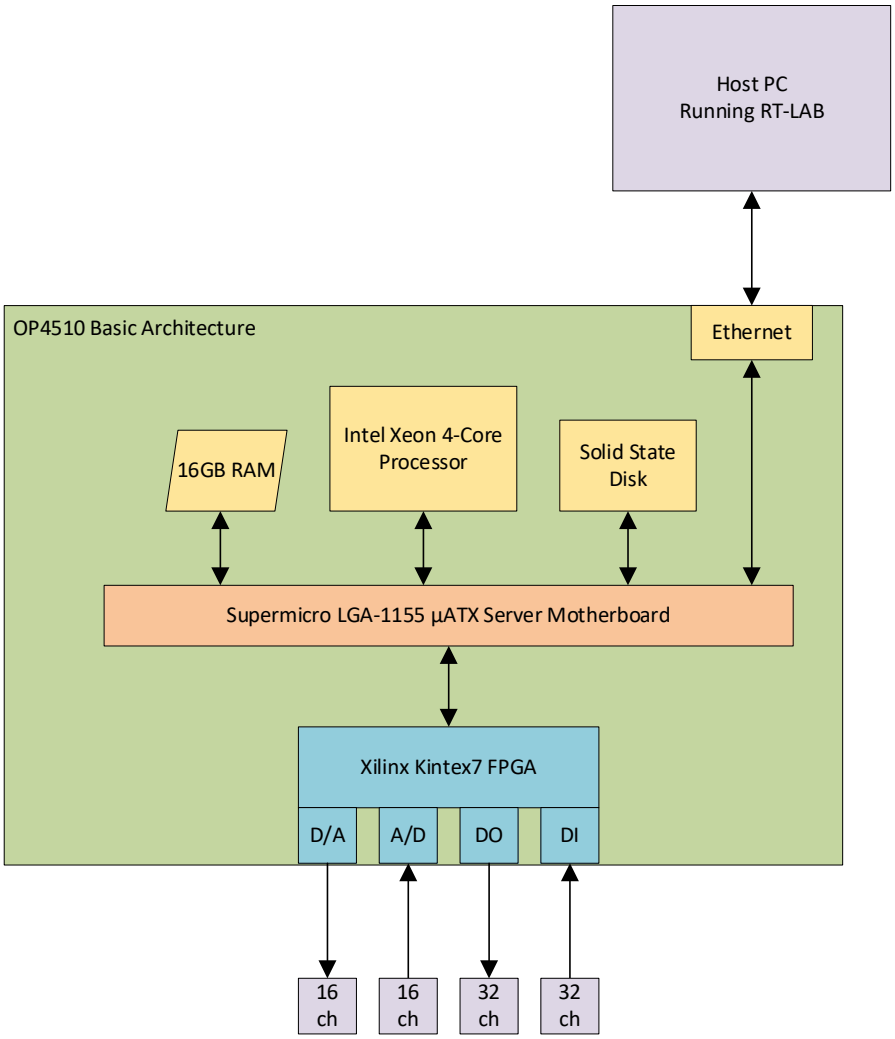


Figure 51. OPAL-RT OP4510 System Architecture. Adapted from [27].

B. SIMULINK MODEL FOR HARDWARE IMPLEMENTATION

The major difference between the model used to conduct the simulations and the model implemented on the hardware is that the equations used to simulate the physical system components (batteries, VSI, load, capacitors, inductors, etc.) are removed, and additionally, the measured currents and voltages need to be supplied as inputs to the model to enable the control system to operate. Finally, outputs need to be added to drive the PWM signals for the VSI, DC/DC converter, as well as cycle the load.

Figure 52 shows the three major subsystems of the OPAL-RT model, where SC_GUI is a graphic user interface that displays on the host PC. SM_INVERTER_AND_CONVERTER is the master subsystem running on one core of the OP4510 system, and SS_PQ_CONTROLLER is a slave subsystem running on a second core of the OP4510.

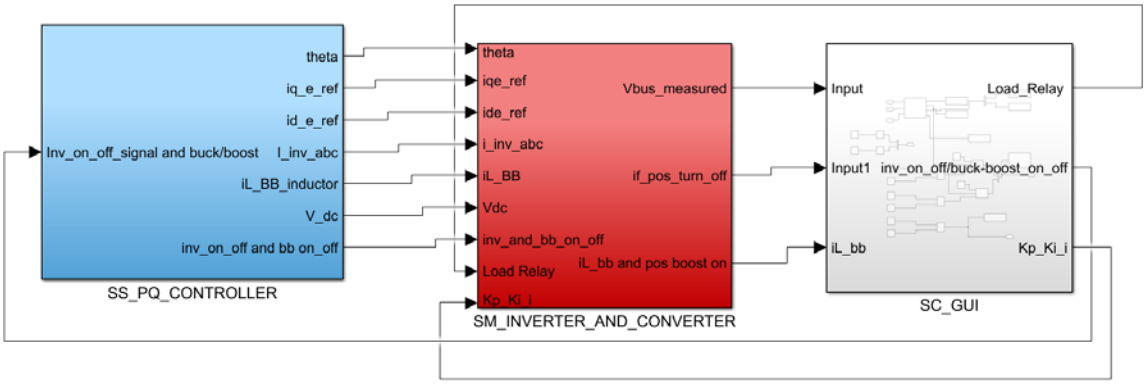


Figure 52. OPAL-RT Simulink Model

Figure 53 shows the internal components of the SS_PQ_CONTROLLER subsystem. The A/D converter section is where the OP4510 has external signals connected. These signals, and their respective gains, are listed in Table 5. The gains are because each parameter is measured using an isolated voltage or current probe at a specific number of amperes/volt or volts/volt. The A/D converters take these values and convert them to digital signals that are inputs to the P-Q control system implemented in the model. Buck/Boost

inductor current (iL_BB_inductor), V_{bus} (V_dc), and inverter phase currents (Iinv_abc) are passed on to the next subsystem as well. Of note, the LPF is set with a frequency of 1 rad/s to enable a slower response. The GUI allows the DC/DC converter and the VSI to be turned on independently, and when they are cycled, the PI controllers also reset. The memory block immediately preceding each subsystem output enables the OP4510 to compute the subsystem calculations in parallel on multiple cores each timestep.

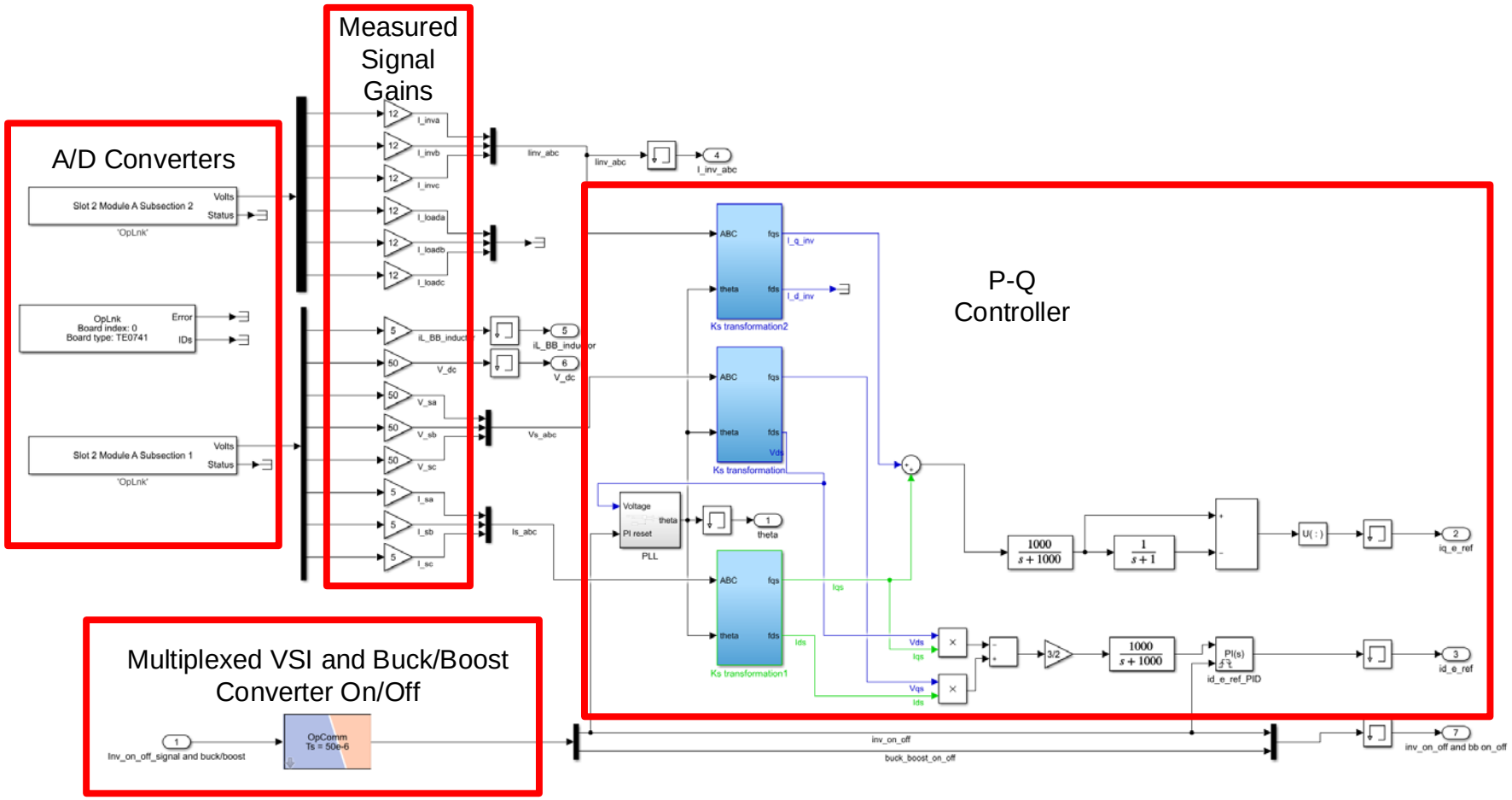


Figure 53. SS_PQ_CONTROLLER Subsystem

Table 5. Analog Inputs to OP4510

Signal	**SIMULINK Signal Label**	**Gain**	**OPAL Slot/Module/ Subsection**	**OPAL Channel**
DC/DC Converter Inductor Current	iL_BB_inductor	5	2/A/1	AIN00
V_{bus}	V_dc	50	2/A/1	AIN01
Source V_{ph} A	V_sa	50	2/A/1	AIN02
Source V_{ph} B	V_sb	50	2/A/1	AIN03
Source V_{ph} C	V_sc	50	2/A/1	AIN04
Source I_{ph} A	I_sa	5	2/A/1	AIN05
Source I_{ph} B	I_sb	5	2/A/1	AIN06
Source I_{ph} C	I_sc	5	2/A/1	AIN07
VSI I_{ph} A	I_inva	12	2/A/2	AIN08
VSI I_{ph} B	I_invb	12	2/A/2	AIN09
VSI I_{ph} C	I_invc	12	2/A/2	AIN10
Step Load I_{ph} A	I_loada	12	2/A/2	AIN11
Step Load I_{ph} B	I_loadb	12	2/A/2	AIN12
Step Load I_{ph} C	I_loadc	12	2/A/2	AIN13

Figure 54 shows the SM_INVERTER_AND_CONVERTER subsystem, which contains the current PI Controller, the SVM computations for the VSI IGBT gate signal duty cycles, the buck/boost DC/DC converter duty cycle computation, overvoltage protection for V_{bus}, and the digital output (PWM) signals from the OP4510.

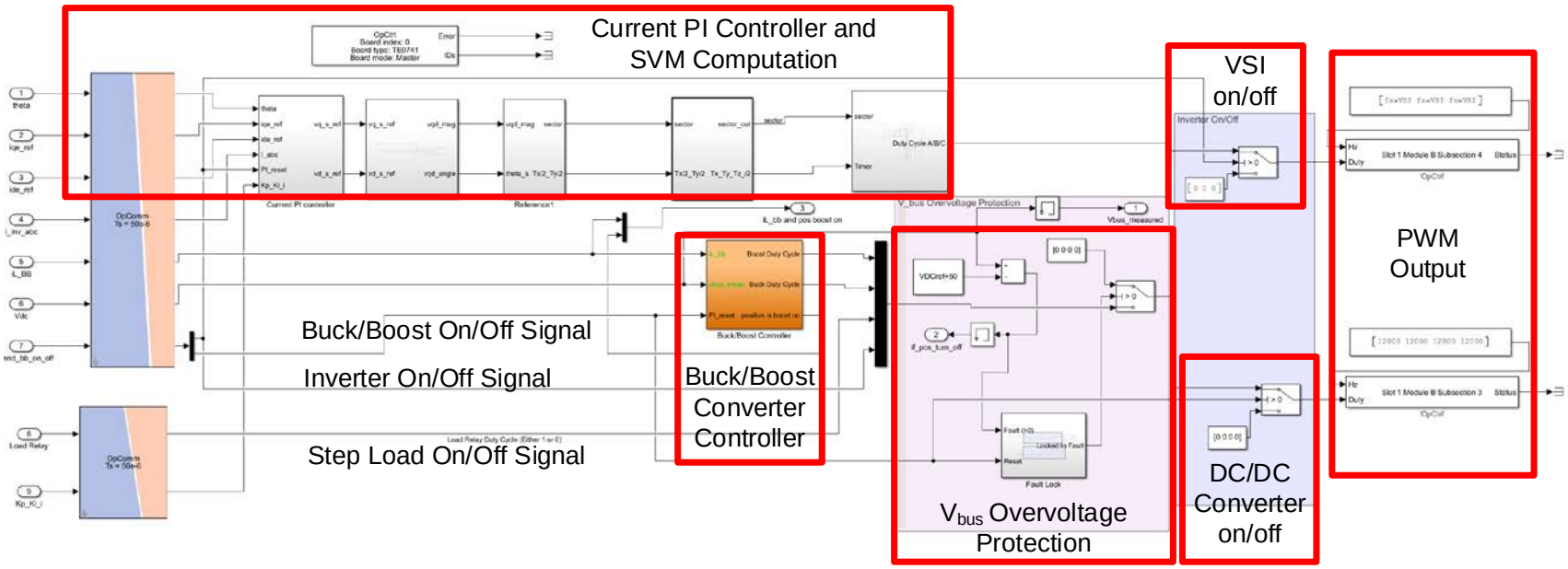


Figure 54. SM_INVERTER_AND_CONVERTER Subsystem

The current PI controller, the SVM duty cycle computations, as well as the buck/boost duty cycle computations, are identical to those in the simulations. The DC bus between the DC/DC converter and the VSI is protected by measuring V_{bus} and shutting down the DC/DC converter and VSI if V_{bus} exceeds the reference (desired) voltage by $50V_{dc}$. The signal is locked in by the logic shown in Figure 55, until the user physically turns off and then turns back on the converter via the GUI.

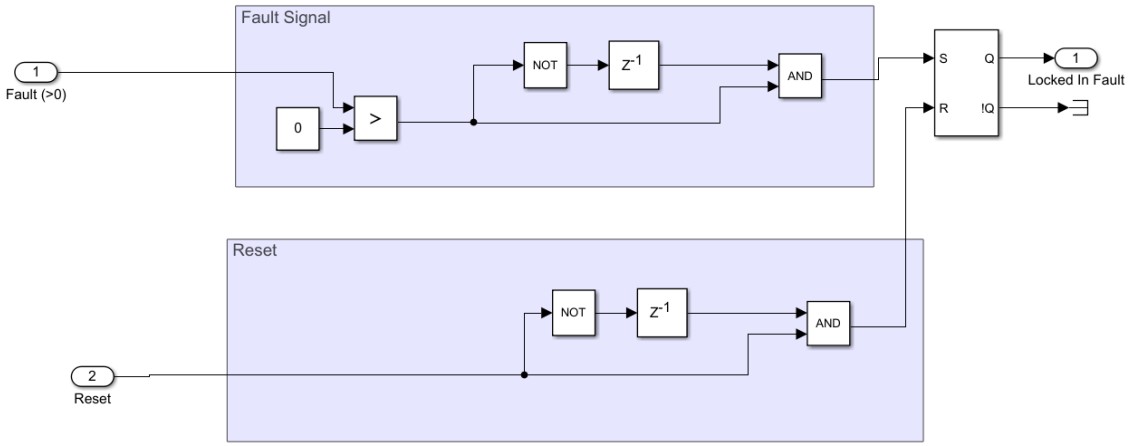


Figure 55. Fault Lock Logic

The duty cycles that are computed for VSI A/B/C Top IGBT are multiplexed and sent to the OPAL-RT PWM block, which for the VSI creates symmetrical PWM at the desired switching frequency (10kHz), and also produces the complementary signal based on the provided duty cycle, for control of the bottom IGBT. To prevent the bottom IGBTs from being turned on simultaneously when the inverter is desired to be off, the inverter on/off signal also controls a DC input/DC output solid state relay that prevents the bottom IGBTs from being turned on, unless the VSI has been turned on by the user. This is due to a limitation of how the OPAL PWM block creates a logic 1 complementary signal anytime 0 is supplied to the PWM block for the main signal; thus, if the top IGBT is off (duty cycle = 0), the bottom IGBT would be on (duty cycle = 1).

The duty cycles that are computed for the buck/boost converter are multiplexed with a load enable signal and the inverter on/off signal. The load enable is a GUI-controlled signal that controls a DC input/AC output solid state relay, which turns on a 3-phase contactor to supply a larger load. Table 6 lists the digital outputs from OP4510.

Table 6. Digital Outputs (PWM) from OP4510

Signal	**OPAL Slot/Module/ Subsection**	**OPAL Channel**	**PWM Frequency (kHz)**
Boost Duty Cycle	1/B/3	DOUT16	12
Buck Duty Cycle	1/B/3	DOUT17	12
Load Enable	1/B/3	DOUT18	12
VSI Enable	1/B/3	DOUT19	12
VSI Phase A Top IGBT	1/B/4	DOUT24	10
VSI Phase A Bottom IGBT	1/B/4	DOUT25	10
VSI Phase B Top IGBT	1/B/4	DOUT26	10
VSI Phase B Bottom IGBT	1/B/4	DOUT27	10
VSI Phase C Top IGBT	1/B/4	DOUT28	10
VSI Phase C Bottom IGBT	1/B/4	DOUT29	10

Figure 56 shows the GUI that is available to the user when running the model in real-time with the hardware. Due to the delay between processing the measurements on the OP4510 CPU and providing them over ethernet to a host PC, the hardware monitor

parameters section provides monitoring only, and not data acquisition. The values displayed in this section are the measured value of V_{bus}, the distance to the V_{bus} overvoltage limit (therefore, if positive, stop the model), the simulation time on target (to verify that it is running in real-time), the buck/boost current (into or out of the battery), and the status of if the boost converter IGBT or buck converter IGBT is on (positive if boost on/negative if buck is on).

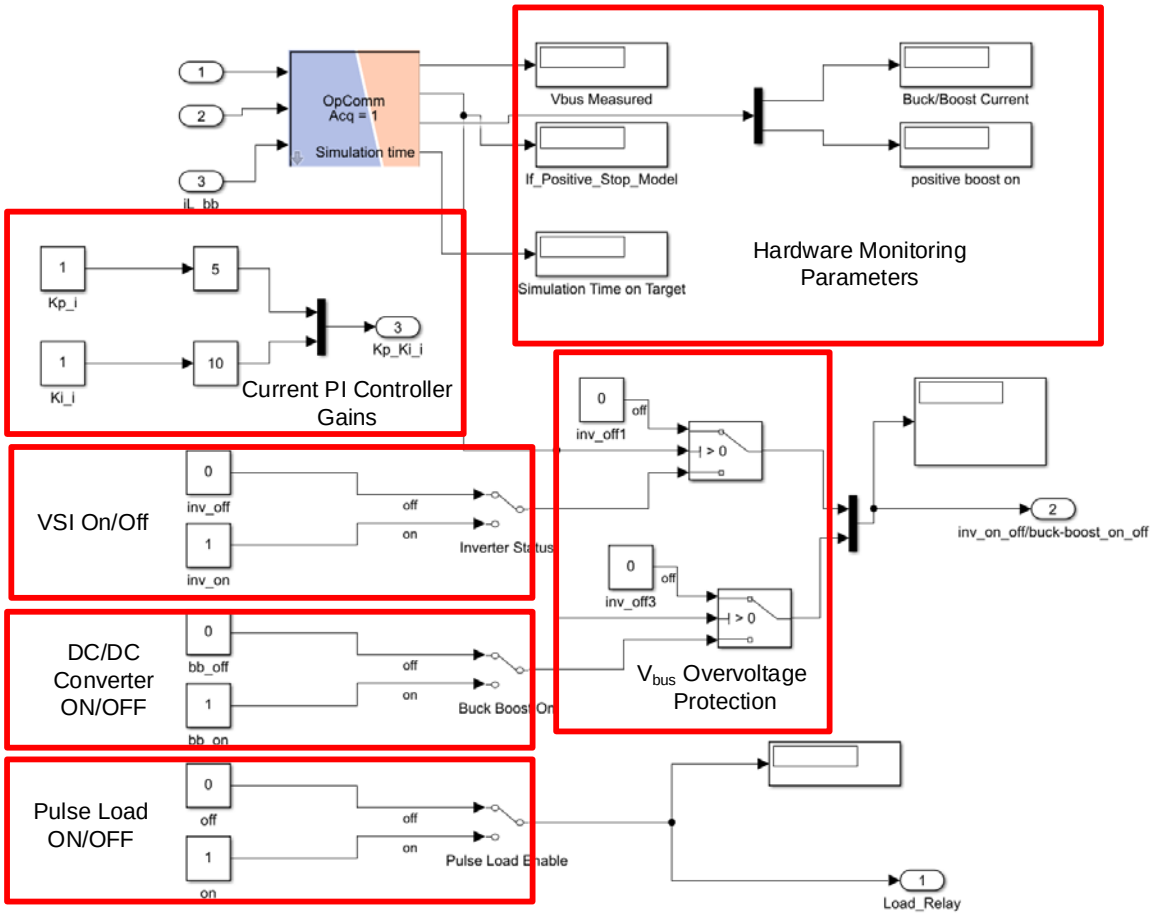


Figure 56. SC_GUI Subsystem

The GUI also provides functionality to turn on the VSI, DC/DC converter, and the pulse load. The pulsed load, when enabled, increases the overall wye-connected AC load from 56Ω/phase to 18Ω/phase. It is also important to note that the VSI on/off is interlocked within SM_INVERTER_AND_CONVERTER to only be on if the buck/boost converter is

on first. Finally, the current PI controller gains can be adjusted in real-time from within the GUI, which allows the PI controller to be tuned in real-time, without the need to rebuild the model on the OP4510.

The model also contains parameters in the InitFcn section of the model callbacks. The parameters, shown in Appendix VI.C, are not readily adjustable but have been selected to be compatible with the hardware implementation.

C. HARDWARE SETUP

The hardware implementation of the designed controller is set up in the power electronics laboratory at the Naval Postgraduate School. A hardware monitoring and operating station was established that contained the host PC, connected to the OPAL-RT OP4510, as well as three oscilloscopes that were used for monitoring and data collection purposes. The monitoring station is shown in Figure 57.

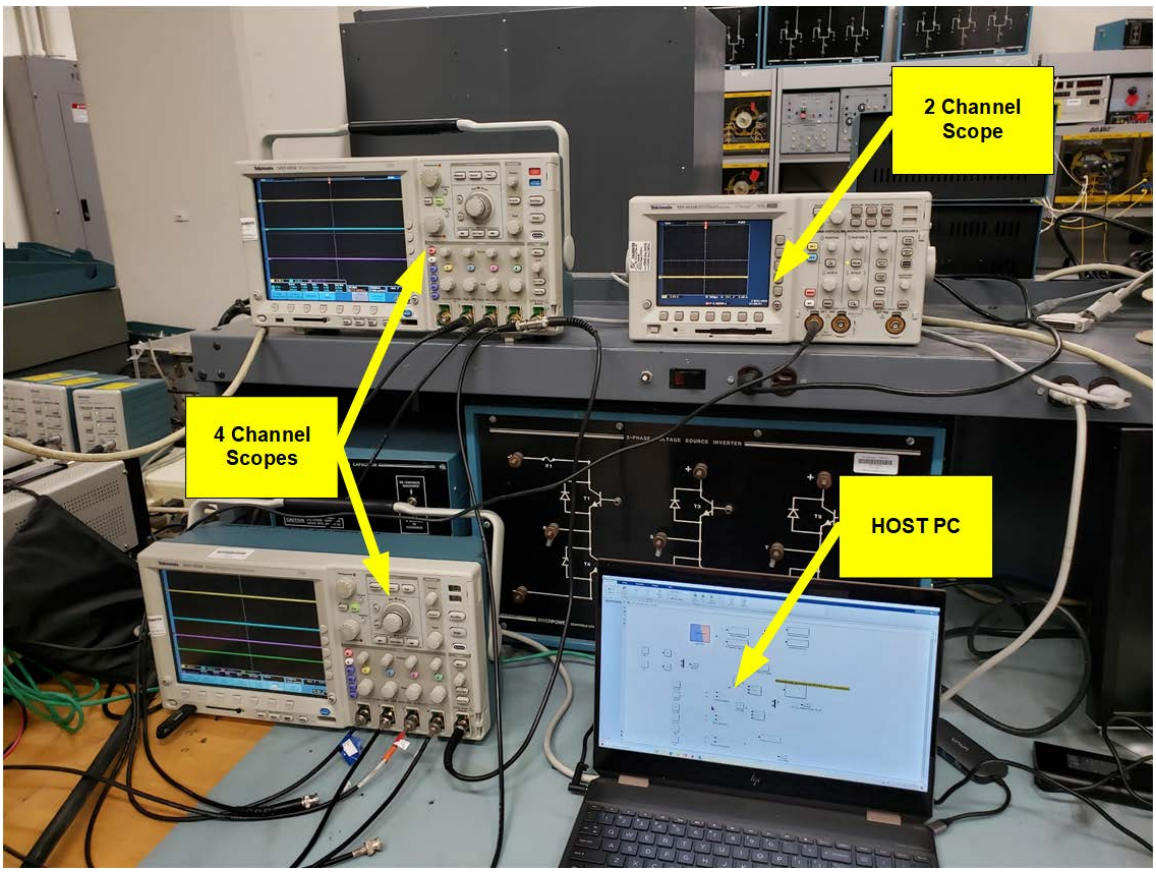


Figure 57. Hardware Monitoring and Operating Station

Figure 58 shows the three-phase variable source, which is current limited to 5A per phase. This source was used to emulate a traditional grid to which the VSI would be connected. Also seen in Figure 58 are current sensors for the additional load that is used to create load steps, the wye-connected filtering capacitors, as well as the three load boxes. Each load box is set up as a wye-connected 56Ω-per-phase 3-phase load. The load towards the top of the picture is powered as soon as the variable 3-phase source is energized. The two load boxes at the bottom of the picture are wired in parallel to create a 28Ω-per-phase wye-connected load. When the step load is enabled on the GUI, the 3-phase contactor closes, placing the 28Ω-per-phase load in parallel with the 56Ω-per-phase load, for an effective load step from 56Ω-per-phase to 18.7Ω-per-phase.

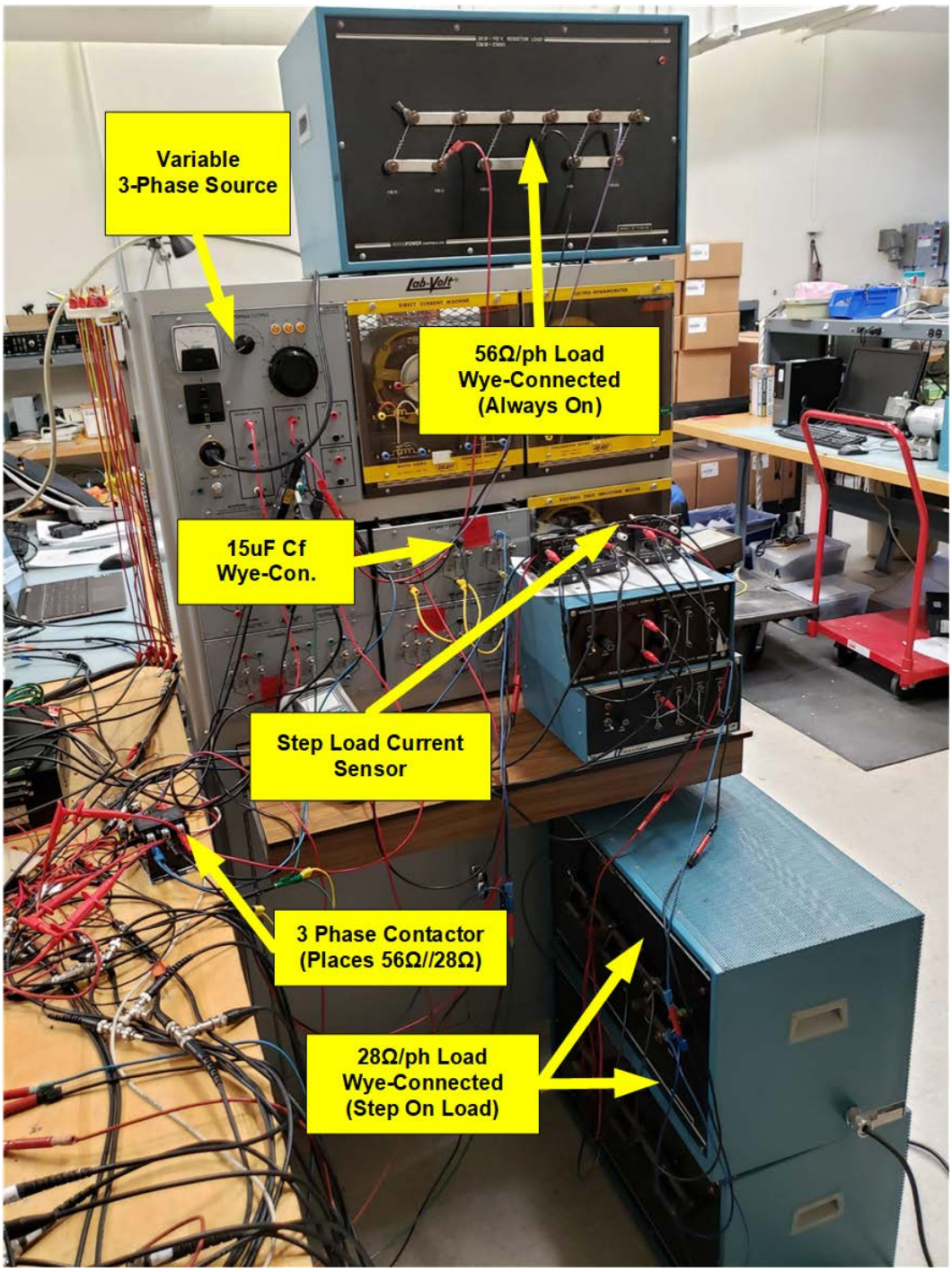


Figure 58. Hardware Implementation – Source, Loads, Filtering Capacitors

Figure 59 and Figure 60 show an overview of the entire hardware implementation. For reference, the oscilloscope seen in the top right of Figure 59 is the top left oscilloscope seen in the hardware monitoring and operating station of Figure 57. Two reconfigurable

Semikron SEMITEACH IGBT Modules are used to implement the DC/DC converter and the VSI [28]. For the DC/DC converter, only one of the three pairs of IGBTs is used, while the VSI uses all three IGBT pairs.

The voltage sensors are Tektronix P5200 50X/500X High Voltage Differential probes, used at 50X. The white-faced current sensors seen in Figure 59 are Tektronix TCPA300 AC/DC Current Probe Amplifiers set to 5X, while the black-faced current sensors are LEM LT 100-S Current Transducers calibrated for 12X. Also pictured are two 0.3mH inductors placed in series for a total of 0.6mH in series with each phase of the VSI output.

Figure 60 shows a basic schematic of the connections between the batteries, DC/DC converter, DC bus capacitor (C_{bus}), and the VSI overlaid on the hardware implementation. Figure 60 also shows the OP4510, with the location of the $15V_{dc}$ externally-powered digital output card, and the interface card for the analog-to-digital converter.

Figure 61 and Figure 62 show the circuitry schematic of the hardware implementation used in the lab. Figure 61 is the left half of the schematic, and Figure 62 is the right half of the schematic. There is a vertical line of demarcation that appears on each figure to show where the two figures connect. Signals coming from or going to the Opal OP4510 are generically represented in the figures but are wired per Table 5 and Table 6 .

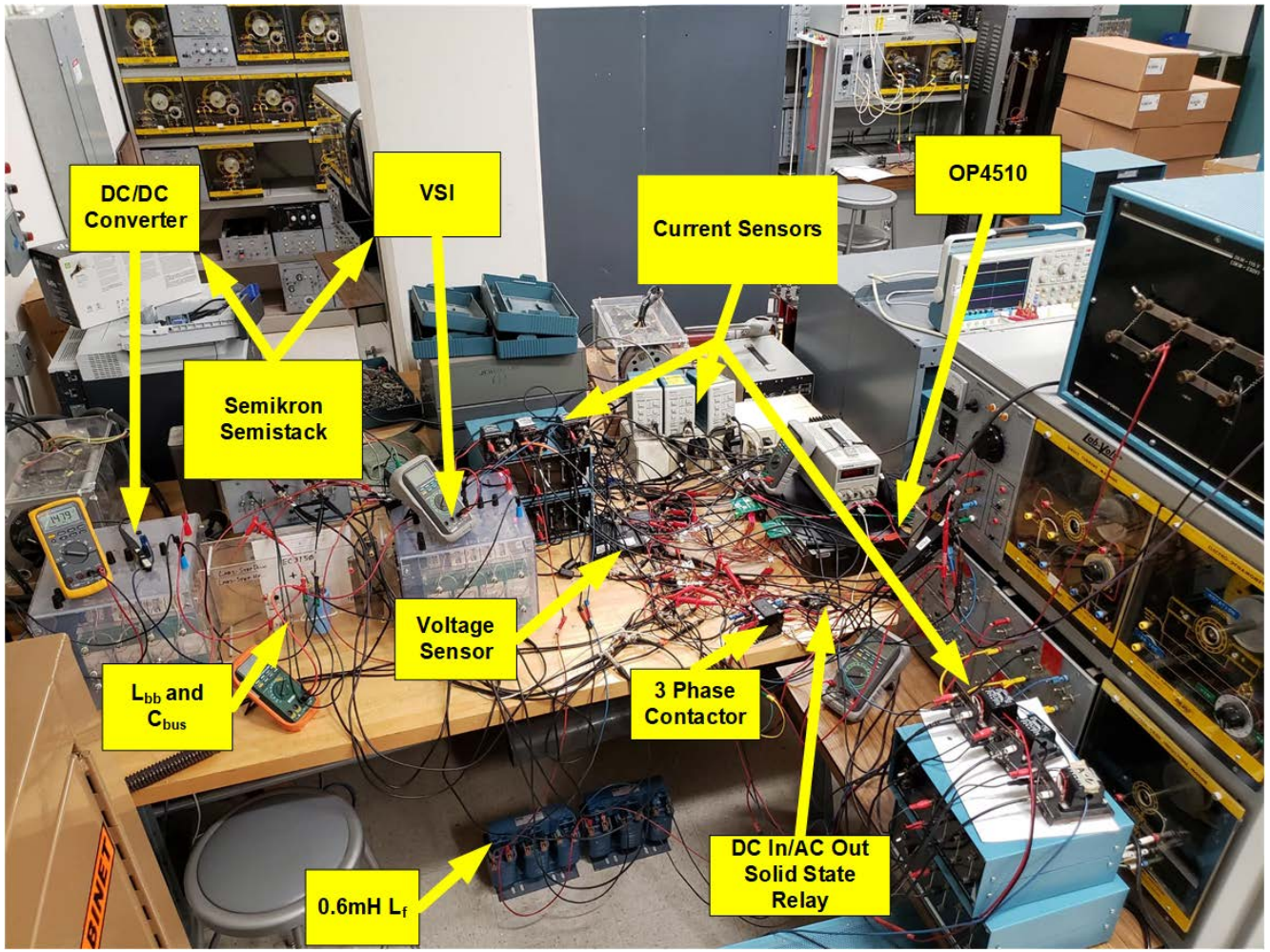


Figure 59. Hardware Implementation – Overview

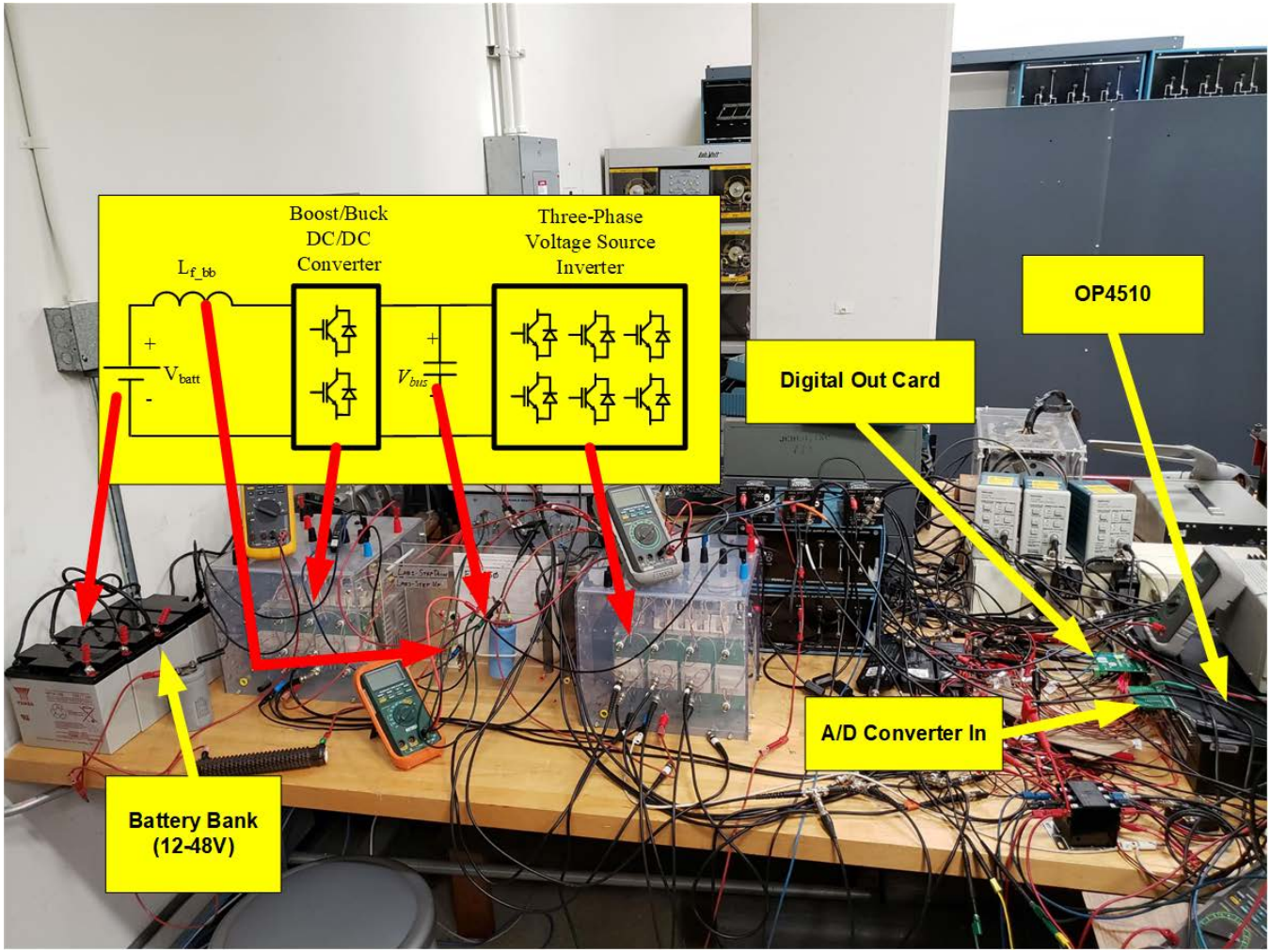


Figure 60. Hardware Implementation – Overlaid with Basic Schematic

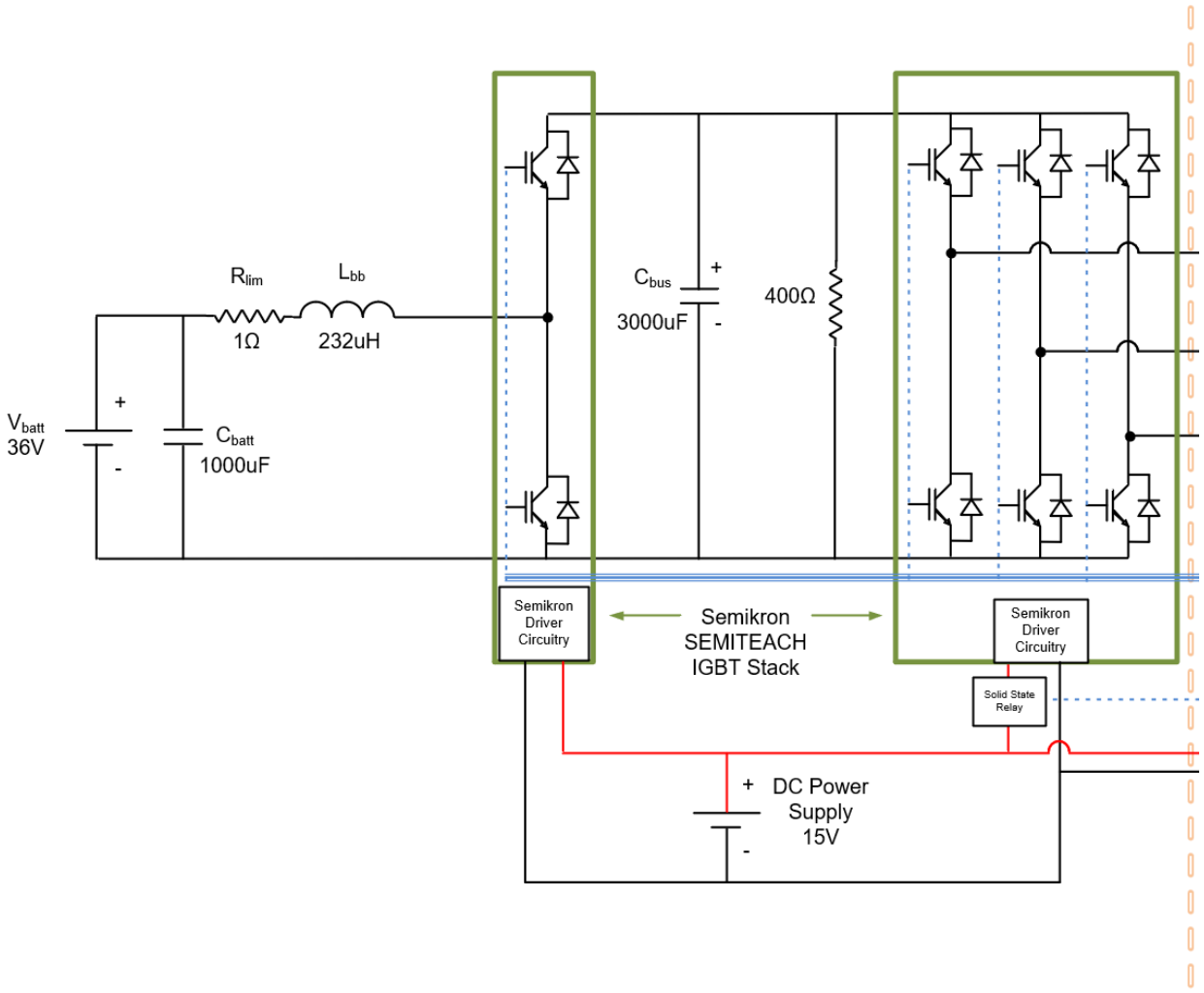


Figure 61. Hardware Implementation Circuitry Schematic (Left)

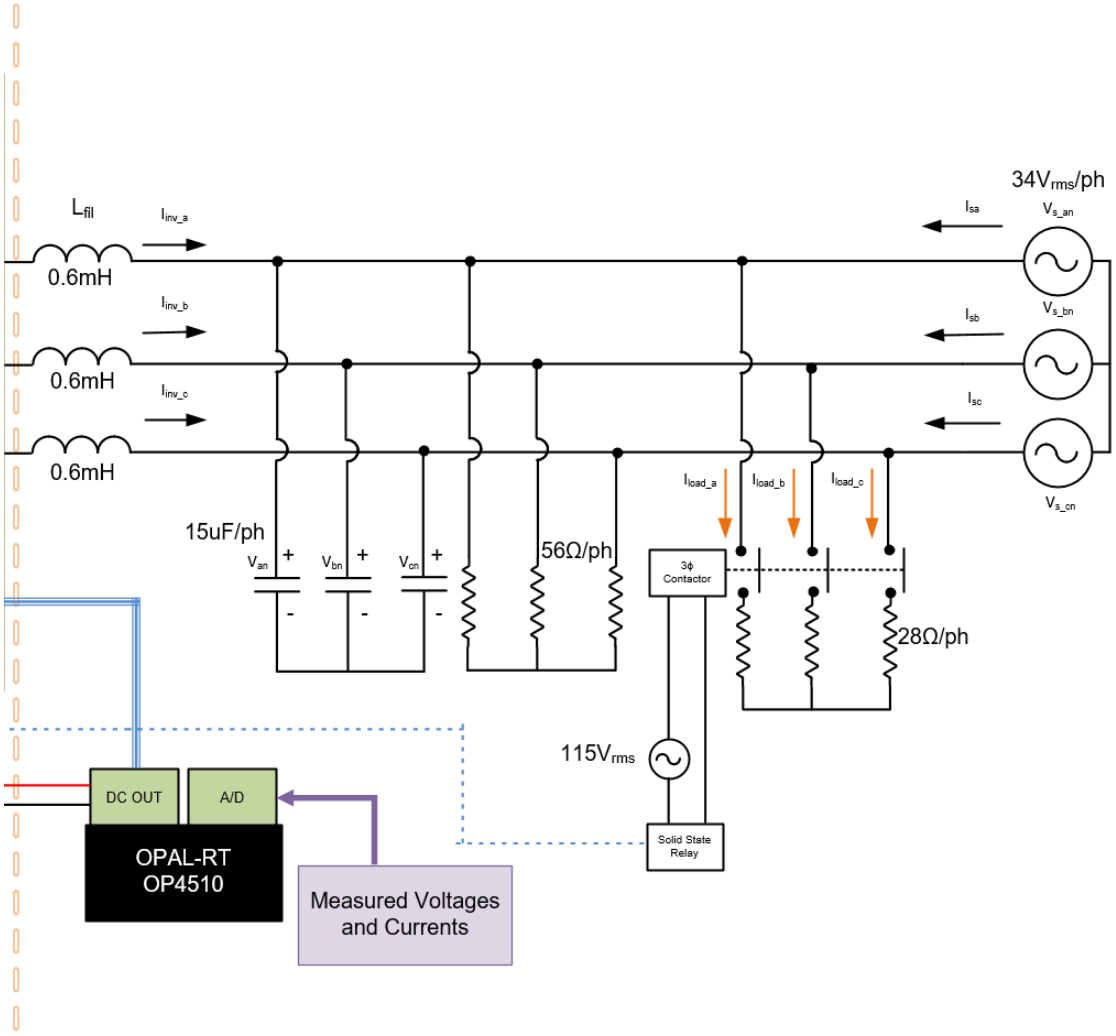


Figure 62. Hardware Implementation Circuitry Schematic (Right)

D. EXPERIMENTAL RESULTS

The experiment to validate the physics-based model of the P-Q controller was implemented on the hardware described in this Chapter, Sections A through C, with the parameters listed in Table 7.

To validate the physics-based model with the hardware, source voltage, source current, and inverter currents were monitored via oscilloscopes, and two seconds worth of data were obtained to include approximately 200ms prior to a load change event, and 1800ms following the load change event. To prepare for the experiment, the following sequence of events was executed:

1. Turn on and boot up OPAL-RT OP4510 (target).
2. Run RT-LAB on the host computer.
3. Build a compatible SIMULINK model on target and load the model onto the target.
4. Energize 15V external power supply for OP4510 Digital Out logic and Semikron SEMITEACH IGBT stack driver circuitry.
5. Verify that all current and voltage probes are powered and prepared to send data to target A/D converters.
6. Turn on Source Power Supply (3ϕ AC source) at the desired voltage.
7. Using RT-LAB, run the model on the target, verify the simulation time counter is increasing.
8. Turn on DC/DC buck/boost converter from GUI, allow to stabilize, and verify GUI displays the desired measured V_{bus} value.
9. Turn on VSI from the GUI, allow currents to stabilize.

With the OPAL OP4510 running the model in real-time on the target, and the DC/DC converter and VSI inverter operating as designed, the GUI was used to step on and off the load, taking data for each load step.

Table 7. Circuit Component List and Values

Device	Value	Note	Parameter Measured
Pb-Acid Battery	36V	N/A6	N/A
SEMIKRON SEMITEACH IGBT Stack	N/A	One for DC/DC Converter One for VSI	N/A
External Power Supply	15V	Powers OPAL-RT Digital Output Card, SEMIKRON SEMITEACH IGBT Stack	N/A
External Power Supply	+15V/-15V	(4) Supplies to Power (6) LEM LT 100-S	N/A
Current Sensor	N/A	(6) LEM LT 100-S (4) Tektronix TCPA300	Load Current x3 Inverter Current x3 Source Current x3 Battery Current
Voltage Sensor	N/A	(4) Tektronix P5200	V_{bus} V_{an}, V_{bn}, V_{cn}
DC Capacitor	1000uF	In Parallel with Battery Bank	N/A
L_{bb}	232uH	Buck/Boost Inductor	N/A
C_{bus}	3000uF	DC Bus Capacitor	N/A
DC Load Resistor	400Ω	In parallel with C_{bus}	
V_{bus_ref}	80V	Operating V_{bus} Value for Experiment	N/A
L_f	0.6mH/phase	VSI Filter Inductor Wye-Connected	N/A
C_f	15uF/phase	VSI Filter Capacitor Wye-Connected	N/A
Lab Volt 3-Phase Power Supply	$48V_{LL\_rms}$	N/A	N/A
Current Limiting Resistor	1Ω	Placed in Series with Battery Bank	N/A
3-Phase Contactor	N/A	N/A	N/A
DC Input/AC Output Solid State Relay	N/A	Controls Three Phase Contactor (Step Load)	N/A
DC Input/DC Output Solid State Relay	N/A	Controls +15V Power to SEMIKRON VSI	N/A
Load Resistor	56Ω/phase 18.7Ω/phase with Step Load on	Wye-Connected 3 Load Resistor Banks (1) 56Ω/phase always on (2) 56Ω/phase added in Parallel on Step Load	N/A

1. Load Step On (56Ω to 18.7Ω)

This section examines the performance of the controller when the load power is increased (load step on). For reference, while looking at the following figures, the load step occurs near -0.46s. The power drawn by the load is increased by stepping a 28Ω resistor in parallel with the original 56Ω, which changes the 3-phase load resistance from 56Ω to 18.7Ω.

Figure 63 shows the measured value of phase *A* line-to-neutral voltage at the point of common coupling, as well as inverter currents versus time. At the time of the load step, there is nearly no observable change in voltage. The inverter currents do demonstrate a notable amount of distortion in the waveform shape, mostly due to the 5^{th} harmonic. At such low currents, noise in the measurement signals also likely affects the distortion of the waveform.

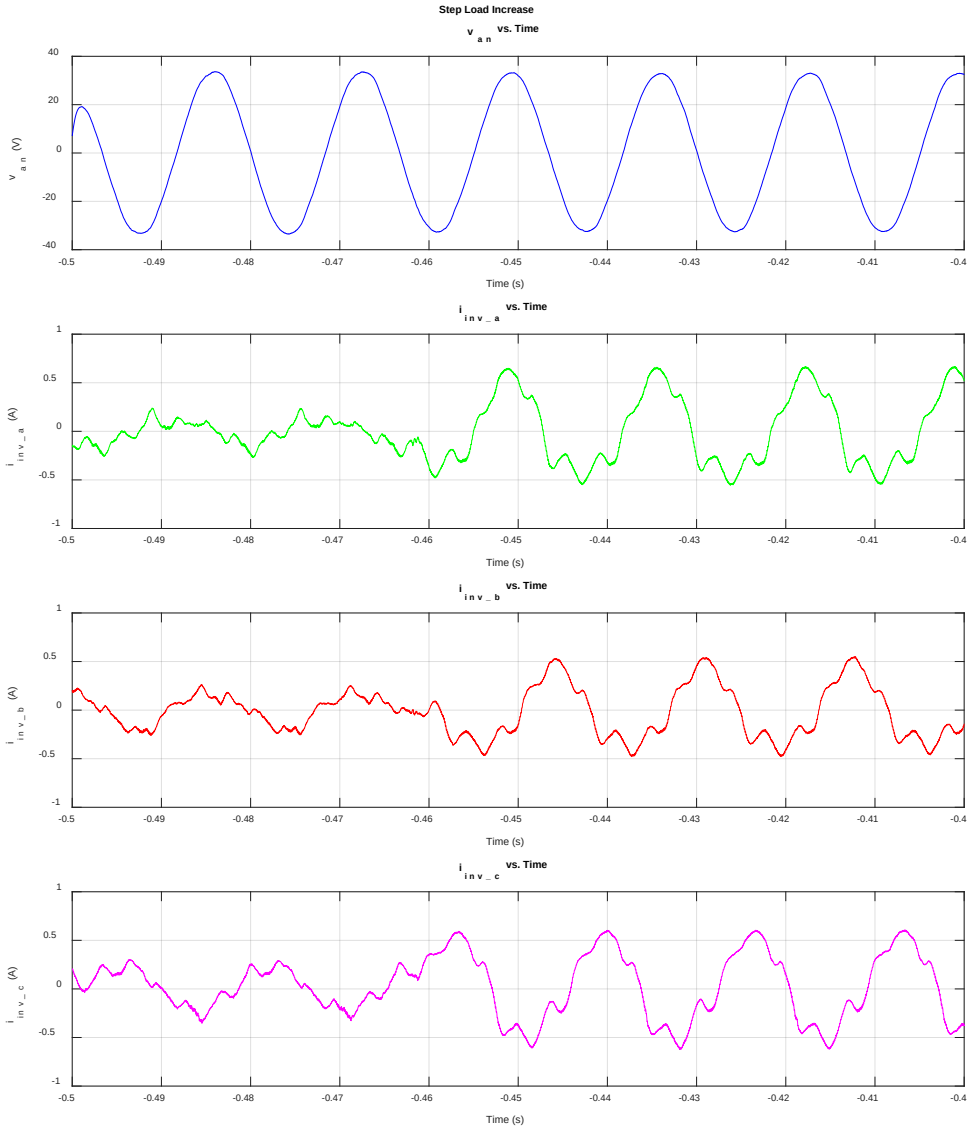


Figure 63. Step Load Increase – v_{an} and Inverter Currents versus Time

Figure 64 shows v_{an} and $10xi_{inv\_a}$ overlaid, as well as the three inverter currents overlaid with each other. While it is evident from the figure that currents become larger once the larger load is stepped on, the most notable observation is that inverter current and voltage are in phase with each other, indicating that power is, in fact, flowing out of the

inverter to the load, at the instant the load is stepped on. This is the desired response of the controller, which is tuned to achieve unity power factor at the grid interface.

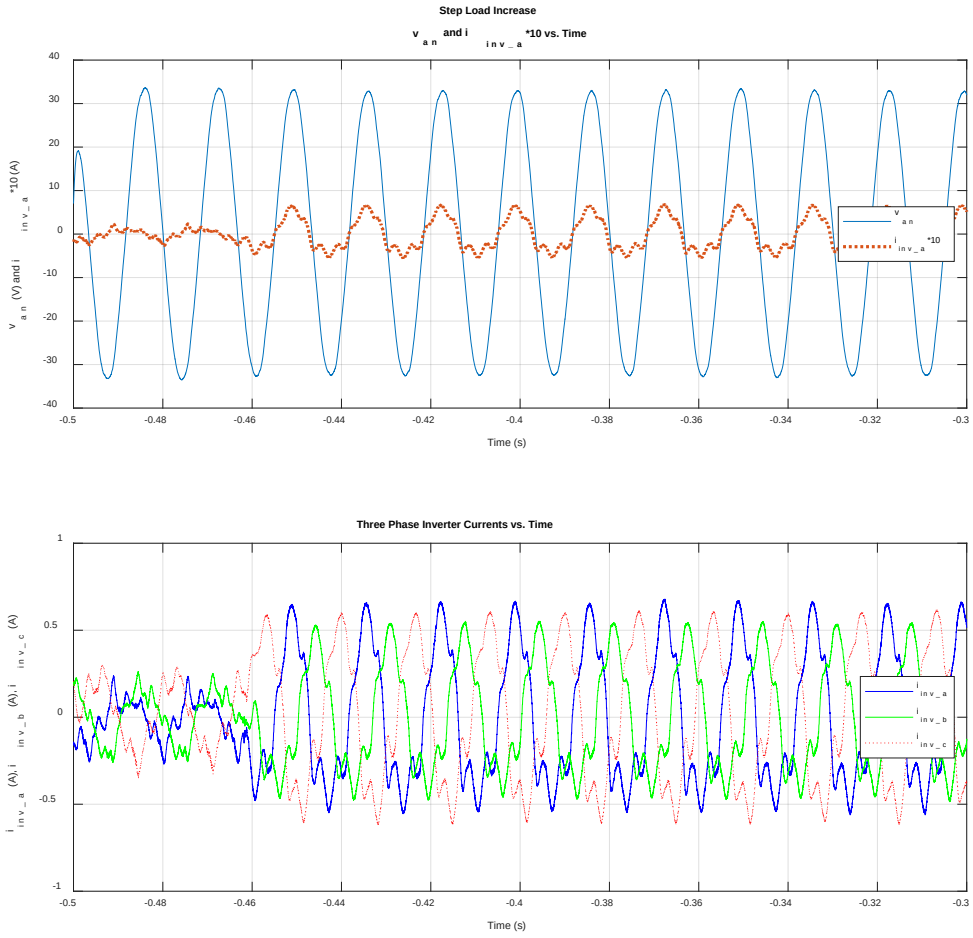


Figure 64. Step Load Increase – v_{an} and i_{inv_a} versus Time, with i_{inv_abc} versus Time

Figure 65, Figure 66, and Figure 67 show the three-phase AC bus voltages versus time, three-phase source currents versus time, and three-phase inverter currents versus time, for the purpose of showing the gross changes over time. From Figure 65 one can see that voltage remains within two volts peak through the duration of the transient. Figure 66 does show that the source current does jump up when the additional load is introduced;

however, there is a clear upward trend over the following 0.9s. Figure 67 shows that there is an immediate step up in inverter current as expected, with inverter current slowly reducing over the next 0.9s. The upward trend in source current and the downward trend in inverter current, coupled with the fact that Figure 64 shows positive power flowing out the inverter, validates the desired response of the controller for a step load increase. Aside from the small initial jump in current for Figure 66, likely due to measurement and control delays in the hardware, the experimental measurements show a similar trend to what is predicted by the model.

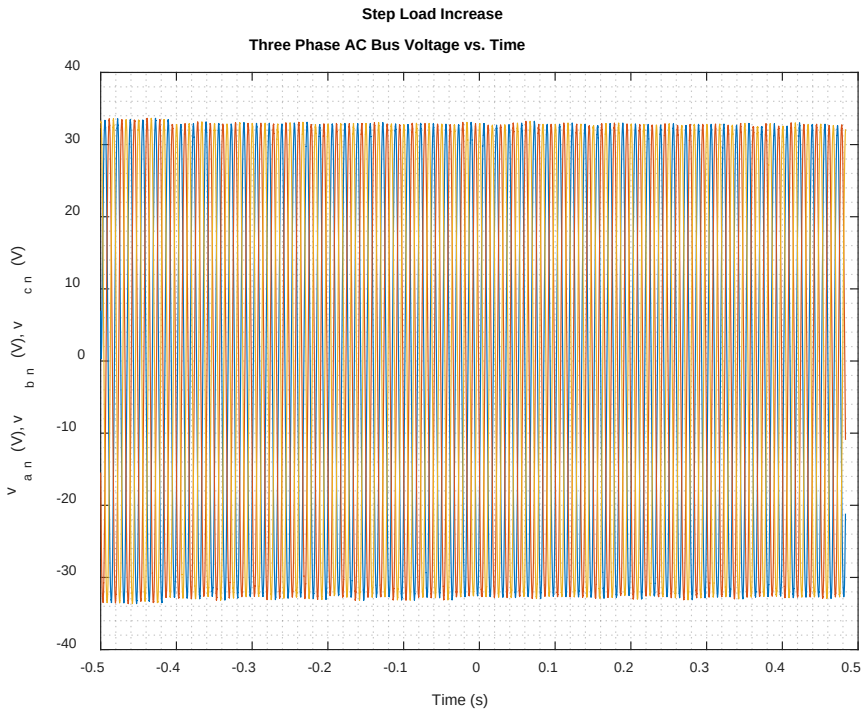
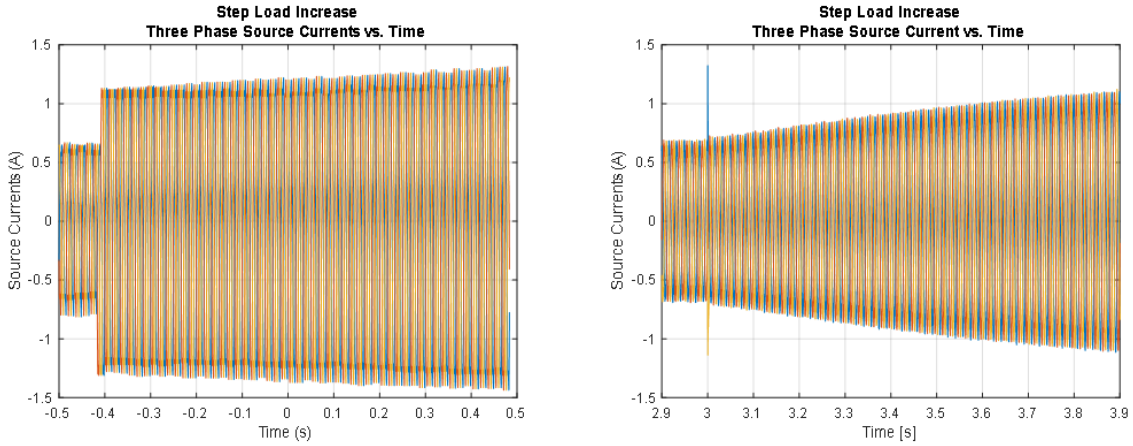
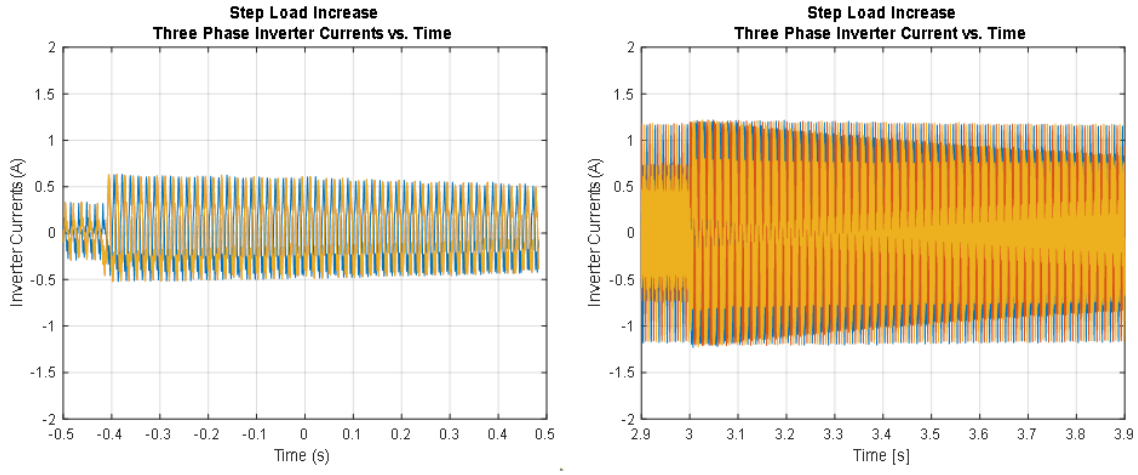


Figure 65. Step Load Increase – Three Phase AC Bus Voltages versus Time



a) Experimental b) Simulation

Figure 66. Step Load Increase – Three Phase Source Current versus Time



a) Experimental b) Simulation

Figure 67. Step Load Increase – Three Phase Inverter Current versus Time

Figure 68 zooms in on the phase A data shown in Figure 65, Figure 66, and Figure 67. Inverter current is roughly in phase with source current and source voltage, and the trends previously observed are present.

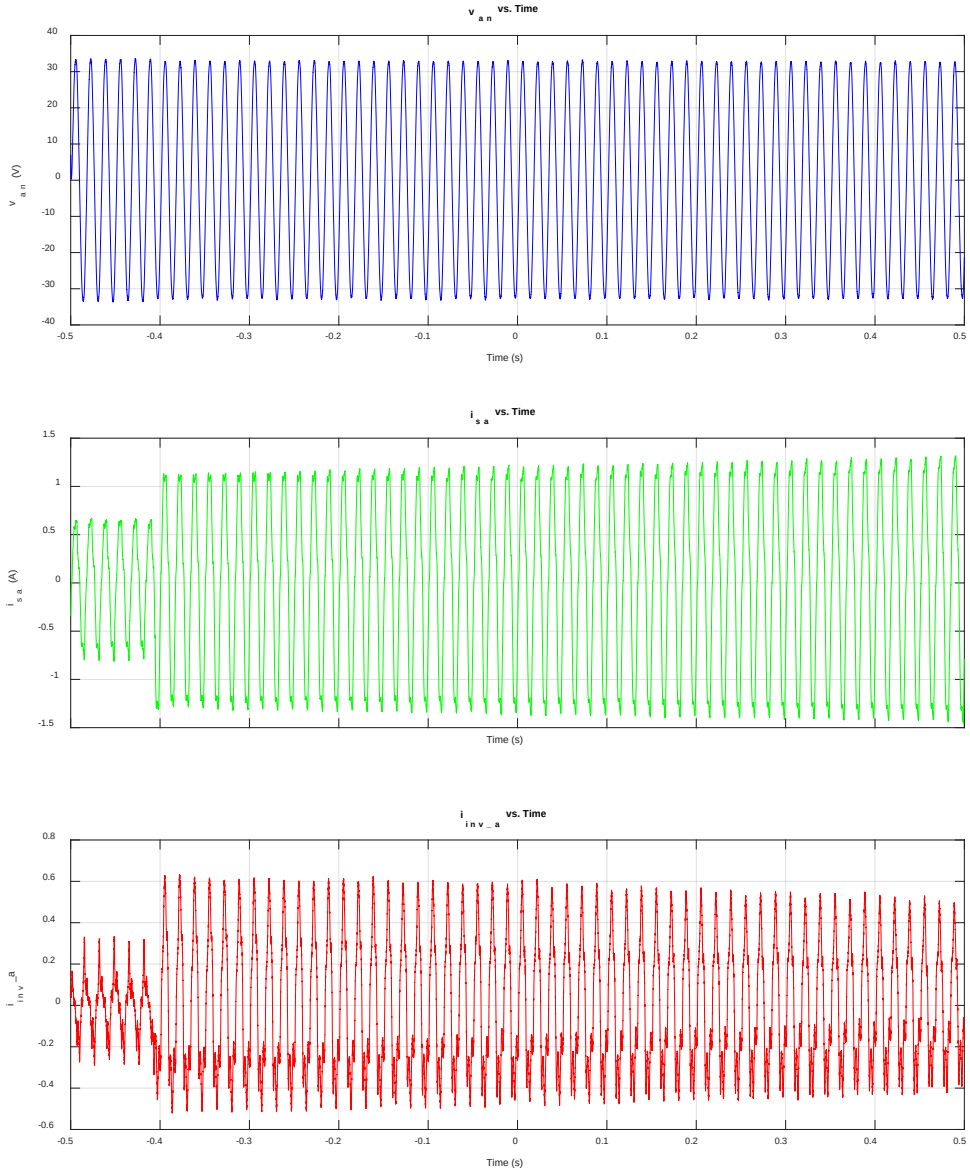
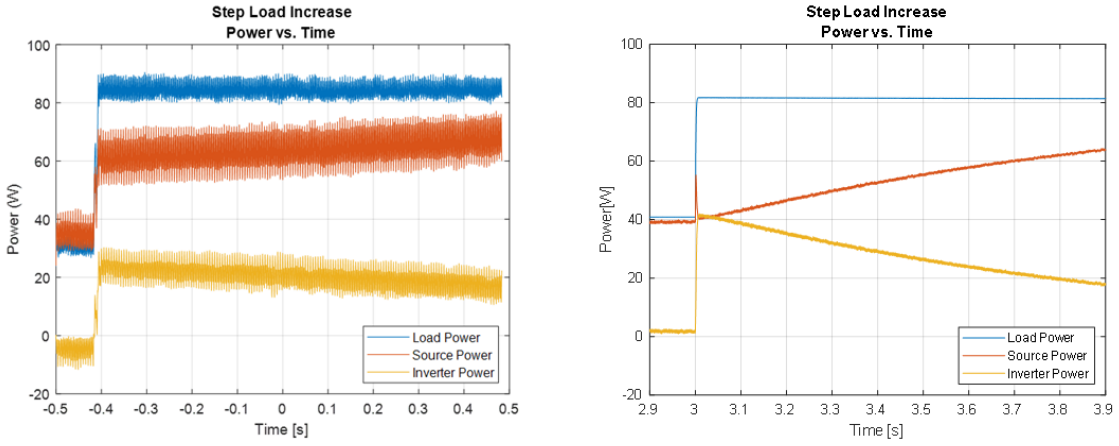


Figure 68. Step Load Increase – v_{an}, i_{sa}, i_{inv_a} versus Time

Figure 69 further validates the response of the controller to the step load increase by showing the active power drawn by the load, the power delivered by the source, and the power delivered by the inverter. Initially, the inverter is sending a small amount of power to the DC bus (negative inverter power), while the load is near 35W. Once the load steps

up near 85W, the source must only supply approximately 65W, with 25W coming from the inverter. Over the remaining 0.9 seconds, there is an observable upward trend in source power with a downward trend in inverter power. In the laboratory, due to measurement and control delay, the source power jumps slightly during the step as the controller respond to cause the inverter to begin supplying power.



a) Experimental b) Simulation

Figure 69. Step Load Increase – Power versus Time

In addition to validating the functionality of the active power controller, the reactive power control is experimentally validated in Figure 70. The desired reactive power from the source is 0VAR. The top plot in Figure 70 shows that the source current and source voltage are perfectly in phase before and after the step load; thus, the power factor at the grid is unity. Furthermore, the bottom plot in Figure 70 shows that initially, the inverter current leads the source voltage, which validates that real power is flowing to the DC bus, charging the batteries through the DC/DC converter. Then, at the instant of the step load increase, both source and inverter currents are in phase, such that real power is being supplied from the batteries, through the DC bus, to the AC bus.

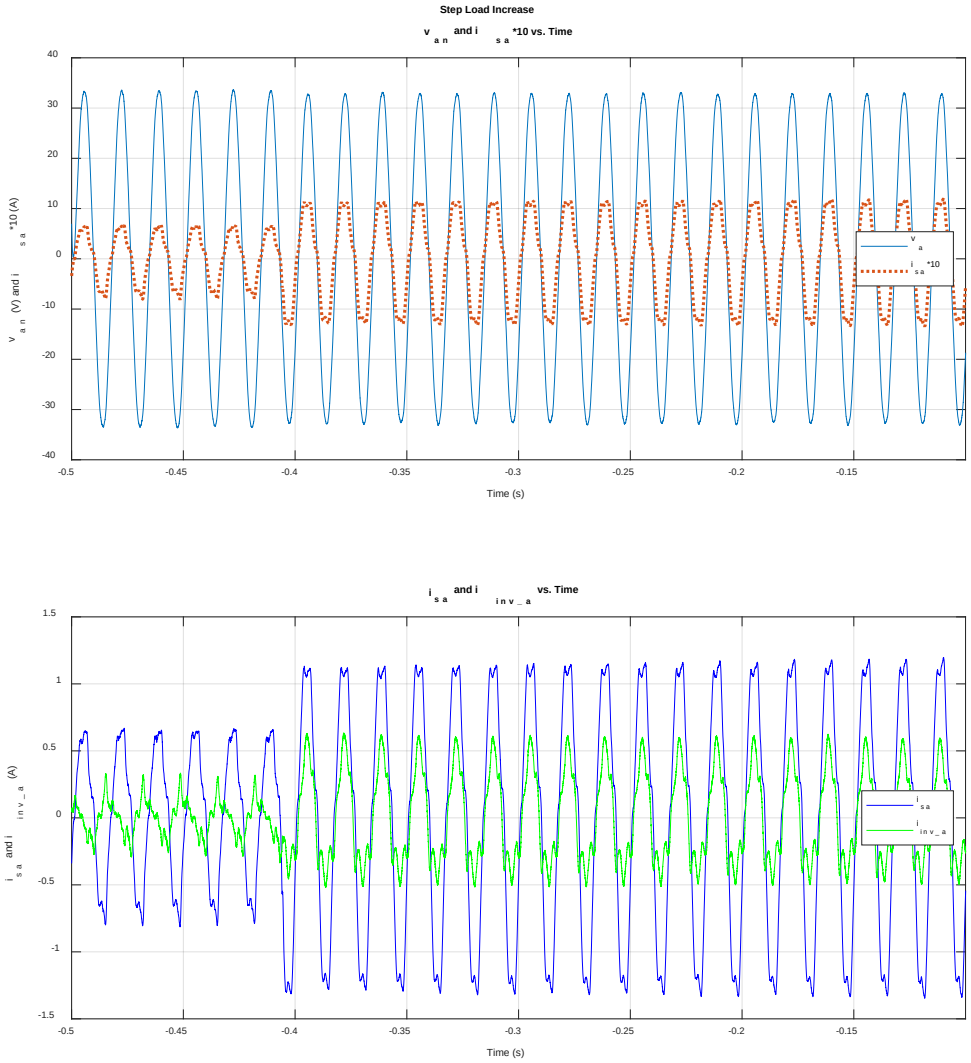


Figure 70. Step Load Increase – v_{an} and i_{sa} versus Time, isa and i_{inv_a} versus Time

Figure 71 analyzes the voltage spectrum of phase *A* voltage. The 5th harmonic is demonstrated to be the largest harmonic. The total harmonic distortion was calculated at 2.99%, which meets the MIL-STD-1399-300 specifications of Table 1, items 17 and 18.

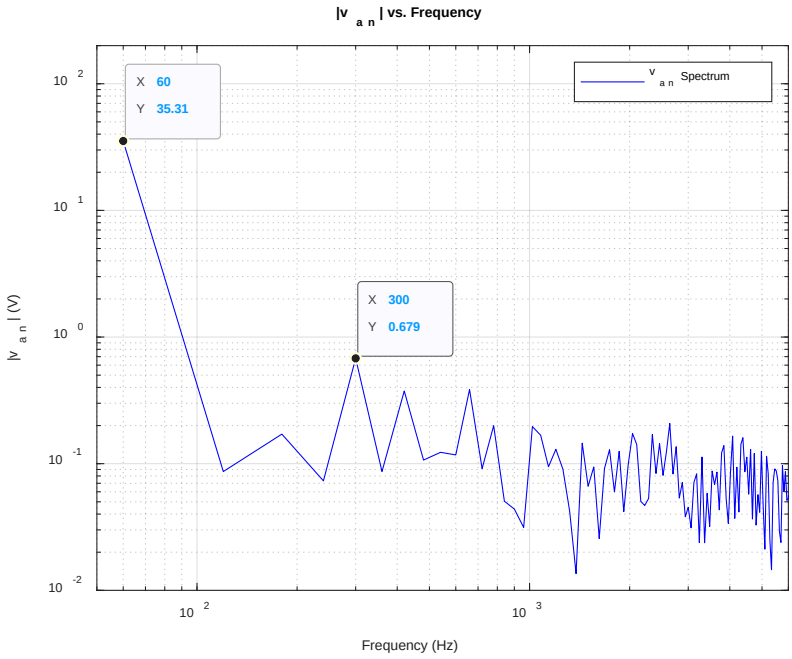


Figure 71. Step Load Increase – $|v_{an}|$ versus Frequency

Much of the low-frequency distortion seen in the experimental plots is caused by the harmonics in the grid voltage available in the laboratory. As a result of those harmonics, and the fact that measured source and inverter currents are used as inputs to the control system, the 5th harmonic is seen in the current waveforms presented in this section. Furthermore, the waveforms presented have had high-frequency noise, captured by the oscilloscope, removed prior to plotting. Filtering high-frequency harmonics reveals the low-frequency harmonics, such as the 5th, in the current and voltage waveforms plotted.

2. Load Step Off (18.7Ω to 56Ω)

This section examines the performance of the controller under a load step decrease. For reference, while looking at the following figures, the load step occurs near -0.38s. When the contactor for the additional load is turned off, the power drawn by the load decreases, the 28Ω resistor in parallel with the 56Ω load is removed, thus increasing the load resistance from 18.7Ω to 56Ω.

Figure 72 shows the measured value of the phase *A* line-to-neutral voltage as well as the inverter currents versus time. At the time of the load step, there is nearly no

observable change in voltage. The inverter currents, while near 0 initially, indicate that the controller is successfully driving the inverter power to 0 over time. Additionally, at the instant of the load step, the inverter currents jump, but it is important to note that the current is nearly 180 degrees out of phase with source voltage. This indicates that the VSI is now supplying power to the DC bus and is working as designed.

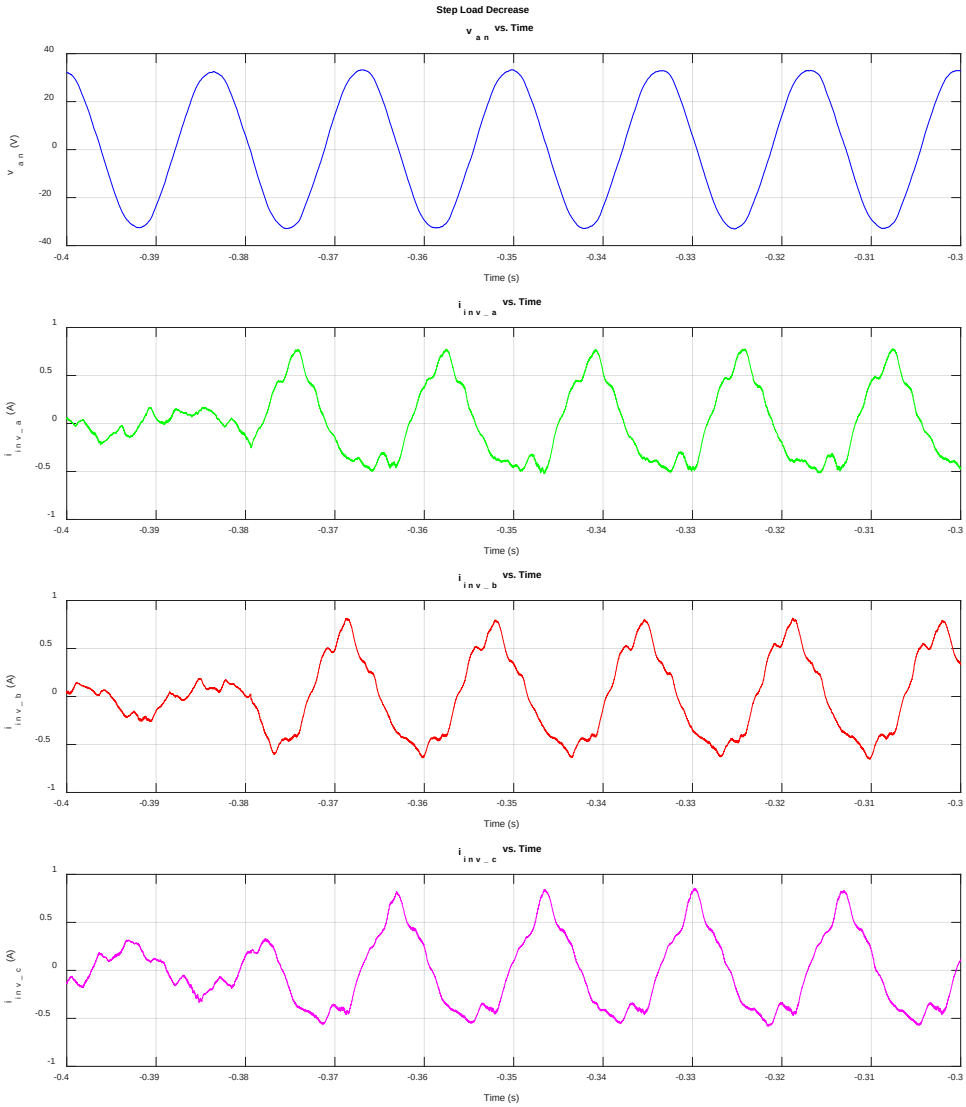


Figure 72. Step Load Decrease – v_{an} and inverter currents versus Time

Figure 73 shows v_{an} and $20xi_{inv\_a}$ overlaid, as well as the three inverter currents overlaid with each other. Figure 73 further shows that inverter current and voltage are out of phase with each other after the load is reduced, and power is now flowing from AC to DC in the VSI.

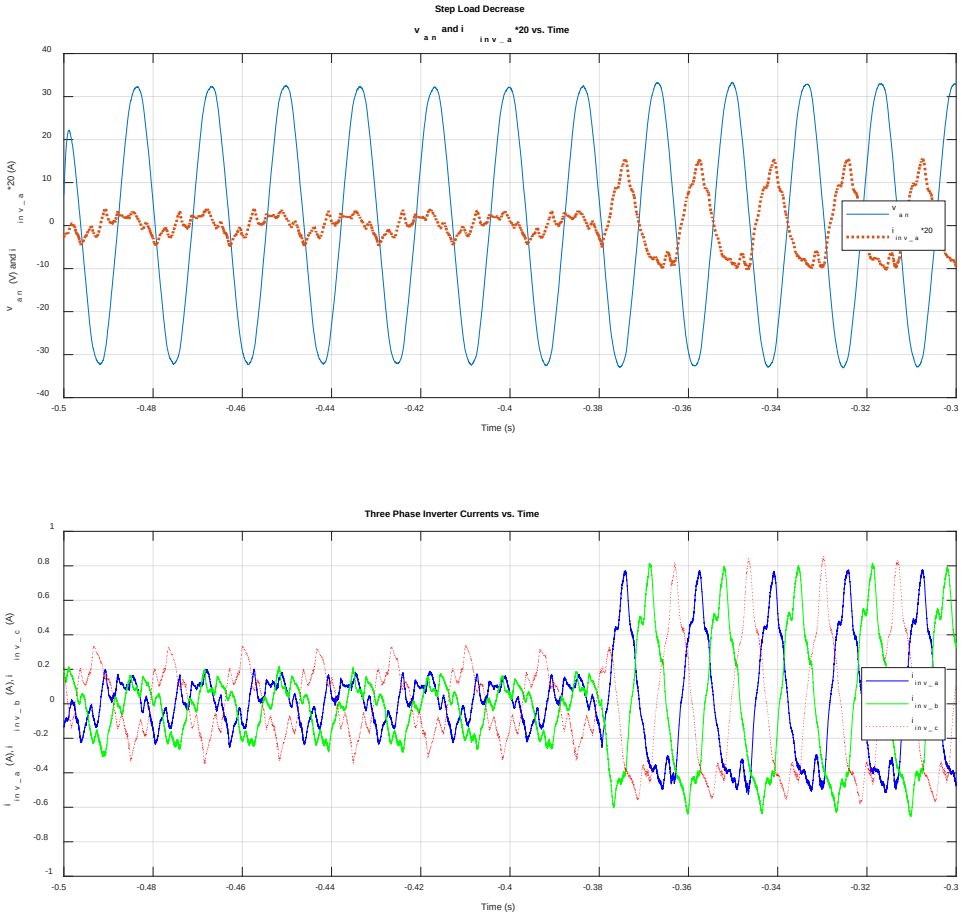


Figure 73. Step Load Decrease – v_{an} and i_{inv_a} versus Time, with i_{inv_abc} versus Time

Figure 74, Figure 75, and Figure 76 show the three-phase AC bus voltages versus time, three-phase source currents versus time, and three-phase inverter currents versus time, for the purpose of showing the gross changes over time. From Figure 74, one can see that voltage remains within two volts peak through the duration of the transient. Figure 75

shows that there is a drop in source current when the higher load is removed, then it rises slightly for the next 0.2s and finally drops. This rise is likely due to the PI gains of the current controller. Figure 76 shows the inverter currents jump as the load decreases, and then the currents begin to reduce afterward. As noted previously, the jump in current is because power flow has been reversed, as designed, through the VSI. The downward trend in source current and the out-of-phase and downward trend in inverter current, coupled with the discussion of Figure 73 shows power is flowing into the VSI to the DC bus and validates the desired response of the controller for a step load decrease. With the exception of the jump in source current and the slight sluggish change in current over time in the lab, the laboratory data validate the Simulink results.

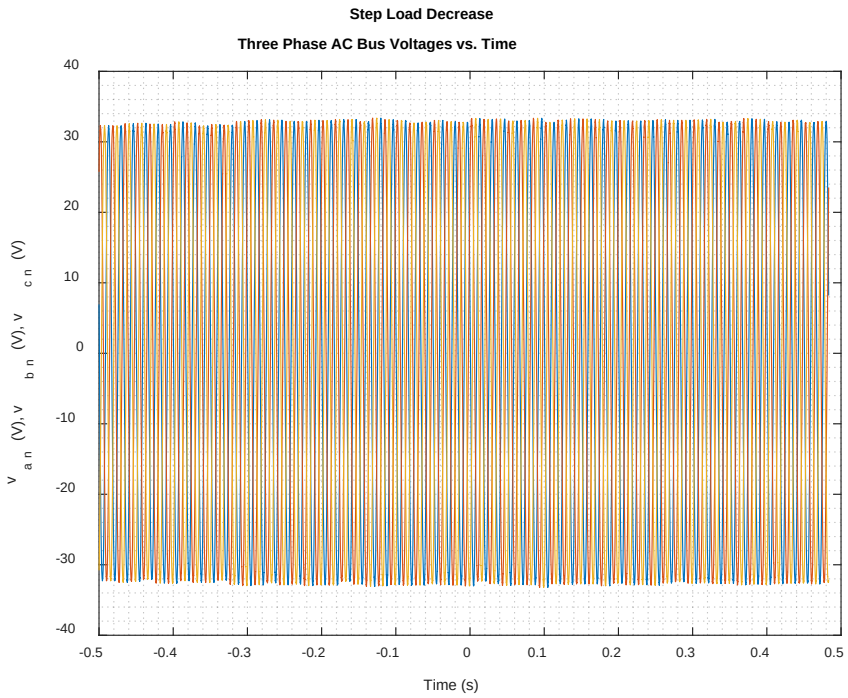
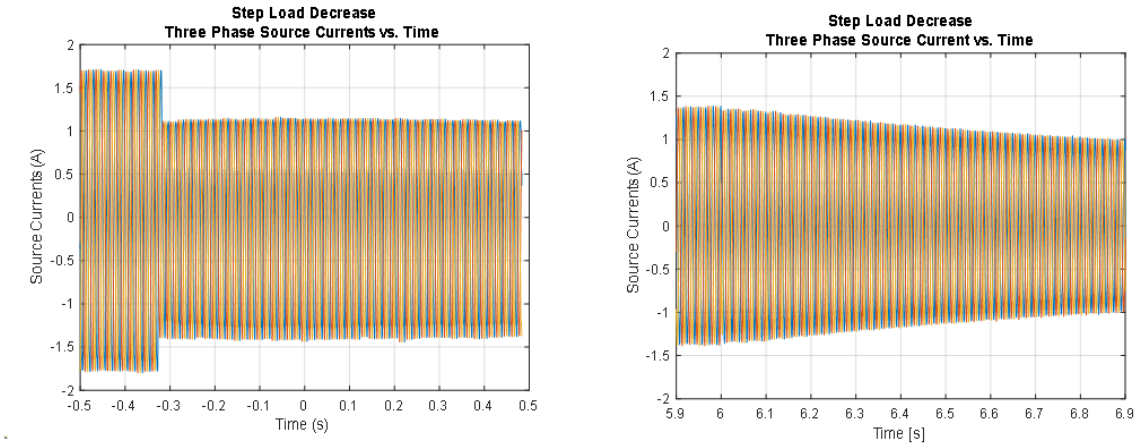
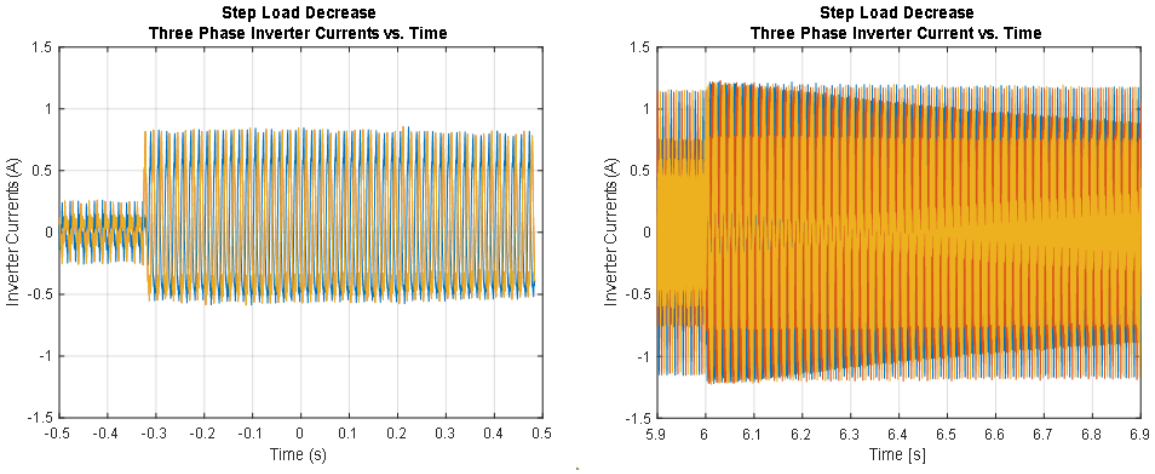


Figure 74. Step Load Decrease – Three Phase AC Bus Voltage versus Time



a) Experimental b) Simulation

Figure 75. Step Load Decrease – Three Phase Source Current versus Time



a) Experimental b) Simulation

Figure 76. Step Load Decrease – Three Phase Inverter Current versus Time

Figure 77 displays phase A data from Figure 74, Figure 75, and Figure 76. As noted previously, the inverter current is out of phase with source current and source voltage.

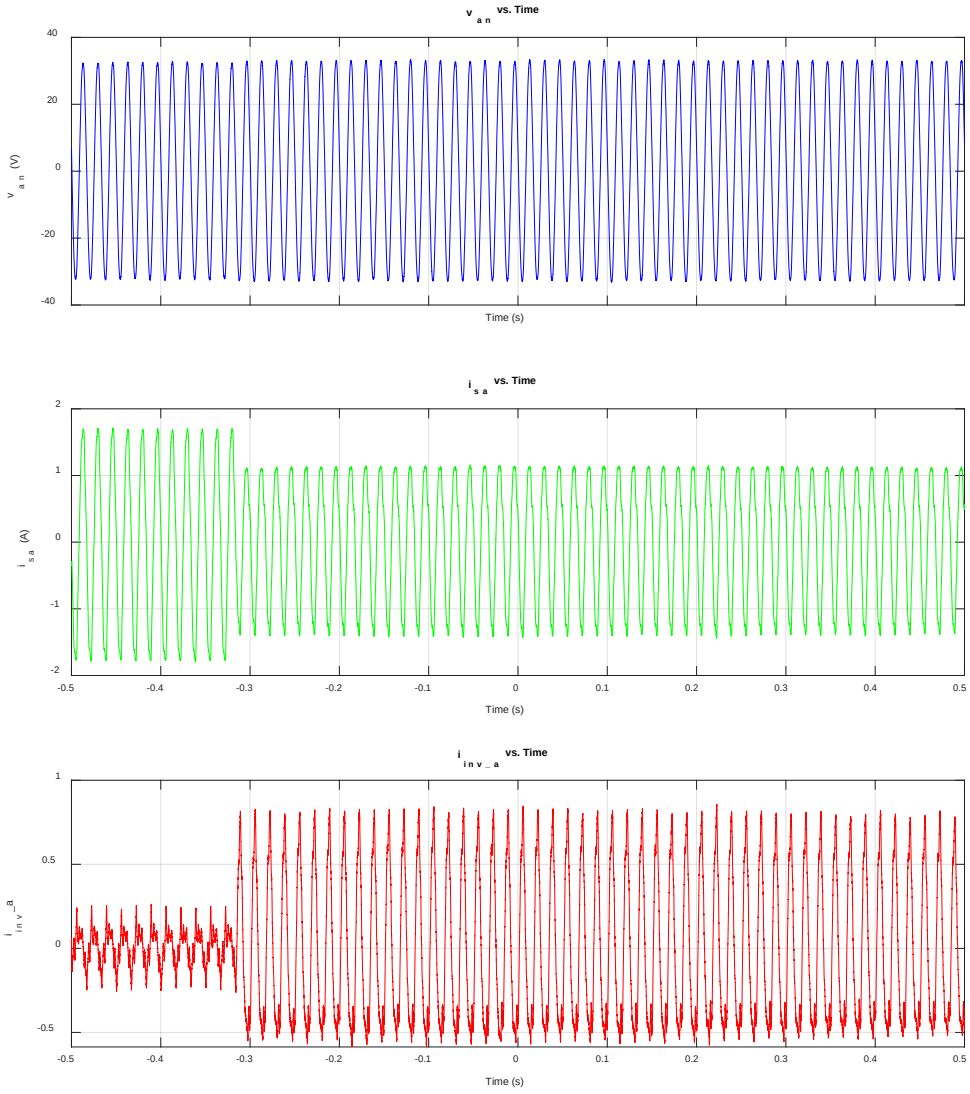
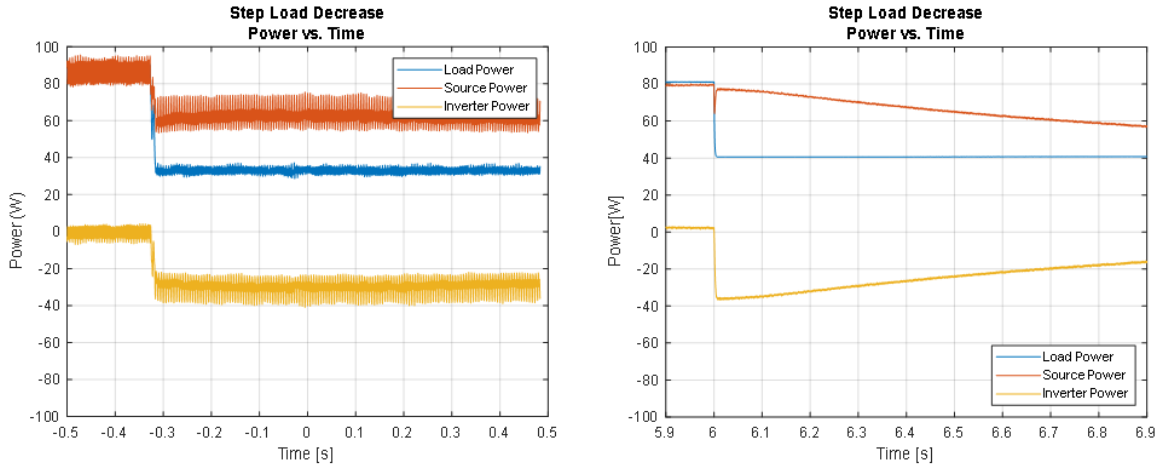


Figure 77. Step Load Decrease – v_{an}, i_{sa}, i_{inv_a} versus Time

Figure 78 also helps to validate the desired response from the P-Q controller by showing the load power, the power delivered by the source, and the power delivered by the inverter. Initially, the inverter is producing on average 0W, indicating that all load power is coming from the source, as designed. At the instant the load is reduced, the inverter power goes negative, allowing the source to supply more power than just the load. This effect validates the desired results from the model, in that the source can more slowly

respond to a large drop in load, which could possibly prevent an overspeed condition. Following the step reduction in load, there is a trend in inverter power towards 0W, as well as a trend in source power down to the load power. Aside from the slightly slower response in the laboratory, the Simulink model is validated by the hardware results.



a) Experimental b) Simulation

Figure 78. Step Load Decrease – Power versus Time

Figure 79 demonstrates that Q control is working for a step load decrease. The desired reactive power from the source is 0VAR. Figure 79 (top) shows that the source current and the source voltage are entirely in phase before and after the step load; consequently, the 'grid' continues to see a unity power factor. Figure 70 (bottom) shows that initially inverter current slightly leads the source current likely due to the fact the L_f causes the AC bus power factor to lag. Since Figure 78 shows that inverter power is initially near 0W, this is the only reason why the inverter current would not be in phase with the source current initially. After the step, the source current is nearly 180 out of phase with the inverter current, and since the source voltage and the source current are in phase, the power flow is definitively from AC to DC through the VSI.

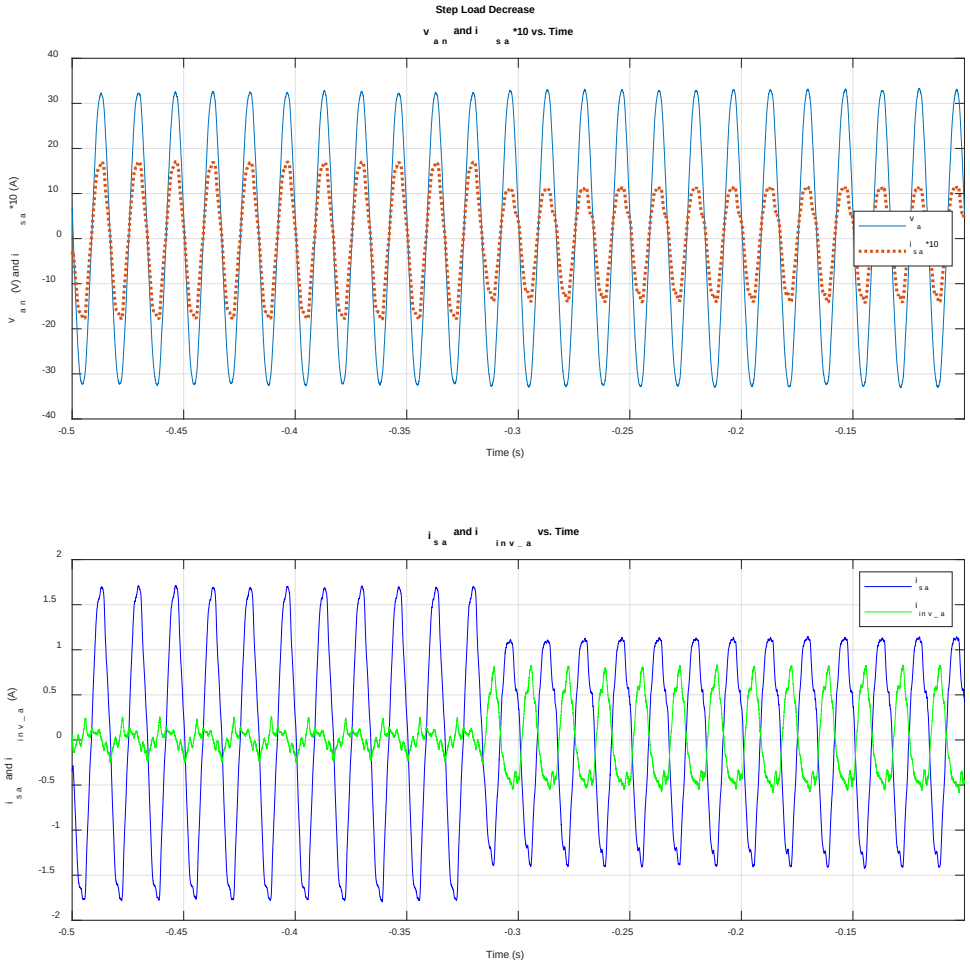


Figure 79. Step Load Decrease – v_{an} and i_{sa} versus Time, isa and i_{inv_a} versus Time

Figure 80 analyzes the voltage spectrum of phase A voltage. The 5th harmonic is demonstrated to be the largest harmonic. The total harmonic distortion was calculated at 3.21%, with the largest single harmonic distortion of 2.25%, which meets the MIL-STD=1399 specification of Table 1, items 17 and 18.

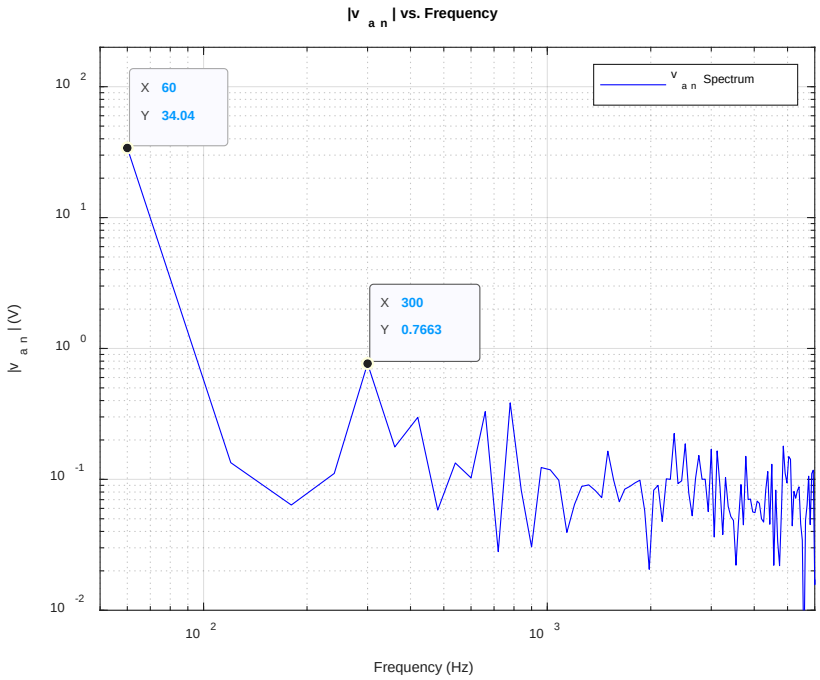


Figure 80. Step Load Decrease – $|v_{an}|$ versus Frequency

Again, the low-frequency distortion seen is likely caused by the harmonics in the grid voltage available in the laboratory. Feeding measured values, containing the 5^{th} harmonic into the control system, results in some difficulty controlling the active power. Note that the plots presented in this section have been filtered to remove high-frequency noise and emphasize the low-frequency harmonics in the waveforms.

VI. CONCLUSION AND FUTURE WORK

A. CONCLUSION

This thesis presents the design, implementation, and experimental validation of a novel three-phase VSI controller, which allows P-Q flow control. Through simulations, the power on a source (generator) was shown to respond slowly to step changes, as the VSI compensated for load steps that cause jumps in power. Additionally, the reactive power is controlled such that the grid saw a unity power factor, despite the change in load. In the laboratory, an experimental system was designed and implemented to test the controller in real-time. While the operating power was much lower than that for the requirements of Type I power, the P-Q control functionality of the controller was proven to work as designed in the scaled-down experimental set-up.

For a step increase in load, the VSI supplied real power to the grid, reducing the real power required from the grid. The real power was then allowed to increase on the grid and reduce on the VSI slowly. Both before and after the step changes, \ Q was controlled to 0 VARS, maintaining unity power factor on the grid. Additionally, for a step decrease in load, it was shown that the VSI began supplying real power back to the DC bus, allowing the grid to more slowly reduce the power it was required to supply than if the VSI was not present. Again, before and after the transient Q was controlled near 0, and unity grid PF was attained at the grid.

Finally, the controller functionality was validated on a scaled-down laboratory set up. The laboratory results demonstrate that the important goal of developing a P-Q controller for a VSI that can minimize abrupt changes in grid-supplied power, while achieving unity grid PF, was definitively achieved. Some difficulty in control of the system did arise as a result of introducing the 5^{th} harmonic into the control system. Removing the 5^{th} harmonic would likely improve the hardware implementation, allowing the source and inverter powers to more closely match the simulated results.

B. FUTURE WORK

As nearly every naval ship and Marine FOB operates on a three-phase grid, there are many directions in which this research can continue in order to benefit the Department of the Navy and Department of Defense.

Harmonic rejection within the control system should be studied. It is hypothesized that removing significant harmonics on the measured voltage and current waveforms could significantly improve the control system operation.

This thesis used only batteries to simulate DERs, but future work could include implementing DERs (photovoltaic cells, wind turbines, etc.) to evaluate their performance and integration with the VSI. Additionally, the effects on grid frequency were not examined, but this could be an important direction for this research to continue as many generators operate with frequency droop load control. Also, large loads starting can reduce grid frequency, so these effects can be studied.

As mentioned, the hardware implementation of the system was not operated at Type I voltages. Accordingly, this controller should be tested at those voltages to validate the applicability of the controller to the DOD. Additionally, larger loads, including actual motors, should be tested. One final direction of research could include improving the controller such that P-Q control can occur as presently designed, but while allowing an operator or automated system to continue to charge a battery or other electrical energy storage device.

APPENDIX. MATLAB CODE

A. SIMULATION PARAMETERS

1. 200V_{rms} Multi-Step

```
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Simulation Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
tstep=1e-6;
%tstep=0.5e-7; %for PWM VSI
ideal_source=1; %0 for PWM VSI, 1 for ideal
f_fund = 60; %fundamental frequency in Hz
tstop=15; %tstop*f_fund should be divisible by 4 for plotting
omega=2*pi*60;
MIL_STD_LOAD_ENABLE=0; %1 makes the load profile >50kW, if 0 <3500W
decimation=1; %write data every 2nd time step

%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Buck Boost Converter Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Kp_boost= .2*10;
Ki_boost=4*10;
sw_freqB=12000; %DC/DC Converter Switching Frequency
Vbatt=96; % battery voltage [V]
VDCref = 450; % reference voltage for boost output [V]

Cboost=2200*10^-6*100; %DC Bus capacitor (F)
Lbuck=330*1000*10^-6; %Buck/Boost Indutance (H)
Lboost=Lbuck;

%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***VSI Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Vref=200*sqrt(2/3); %Peak Phase Voltage (Type I 200Vrms or  440Vrms)
Kp_i=1;     %current PI gain is amplified to account for the SV modulation scaling
Ki_i=10;    %Current control loop gain
Kp_v=.2;
Ki_v=20;
%Initial conditions help start the simulation near steady state
Ki_i_icq=.6*VDCref/sqrt(3);
Ki_i_icd=0;
Ki_v_icq=.65;
Ki_v_icd=-2.5;
%abc to qd0 transformation in the stationary frame
Ks=2/3*[1 -1/2 -1/2;0 -sqrt(3)/2 sqrt(3)/2;1/2 1/2 1/2];
Tsw = 100e-6; %VSI switching frequency 10kHz
Lf=440e-6; %VSI Filter inductance (H)
Cf= 20e-6; %VSI Filter capacitance (F)
%For SVM Sector Selection
sector_matrix = [1 0 0 0 0 0;...
                 0 2 0 0 0 0;...
                 0 0 3 0 0 0;...
                 0 0 0 4 0 0;...
                 0 0 0 0 5 0;...
                 0 0 0 0 0 6];
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Grid Model Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%Matrices for Current/Voltages on Grid
Amat_indI = zeros(2);
Bmat_indI = inv([Lf -Lf;Lf Lf+Lf]);
Cmat_indI = [1 0 ;0 1 ;-1 -1 ];    %Ic = -Ia-Ib
Dmat_indI = zeros(3,2);
Amat_caps = zeros(3);
```

```
Bmat_caps = [1/Cf 0 0; 0 1/Cf 0; 0 0 1/Cf];
Cmat_caps = eye(3);
Dmat_caps = zeros(3);
%Load Step Times %Reference MIL-STD-300
tstep1=1.5;
tstep2=2.75;
tstep3=4.25;
tstep4=5.5;
tstep5=7;
tstep6=7.5;
tstep7=8.75;
tstep8=10.5;
tstep9=11;
tstep10=12.25;
tstep11=13.5;
tstep12=13.75;
tstep13=15;
```

2. 200V_{rms} Single-Step

```
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Simulation Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
tstep=1e-6;
%tstep=0.5e-7; %for PWM VSI
ideal_source=1; %0 for PWM VSI, 1 for ideal
f_fund = 60; %fundamental frequency in Hz
tstop=15; %tstop*f_fund should be divisible by 4 for plotting
omega=2*pi*60;
MIL_STD_LOAD_ENABLE=0; %1 makes the load profile >50kW, if 0 <3500W
decimation=1; %write data every 2nd time step

%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Buck Boost Converter Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Kp_boost= .2*10;
Ki_boost=4*10;
sw_freqB=12000; %DC/DC Converter Switching Frequency
Vbatt=96; % battery voltage [V]
VDCref = 450; % reference voltage for boost output [V]

Cboost=2200*10^-6*100; %DC Bus capacitor (F)
Lbuck=330*1000*10^-6; %Buck/Boost Indutance (H)
Lboost=Lbuck;

%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***VSI Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Vref=200*sqrt(2/3); %Peak Phase Voltage (Type I 200Vrms or  440Vrms)
Kp_i=1;     %current PI gain is amplified to account for the SV modulation scaling
Ki_i=10;    %Current control loop gain
Kp_v=.2;
Ki_v=20;
%Initial conditions help start the simulation near steady state
Ki_i_icq=.6*VDCref/sqrt(3);
Ki_i_icd=0;
Ki_v_icq=.65;
Ki_v_icd=-2.5;
%abc to qd0 transformation in the stationary frame
Ks=2/3*[1 -1/2 -1/2;0 -sqrt(3)/2 sqrt(3)/2;1/2 1/2 1/2];
Tsw = 100e-6; %VSI switching frequency 10kHz
Lf=440e-6; %VSI Filter inductance (H)
Cf= 20e-6; %VSI Filter capacitance (F)
%For SVM Sector Selection
sector_matrix = [1 0 0 0 0 0;...
                 0 2 0 0 0 0;...
                 0 0 3 0 0 0;...
                 0 0 0 4 0 0;...
```

```
                0 0 0 0 5 0;...
                0 0 0 0 0 6];
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Grid Model Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%Matrices for Current/Voltages on Grid
Amat_indI = zeros(2);
Bmat_indI = inv([Lf -Lf;Lf Lf+Lf]);
Cmat_indI = [1 0 ;0 1 ;-1 -1 ];    %Ic = -Ia-Ib
Dmat_indI = zeros(3,2);
Amat_caps = zeros(3);
Bmat_caps = [1/Cf 0 0; 0 1/Cf 0; 0 0 1/Cf];
Cmat_caps = eye(3);
Dmat_caps = zeros(3);

%Load Step Times
tstep1=3;
tstep2=6;
tstep3=9;
tstep4=12;
tstep5=15;
```

3. 440V_{rms} Multi-Step

Note: Only changes to the 200V_{rms} simulation parameters are listed.

```
MIL_STD_LOAD_ENABLE=1; %1 makes the load profile >50kW, if 0 <3500W
Vbatt=300; % battery voltage [V]
VDCref = 900; % reference voltage for boost output [V]
Vref=440*sqrt(2/3); %Peak Phase Voltage (Type I 200Vrms or  440Vrms)
Kp_i=10; %current PI gain is amplified to account for the SV modulation scaling
Ki_i=100; %Current control loop gain
Kp_v=.67*4;
Ki_v=60*4;
Lf=800e-6*3; %VSI Filter inductance (H)
Cf= 20e-6*2; %VSI Filter capacitance (F)
```

4. Simulation with Laboratory Parameters

```
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Simulation Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
tstep=.5e-6;
ideal_source=0; %0 for PWM VSI, 1 for ideal
f_fund = 60; %fundamental frequency in Hz
tstop=15; %tstop*f_fund should be divisible by 4 for plotting
omega=2*pi*60;
MIL_STD_LOAD_ENABLE=0; %1 makes the load profile >50kW, if 0 <3500W
decimation=1; %write data every 2nd time step

%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Buck Boost Converter Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Kp_boost= .2*10/2;
Ki_boost=4*10/2;
sw_freqB=12000; %DC/DC Converter Switching Frequency
Vbatt=36; % battery voltage [V]
VDCref = 80; % reference voltage for boost output [V]

Cboost=3200*10^-6; %DC Bus capacitor (F)
Lbuck=232*10^-6; %Buck/Boost Indutance (H)
Lboost=Lbuck;

%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
%***VSI Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Vref=48*sqrt(2/3); %Peak Phase Voltage (Type I 200Vrms or  440Vrms)
Kp_i=5;     %current PI gain is amplified to account for the SV modulation scaling
Ki_i=10;    %Current control loop gain
Kp_v=.2;
Ki_v=20;
%Initial conditions help start the simulation near steady state
Ki_i_icq=.6*VDCref/sqrt(3);
Ki_i_icd=0;
Ki_v_icq=.65;
Ki_v_icd=-2.5;
%abc to qd0 transformation in the stationary frame
Ks=2/3*[1 -1/2 -1/2;0 -sqrt(3)/2 sqrt(3)/2;1/2 1/2 1/2];
Tsw = 100e-6; %VSI switching frequency 10kHz
Lf=0.3e-3*2; %VSI Filter inductance (H) [(2) 0.3mH Inductors in Series]
Cf= 15e-6; %VSI Filter capacitance (F)
%For SVM Sector Selection
sector_matrix = [1 0 0 0 0 0;...
                 0 2 0 0 0 0;...
                 0 0 3 0 0 0;...
                 0 0 0 4 0 0;...
                 0 0 0 0 5 0;...
                 0 0 0 0 0 6];
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%***Grid Model Parameters
%~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
%Matrices for Current/Voltages on Grid
Amat_indI = zeros(2);
Bmat_indI = inv([Lf -Lf;Lf Lf+Lf]);
Cmat_indI = [1 0 ;0 1 ;-1 -1 ];    %Ic = -Ia-Ib
Dmat_indI = zeros(3,2);
Amat_caps = zeros(3);
Bmat_caps = [1/Cf 0 0; 0 1/Cf 0; 0 0 1/Cf];
Cmat_caps = eye(3);
Dmat_caps = zeros(3);

%Load Step Times %Reference MIL-STD-300
tstep1=3;
tstep2=6;
```

B. PLOTTING

1. 200V_{rms} Multi-Step

```
num_cyc=1;
length_v=round((num_cyc/f_fund)/tstep);
length_vector=length(out.Vabc(:,1));
ti=out.time(length_vector-length_v+1:length_vector);

vab=out.Vabc(:,1)-out.Vabc(:,2);
vbc=out.Vabc(:,2)-out.Vabc(:,3);
vca=out.Vabc(:,3)-out.Vabc(:,1);
vab_ss=vab(length_vector-length_v+1:length_vector);
vbc_ss=vbc(length_vector-length_v+1:length_vector);
vca_ss=vca(length_vector-length_v+1:length_vector);
vab_spect= fft(vab_ss)/round(length_v/2);
freq=[0:round(length_v/2)-1]*f_fund/num_cyc;

iLa=out.Iabc(:,1);
iLb=out.Iabc(:,2);
iLc=out.Iabc(:,3);
iLa_ss=iLa(length_vector-length_v+1:length_vector);
iLb_ss=iLb(length_vector-length_v+1:length_vector);
iLc_ss=iLc(length_vector-length_v+1:length_vector);
```

```
iLa_spect= fft(iLa_ss)/round(length_v/2);

iinva_ss=out.Iabc_inv(length_vector-length_v+1:length_vector,1);
iinvb_ss=out.Iabc_inv(length_vector-length_v+1:length_vector,2);
iinvc_ss=out.Iabc_inv(length_vector-length_v+1:length_vector,3);

iasource_ss = out.Iabc_source(length_vector-length_v+1:length_vector,1);
iasource_spect= fft(iasource_ss)/round(length_v/2);

figure(1)
plot(ti,vab_ss,'b')
hold on;
plot(ti,vbc_ss,'g')
plot(ti,vca_ss,'r')
xlabel('time [s]')
ylabel('Output voltages [V]')
grid
title("Line to Line Capacitor Voltages:Final Cycle vs. Time");
legend('v_a','v_b','v_c');

figure(2)
plot(ti,iinva_ss,'b')
hold on;
plot(ti,iinvb_ss,'g')
plot(ti,iinvc_ss,'r')
hold off;
xlabel('Time [s]')
ylabel('Output Inverter currents [A]')
grid
title("Inverter currents:Final Cycle vs. Time");
legend('i_a','i_b','i_c');


figure(3)
loglog(freq,abs(vab_spect(1:length(freq))),'linewidth',2);
grid on
title('Output Line to Line Voltage Spectrum');
ylabel('Peak Voltage Amplitude [V]');
xlabel('frequency [Hz]');

figure(4)
loglog(freq,abs(iLa_spect(1:length(freq))),'linewidth',2);
grid on
title('Load Current Spectrum');
ylabel('Peak Current Amplitude [A]');
xlabel('frequency [Hz]');

disp(['iL_rms = '  num2str(sqrt( mean(iLa_ss.^2)))]);
disp(['vab_rms = ' num2str(sqrt( mean(vab_ss.^2)))]);

% figure(5)
% plot(out.time,out.Vabc_source(:,1)/10,'b')
% hold on;
% plot(out.time,out.Vabc_source(:,2)/10,'g')
% plot(out.time,out.Vabc_source(:,3)/10,'r')
% plot(out.time,out.Iabc_source(:,1),'b:')
% plot(out.time,out.Iabc_source(:,2),'g:')
% plot(out.time,out.Iabc_source(:,3),'r:')
% hold off;
% xlim([tstop-3/60 tstop]);
% ylim([-60 60]);
% grid;
% title('Source V/10 and I: end of simulation');
% xlabel('Time [s]')
% ylabel('Source Voltage/10 [V] and Current [A]')


figure(6)
plot(out.time,out.Vabc_source(:,1)/10)
```

```
hold on;
plot(out.time,out.Vabc_source(:,2)/10)
plot(out.time,out.Vabc_source(:,3)/10)
plot(out.time,out.Iabc_source(:,1), 'Color', '#0072BD', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,2), 'Color', '#D95319', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,3), 'Color', '#EDB120', 'LineStyle', '-.')
hold off;
xlim([0.01 9/60]);
grid;
title('Source V/10 and I: beginning of simulation');
xlabel('Time [s]')
ylabel('Source Voltage/10 [V] and Current [A]')
legend('V_a/10', 'V_b/10', 'V_c/10', 'I_a', 'I_b', 'I_c')


figure(7)
plot(out.time,out.Vabc_source(:,1)/10)
hold on;
plot(out.time,out.Vabc_source(:,2)/10)
plot(out.time,out.Vabc_source(:,3)/10)
plot(out.time,out.Iabc_source(:,1), 'Color', '#0072BD', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,2), 'Color', '#D95319', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,3), 'Color', '#EDB120', 'LineStyle', '-.')
hold off;
xlim([2.75-3/60 2.75+3/60]);
grid;
title('Source V/10 and I: at 2.75s Step');
xlabel('Time [s]')
ylabel('Source Voltage/10 [V] and Current [A]')
legend('V_a/10', 'V_b/10', 'V_c/10', 'I_a', 'I_b', 'I_c')

figure(8)
subplot(3,1,1)
plot(out.time, out.Iabc)
title({'Step Load Increase at 1.5 Seconds' 'Iabc_l_o_a_d vs. Time'})
xlabel('Time [s]')
ylabel('Load Current [A]')
xlim([1.5-3/60 1.5+3/60])
subplot(3,1,2)
plot(out.time, out.Iabc_inv)
xlim([1.5-3/60 1.5+3/60])
title('Iabc_i_n_v vs. Time')
xlabel('Time [s]')
ylabel('Inverter Current [A]')
subplot(3,1,3)
plot(out.time, out.Iabc_source)
title('Iabc_s_r_c vs. Time')
xlim([1.5-3/60 1.5+3/60])
xlabel('Time [s]')
ylabel('Source Current [A]')


figure(9)
subplot(3,1,1), plot(out.time,out.Q_load)
xlabel('time [s]')
ylabel('Q_l_o_a_d [VAR]')
grid minor
axis([0 15 -600 3000])
title({'Reactive Power vs. Time' 'Load'})
subplot(3,1,2), plot(out.time,out.Q_src)
xlabel('time [s]')
ylabel('Q_s_r_c [VAR]')
grid minor
title({'Reactive Power vs. Time' 'Source'})
axis([0 15 -600 3000])
subplot(3,1,3), plot(out.time,out.Q_inv)
xlabel('time [s]')
ylabel('Q_i_n_v [VAR]')
grid minor
```

```
axis([0 15 -600 3000])
title({'Reactive Power vs. Time' 'Inverter'})

figure(10)
subplot(3,1,1), plot(out.time,out.P_load)
xlabel('time [s]')
ylabel('P_l_o_a_d [W]')
grid minor
axis([0 15 -1500 4000])
title({'Real Power vs. Time' 'Load'})
subplot(3,1,2), plot(out.time,out.P_src)
xlabel('time [s]')
ylabel('P_s_r_c [W]')
grid minor
title({'Real Power vs. Time' 'Source'})
axis([0 15 -1500 4000])
subplot(3,1,3), plot(out.time,out.P_inv)
xlabel('time [s]')
ylabel('P_i_n_v [W]')
grid minor
axis([0 15 -1500 4000])
title({'Real Power vs. Time' 'Inverter'})

figure(11)
subplot(3,1,1)
plot(out.time, out.Iabc)
title({'Step Load Decrease at 2.75 Seconds' 'Iabc_l_o_a_d vs. Time'})
xlabel('Time [s]')
ylabel('Load Current [A]')
xlim([2.75-3/60 2.75+3/60])
subplot(3,1,2)
plot(out.time, out.Iabc_inv)
xlim([2.75-3/60 2.75+3/60])
title('Iabc_i_n_v vs. Time')
xlabel('Time [s]')
ylabel('Inverter Current [A]')
subplot(3,1,3)
plot(out.time, out.Iabc_source)
title('Iabc_s_r_c vs. Time')
xlim([2.75-3/60 2.75+3/60])
xlabel('Time [s]')
ylabel('Source Current [A]')

figure(12)
subplot(2,1,1)
plot(out.time, out.Vabc)
xlim([1.5-3/60 1.5+3/60])
title('Phase Voltage vs. Time')
xlabel('Time [s]')
ylabel('Phase Voltage [V]')
subplot(2,1,2)
plot(out.time, out.Vabc)
xlim([2.75-3/60 2.75+3/60])
xlabel('Time [s]')
ylabel('Phase Voltage [V]')

figure(13)
plot(out.tout, out.Vbus')
title('DC Bus Voltage vs. Time')
ylabel('V_D_C [V]')
xlabel('Time [s]')
grid minor
ylim([430 470])

vab_THD_pct = 100*sqrt(sum(abs(vab_spect(3:1:400)).^2)/abs(vab_spect(2)).^2);
disp(['THD only includes muliples of 60 Hz. >> THD = ' num2str(vab_THD_pct,3) ' %'])
van=out.Vabc(:,1);
van_ss=van(length_vector-length_v+1:length_vector);
van_spect= fft(van_ss)/round(length_v/2);
```

```
DPF_V_over_I=cos(angle(van_spect(2)/iasource_spect(2)));
disp(['cosine of angle between Van and ILa = ' num2str(DPF_V_over_I,3)])
```

2. 200V_{rms} Single-Step

```
num_cyc=1;
length_v=round((num_cyc/f_fund)/tstep);
length_vector=length(out.Vabc(:,1));
ti=out.time(length_vector-length_v+1:length_vector);

vab=out.Vabc(:,1)-out.Vabc(:,2);
vbc=out.Vabc(:,2)-out.Vabc(:,3);
vca=out.Vabc(:,3)-out.Vabc(:,1);
vab_ss=vab(length_vector-length_v+1:length_vector);
vbc_ss=vbc(length_vector-length_v+1:length_vector);
vca_ss=vca(length_vector-length_v+1:length_vector);
vab_spect= fft(vab_ss)/round(length_v/2);
freq=[0:round(length_v/2)-1]*f_fund/num_cyc;

iLa=out.Iabc(:,1);
iLb=out.Iabc(:,2);
iLc=out.Iabc(:,3);
iLa_ss=iLa(length_vector-length_v+1:length_vector);
iLb_ss=iLb(length_vector-length_v+1:length_vector);
iLc_ss=iLc(length_vector-length_v+1:length_vector);
iLa_spect= fft(iLa_ss)/round(length_v/2);

iinva_ss=out.Iabc_inv(length_vector-length_v+1:length_vector,1);
iinvb_ss=out.Iabc_inv(length_vector-length_v+1:length_vector,2);
iinvc_ss=out.Iabc_inv(length_vector-length_v+1:length_vector,3);

iasource_ss = out.Iabc_source(length_vector-length_v+1:length_vector,1);
iasource_spect= fft(iasource_ss)/round(length_v/2);

figure(1)
plot(ti,vab_ss,'b')
hold on;
plot(ti,vbc_ss,'g')
plot(ti,vca_ss,'r')
xlabel('time [s]')
ylabel('Output voltages [V]')
grid
title("Line to Line Capacitor Voltages:Final Cycle vs. Time");
legend('v_a','v_b','v_c');

figure(2)
plot(ti,iinva_ss,'b')
hold on;
plot(ti,iinvb_ss,'g')
plot(ti,iinvc_ss,'r')
hold off;
xlabel('Time [s]')
ylabel('Output Inverter currents [A]')
grid
title("Inverter currents:Final Cycle vs. Time");
legend('i_a','i_b','i_c');


figure(3)
loglog(freq,abs(vab_spect(1:length(freq))),'linewidth',2);
grid on
title('Output Line to Line Voltage Spectrum');
ylabel('Peak Voltage Amplitude [V]');
xlabel('frequency [Hz]');

figure(4)
loglog(freq,abs(iLa_spect(1:length(freq))),'linewidth',2);
```

```
grid on
title('Load Current Spectrum');
ylabel('Peak Current Amplitude [A]');
xlabel('frequency [Hz]');

disp(['iL_rms = '  num2str(sqrt( mean(iLa_ss.^2)))]);
disp(['vab_rms = ' num2str(sqrt( mean(vab_ss.^2)))]);

% figure(5)
% plot(out.time,out.Vabc_source(:,1)/10,'b')
% hold on;
% plot(out.time,out.Vabc_source(:,2)/10,'g')
% plot(out.time,out.Vabc_source(:,3)/10,'r')
% plot(out.time,out.Iabc_source(:,1),'b:')
% plot(out.time,out.Iabc_source(:,2),'g:')
% plot(out.time,out.Iabc_source(:,3),'r:')
% hold off;
% xlim([tstop-3/60 tstop]);
% ylim([-60 60]);
% grid;
% title('Source V/10 and I: end of simulation');
% xlabel('Time [s]')
% ylabel('Source Voltage/10 [V] and Current [A]')


figure(6)
plot(out.time,out.Vabc_source(:,1)/10)
hold on;
plot(out.time,out.Vabc_source(:,2)/10)
plot(out.time,out.Vabc_source(:,3)/10)
plot(out.time,out.Iabc_source(:,1), 'Color', '#0072BD', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,2), 'Color', '#D95319', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,3), 'Color', '#EDB120', 'LineStyle', '-.')
hold off;
xlim([0.01 9/60]);
grid;
title('Source V/10 and I: beginning of simulation');
xlabel('Time [s]')
ylabel('Source Voltage/10 [V] and Current [A]')
legend('V_a/10', 'V_b/10', 'V_c/10', 'I_a', 'I_b', 'I_c')


figure(7)
plot(out.time,out.Vabc_source(:,1)/10)
hold on;
plot(out.time,out.Vabc_source(:,2)/10)
plot(out.time,out.Vabc_source(:,3)/10)
plot(out.time,out.Iabc_source(:,1), 'Color', '#0072BD', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,2), 'Color', '#D95319', 'LineStyle', '-.')
plot(out.time,out.Iabc_source(:,3), 'Color', '#EDB120', 'LineStyle', '-.')
hold off;
xlim([3-3/60 3+3/60]);
grid;
title('Source V/10 and I: at 3s Step');
xlabel('Time [s]')
ylabel('Source Voltage/10 [V] and Current [A]')
legend('V_a/10', 'V_b/10', 'V_c/10', 'I_a', 'I_b', 'I_c')

figure(8)
subplot(3,1,1)
plot(out.time, out.Iabc)
title({'Step Load Increase at 3 Seconds' 'Iabc_l_o_a_d vs. Time'})
xlabel('Time [s]')
ylabel('Load Current [A]')
xlim([3-3/60 3+3/60])
subplot(3,1,2)
plot(out.time, out.Iabc_inv)
xlim([3-3/60 3+3/60])
title('Iabc_i_n_v vs. Time')
```

```
xlabel('Time [s]')
ylabel('Inverter Current [A]')
subplot(3,1,3)
plot(out.time, out.Iabc_source)
title('Iabc_s_r_c vs. Time')
xlim([3-3/60 3+3/60])
xlabel('Time [s]')
ylabel('Source Current [A]')


figure(9)
subplot(3,1,1), plot(out.time,out.Q_load)
xlabel('time [s]')
ylabel('Q_l_o_a_d [VAR]')
grid minor
axis([0 15 -600 3000])
title({'Reactive Power vs. Time' 'Load'})
subplot(3,1,2), plot(out.time,out.Q_src)
xlabel('time [s]')
ylabel('Q_s_r_c [VAR]')
grid minor
title({'Reactive Power vs. Time' 'Source'})
axis([0 15 -600 3000])
subplot(3,1,3), plot(out.time,out.Q_inv)
xlabel('time [s]')
ylabel('Q_i_n_v [VAR]')
grid minor
axis([0 15 -600 3000])
title({'Reactive Power vs. Time' 'Inverter'})

figure(10)
subplot(3,1,1), plot(out.time,out.P_load)
xlabel('time [s]')
ylabel('P_l_o_a_d [W]')
grid minor
axis([0 15 -2500 4000])
title({'Real Power vs. Time' 'Load'})
subplot(3,1,2), plot(out.time,out.P_src)
xlabel('time [s]')
ylabel('P_s_r_c [W]')
grid minor
title({'Real Power vs. Time' 'Source'})
axis([0 15 -2500 4000])
subplot(3,1,3), plot(out.time,out.P_inv)
xlabel('time [s]')
ylabel('P_i_n_v [W]')
grid minor
axis([0 15 -2500 4000])
title({'Real Power vs. Time' 'Inverter'})

figure(11)
subplot(3,1,1)
plot(out.time, out.Iabc)
title({'Step Load Decrease at 6 Seconds' 'Iabc_l_o_a_d vs. Time'})
xlabel('Time [s]')
ylabel('Load Current [A]')
xlim([6-3/60 6+3/60])
subplot(3,1,2)
plot(out.time, out.Iabc_inv)
xlim([6-3/60 6+3/60])
title('Iabc_i_n_v vs. Time')
xlabel('Time [s]')
ylabel('Inverter Current [A]')
subplot(3,1,3)
plot(out.time, out.Iabc_source)
title('Iabc_s_r_c vs. Time')
xlim([6-3/60 6+3/60])
xlabel('Time [s]')
ylabel('Source Current [A]')
```

```
figure(12)
subplot(2,1,1)
plot(out.time, out.Vabc)
xlim([3-3/60 3+3/60])
title('Phase Voltage vs. Time')
xlabel('Time [s]')
ylabel('Phase Voltage [V]')
subplot(2,1,2)
plot(out.time, out.Vabc)
xlim([6-3/60 6+3/60])
xlabel('Time [s]')
ylabel('Phase Voltage [V]')

figure(13)
plot(out.tout, out.Vbus')
title('DC Bus Voltage vs. Time')
ylabel('V_D_C [V]')
xlabel('Time [s]')
grid minor
ylim([430 470])

vab_THD_pct = 100*sqrt(sum(abs(vab_spect(3:1:400)).^2)/abs(vab_spect(2)).^2);
disp(['THD only includes muliples of 60 Hz. >> THD = ' num2str(vab_THD_pct,3) ' %'])
van=out.Vabc(:,1);
van_ss=van(length_vector-length_v+1:length_vector);
van_spect= fft(van_ss)/round(length_v/2);
DPF_V_over_I=cos(angle(van_spect(2)/iasource_spect(2)));
disp(['cosine of angle between Van and ILa = ' num2str(DPF_V_over_I,3)])
```

3. 440V_{rms} Multi-Step

```
figure
subplot(3,1,1), plot(out.time,out.Q_load/1000)
xlabel('time [s]')
ylabel('Q_l_o_a_d [kVAR]')
grid minor
axis([0 15 -100 400])
title({'Reactive Power vs. Time' 'Load'})
subplot(3,1,2), plot(out.time,out.Q_src/1000)
xlabel('time [s]')
ylabel('Q_s_r_c [kVAR]')
grid minor
title({'Reactive Power vs. Time' 'Source'})
axis([0 15 -100 400])
subplot(3,1,3), plot(out.time,out.Q_inv/1000)
xlabel('time [s]')
ylabel('Q_i_n_v [kVAR]')
grid minor
axis([0 15 -100 400])
title({'Reactive Power vs. Time' 'Inverter'})

figure
subplot(3,1,1), plot(out.time,out.P_load/1000)
xlabel('time [s]')
ylabel('P_l_o_a_d [kW]')
grid minor
axis([0 15 -100 400])
title({'Real Power vs. Time' 'Load'})
subplot(3,1,2), plot(out.time,out.P_src/1000)
xlabel('time [s]')
ylabel('P_s_r_c [kW]')
grid minor
title({'Real Power vs. Time' 'Source'})
axis([0 15 -100 400])
subplot(3,1,3), plot(out.time,out.P_inv/1000)
xlabel('time [s]')
```

```
ylabel('P_i_n_v [kW]')
grid minor
axis([0 15 -100 400])
title({'Real Power vs. Time' 'Inverter'})
```

4. Plots for Simulation with Laboratory Parameters

```
figure(1)
plot(out.time,out.P_load)
hold on
xlabel('Time [s]')
ylabel('Power[W]')
grid on
axis([2.9 3.9 -20 100])
plot(out.time,out.P_src)
plot(out.time,out.P_inv)
title({'Step Load Increase' 'Power vs. Time'})
legend('Load Power', 'Source Power', 'Inverter Power', 'Location', 'southeast')
hold off

figure(2)
plot(out.time,out.P_load)
hold on
xlabel('Time [s]')
ylabel('Power[W]')
grid on
axis([5.9 6.9 -100 100])
plot(out.time,out.P_src)
plot(out.time,out.P_inv)
title({'Step Load Decrease' 'Power vs. Time'})
legend('Load Power', 'Source Power', 'Inverter Power', 'Location', 'southeast')
hold off

figure(3)
plot(out.time, out.Iabc_source)
axis([2.9 3.9 -1.5 1.5])
grid on
xlabel('Time [s]')
ylabel('Source Currents (A)')
title({'Step Load Increase' 'Three Phase Source Current vs. Time'})


figure(4)
plot(out.time, out.Iabc_inv)
axis([2.9 3.9 -1.5 1.5])
grid on
xlabel('Time [s]')
ylabel('Inverter Currents (A)')
title({'Step Load Increase' 'Three Phase Inverter Current vs. Time'})

figure(5)
plot(out.time, out.Iabc_source)
axis([5.9 6.9 -1.5 1.5])
grid on
xlabel('Time [s]')
ylabel('Source Currents (A)')
title({'Step Load Decrease' 'Three Phase Source Current vs. Time'})


figure(6)
plot(out.time, out.Iabc_inv)
axis([5.9 6.9 -1.5 1.5])
grid on
xlabel('Time [s]')
ylabel('Inverter Currents (A)')
title({'Step Load Decrease' 'Three Phase Inverter Current vs. Time'})
```

C. SIMULINK PARAMETERS FOR OPAL-RT MODEL

```
f_fund = 60; %fundamental frequency in Hz
omega=2*pi*f_fund;
Kp_boost=1; %Boost PI Proportional Gain
Ki_boost=20;  %Boost PI Integral gain
VDCref=80; %reference voltage for boost output [V_bus]
Kp_v=.2; %Voltage Controller Proportional Gain
Ki_v=20; %Voltage Controller Proportional Gain

%abc to qd0 transformation in the stationary frame
Ks=2/3*[1 -1/2 -1/2;0 -sqrt(3)/2 sqrt(3)/2;1/2 1/2 1/2];

%For SVM Sector Selection
sector_matrix =
[1 0 0 0 0 0;...
0 2 0 0 0 0;...
0 0 3 0 0 0;...
0 0 0 4 0 0;...
0 0 0 0 5 0;...
0 0 0 0 0 6];

fswVSI=10000; %VSI Switching Frequency
```

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LIST OF REFERENCES

[1] Office of the Assistant Secretary of Defense for Sustainment, “Department of Defense annual energy management and resilience report (AEMRR) fiscal year 2018,” Washington, DC, USA, Jun. 2019. [Online]. Available: https://www.acq.osd.mil/eie/Downloads/IE/FY%202018%20AEMR.pdf

[2] Pacific Gas and Electric Company, “Economics of power factor correction in large facilities, >400kW.” Aug. 2007. [Online]. Available: https://www.pge.com/includes/docs/pdfs/mybusiness/customerservice/energystatus/powerquality/power%20factor--revised-8-9-07.pdf#:~:text=PG%26E%20uses%20power%20factor%20correction%20capacitors%20on%20the,better%20than%2098%25%20going%20in%20to%20the%20substations

[3] A. Kwasinski, W. Weaver, and R. S. Balog, *Microgrids and Other Local Area Power and Energy Systems*. Cambridge, U.K.: Cambridge University Press, 2016.

[4] J. J. A. van der Burgt, P. van Gelder, and E. van Dijk, “Pulsed power requirements for future naval ships,” in *Dig. of Tech. Papers. 12th IEEE Int. Pulsed Power Conf.*,1999. [Online]. doi: https://doi.org/10.1109/PPC.1999.823779.

[5] L. N. Domaschk, A. Ouroua, R. E. Hebner, O. E. Bowlin, and W. B. Colson, “Coordination of large pulsed loads on future electric ships,” *IEEE Trans. Magn.*, vol. 43, no. 1, pp. 450-455, Jan. 2007. [Online]. doi: https://doi.org/10.1109/TMAG.2006.887676.

[6] S. Kulkarni and S. Santoso, “Impact of pulse loads on electric ship power system: with and without flywheel energy storage systems,” in *2009 IEEE Electric Ship Technologies Symp.*, 2009. [Online]. doi: https://doi.org/10.1109/ESTS.2009.4906568.

[7] H. Ebrahimi, H. El-Kishky, M. Biswass, and M. Robinson, “Impact of pulsed power loads on advanced aircraft electric power systems with hybrid APU,” in *2016 IEEE Int. Power Modulator and High Voltage Conf. (IPMHVC)*, 2016. [Online]. doi: https://doi.org/10.1109/IPMHVC.2016.8012857.

[8] J. M. Crider and S. D. Sudhoff, “Reducing impact of pulsed power loads on microgrid power systems,” *IEEE Trans. Smart Grid*, vol. 1, no. 3, pp. 270-277, Dec. 2010. [Online]. doi: https://doi.org/10.1109/TSG.2010.2080329.

[9] G. Oriti, A. L. Julian, and N. J. Peck, “Power-electronics-based energy management system with storage,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 452-460, Jan. 2016. [Online]. doi: https://doi.org/10.1109/TPEL.2015.2407693.

[10] D. Kanavaros, G. Oriti, and A. L. Julian, “Novel implementation and comparison of active and reactive power flow control methods in a single phase grid-connected microgrid,” *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1631-1639, 2020. [Online]. doi: https://doi.org/10.1109/TIA.2020.2965080.

[11] C. Mendoza, “Implementation of reactive power flow control in a single-phase microgrid” M.S. thesis, Dept. of Elect. and Comput. Eng., NPS, Monterey, CA, 2018.

[12] D. Kanavaros, “Implementation of active and reactive power flow control in a single phase microgrid,” M.S. thesis, Dept. of Elect. and Comput. Eng., NPS, Monterey, CA, 2019.

[13] Naval Sea Systems Command (Ships Systems), “Department of Defense interface standard section 300, part 1 low voltage electric power, Alternating Current,” Sep. 25, 2018. [Online]. Available: https://quicksearch.dla.mil/qsDocDetails.aspx?ident_number=283082

[14] Office of Electricity Delivery and Energy Reliability Smart Grid R&D Program, “DOE microgrid workshop report,” San Diego, CA, USA, Aug. 2011. [Online]. Available: https://www.energy.gov/sites/prod/files/Microgrid%20Workshop%20Report%20August%202011.pdf

[15] S. B. Van Broekhoven, N. Judson, S. V. Nguyen, and W. D. Ross, “Microgrid study: energy security for DoD installations:,” Defense Technical Information Center, Fort Belvoir, VA, Jun. 2012. [Online]. doi: https://doi.org/10.21236/ADA565751.

[16] M. Ceraolo and D. Poli, *Fundamentals of electric power engineering: engineering: from electromagnetics to power systems*, Hoboken, New Jersey, USA: IEEE Press/Wiley, 2014.

[17] M. V. Prato, “Reactive power compensation using an energy management system,” M.S. thesis, Dept. of Elect. and Comput. Eng., NPS, Monterey, CA, 2014.

[18] J. W. Nilsson and S. A. Riedel, *Electric Circuits*, 10th ed. Upper Saddle River, NJ, USA: Prentice Hall, 2015.

[19] J. Katz, “PACFLT amphib demos navy laser tech, more experiments to come,” *InsideDefense.Com’s SitRep*, May 26, 2020. [Online]. Available: https://insidedefense.com/daily-news/pacflt-amphib-demos-navy-laser-tech-more-experiments-come

[20] P. C. Krause, *Analysis of Electric Machinery and Drive Systems*, 3rd ed. Hoboken, NJ, USA: Wiley, 2013.

[21] A. Roshan, R. Burgos, A. C. Baisden, F. Wang, and D. Boroyevich, “A D-Q frame controller for a full-bridge single phase inverter used in small distributed power generation systems,” in *APEC 07 - Twenty-Second Annu. IEEE Appl. Power Electronics Conf. and Expo.*, 2007. [Online]. doi: https://doi.org/10.1109/APEX.2007.357582.

[22] “Derivation of state space model,” class notes for EC4150 Applied Power Electronics, Dept. of Elect. and Comput. Eng., Naval Postgraduate School, Monterey, CA, USA, winter 2020.

[23] G. Oriti and A. L. Julian, “Three phase VSI with FPGA-based multisampled space vector modulation,” *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1813-1820, Jul. 2011. [Online]. doi: https://doi.org/10.1109/TIA.2011.2154295

[24] N. Mohan, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Hoboken, NJ, USA: John Wiley & Sons, 2003.

[25] G. Oriti, N. Anglani, and A. L. Julian, “Hybrid energy storage control in a remote military microgrid with improved supercapacitor utilization and sensitivity analysis,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5099-5108, 2019. [Online]. doi: https://doi.org/10.1109/TIA.2019.2923380.

[26] *CC-180849 System Description*, OPAL-RT., Montreal, Quebec, Canada, Jun. 2019.

[27] OPAL-RT, *OP4510 Simulator RT-LAB/RCP/HIL System*. [Online]. Available: https://blob.opal-rt.com/medias/L00161_0124.pdf

[28] SEMIKRON, *SEMITEACH IGBT Datasheet*, 2015. [Online]. Available: http://shop.semikron.com/out/media/ds/SEMIKRON_DataSheet_SEMITEACH_IGBT_3M50GB123D_1M50GAL123D_P3_250F_08753450.pdf

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