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# Modeling a IF Double Sampling Bandpass Switched Capacitor ΣΔ ADC with a Symmetric Noise Transfer Function for WiMAX/WLAN

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*Abstract*—**4G technology aims to revolutionize private and professional communication with its ubiquity and high-speed transmission (averaging 100Mbps). WiMAX and WLAN are two of the high speed access technologies to be used in the 4G mobile communication. Apropos to their high bandwidths,oversampling converters, e.g.ΣΔ ADCs, used for these standards would entail high levels of power consumption. Double sampling technique used in ΣΔ ADCs help in reducing the power consumption, since the actual sampling rate is only half the sampling frequency required to achieve a target resolution. But for conventional modulators, with low pass noise transfer functions (NTF), this benefit is hampered by the introduction of folded noise due to the mismatch of sampling capacitances. This paper presents a novel method of designing IF bandpass switched capacitor (SC)ΣΔ modulators with symmetric NTFs. Such a bandpass NTF is formulated with its center frequency at one-fourth the effective sampling frequency. The symmetricity ensures that the folded noise is 'noise-shaped' along with the quantization noise. The idea is verified with a discrete time bandpassΣΔ modulator modeled using Simulink®, including various nonlinearities, viz. clock jitter, opampnonidealities, and capacitive mismatch effects owing to double sampling and use of a multibitquantizer. Behavioral simulations of the proposed non-ideal model for WiMAX and WLAN, with a bandwith of 10MHz and 11MHz, respectively, achieved a peak resolution greater than 10 bits for each of the standards.**

***Keywords-4G mobile communication, A/D converter modeling,Delta-sigma modulation, double sampling, noise folding, nonlinearities.***

## I. INTRODUCTION

4G, or the fourth generationof mobile communications standards, intents to conjoin a plethora of different services, modes, and hence, the corresponding different standards in different parts of the world. It promises the user a multitude of facilities, viz. localized/personalized information (e.g. general news, financial news, location guides, mobile commerce and travel services), communications (e.g. short messaging service, e-mail, video conferencing, fax and bulletin boards),organizational (personal digital assistant capabilities, currency exchange based on user location and other personal management application) and entertainment (streaming audio, streaming video, chat,photo trading and gaming)[1]. It promises the user ten times larger capacity than 3G systems, average data rates of 100Mbps and seamless "*always best connected*" networking at system costs 1/10 ~ 1/100 of 3G systems [2]-[4]. WiMAXand WLAN are two key proponents of 4G communication, both being high bandwidth technologies. Power consumption is one of the prime concerns for systems designed for these high speed access technologies. This beseeches the designers to come up with systems consuming low power, or, to find techniques to reduce power consumption in the existing designs.

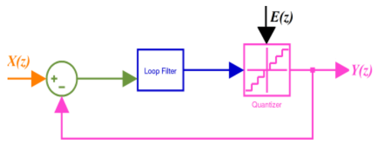

Figure 1. Generic scheme of a ΣΔ modulator

ΣΔ modulator(Fig. 1) is an ubiquitous choice for high resolution A/D converters (*vis a vis* their other popular counterparts like the flash and SAR ADC) owing to their excellent ability to alleviate quantization noise in the frequency band of interest ( endowed to them because of the combined effect of oversampling and noise-shaping)and robustness to circuit nonlinearities. The equation for the dynamic range (DR) of a ΣΔ modulator is given by

$$DR \approx \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(OSR)^{2L+1}(2^{B}-1)^{2} \quad (1)$$

where*L* is the order of the modulator, *OSR* is the oversampling ratio, and *B* is the number of bits of the internal quantizer. It is

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evident from (1) that it gives the designer higher degrees of freedom for design, since a target resolution can be achieved by an optimal choice of these parameters. Application speeds of ΣΔ modulators vary from lesser than 6ksps and 10Msps for 24 bits and 16-18 bits of resolution,respectively. ΣΔ ADCs find enormous applications in systems designed for reconfigurableIF and RF communication systems for multi-standard wideband 'next-generation' 4G communication.

Double sampling is a technique which used to reduce the power consumption in the ΣΔ ADCs. Both, sampling and integration are done on both the phases of the master clock. In this way, the effective sampling rate becomes twice the frequency of the master clock. Hence, a target resolution is achieved incurring lower power consumption. But this technique is impeded by the mismatch in the sampling capacitances. For the case of conventionalΣΔ modulators, with low pass NTF, this path mismatch results in the quantization noise getting folded back from the half the sampling frequency into the signal band[12]. Various strategies have been implemented to deal with this folded noise, viz. dynamic mismatch techniques [5]-[6], using a bilinear input integrator [7]-[9], and using a modified NTF [10]-[12].

This paper presents a yet another scheme of using a modified NTF while using double sampling technique. It points out that a symmetric NTF can be synthesized if the center frequency of the bandpassΣΔ modulator is at *0.25fs*, where *fs*is the effective sampling rate achieved with double sampling. Such an NTF, noise shapes the folded noise along with the quantization noise, hence significantly reducing the folded noise in the frequency band of interest. The behavioral simulations using the Simulink model of a bandpassΣΔ modulator, with nonlinearities incorporated and having a symmetrical NTF discussed above, vindicates that excellent resolutions can be obtained for high bandwidth(10-11MHz) standards like WiMAX and WLAN. The concept of having a bandpass NTF with center frequency at *fs/4* is not a new idea. Designers normally choose IF at that location keeping the subsequent design ofthe decimation filter in mind. To the best of our knowlwdge, this is the first claim that such an NTF can also be used to alleviate the problem of folded noise in the frequency band of interest.

## II. SYMMETRIC NTF FOR DOUBLE SAMPLED ΣΔ MODULATORS

Following the convention used in Rosa *et. al* [13], the *z*-domain equation for the final output can be written as

$$Y(z) = STF(z) * X(z) + NTF(z) \cdot \qquad (2)$$

where STF(*z*) is the signal transfer function, X(*z*) is the input signal, NTF(*z*) is the noise transfer function and E(*z*) is the quantization error. Contribution of the quantization noise in the output is

$$Y_Q(z) = NTF \qquad (3)$$

A simplistic depiction of the integrator used in the double sampling modulators is shown in [12]. Here both sampling and integration actions occurs at both the phases of the master clock. The net result is that

$$f_{effective} = 2 * f_{m} \qquad (4)$$

Hence, a target resolution can be achieved at half the theoretical OSR, saving significant amount of power.

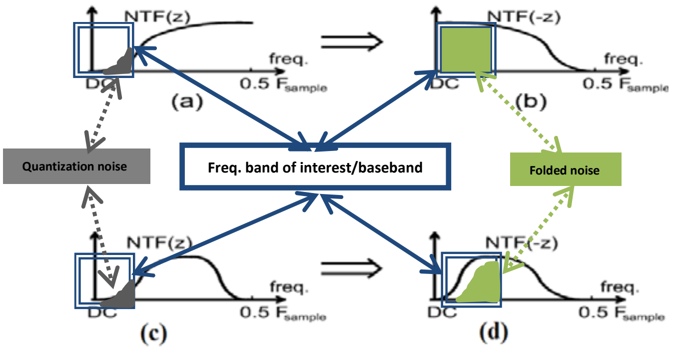
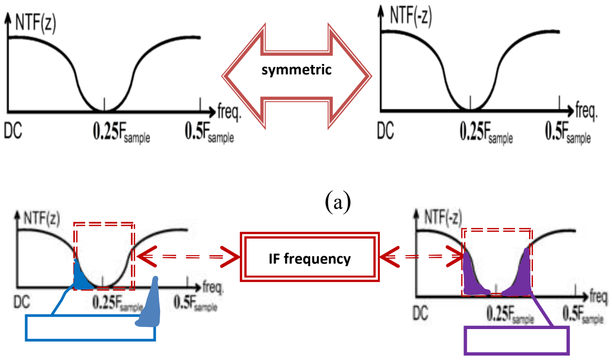


Figure 2. (a) NTF and (b) folded NTF of a conventional low pass ΣΔ modulator. The corresponding shaded regions regions represent the quantization noise(grey) and the folded noise(light green). (c) NTF and (d) folded NTF of the same modulator with an additional zero inserted at *f=fs/2*. The corresponding noises are also depicted by the shaded region – reduction in the folded noise in the band of interest is evident.

On the dark side, this technique is impeded by the introduction of folded noise into the band of interest. A quantitative expression for this additional noise is (as is given in [11])

$$N_{Fold}(z) \approx \delta * E(-z) NTF(-z);\ \delta = \frac{(C_{s1} -}{(C_{s1} +} \qquad (5)$$

where is the sampling capacitance mismatch. Fig. 2a and 2b shows the NTF, and corresponding folded NTF of the normal low pass ΣΔ modulator along with the noises pointed out. It is apparent that folded noise is not small in the baseband. Romboutset*et. al* [12] proposes an idea wherein an additional zero is inserted at *z*=-1 (or *θ=π*, or *f=fs/2* ). The benefit of reducing the folded noise in the baseband can be easily comprehended from the illustration (Fig. 2c and 2d).



(a)

(b)

Figure 3. (a)NTF and folded NTF of the proposed scheme with symmetric NTF. (b) The corresponing noises in the band of interest are also shown.

This paper intends to show that an analogous leverage can be achieved by using a bandpass NTF with its center frequency at *fs/4*. Fig. 3 illustrates the NTFs and the corresponding noises for this strategy. It is pretty clear that folded noise is "noise-shaped" along with the quantization noise. The advantage of this scheme over that proposed in [12] is that no additional zeros need to be inserted, hence saving any extra hardware and power.

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## III. SYSTEM LEVEL MODELING OF A NONLINEAR BANDPASS SC ΣΔ MODULATOR WITH SYMMETRIC NTF

To start with, the modulator specifications are adopted from [14]. The chosen specifications are summarized in the Table I. A ΣΔ modulator for these specifications is modeled using Simulink. The NTF is formulated using the *'cookbook'* procedure in [15], [16]. The 4th order bandpass NTF and STF used here is

$$\left\{ \begin{array}{c} NTF(z) = \dfrac{(z^2+1)^2}{(z^2-0.2222z+0.6648)(z^2+0.2222z+0.61} \\ STF(z) = 1 \end{array} \right\} \quad (6)$$

Fig. 4a shows the magnitude plot of the NTF. The NTF is synthesized using cascade-of-resonatorsfeedforward form (CRFF) topology (Fig. 4b), preferably because of its universal usage[15].

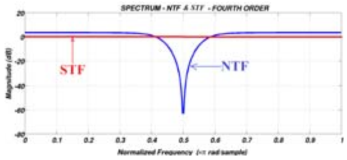
The *'cookbook'* procedure allows us to have our STF equal to unity. This reduces the signal swings at the input/output of the integrators in the loop filter, relaxing their linearity requirements, hence reducing static power consumption in the actual circuit. Also, since for unity-STF ΣΔ ADCs the integrator outputs are independent of the input, single stage opamps are sufficient to implement the analog filter, hence further reducing the powers [22],[23].

TABLE I. ΣΔ MODULATOR MODEL PARAMETERS

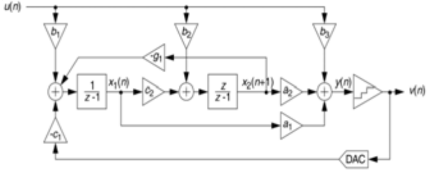
| Parameter | Value | |
|---|---|---|
| | ***WiMAX*** | ***WLAN*** |
| Order of the modulator | 4 | 4 |
| OSR[1] | 16 | 16 |
| Number of bits in the internal quantizer | 4 | 4 |
| IF center frequency | 80 MHz | 80MHz |
| Sampling frequency (*fs*)[1] | 320MHz | 320MHz |
| Bandwidth (BW) | 10 MHz | 11MHz |
| Target ENOB[2] | 8-14 | 7-11 |
| Input amplitude | -2.3 dB | -2.3 dB |
| Input signal frequency (*fin*) | 80MHz | 80MHz |

| **Nonlinearities incorporated into the model** | |
|---|---|
| ***Circuit nonlinearity*** | ***Value*** |
| Finite DC gain [3] | 100 dB |
| GBW[3] | 1000 MHz |
| Slew rate[3] | 574 V/µs |
| Capacitor mismatch of quantizer[4] | σ = 0.496<br>$N_{COMP}$ = 15<br>$C_{TOT}$ = 1.5pF |
| Sampling capacitor mismatch[4] | δ = 0.1% |
| Clock jitter[4] | 1ps |

1. Values in the table are double that mentioned in [15], taking into account the effect of double sampling. Actual *fs*= 160MHz, 2. Effective number of bits, c. Adopted from [15], d. Adopted from [16]



(a)



(b)

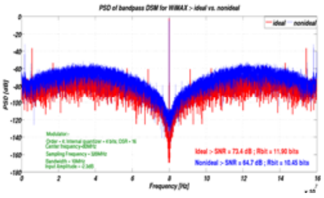
Figure 4. (a) Magnitude plot of the proposed NTF and STF (b) The generic even order CRFF topology used to model the loop filter of the ΣΔ modulator [15].

The various sources of nonlinearities are also incorporated into the design. The models are adopted from [18],[19]. The model of the nonideal quantizer is taken from the toolbox available in [21]. The mismatch due to the sampling capacitances in double sampling is modeled using the concept mentioned in [17] and [20].

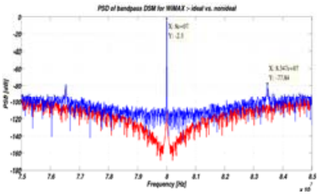
## IV. SIMULATION AND RESULTS

Two different Simulink models of the ΣΔ modulator are obtained following the procedure and specifications discussed in the previous section. The first one is an ideal system, built from all the ideal blocks. The second one is a nonlinear system, which includes all the nonidealities mentioned in Table I. Both the systems were simulated for the targeted WiMAX (BW = 10MHz) and WLAN (BW = 11MHz) standards.

The behavioral simulations for WiMAX achieved a peak SNR of 73.4dB and 64.7dB for the ideal and the nonideal model respectively (Fig. 5).



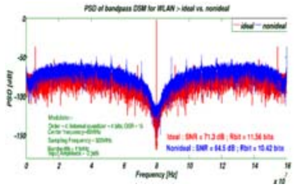
(a)



(b)

Figure 5. (a) PSD plot of the ΣΔ modulator for WiMAX standard – ideal (red) and nonideal (blue). (b) A zoomed-in view of the PSD for the frequency band of interest i.e. from 75-85MHz (BW = 10MHz).

Similar simulations were caried out for the WLAN standard. The results reveal that a peak SNR of 71.3dB and 64.5dB can be obtained from the ideal and nonideal modulator respectively (Fig. 6).



(a)

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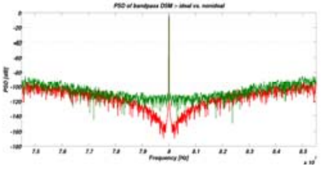

(b)

Figure 6. (a) PSD plot of the ΣΔ modulator for WLAN standard – ideal (red) and nonideal (green). (b) A zoomed-in view of the PSD for the frequency band of interest i.e. from 74.5-85.5MHz (BW = 11MHz).

The behavioral simulations show that the targets set for SNR values, set in the beginning of the previous section, can be achieved using the model proposed in this paper. Also, Fig. 5b and 6b reveal that the PSD is devoid of any menacing tones in the frequency band of interest.Table II summarizes the performance of this work along with a couple of other related works.

TABLE II. PERFORMANCE SUMMARY

| | **Reference & year of publication** | | |
|---|---|---|---|
| ***ΣΔ modulator parameters*** | ***[17];2011*** | ***[24];2010*** | ***This work*** |
| Topology | Bandpass with tunable resonators and noise-coupling | 2-1-1 cascade with low pass NTF | CRFF |
| Quantizer (bits) | 4 | 1bit for all stages | 4 |
| BW(MHz) | WLAN : 20<br>WiMAX : --- | WLAN : 22<br>Wimax : 28 | WLAN : 11<br>Wimax : 10 |
| SNDR (dB) | Wlan : 55<br>Wimax : ---- | Wlan : 57<br>Wimax : 48 | Wlan:64.5<br>Wimax:64.7 |
| Order (effective) | 6 | 4 | 4 |
| OSR (effective) | ≈12 | Wlan : 12<br>Wimax : 10 | Wlan : 16<br>Wimax : 16 |
| Actual *fs* (MHz) | 125 | WLAN : 132<br>WiMAX : 140 | 160 |
| IF Center frequency | 62.5 MHz | --- | 80MHz |

## V. CONCLUSION

A bandpass NTF with its center frequency at *fs/4* is proposed to alleviate the folding noise in the frequency band of interest. A nonlinear model of SC ΣΔ modulator with such a NTF is simulated using Simulink. The behavioral simulations affirm that system can be used for WiMAX and WLAN standards. A peak SNR of 64.7dB and 64.5dB is obtained for WiMAX and WLAN respectively. A logical step could be to try the same using quadrature ΣΔ modulator, which is expected to give the similar results with a lower order loop.

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