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Stress Analysis in 3D IC having Thermal Through Silicon Vias (TTSV)

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Abstract

TTSV is proposed for the removal of heat from between the IC layers as these TTSVs carries heat down to the sink. However, it may generate stress in Silicon. In the present paper, thermal-stress simulation of stack consists of three IC layers bonded face up is performed using finite element modeling tools. We also analyzed the stress generated in 3D IC containing TTSV. Further we proposed a method for lower stress around the TTSV. The method proposed decreases the Von Misses Stress by a value of 40Mpa on average considering all the IC layers. Thus by achieving this, functionality of the chip becomes more reliable.

Keywords

3D IC, CNT (Carbon Nano Tube), CVD Diamond, TTSV

1. Introduction

In today's world with ever increasing demand for higher computational speed of systems or processors, there is a lot of ongoing work. So in this process we have entered into a generation of making 3D Integrated Circuits which increases the speed by many folds through decrease in the latency by reducing the interconnect length between IC layers, also allows for heterogeneous integration and increase in bandwidth. With many wafers stacked one over the other, there is a large amount of heat generated in it. Work is being done on the removal of heat from the IC which spoils the functionality of CMOS devices, which are present in it. Few methods to achieve lower temperature are by the use of Micro channel method [1] and Thermal Through Silicon via (TTSV) [2-3]. By the introduction of TTSVs in 3-D ICs, we achieve lower temperature [2-4], but because of unequal young's modulus of the material being used, stress is generated around TTSVs. This makes the device unreliable as it decreases its functionality if the stress generated is more than yield strength of the material used [5-6]. Besides this, the lattice mismatch due to the placement of the TTSVs also produces stresses in 3-D IC. The yield strength of copper varies from 225Mpa to 600Mpa depending on thickness, grain size and temperature. Silicon has yield strength of around 6000Mpa. So it is essential that stress generated in 3D IC is lesser than the yield strength of Copper as the yield strength of silicon is a lot higher than copper. In literature, however, there is lack of comprehensive study of the stress analysis in Si substrate due to the presence of TTSV in multilayer ICs stacks. This paper studies the stress generated in 3-D IC in the presence of TTSV for vertically stacked three IC layer facing up and is carried out by using commercially available FEM tool. Further a new model is proposed in this paper by which we can achieve a decrease in stress value. This will allow using the TTSVs more efficiently and more reliably.

2. Simulation Model

3D FEM Model

The model is simulated using commercially available COMSOL Multiphysics FEM tools. The physics used in this simulation process is thermal stress and the equations solved in the stationary analysis are as follows:

$$\nabla.\sigma = F_v \quad (1)$$

$$\Delta\rho C_p u_{tran.} \nabla T = \nabla.(K \nabla T) + Q + W_p \quad (2)$$

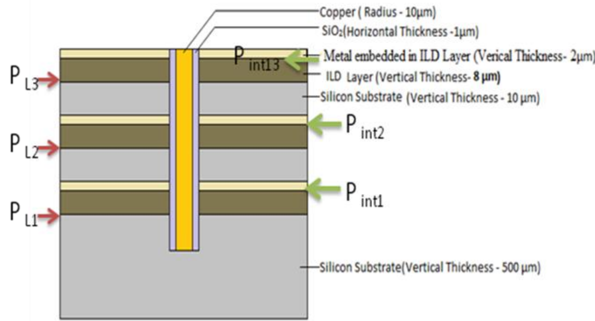
σ – Stress
ρ – Density
C_p – Heat Capacity at constant pressure
K – Thermal Conductivity
Q – Heat Source

The equation considers that the change in temperature of an object will be dependent on its conductivity, temperature gradient in the material, energy being generated in the device and external work being done on the structure. Figure 1 is the schematic of simulated 3D stack with TTSV. The meshing has been done using fine element size which is calibrated for general physics and tetrahedral mesh structure has been used for its study. The Fig.1 shows a schematic of the simulated 3-D stack with TTSV. The TTSV with a diameter of 22 µm consists of Cu as the heat conductor core (20 µm) and SiO2 dielectric as the liner shell (1 µm) are used unless stated differently. The primary role of liner is to act as an electric insulation layer between semiconductors to Cu, but its thermal property also crucial, as it can assist in heat removal from top IC layers to the substrate in 3-D ICs. In this proposed model, we assume a uniform heat flux (generated by devices and interconnects Joule heating) across the entire chip. Device power density is applied at the top of each Si layers (70 W/cm2) and interconnects heat flux is applied in the inter-layer dielectric (ILD) layer (50 W/cm2). In addition, we also assume that heat sink is efficient enough to maintain the bottom substrate at a temperature of 358.2K. Materials properties used in FEM analysis are listed in Table 1.

Table1: Properties of materials used in the simulation.

Material	*Thermal Conductivity (W/m.K)*	*Density (kg/m^3)*	*Heat Capacity (J/kg.K)*	*Dielectric Constant*	*Young's Modulus (G Pa)*
Air	0.048	0.524	1055	1	0.011
Silicon	163	2330	703	12.1	131
SiO2	1.38	2203	703	3.9	70

Copper	400	8700	385	-	110
CNTube	2500 (in plane) 25 (normal)	1300	1100	2.4-3.2	0.42
CVD Diamond	1100	3515	502	2- 3.4	1050



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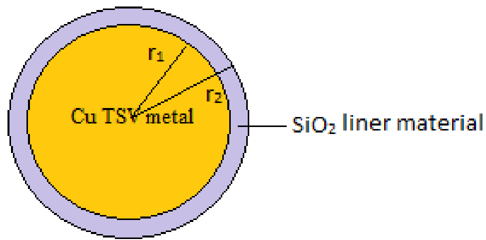

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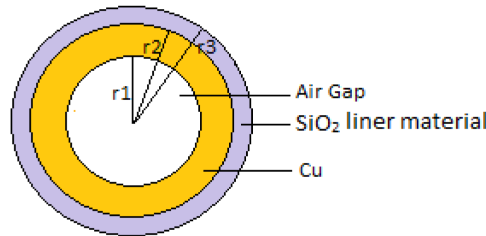

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Figure 1: Schematic of heat removal model using TTSV across different IC layers which will eventually causes stress in substrate. Si substrate thickness is 500µm, and other Si layers are 10 µm thick. Carbon doped oxide is used as ILD with thermal conductivity of 0.39W/mK. TTSV diameter is 22µm, which consists of Cu core (20µm) and SiO2 shell liner (1µm). P3d is the heat flux at the top surface of each Si generated due to device power while Pint is the heat flux due to joule heating in metal wires embedded in ILD layers. (a) FEM Model Structure (b) Cross-section view (Top View) of TTSV inserted in Si. (c) Cross-section view (Top View) of TTSV with air gap inserted in Si (Void exists inside the Practical TTSV structure).

2D FEM Model

In order to analyze the effect of bundled TTSV structure, this paper analyses the Von Misses Stress using 2D FEM PDE tool in MATLAB. The structure used is as follows: The silicon substrate (Radius = 500µm) and Copper material (Radius = 20µm) surrounded by the liner material silicon dioxide (thickness = 1µm). The stress due to lattice mismatch through the placement of TTSV is modeled by having volume stress built up inside the Copper structure.

3. Result and Discussion

3.1. Stress Analysis Ideal TTSV Structure

In literature, the researchers reported varied yield strength of Cu ranging from 225MPa to 600MPa and its variation depends upon thickness, grain size and temperature. In this analysis, we have kept 280MPa as its yield strength, but our objective is to reduce the stress observed in Cu as low as possible especially below 225MPa. In this work, a Von Misses Stress (VMS) criterion is used for analyzing the mechanical reliability of the substrate and TTSV. If the stress increases than the yield strength, it initiates the material yielding. Until the elastic limit, the material can deform back to its original shape when the applied stresses is removed. We have evaluated the VMS along the substrate plane for considering ideal TTSV as described in the earlier section is depicted in Fig. 2. It shows that presence of TTSV results in VMS at different IC layer. IC3 has highest stress as compared with other IC layers. It is due the fact that the heat from the top IC layers can be conducted via TTSV and subsequently spreads in the Si substrate and dissipates through the heat sink, hence temperature of TTSV near the IC-3 is highest and causes high stress at IC-3 and subsequently reduces at nearer sink level. Further due to the liner around TTSV structure has low temperature gradient in the horizontal direction and a higher temperature gradient in the vertical direction. The temperature of the IC layer increases from the liner and then it almost becomes a constant temperature value due to the high conductivity of Si substrate. For this reason at the edge of the liner, high temperature gradient causes more expansion in silicon, Cu and liner and thus results in higher stress at the interface.

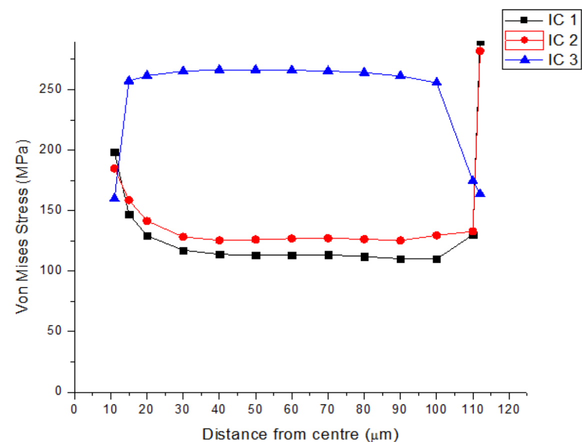

Figure 2: Comparison of stress at each IC layers with in the presence of TTSV. Stress of IC1 is higher. The heat source is applied in both cases (70 W/cm2 due to device power, and an average of 50W/cm2 due to joule heating). TTSV diameter is 22 µm (20µm Cu core and 1 µm SiO2 shell liner)

3.2. Stress Analysis in Practical TTSV Structure

TTSV described in the earlier section is ideal in nature. However it is exceedingly difficult to get a fully filled Cu via. So in this section we have done analysis considering air in between Cu via i.e., their always exists an air gap after the TTSV is made. In this work, we have taken radius of 2 micron of air gap within the 20 micron diameter of Cu cores and the Cu is surrounded by 1 micron thickness of SiO2 liner.

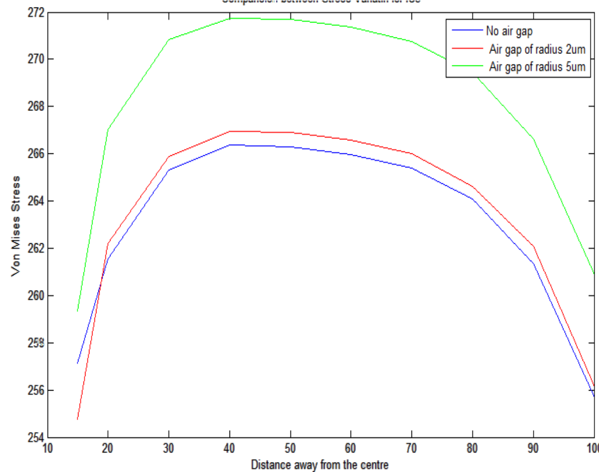

Figure 3: Comparison of stress at IC-3 layer in the presence of practical TTSV with respect to ideal TTSV. Stress increases nominally for 5 µm air gap and, in fact, more than what it increases for 2 µm air gap. Similar trend is observed in other IC layers.

Figure 3 shows that, in the presence of air gap in TTSV, the stress developed on IC layers increases with an increase in the air gap dimension in TTSV as compared to ideal TTSV. However the stress variation for a micron air gap, is less, due to the fact that the temperature variation is slightly more than in full filled TTSV. As the air gap increases i.e. to 5 micron (in this study) the TTSV temperature rises due to smaller surface area to conduct heat from top IC layer to sink and hence stress increases more as compared to the ideal TTSV, which can be observed in Fig.3. Since most affected IC layer is the third one, we are giving comparison only for this layer.

3.3 Stress Reduction Strategies

3.3.1 CNT as Core of TTSV

After having the impact of TTSV on stress front it is essential to get an engineering solution to reduce the stress in Si substrate. For this purpose having the high thermal conductivity in the vertical and low conductivity in horizontal direction helps in achieving a better temperature reduction and hence the Von Misses stress. Thus, we have introduced carbon nano tube (CNT) as core material in TTSV in place of 5 micron air and evaluated the stress across the surface. Figure 4 showed the decrease in stress is observed when compared to having only an air gap or having it fully filled. The CNT deposition in TTSV can be done using Plasma Enhanced CVD [7], but it is still a serious difficulty to grow CNT bundles inside TTSV.

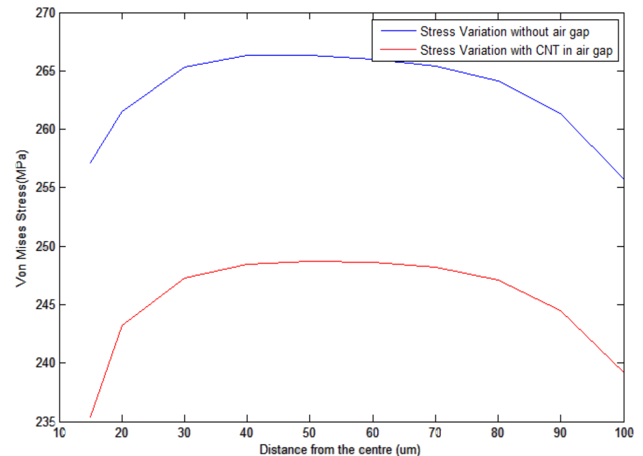

Figure 4: Comparison of stress at IC-3 layer by incorporating 5µm CNT as core material and then Cu in TTSV with respect to ideal TTSV. Stress decreases significantly. Similar trend is observed in other IC layers.

3.3.2 CVD Diamond as Liner of TTSV

Further in the earlier studied structure, we have used SiO2 as liner, which is a good electrical insulator but it also acts like a heat insulator. This may slow down flow of heat from substrate to TTSV. To increase the thermal conductivity and at the same time, ensuring low electrical conductivity, we have proposed to introduce CVD diamond as a liner material which has high thermal conductivity but poor electrical conductivity (which resolved the insulation from the substrate) and evaluate the stress. We have again observed significant improvement in stress level in the substrate as shown in Fig.5.

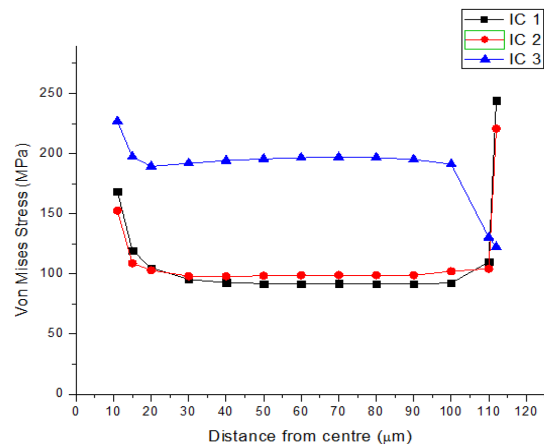

Figure 5: Stress at each IC layers by incorporating CVD diamond as liner material. Stress of IC layers reduces further, as compared to initial TTSV structure shown in Fig.2

3.3.3 CNT as Core and CVD Diamond as liner TTSV

Integration of both CNT and CVD diamond with Cu and SiO2 respectively, it was observed that there is a significant reduction of stress about (~86 MPa) at most stressed IC3 level as observed in Fig.6.

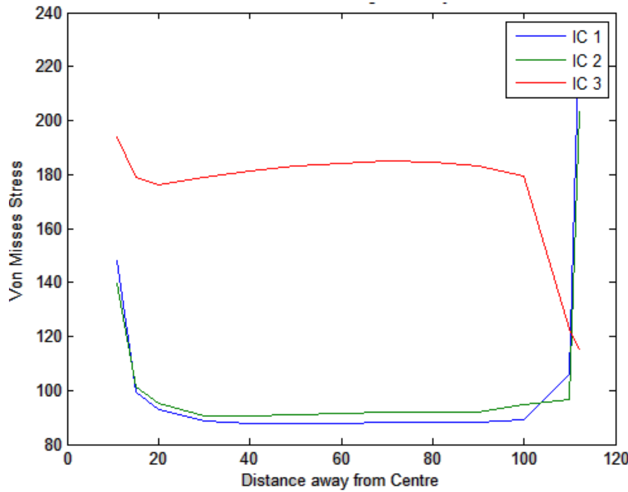

Figure 6: Stress at each IC layers by incorporating CVD diamond as liner material and CNT as core material in place of air and followed by Cu. Stress of IC layers substantially decreases as compared to initial TTSV structure shown in Fig.2.

3.4 Stress Analysis in bundled TTSV structures

The analysis considers that the placement of TTSVs generates stress in the Silicon material as it would arise in actual fabrication and thus displays the possible defect occurrence with such generation of stress due to lattice mismatch due to the placement of TTSVs in 3D IC. Figure 7 depicts the Von Misses Stress (VMS) in the structure when the stress generation in silicon is such that all Volume force in TTSV is aligned in same direction. Considering the element B in the structure, the effective force at the cross section in middle of the element is only due to the boundary force of Silicon substrate. There by the stress in the IC, is less in that region.

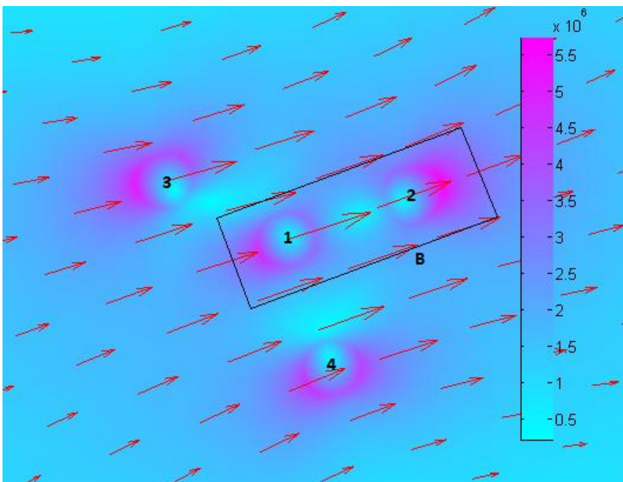

Figure 7: Stress generated in silicon due to the same alignment direction of force generation due to the presence of lattice defects. (Arrow depicts displacement and Block B is considered for analysis)

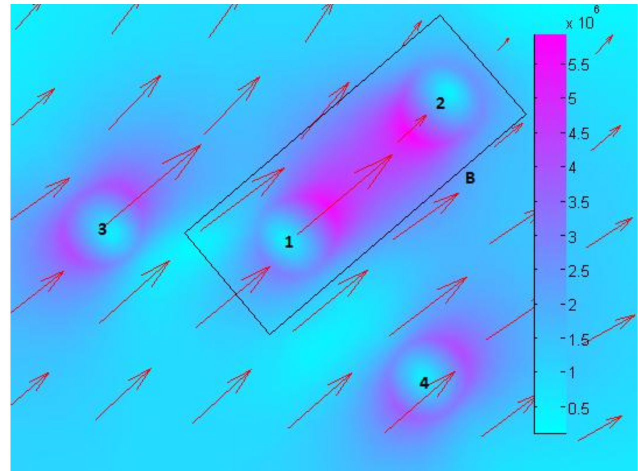

Figure 8: Stress generated in silicon due to the alignment direction of volume force due to the presence of lattice defects such that TTSV2 has it in opposite direction with respect to all other TTSV.

However, Figure 8 depicts that due to opposite alignment of volume force of TTSV structure 2 with respect to other TTSVs, the VMS value goes to high value. Considering element B, the effective force at the cross section in the middle of the element is the sum of volume force on the TTSV structure and the boundary force. There by, the VMS value is higher in that region. From the above analysis, it is understood that the placement of TTSV structure in Silicon substrate plays an important role in stress generation. However, the reason for such a generation of stress has to be analyzed and we should come up with proper fabrication process which should overcome this stresses.

4. Conclusions

This is the first comprehensive study on such extensive effect of TTSV insertion and mitigation strategy in 3D IC Layer stacking. It was found that it leads to substantial stress at different IC levels which degrades the performance and reliability of the device. We also observed that process limitation such as void formation in via filling even further increase the stress in a different layer. We have also proposed plan to reduce the stress at different IC level by introducing CNT in the void and CVD as the liner and witness significant reduction of stress level by about 30%. Finally, in order to have mechanical reliability during the usage of 3D IC the stresses developed must be below the yield strength of Copper. Thus, the above proposed solution will be able to give the desired result in 3D IC development. Thus, from the above graph, by using CNT material to fill the air gap and using CVD as a liner material, the stress generated in 3D IC is the least among all the configurations. CNT, CVD having a higher conductivity reduces the temperature of the structure, thus, it also decreases the stress in the IC layers. We have also analysed the stresses which arise due to the lattice defects through the placement of TTSVs in 3D IC but the reason for such stress has to be found.

5. References

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