A Reconfigurable Medically Cohesive Biomedical Front-End with $\Sigma\Delta$ ADC in $0.18\mu m$ CMOS

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***Abstract*—This paper presents a generic programmable analog front-end (AFE) for acquisition and digitization of various biopotential signals. This includes a lead-off detection circuit, an ultra-low current capacitively coupled signal conditioning stage with programmable gain and bandwidth, a new mixed signal automatic gain control (AGC) mechanism and a medically cohesive reconfigurable $\Sigma\Delta$ ADC. The full system is designed in UMC $0.18\mu m$ CMOS. The AFE achieves an overall linearity of more 10 bits with $0.47\mu W$ power consumption. The ADC provides 2^{nd} order noise-shaping while using single integrator and an ENOB of $\sim$11 bits with $5\mu W$ power consumption. The system was successfully verified for various ECG signals from PTB database. This system is intended for portable batteryless u-Healthcare devices.**

I. Introduction

Cardiovascular diseases (CVDs) have been reported to cause most number of deaths globally [1]. This calls for a system which focuses not only on curing the illness (hospital-centric approach), but also on prevention and early detection of symptoms (patient-centric approach). Continuous electrocardiogram (ECG) monitoring of biosignals become mandatory for such systems. All this, augmented with the radical advancement in CMOS and wireless communication technologies, has given impetus to concept of u-Health (ubiquitous healthcare) and use of wireless body area network (WBAN) based applications [2]-[4].

Lately there has been a spur in the number of research and publications related to self-powered acquisition systems for body sensor nodes (BSN). Incorporating energy harvesting mechanism can endow BSNs an indefinite lifetime. An ultra-low power system rendering the functionality of acquiring, processing and transmitting is presented in [5]. The BSN chip is powered by the energy harvested from human body heat through a thermoelectric generator (TEG). Another batteryless acquisition system powered by an adaptive RF scheme is reported in [6]. Reference [7] presents an excellent review on self-sustainable systems. Some related works make their system reconfigurable also. Such a system with different types of monitoring is described in [8].

The block diagram of the proposed ultra-low power system for acquisition and digitization is shown in Fig. 1. The prime features of the system are:

1) Leadoff detection circuit. The subsequent blocks are powered on only if the signal $Lead-off$ is low [9].
2) An ultra-low power two stage capacitive-coupled signal conditioning circuit (AFE). Apart from providing programmable amplification, it also includes tunable 2^{nd} order highpass and lowpass characteristics. Hence it is useful as a generic scheme for acquisition of various biopotential signals (ExG) with different bandwidth and dynamic ranges or gain requirements.
3) An efficient gain control (AGC) mechanism to maintain the input of the ADC to an optimum level for which the ADC provides maximum SNR. In all of the acquisition schemes (even those where gain is controlled via DSP) reported till date, the ADC is kept continuously on. Hence, the present scheme is envisaged to consume lesser power than the conventional ones because
   a) ADC is turned on only after AGC has finished its job, and
   b) it avoids gain control through a DSP which is very power hungry [10].
4) A low power high resolution discrete-time (DT) $\Sigma\Delta$ ADC that achieves 2^{nd} order noise shaping while using a single integrator. The high resolution is justified as follows
   a) Accuracy of the classification and feature extraction algorithms processing the output of the ADC are proportional to the resolution of the ADCs. Hence the high ENOB achieved here is more medically cohesive to diagnosis, similar to the data available at [11].
   b) It extends the utility of the scheme for the digitization of a wide range of ExG signals [12].
5) Seamless $\Sigma\Delta$ ADC resolution reconfigurability with minimal hardware and almost zero power overhead.
   a) This facilitates the digital circuit, following the $\Sigma\Delta$ ADC, to reduce its power consumption by opting to process low resolution data. The proposed $\Sigma\Delta$ ADC implementation aids area and power cost-efficient switching between the two modes vis-a-vis other ADC architectures e.g. SAR ADC, pipeline ADC, etc.
   b) Facilitates reconfigurability between low and high resolution for preliminary and final diagnostics, respectively.

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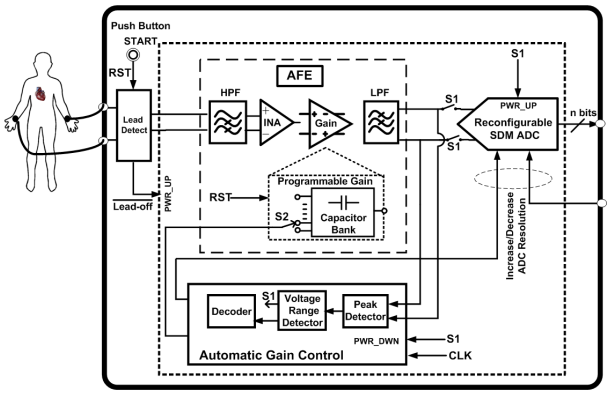

Fig. 1. Block diagram of the proposed acquisition system.

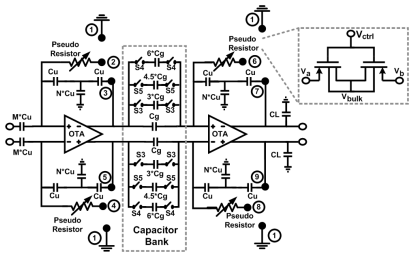

Fig. 2. Analog front-end providing both amplification and LPF and HPF characteristics. (M=10, N=8, C_U=1.03pF, C_g=103fF, and C_L=2-12pF). An input signal strength from 0.1mV to 1mV is considered here.

c) Since the noise power at ADCs input is inversely proportional to AFE′s gain, this scheme provides a choice between low and high resolution for high and low gain, respectively.

II. MOS TRANSISTOR LEVEL IMPLEMENTATION OF INDIVIDUAL BLOCKS

A. Signal Conditioning Stage with Programmable Gain and Tunable Bandwidth

In this work, the signal conditioning stage is implemented as a two stage amplifier with capacitive feedback (see Fig. 2). The pair of nodes connected are (2,1), (4,1), (6,1) and (8,1). The connection between the pairs (2,3), (4,5), (6,7) and (8,9) is avoided due to the problem related to gate leakage current of the OTA input transistors [13]. Also it is important to keep the HPF cut-off frequency below 50mHz, else the output waveform exhibits a slight ramp for each T-P segment. The heart of each of the stages is a fully differential recyclic folded cascode (RFC) OTA adopted from [14]-[16]. All the transistors are operated in weak inversion to obtain such low drain currents.

The voltage gain of the closed loop amplifier is varied by changing the feedback factor. Coincidentally, this feedback resistor also determines the HPF cutoff frequency of the AFE, which is supposed to remove the low frequency noise and dc offset [17]. Realizing a pole $\sim$ 0.25Hz-1Hz, would require a very high resistance. The high resistance value is obtained using a tunable pseudo-resistor [19] .While the high pass cutoff frequency is varied by changing the gate voltage of the pseudo-resistor, the lowpass cut-off frequency is varied changing the load capacitance C_L. Further, a T-feedback network is used to reduce the effective feedback capacitance so that the same gain can be achieved with much smaller capacitance [20].

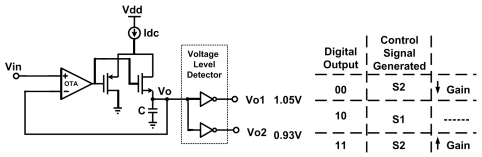

Fig. 3. Block diagram of the peak detector and voltage level detector. The digital output and the control signals generated are also shown. Here C=30pF and I_{dc}=92pA.

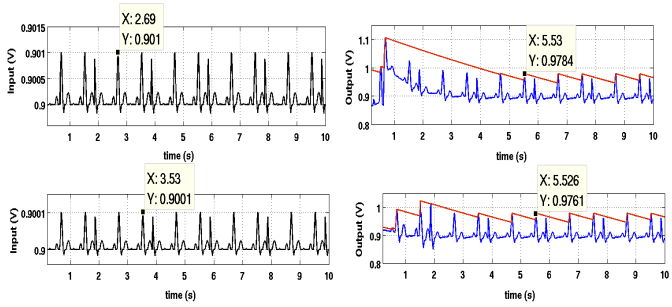

Fig. 4. Plots showing automatic gain control using the peak detector. The figure shows the input (top and bottom left) and output (top and bottom right) wavefroms of the AFE for an input signal strength of 0.1mV to 1mV, respectively. The output of the peak detector is shown in brown color.

B. Automatic Gain Control

Gain of the system is controlled using a peak detector, digital control logic and a logic isolation block which decouples the gain control mechanism from the analog front end once the input falls in the desired amplitude range [21]-[22]. Fig. 3 shows the scheme for peak and voltage level detection. The peak detector is adopted from [23]. The OTA of the peak detector is a low power folded cascode amplifier with all its transistors operating in weak inversion.

Also, the peak detector is designed such that it's total discharge time is higher than the time duration between two R peaks. Hence, here the discharge time is kept greater than 1s to prevent the digital control logic from varying the gain during low amplitude peaks (P,Q,T) of the ECG signal [24]. Fig. 4 shows that the voltage level detector is able to generate the required digital output for proper selection of capacitors from the capacitor bank (see Fig. 2) such that output V_0 satisfies 0.93V $\leq V_0 \leq$ 1.05V , as expected.

C. Opamp-shared $\Sigma\Delta$ ADC

A conventional DT cascaded integrator feedback (CIFB) $\Sigma\Delta$ modulator with 2^{nd} order noise shaping is chosen for this work. Owing to the fact that the integrator is the most power hungry block of the $\Sigma\Delta$ ADC, twofold strategy was employed to minimize the ADCs power consumption. First, the whole ADC was designed for as minimum current as

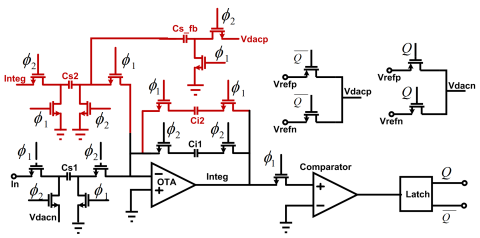

Fig. 5. Single ended representation of the fully differential opamp shared DT $\Sigma\Delta$ ADC . The circuit renders 1^{st} order noise shaping when only components in black color are activated, and 2^{nd} order noise shaping when the components in dark red are also activated. Here C_{S1}=1.3428pF , C_{S2}=2.136pF, C_{S_fb}=0.79pF, C_{i1}=8.132pF, C_{i2}=4.066pF and V_{cm}= 0.9V. Here ϕ_1 and ϕ_2 are the two non-overlapping clock phases, V_{refp} and V_{refn} are positive and negative reference voltages , and, Q and $\overline{Q}$ are the ADC's output and it's compliment respectively.

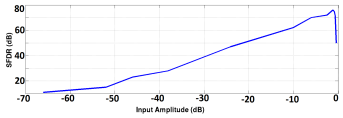

Fig. 6. Variation of SFDR with input amplitude for the $\Sigma\Delta$ ADC in Fig. 6.

possible keeping the target SNR intact. Second, the 2^{nd} order noise shaping was achieved using only a single integrator, which reduces the power consumption to nearly half that of the ADC employing two integrators. The plot of variation of the spurious free dynamic range (SFDR) with input amplitude (see Fig. 6) is used to determine the optimum input level of the ADC, and hence the gain ratios required from the AFE. The integrator is implemented using the enhanced recyclic folded cascode (ERFC) [14]-[16]. The ERFC OTA has twice the bandwidth of a conventional folded cascode OTA for the same power and area.

D. Seamless ADC Resolution Reconfigurability

The output of the $\Sigma\Delta$ ADC is taken up by the subsequent digital circuit for relevant signal processing like classification and feature extraction. Since the power consumed by this digital circuit is proportional to the resolution of the data it is processing, the digital circuit may opt to reduce its power consumption by reducing the resolution of the data it is processing. A control signal from the digital subsequent digital classification and feature extraction circuit selects the output resolution of the $\Sigma\Delta$ ADC. The proposed $\Sigma\Delta$ ADC is designed to work in two modes controlled by the digital block (1) the low resolution (6-8 bits), and (2) high resolution (10-12 bits) mode. In the first mode the $\Sigma\Delta$ modulator provides 1^{st} order noise shaping using one integrator. In the second mode the $\Sigma\Delta$ ADC modulator provides 2^{nd} order noise shaping, while using only a single integrator. Since integrators are the most power hungry circuit in the $\Sigma\Delta$ ADCs, here, a higher resolution is extracted keeping the power consumption nearly the same.

III. Results

The performance of the AFE and the ADC are tabulated in Table I and Table II, respectively. The figure of merit for the ADC are defined as in (1).

$$FOM1 = \frac{Power(W) * 10^{12}}{2^{\frac{SNR(dB)-1.76}{6.02}} * 2 * BW(Hz)} \; pJ/Conv. \quad (1)$$

TABLE I. AFE Performance

Parameter	Value			
	This work	[25]	[19]	[26]
Technology (μm)	0.18	0.35	0.35	0.18
Voltage Supply (V)	1.8	2.5	1	1
Power Consumption (μW)	0.47	0.62	0.9	0.8
CMRR (dB)	110	70	71.2	60
DC Gain (dB)	40-60	40.7	45.6-60	34
Bandwidth (Hz)	0.25-250	5m-200	4.5m-290	0.2-5.8k
NEF	6.4	1.96	3.26	2.79

TABLE II. Opamp Shared $\Sigma\Delta$ ADC Performance

Parameter	Value		
	This work	[27]	[28]
Technology (μm)	0.18	0.18	0.18
Voltage Supply (V)	1.8	0.9	0.7
Order	2^{nd}	2^{nd}	2^{nd}
Bandwidth (Hz)	500	10k	8k
Fs (kHz)	64	5	1024
Power Consumption (μW)	5.0652	200	80
Dynamic Range (dB)	70	83	75
FOM1 (pJ/Conv.)	1.96	0.866	1.087

TABLE III. Quality Assessment of the Reconstructed Signal

Parameter	Value
Percent Root Mean Square Difference (PRD)	86.11
Root Mean Square Error	2.03e-6
Signal to Noise Ratio (dB)	41.29
Maximum Amplitude Error (MAE)	9.05e-6
R-squared Score	0.99

Frequency response of the AFE is shown in Fig. 7. The tunability of the AFE (in terms of gain, HPF and LPF cut-off frequency) to match different bandwidth and amplification requirements, evinces the utility of this system for the acquisition of various ExG signals. The plot for spectral density of the ADC's output is shown in Fig. 8. The figure clearly shows that the ADC renders 2^{nd} order noise shaping and SNR of 70dB. The complete system was validated for a scaled ECG signal taken from the PTB database [11]. The digital output of the $\Sigma\Delta$ ADC (stream of 1s and 0s) generated by the Spectre simulator is exported to Matlab Simulink, where it is passed through a CIC filter to reconstruct the ECG signal. The quality assessment of the reconstructed signal wrt. the input ECG signal is tabulated in Table III [30], [29]. As is shown in Fig. 9 (bottom most) the reconstructed waveform captures all the essential features of the ECG signal.

IV. Conclusion

An ultra-low power acquisition and digitization system is presented. While the AFE does the job of filtering and amplification, the $\Sigma\Delta$ modulator ADC digitizes the output. All the blocks are implemented in UMC $0.18\mu m$ CMOS technology. Each block is designed with minimum current consumption. Power dissipation is further saved by hardware sharing and keeping the ADC turned off during the

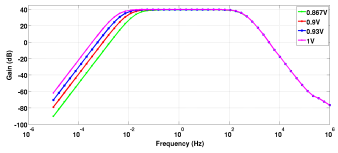

Fig. 7. Frequency response of the AFE. The high pass cut-off frequency is tuned by the gate potential V_{ctrl} of the pseudo-resistor. Different high pass cut-off frequency for different values of V_{ctrl} is shown.

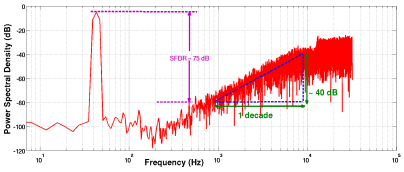

Fig. 8. PSD of the opamp shared $\Sigma\Delta$ ADC for an input of -5.2dB.

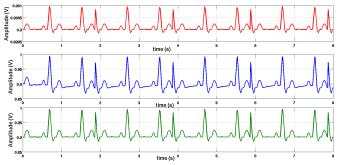

Fig. 9. The topmost waveform is the input ECG signal. The center waveform is obtained with connection between the pairs (2,3), (4,5), (6,7) and (8,9) as shown in Fig. 2 . The waveform exhibits slight ramp for each T-P segment. The bottom most waveform is the correct output signal, with the connection pairs (2,1), (4,1), (6,1) and (8,1).

initial phase of operation. All the blocks meet the desired expectations. The scheme is tested with scaled version of various ECG signals taken from PTB database. The quality assessment of the reconstructed signal wrt. the input ECG signal reveals it's fidelity. The overall system consumes $\sim 6\mu W$ power. This system is useful for u-Healthcare.

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