A study of the precise alignment of mask patterns to the crystallographic orientation of silicon wafers

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“Dedicated to my parents and guide”

Abstract

In the silicon wet anisotropic etching, which is usually performed in alkaline solutions (e.g. potassium hydroxide (KOH), Tetramethylammonium hydroxide (TMAH), etc.), the etch rate is highly orientation-dependent. {111}Si planes are slowest etch rate planes in all kinds of anisotropic etchants. In order to align the mask patterns with respect to the crystallographic directions on silicon wafer, primary flat is commonly employed as reference. In this case, any degree of misorientation in primary flat leads to the misalignment of mask patterns with respect to crystallographic directions. A small degree of misalignment of the mask edge with crystallographic direction result in oversized microstructure due to the underetching at the misaligned mask edges. Hence, in the fabrication of silicon-based microelectromechanical system (MEMS) structures using wet etching, a high precision alignment of mask pattern to crystal orientation is desirable in order to control the dimensions of fabricated structures. Several studies have been performed for the precise alignment of mask patterns with respect to crystallographic directions on {110} and {100} silicon wafers. All these techniques are based on the development of mask patterns to create the pre-etched pattern for the identification of crystallographic directions, for instance, <110> direction on {100}Si wafers. In the existing methods, mask design for pre-etched patterns varies with wafer orientation.

In this dissertation, a mask design comprising a series of circle windows is developed that can be employed for the determination of crystal orientation on both {110} and {100} wafers. The pre-etched patterns formed by this mask are used as reference for the subsequent alignment of mask geometries. The mask are designed using the IntelliMask software. The diameter of the circle is 32 μm and the distance between the centers of two neighboring circles is 48 μm. The accuracy of the correct crystallographic orientation varies with size of the wafer. It increases with wafer diameter. The verification and the validation of the proposed mask design are performed by simulation using IntelliEtch and IntelliMask software.

Contents

Chapter 1: Introduction

1.1 Introduction of MEMS

Microelectromechanical systems (MEMS) is a process technology used to create tiny integrated devices or systems that combine mechanical and electrical components on to the same substrate. They are fabricated using integrated circuit (IC) batch processing techniques such as deposition, lithography, and etching. Generally the size of devise is a few micrometers to millimeters. The term used to define MEMS varies in different parts of the world. In the United States they are predominantly called MEMS; while in some other parts of the world they are called Microsystem Technology or Micromachined devices [1]. These devices (or systems) have the ability to sense, control and actuate on the micro scale and generates effects on the macro scale. While the functioning elements of MEMS are miniaturized structures, sensors, actuators, and microelectronics, the most interesting elements among these are microsensors and microactuators are properly categorized as "transducers", which are defined as devices that convert energy from one form to another. In the case of microsensors the device typically converts a measured mechanical signal into an electrical signal [2].

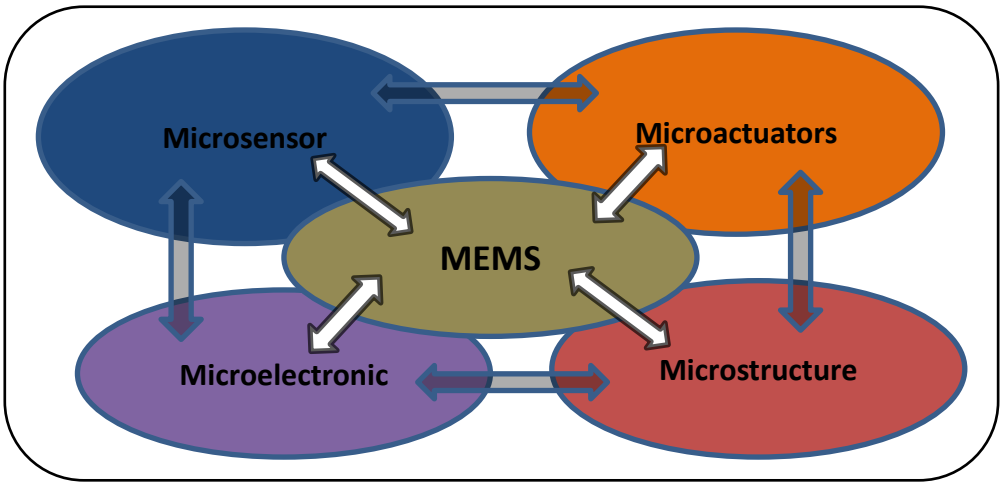


Figure 1.1: Schematic illustration of various components of MEMS devices.

The real potential of the MEMS starts to become fulfilled when these miniaturized sensors, actuators, and structures can all be merged onto a common silicon substrate along with integrated circuits (i.e., microelectronic). While the electronic are fabricated using

integrated circuit (IC) process sequences (e.g., CMOS, Bipolar, or BICMOS processes), the micromechanical components are fabricated using compatible micromachining processes (Bulk and Surface micromachining) that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices [3]. But MEMS are not just about the miniaturization of mechanical components or making things out of silicon (in fact, the term MEMS is actually misleading as many Micromachines devices are not mechanical in any sense). MEMS is a manufacturing technology; a paradigm for designing and creating complex mechanical devices and systems as well as their integrated electronics using batch fabrication techniques[1]. From a very early vision in the early 1950's, MEMS has gradually made its way out of research laboratories and into everyday products [3]. In the mid-1990's, MEMS components began appearing in numerous commercial products and applications including accelerometers used to control airbag deployment in vehicles, pressure sensors for medical applications, and inkjet printer heads [2]. Today, MEMS devices are also found in projection displays and for micropositioners in data storage systems. However, the greatest potential for MEMS devices lies in new applications within telecommunications (optical and wireless), biomedical and process control areas [4].

MEMS have several distinct advantages as a manufacturing technology [5]. In the first place, the interdisciplinary nature of MEMS technology and its micromachining techniques, as well as its diversity of applications has resulted in an unprecedented range of devices and synergies across previously unrelated fields (for example biology and microelectronics). Secondly, MEMS with its batch fabrication techniques enables components and devices to be manufactured with increased performance and reliability, combined with the obvious advantages of reduced physical size, volume, weight and cost. Thirdly, MEMS provides the basis for the manufacture of products that cannot be made by other methods. These factors make MEMS potentially a far more persistent technology than integrated circuit microchips. However, there are many challenges and technological obstacles associated with miniaturization that need to be addressed and overcome before MEMS can realize its overwhelming potential [1].

1.2 MEMS fabrication Techniques

There are many fabrication techniques employed in the MEMS fabrication. The most commonly used techniques are Micromachining, Microstereolithography and LIGA.

1.2.1 Micromachining

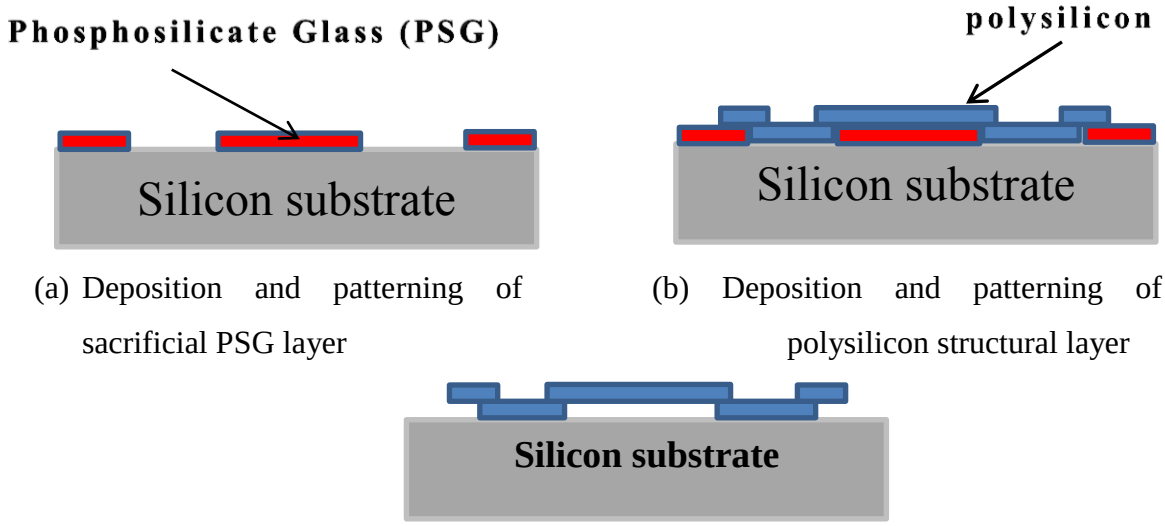
Micromachines are the mechanical objects that are fabricated in the same general manner as integrated circuits. The size of the micromachines is 100 nanometers to 100 micrometers [5]. Micromachining is the most widely used method in MEMS fabrication. This fabrication technique is very simple and cheap. The applications of micromachines include accelerometers that detect when a car has hit an object and trigger an airbag. Complex systems of gears and levers are another application. Most micromachines act as sensors and actuators [6].

The micromachine fabrication techniques are divided into two parts, one is the surface micromachining and another is bulk micromachining.

1.2.1.1 Surface Micromachining

Surface micromachining is one of the most common technologies used to manufacture MEMS devices. It was initiated in the 1980's and is the newest MEMS production technology. Surface micromachining is a fabrication technology used to make the micromechanical structures or devices entirely on the surface of the wafer without ever penetrating the wafer surface. Typically, the micromechanical structure is fabricated from a thin-film material layer such as polysilicon or silicon Nitride [5]. Figure 1.2 presents a generic surface micromachining process flow. The first step is to deposit a sacrificial material layer such as a chemical vapor deposited (CVD) oxide to provide a temporary standoff from the substrate during the subsequent processing steps to form the structural layer Openings are etched entirely through the sacrificial layer so as to provide anchoring points for the structural layer and to prevent the structural layers from floating away during the release step at the end of the process in the step, a thin-film layer of the structural material (commonly with polysilicon) is deposited and etched. After etching the structural

layer, the sacrificial layer is removed, usually by immersion in a wet etchant, and the polysilicon layer is now free to move as a cantilever [1].



(a) Deposition and patterning of sacrificial PSG layer

(b) Deposition and patterning of polysilicon structural layer

(c) Release of structural layer by removal of sacrificial layer.

Figure 1.2: Illustration of surface micromachining process steps involved in fabricating doubly anchored Polysilicon Bridge.

Some of the reasons surface micromachining is so popular are that it provides for precise dimensional control in the vertical direction. This is due to the fact that the structural and sacrificial layer thicknesses are defined by deposited film thicknesses which can be accurately controlled. Also, surface micromachining provides for precise dimensional control in the horizontal direction, since the structural layer tolerance is defined by the fidelity of the photolithography and etch processes used. Other benefits of surface micromachining are that a large variety of structure, sacrificial and etchant combinations can be used; some are compatible with microelectronics devices to enable integrated MEMS device [4]. One of the disadvantages of surface micromachining is that the mechanical properties of most deposited thin-films are usually unknown and must be measured. Also it is common for these types of films to have a high state of residual stress, frequently necessitating a high temperature anneal to reduce residual stress in the structural layer. Also, the reproducibility of the mechanical properties in these films can be difficult

to achieve. Additionally, the release of the structural layer can be difficult due to a stiction effect whereby the structural layer is pulled down and stuck to the underlying substrate due to capillary forces during release which eventually leads to loose of the fabricated structure. Stiction can also occur in use and an anti-stiction coating material may be needed to overcome the stiction problem. The major disadvantage of surface micromachining is that it is inherently a two-dimensional planar process which can limit the flexibility of the design compared to bulk micromachining [5]. Surface micromachining is a relatively new technology and has not been widely employed in commercial production. However, it is expected to become a preferred method of fabrication in the future due to the cost savings and the compatibility with integrated circuit processes.

1.2.1.2 Bulk Micromachining

Bulk micromachining is a process to selectively remove unprotected portion of the silicon substrate to shape and form micromechanical elements. It is the oldest of the micromachining technologies that have been developed as an extension of integrated circuit processes between 1970 and 1980 [1]. It is a subtractive process that uses wet anisotropic etching or a dry etching method such as reactive ion etching (RIE), to create large pits, grooves and channels. Materials typically used for wet etching include silicon and quartz, while dry etching is typically used with silicon, metals, plastics and ceramics [6].

A great advantages bulk micromachining has over surface micromachining is that bulk wet etching techniques can be used quickly and uniformly over a large wafer surface area. This quality makes bulk micromachining a relatively cheap process; in terms of both money and time. Bulk micromachining is a relatively straightforward process and does not require elaborate equipment. Nevertheless, it has several disadvantages. The etchant chemicals commonly used in bulk micromachining are incompatible with integrated circuits or integrated circuit fabrication equipment. Further, compared to other technologies bulk micromachining inherently consumes an inordinate amount of wafer surface area and is usually more costly [4]. Despite these limitations, silicon bulk micromachining is the most widely used micromachining technology and probably will continue to be for the immediate future.

1.2.1.3 Dry Etching

The dry etching technology can split in three separate classes called reactive ion etching (RIE), sputter etching, and vapor phase etching [6].

In RIE, the substrate is placed inside a reactor in which several gases are introduced. Plasma is struck in the gas mixture using an RF power source, breaking the gas molecules into ions. The ion is accelerated towards, and reacts at, the surface of the material being etched, forming another gaseous material. This is known as the chemical part of reactive ion etching. There is also a physical part which is similar in nature to the sputtering deposition process. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction, as shown figure 1.3 [1].

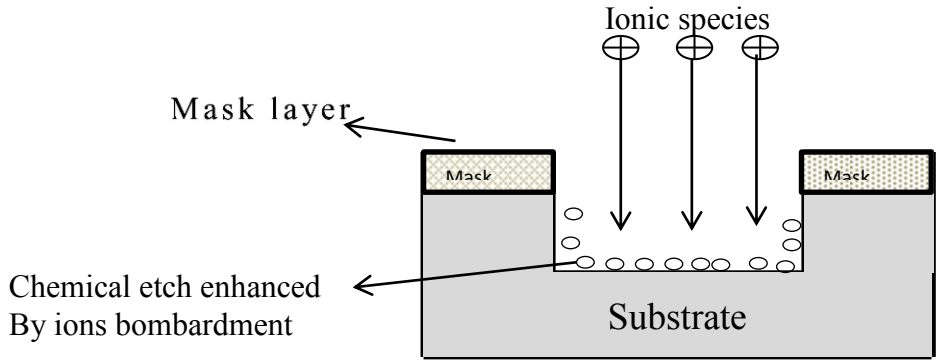


Figure 1.3: Illustration of the chemical etch reaction enhanced by ions bombardment.

It is very complex tasks to develop dry etch processes that balance chemical and physical etching, since there are many parameters to adjust. By changing the balance it is possible to influence the anisotropy of the etching, since the chemical part is isotropic and the physical part highly anisotropic the combination can form sidewalls that have shapes from rounded to vertical.

Sputter etching is essentially RIE without reactive ions. The systems used are very similar in principle to sputtering deposition systems. The big difference is that substrate is now subjected to the ion bombardment instead of the material target used in sputter deposition. Vapor phase etching is another dry etching method, which can be done with simpler equipment than what RIE requires. In this process the wafer to be etched is placed inside a chamber, in which one or more gases are introduced. The material to be etched is

dissolved at the surface in a chemical reaction with the gas molecules. The two most common vapor phase etching technologies are silicon dioxide etching using hydrogen fluoride (HF) and silicon etching using xenon diflouride (XeF2), both of which are isotropic in nature. Usually, care must be taken in the design of a vapor phase process to not have bi-products form in the chemical reaction that condense on the surface and interfere with the etching process [3].

The first thing one should note about this technology is that it is expensive to run compared to wet etching. If you are concerned with feature resolution in thin film structures or you need vertical sidewalls for deep etchings in the substrate, you have to consider dry etching. If you are concerned about the price of your process and device, you may want to minimize the use of dry etching. The IC industry has long since adopted dry etching to achieve small features, but in many cases feature size is not as critical in MEMS. Dry etching is an enabling technology, which comes at a sometimes high cost.

1.2.1.4 Wet Etching

Wet etching describes the removal of material through the immersion of a material (typically a silicon wafer) in a liquid bath of chemical etchant. These etchants can be isotropic or anisotropic. Isotropic etchants etch the material at the same rate in all directions, and consequently remove material under the etch masks at the same rate as they etch through the material; this is known as undercutting which is illustrated in Figure 1.4a and 1.4b. The most common form of isotropic silicon etch is HNA, which comprises a mixture of hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH). Isotropic etchants are limited by the geometry of the structure to be etched [16]. Etch rates can slow down and in some cases (for example, in deep and narrow channels) they can stop due to diffusion limiting factors. However, this effect can be minimized by agitation of the etchant, resulting in structures with near perfect and rounded surfaces as shown in Figure1.4a. Anisotropic etchants have different etch rate in different directions. Potassium hydroxide (KOH) is the most common anisotropic etchant as it is relatively safe to use. Structures formed in the substrate are dependent on the crystal orientation of the substrate or wafer [7, 8, and 9]. Most of the anisotropic etchants high rapidly in {110} planes and less rapidly in the {100} planes.

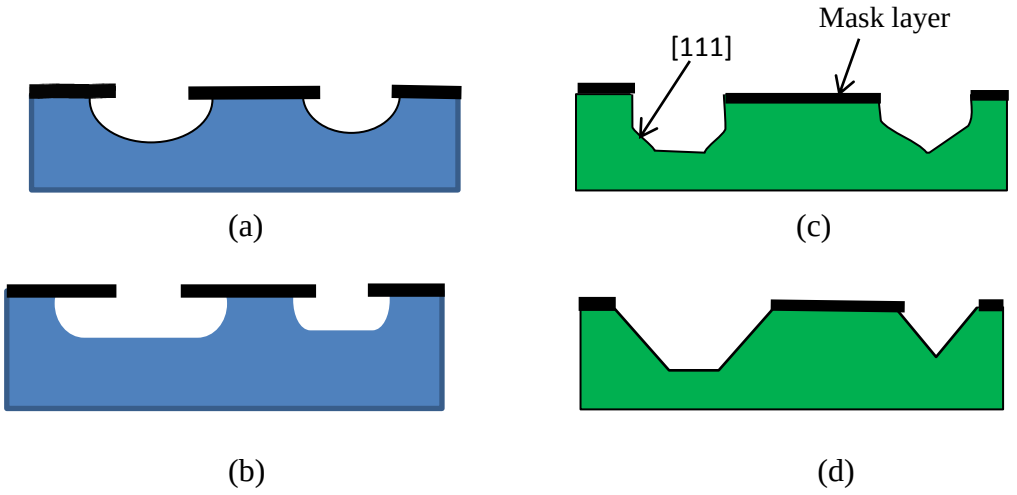


Figure 1.4: Isotropic wet etching with (a) with and (b) without agitation, and anisotropic wet etching of (c) {100} and (d) {110} silicon surfaces.

The (111) plane etches very slowly if at all. Figures 1.4c and 1.4d show examples of anisotropic etching in (100) and (110) silicon wafers, respectively. Silicon wafers, originally cut from a large ingot of silicon grown from single seed silicon, are cut according to the crystallographic plane [9, 10]. They can be supplied in term of the orientation of the surface plane. Dopant levels within the substrate can affect the etch rate by KOH, and if levels are high enough, can effectively stop it. Boron is one such dopant and is implanted into the silicon by a diffusion process. This can be used to selectively etch regions in the silicon leaving doped areas unaffected.

1.2.2 LIGA

LIGA is an important tooling and replication method used widely for high-aspect-ratio microstructures fabrication [3]. This involves the spin deposition of a relatively thick (up to 500µm) layer of polymethylmethacrylate (PMMA) onto a suitable substrate. The PMMA is photo-exposed using X-rays from a synchrotron radiation source and after exposure; a development solution is used to remove the PMMA from the exposed areas thereby creating a plating mould [1]. In the next step the mould cavity is electroplated with metal (example: Ni) by using electroplating or filled with plastic material by using injection molding. In final step the PMMA accompanying the metal or plastic part is removed by inserting it in liquid solution there by finally left with the desired high aspect ratio structures. X-ray exposure is widely employed in the LIGA process because of its high

energy X-ray radiation allows the entire thickness of the PMMA to be completely exposed without significant diffraction effects. Consequently, the aspect ratio of the resultant PMMA moulds is very large, with aspect ratios of more than 100 routinely achieved [6].

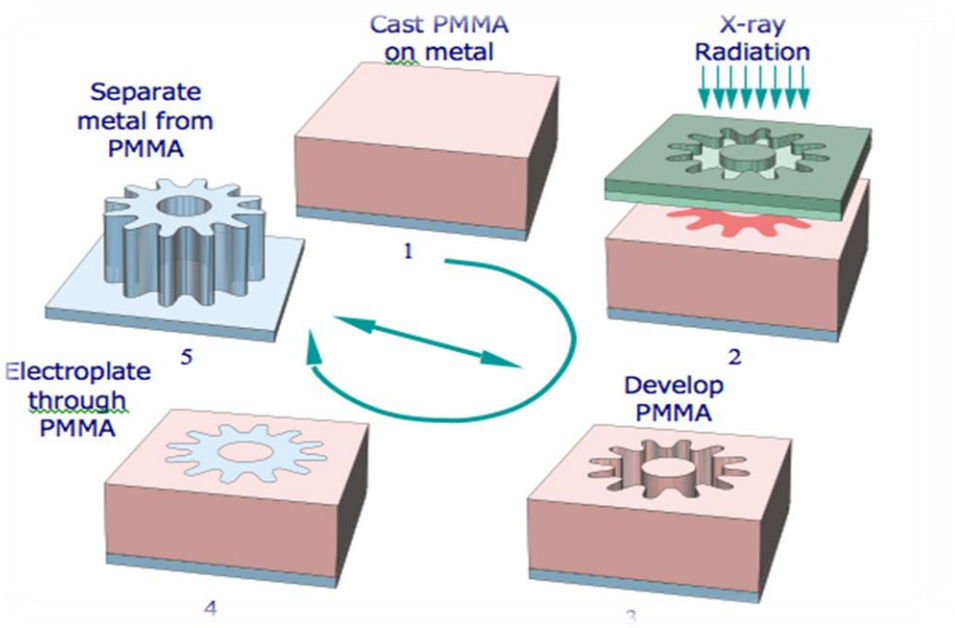


Figure 1.5: Illustration of processing steps involved in the LIGA process.

The high fidelity of the LIGA photoengraving process allows very dense patterns with very small dimensions to be faithfully reproduced in the PMMA material. However, LIGA processing requires a synchrotron radiation source and therefore has limited accessibility, as shown figure 1.5. Commercially available photo resists or photosensitive polyimide layers combined with near-UV light sources have enabled many research groups to realize high-aspect-ratio plating moulds suitable for micromechanical component fabrication. Because LIGA requires a special mask and a synchrotron (X-ray) radiation source for the exposure, the cost of this process is relatively expensive. A variation of the process which reduces the cost of the micromachined parts made with this process is to reuse the fabricated metal part (step 5) as a tool insert to imprint the shape of the tool into a polymer layer (step 3), followed by electroplating of metal into the polymer mold (step 4) and removal of the polymer mold (step 5). Obviously this sequence of steps eliminates the need for a synchrotron radiation source each time a part is made and thereby significantly lowers

the cost of the process. The dimensional control of this process is quite good and the tool insert can be used many times before it is worn out [1].

1.3 Alignment.

Alignment is a process in which we align the mask patterns along different crystallographic directions or with respect to the pattern that already exists on the wafer. If the mask pattern is perfectly aligned with respect to the pre-etched pattern it is termed as perfect alignment, and if it is not perfectly aligned then it is known as misalignment. In the fabrication of MEMS components, Bulk and Surface micromachining processes basically involves several processing steps. Photolithography is one of the major steps which involve transferring of required pattern on the substrate from the photo mask by accurately aligning the photo mask edge with the wafer flat. The exact structure of the desired pattern mainly depends on two things one is how accurately the mask edge is aligned with the wafer flat and another thing how accurately the wafer flat is defined by the manufacturers [7, 12]. Generally (100), (110) and (111) silicon wafers with different flat orientations such as <100>, <110> and <111> are available in the market to fabricate different types of MEMS structures on wafer surfaces. A small degree of misalignment of the mask edge with the wafer flat or a minor manufacturing error in the wafer flat orientation results in significant change in the final desired structure.

Various methods have been developed to determine the different orientations on different silicon wafers for anisotropic wet etching. X-ray diffraction is commonly used to determine crystallographic orientation with very high precision, but it is not very advisable to put x-ray equipment into a mask aligner [13]. So that the pre-etch method is commonly used to get the correct orientation on silicon wafer. Because this method is simple and suitable for the mask aligner and also it is not costly comparing to other method. In this method a series of masks are aligned along an arc with a regular angular pitch on the wafer. Upon etching, we obtain the under-etched patterns. Then, we prefer the orientation of minimum under-etched pattern as a reference to align the subsequent masks in that direction. This process is called alignment and it plays a vital role in MEMS fabrication to get the accurate pattern of the mask on a wafer with a good accuracy of misalignment. We can overcome the effect of

under-etching and obtain the patterns with perfect sidewalls [1]. Thus, we can fabricate the microstructures with an enhancement in the working efficiency.

1.4 Literature survey

There are several methods available to determinate the crystallographic orientation of the wafer. Steckenborn was the first person who proposed the pre-etching process to find the <110> crystallographic orientation. He designed a sophisticated mask pattern to align the subsequent mask to the <110> direction [Steckenborn et al.]. However, lack of quantitative results constrains its application [13]. Ensell [Ensell.*et*] suggested an orientation etchmask design to find the <110> crystallographic orientations with accuracy ±0.1 in (100) wafers [14]. Schroder improved Ensell's design by adding a dial and doubling the resolution via size reduction of the circular patterns, respectively. The method used by Ensell and Schroder could be used together with an optical microscope to find <100> crystal orientation without any other special equipment. To meet the requirements of both good observability and higher resolution, Vangbo proposed an alignment fork to detect the orientation with the resolution up to ±0.05 and developed a method which clearly points out the orientation of both (100) and (110) wafers [15]. Lai [Lai *et al*] also proposed a new pre-etching mask pattern to find <110> crystal orientation on the (100) silicon patterns with resolution achieving ±0.01 [16]. This principle is based on the rectangular undercutting of etchmask patterns in a pre-etch step. Both Vangbo and Lai's etching patterns had the advanced resolution and observability.

1.5 Objective of the work

There are several mask patterns already developed to get correct orientation of the primary flat on the wafers by using pre-etching method. But, these entire mask patterns vary from wafer to wafer. These pre-etching mask patterns are different for different silicon wafer and also for different primary flats.

The present work is aimed to develop a single mask pattern which can be used as a pre etching pattern to find out the <100> and <110> orientation of the primary flat on both (100) and (110) silicon wafers using IntelliMask software. In order to determine the accurate crystallographic directions using pre-etched geometries, the size of mask patterns

is optimized. Accuracy of the proposed pre-etching pattern is validated using IntelliEtch simulation software.

Chapter 2: Mask design

2.1 Design of pre-alignment pattern

A pre-alignment mask pattern is proposed for finding the accurate direction of the primary flat on both {110} and {100} silicon wafers. The mask layouts consist of a series of circular windows in the dark-field mask, as shown figure 2.1. The pattern contains a number of circular windows in order to get the correct orientation of the primary flat in both Si{110} and Si{100}.The dimension of the circular window is also very important for getting the accurate orientation of the primary flats. In the alignment set, the diameter of the circles is 32 µm. and the distance between the centers of two neighboring circles is 48 µm. The alignment sets are positioned annually on an arc of radius R_0 which varies according to the diameter of the wafer.

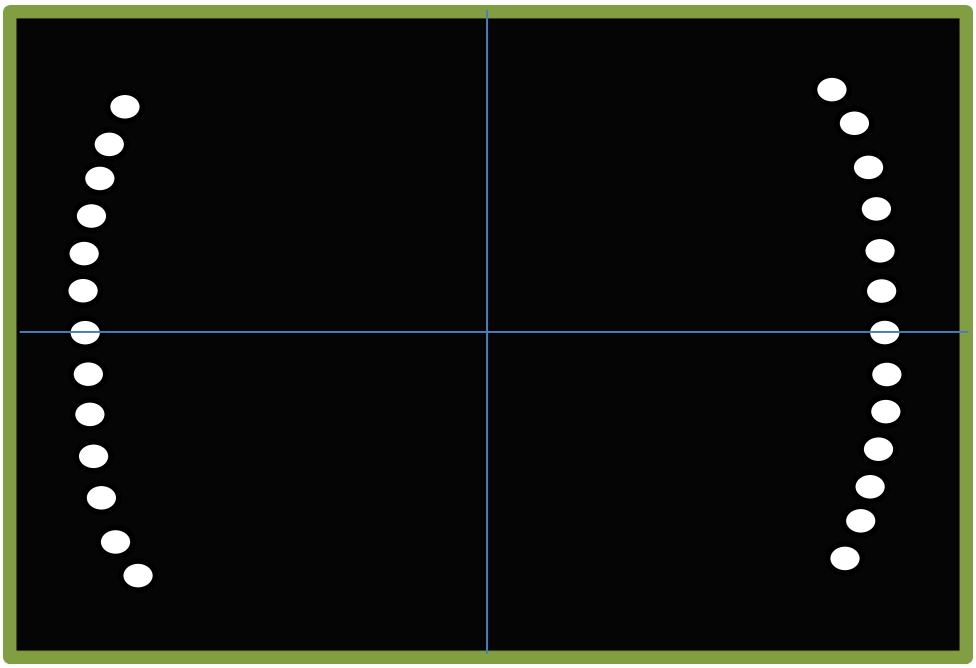


Figure 2.1: Illustration of pre-etching mask pattern

In the pre-etching pattern, the diameter of one of the circular window is made parallel to the edge of the mask such that the centerline of the mask passes diametrically through this circle, as shown figure 2.1.

Circles are made by considering an angular pitch above and below are same from this central circle. In order to get a symmetric pattern, the number of circles in the series above and below the central circle is made same. The symmetry of the pattern has a very important role on pre-etching method. When the mask pattern is transferred to the silicon wafers, the edge of the mask aligns with the primary flat of the wafer. So the wafers have same symmetry pattern as that of the mask. If there is any misorientation of the primary flat of the wafer then the symmetry of the mask pattern is shifted to a new position on the wafer after etching [15]. The line of symmetry of the pattern which is identified after etching represents the correct orientation of the primary flat. Similarly the same alignment set is also designed on the other side of the mask. The purpose of using a pair of circular window with symmetry location on opposite side of the wafer is to increase the accuracy for the correct orientation indication. The angular pitch of each circle depends on the wafer diameter and also distance between two neighboring circle's centers.

Table 2.1: The error calculated for wafers of different diameters.

Size of wafer (Diameter) (mm)	Radius of arc (mm)	No. of circle for 5^0 mis- alignment	No. of circle for 10^0 mis-alignment	Error (Degree)
25	11.5	13	23	0.1
51	24.5	27	47	0.06
75	36.5	41	72	0.04
100	48.9	52	97	0.03
130	64	69	127	0.0225
150	74	81	147	0.0945
200	99	107	197	0.0145
300	149	162	298	0.0096
450	224	225	446	0.0064

This mask layout is use to get the correct orientation of different type of primary flat on {110} and {100} silicon wafer. After conducting number of simulations, it has been found

out that as the radius of the arc increases, the error of the determination of the correct orientation decreases. It is also found out that the number of circles is dependent on the radius of arc and the misorientation of the primary flat, as shown in table 1. Unfortunately, the wafer flat, used to pre-alignment process, it is having crystal orientation error from 1° to 10° depending on the wafer grades [17]. In the wafers manufacturing factory, primary flat orientation is found out using X-ray crystallographic process. In this process the maximum error is 10°.

Chapter 3: Result and Discussion

3.1 Principal of Alignment scheme

There are various types of silicon wafers in MEMS fabrication process. However the most commonly used wafers are {100} and {110}. <110> flat is a standard flat in {100} Silicon wafer. However the wafers with <100> primary flat are also available. In the case of {110} orientation, the silicon wafers are available with <100>, <110> and <111> primary flats. The {111}Si wafers are used only for specific applications.

The manufacturing of the silicon wafers with accurately oriented primary flat is very difficult. Inaccurately aligned flat leads to an error during the mask alignment process if the primary flat is used as reference. In this thesis a mask design methodology to get accurate orientation of the crystallographic planes on different type of silicon wafers is described. The study is carried out using IntelliEtch and IntelliMask software.

3.1.1 (100) Silicon wafer with primary flat <110>

First, a masking layer is deposited on the Silicon {100} wafer with a primary flat in the direction of <110>.

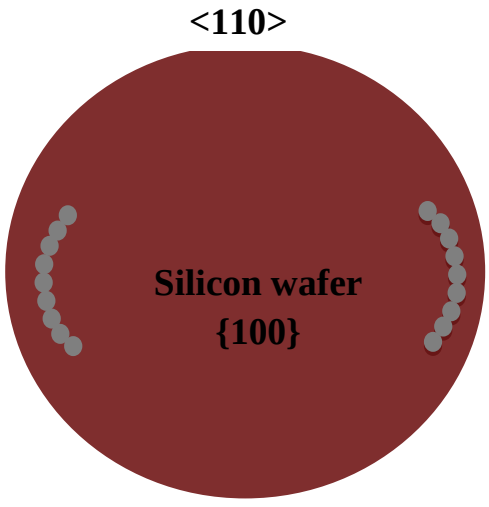


Figure: 3.1: Illustration of pre-etching pattern on the {100} silicon wafer

Selectivity between silicon and the masking layer is very high as a result the etchant etches only the silicon wafer and not the masking layer. In this study, silicon nitride is used as masking layer because this masking material reduces the risk of mobile ion contaminations from the etchant. After deposition of the masking layer, the wafer is coated with the photoresist using spin coater. Photoresist is polymers materials which are sensitive with ultra-violet light. There are two type of photoresist which are used in MEMS fabrication process. One is positive photoresist and the other is negative photoresist. In positive photoresist, that portion on the photoresist where the light falls is soluble in the developer. In the negative photoresist, that portion on the photoresist where the light falls is insoluble in the developer [3]. Then, pre-etching mask pattern is transferred to the silicon wafer using the photolithographic process. In this process pre-etching mask is aligned with the primary flat on the wafer and the ultra-violate (UV) light is made to fall on the wafer through the mask. The portion of the wafer where the light falls through the mask becomes either soluble or insoluble in the developer solution depending on the property of the photoresist materials. This pattern gets transferred near to the edge of the wafer and the mirror image is printed to the opposite wafer, as shown in figure 3.1.

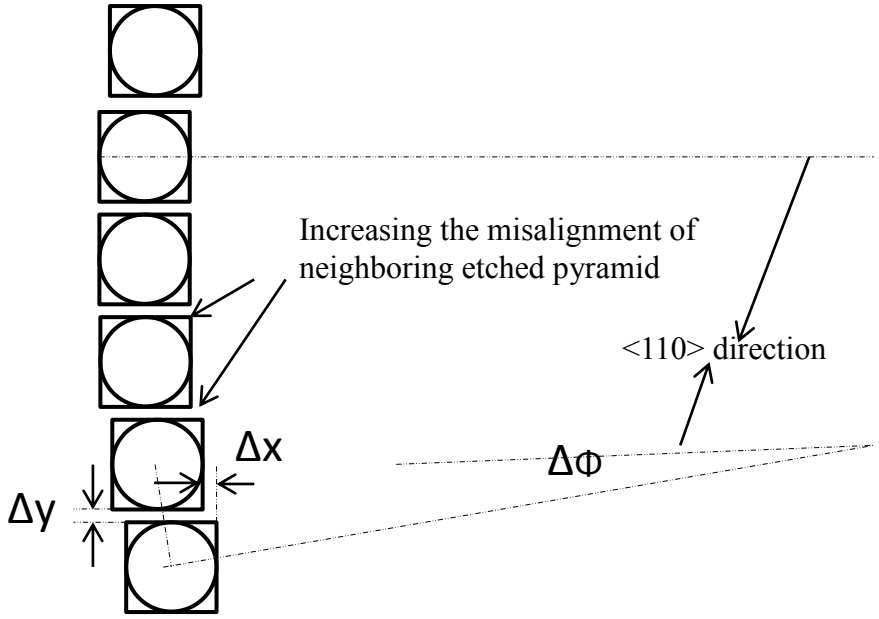
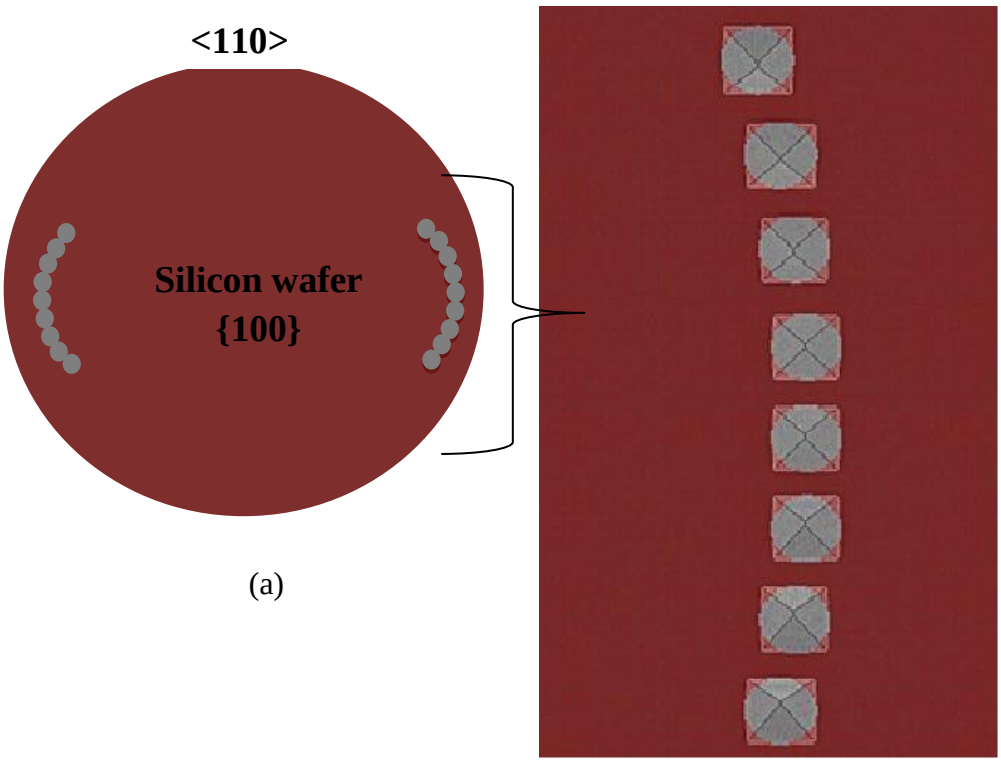


Figure 3.2: Part of the proposed pre etching pattern on the {100} silicon wafer after wet anisotropic etching.

The wafer is then etched using 40% KOH solution at 80^0C for sufficient time for the {111} plane to be exposed [14]. The exposure of the {111} planes occurs because {111} plane has the slowest etch rate as compared to other planes [8-11]. The silicon wafer is etched through the circular windows and as a result of the etching process squares are formed on the surface of the wafer. If prolonged etching is carried out these squares form the bases of an inverted etched pyramid. {111} plane intersects the surface of the wafer along the <110> direction. The position of the etched pyramid relative to its neighbors depends on the alignment of their center circle to the <110> direction. The edges at the bases of neighboring pyramid are misaligned by Δx according to the misorientation of the mask direction and the primary flat of the wafer as shown figure 3.2. The spacing between neighboring pyramids is less than 16 µm, although the minimum misalignment of the pyramids edge was only 0.064 µm.



(a)

(b)

Figure 3.3: (a) Shows the pattern after wet anisotropic etching. (b) Shows zoomed portion of the etched pattern of one side silicon wafer.

The value of Δx increases when the angular pitch increases from the accurate direction of <110>. The Figure: 3.3(a) shows that only a small area at edges of the wafer is etched out during this process, leaving most of the wafer free for devices. etched pyramid on the wafer before the masking layer is stripped.

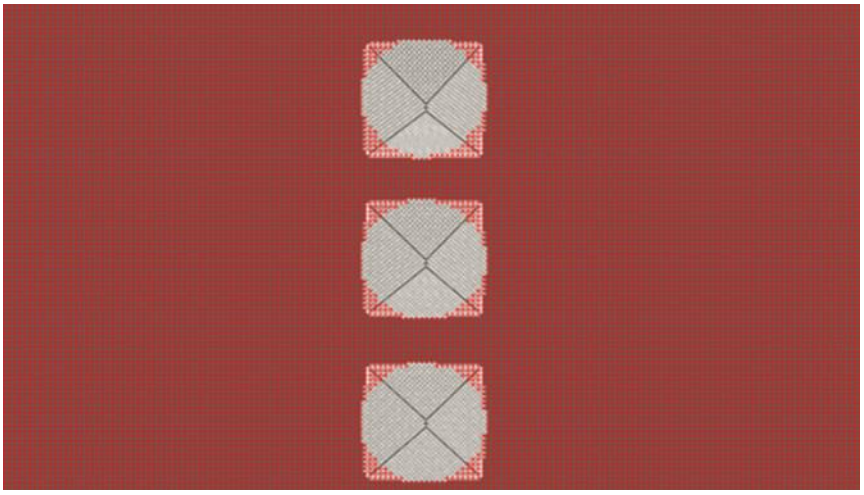


Figure 3.4: Neighboring etched pyramids. The alignment of their edges indicates that their center are aligned to the <110> direction.

The misorientation of the primary flat can be clearly seen in Figure 3.3 (b). Because edges of the center square of the etched pattern are not aligned perfectly to their neighboring squares edges. Figure 3.4 shows that the edges of squares are almost aligned to their neighboring square edges on one side of the wafer. Similarly on the other side of the wafer, edges of squares are aligned to their neighboring squares. The square at the center of all aligned squares is aligned along the <110 > direction [14]. To align the main device mask to the < 110 > direction, the center square of the both side of wafer are used.

3.1.2 {100} silicon wafer with the primary flat <100>

Before etching, the method followed is the same as followed for the pervious wafer. After etching, the circular window becomes square. But these squares are not same as the pervious squares. Since the angle between <110> and <100> is 45^0, this square sides make a 45^0 angle with <100> direction. Along the <110> direction {111} is exposed which has a

slow etch rate. So these squares are surrounded by four {111} planes. The lateral position deviation between the two closest corners on the neighbouring squares indicates how close the square are to the position that the <100> direction line passes. If the two corners of the square are perfectly aligned to each other, as shown in figure 3.5 (a), the direction of <100> line will pass through the center point of the two squares.

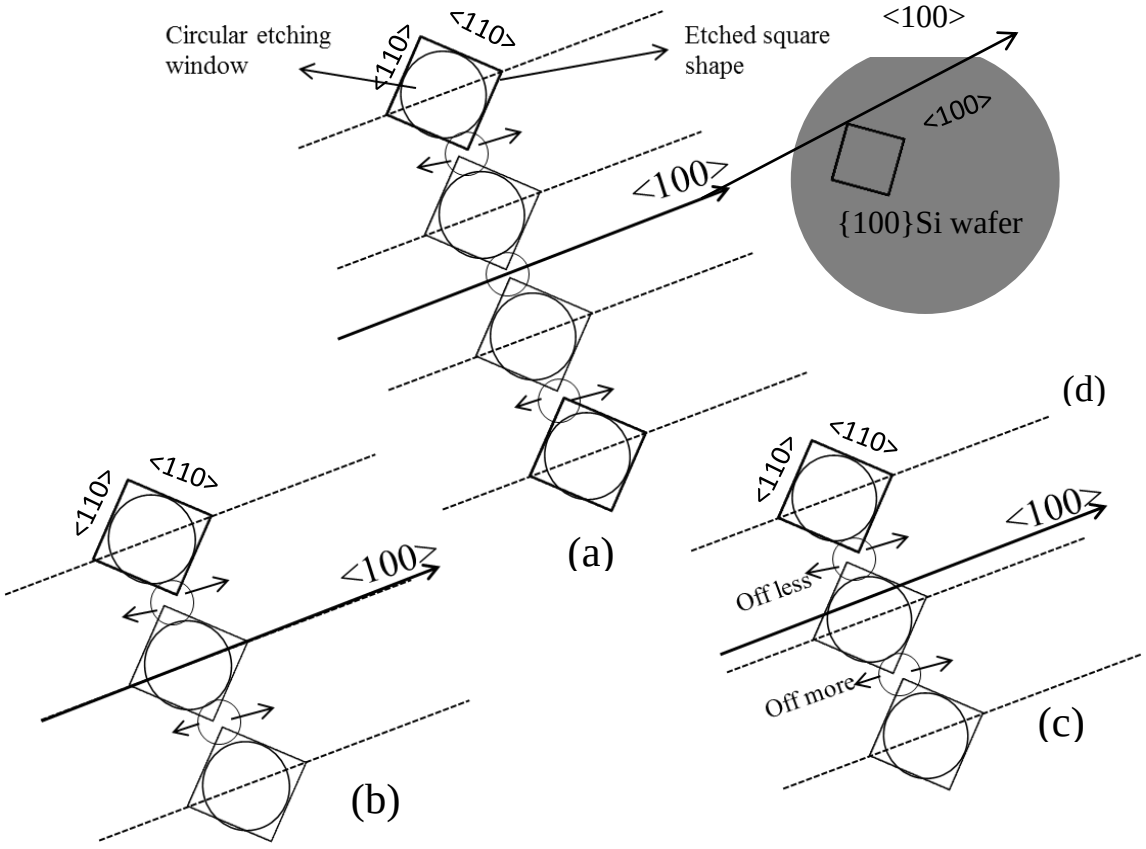


Figure 3.5: The determination <100> direction on (100) silicon wafer: the <100> direction line passes (a) through the center of the corner of two square, (b) through the center of the square, and (c) between the above two extreme cases. (d) is the silicon wafer with flat <100> and also indicate <110> direction.

On the other hand, if the top and bottom of one square laterally deviate from the corner of its neighboring squares with opposite direction but the same magnitude, the <100>

direction line will pass through the center of the square, as shown in figure 3.5(b). Figure 3.5(c) illustrates an intermediate case in which the <100> line passes through the point between the aforementioned two extreme cases, thus the deviation on the top corner is less than that of the bottom corner and has an opposite direction. The <100> direction can be determined accurately from the connection of the pre-determined position indicated by the squares on the opposite sides of the wafer, as shown figure 36 (a).

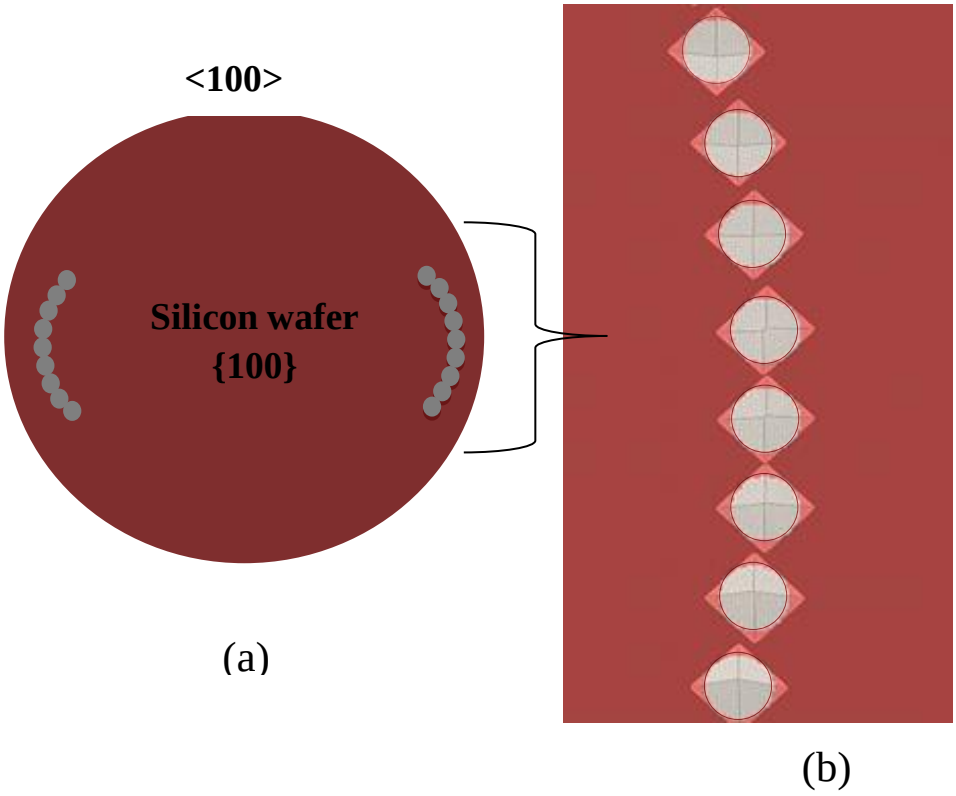


Figure 3.6: (a) Shows the generated pattern after wet anisotropic etching. (b) Close-up view of the etched pattern.

The purpose of using of a pair of squares with symmetry location of the opposite side of the wafer is to increase the accuracy for correct orientation indication [17]. Figure 3.6(b) is the photograph of the etched pattern of one side of the wafer. And also show that the error of the primary flat of the silicon wafer. Similarly pattern is also made on other side of the wafer before masking layer is stripped as shown figure 3.6 (a).

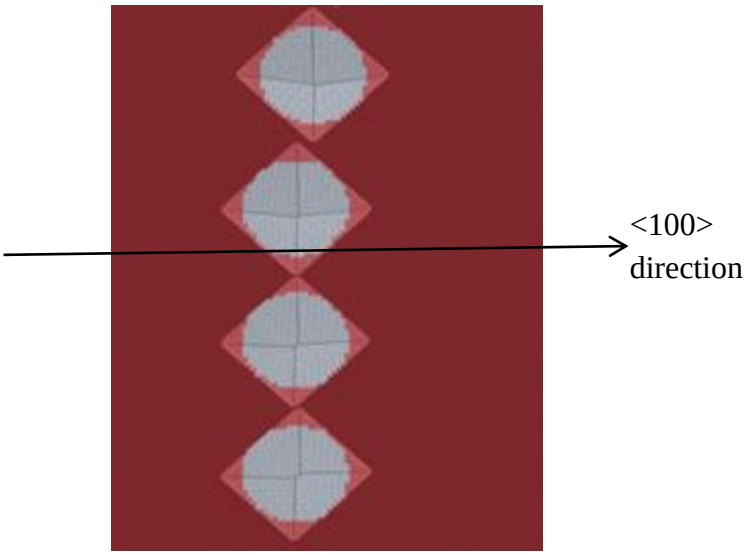


Figure 3.7: Neighboring etched squares. The alignment of their corners are indicates that the <100> direction line are passes through between these two corners.

Figure 3.7 shows that the two squares corners are exactly aligned to each other. Similarly on the other side of the wafer, are also two squares corners are aligned to each other. So <100> direction of line passes through the center of these squares. To align the main device mask along <100> direction the center of these squares of the both side of wafer are used.

3.1.3 {110} silicon wafer with the primary flat <110>

Before etching the process followed is the same as that of followed for the pervious wafers. In this wafer circle becomes a hexagonal structure after etching. In this silicon wafer, the angle between <110> orientations and <100> orientations is 90°. These hexagonal structures have two angles of 109° and four other angles of 125.5° [17]. The hexagon is surrounded by four {111} planes because {111} have a slowest etch rate comparing to the other planes. Two line are in <110> direction, and other four lines are along <211> direction. In the direction of <211> and <110>, {111} planes are exposed. The angle between the line along the <211> direction and the line along the <110> direction is 125.5° and the angle between {111} planes is 109°. Figure 3.8 (a) is an etched pattern on the silicon wafer before the masking layer is stripped off.

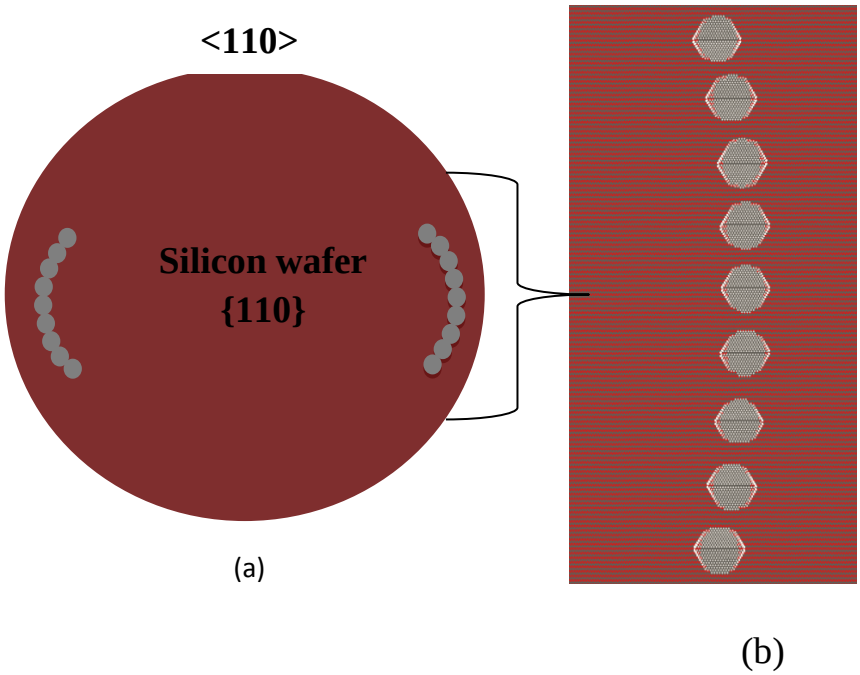


Figure 3.8: (a) Shows pattern on {110} silicon wafer after wet anisotropic etching. (b) Magnified view of the pre-etched patterns.

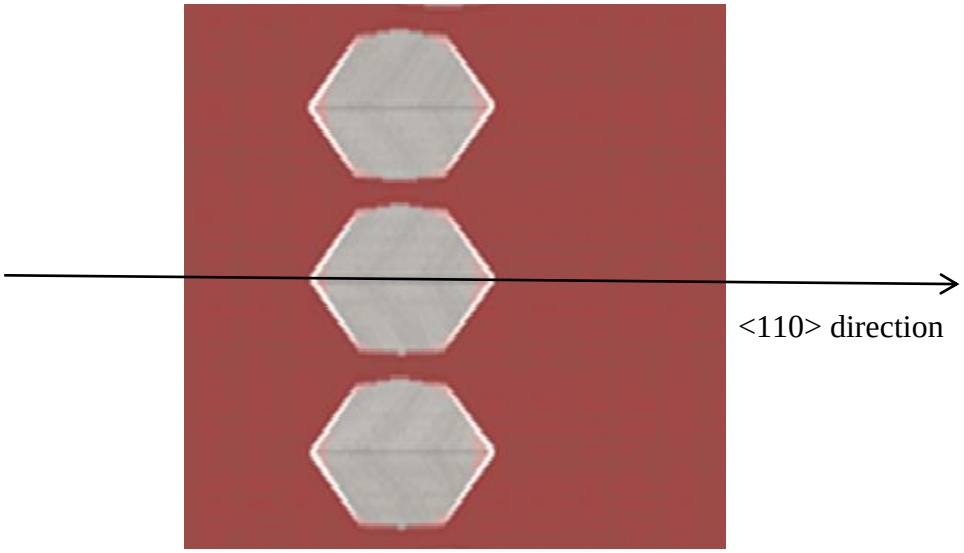


Figure 3.9: Shows the center hexagon edge are alinged to their neighbouring hexagons edges. These lines indicate the <110> orientation.

The etch pattern on the opposite side of the wafer helps to determine the correct orientation of primary flat easily. This mask pattern is called subsequent mask pattern [13]. In figure:

3.8 (b) the edges of the center hexagon are misaligned to their neighboring hexagons, according to the misorientation of primary flat. The spacing between neighboring hexagons is same as the spacing between two neighboring pyramid structure on the {100} silicon wafer with the primary flat direction <110>. The mask pattern of pre-etching alignment set is symmetric, but after etching the etch pattern is not symmetric because the primary flat is not correctly oriented. Figure 3.9 shows that the center hexagon's base sides are aligned exactly to their neighboring hexagons base sides. Similarly other side of the wafer is also having same pattern where the hexagons base sides are aligned to their neighboring hexagons sides. The line which joins corners of the center hexagons on both sides of the wafer indicates the <110> direction as shown figure 3.9. So to align the main devices mask to the <110> direction on {110} silicon wafer the center hexagons corners of the both sides of wafer are used as reference.

3.1.4 {110} silicon wafer with primary flat <100>

Before etching the process followed is the same as that of followed for the pervious wafers. After etching the bulk- etched structure, the circular windows formed to a hexagonal shape surrounded by circular window. The hexagon has two angles of 109° and four other angles of 125.5°. The hexagons are surrounded by four {111} plane and two line along the <110> direction [17]. These hexagonal and previous hexagonal patterns are not exactly same. In the previous hexagons, the lines along the <110> direction are nearly parallel to the primary flat. But in this case, the lines along <110> direction are almost perpendicular to the primary flat. In the previous case the sides of hexagons are aligned to their neighbouring hexagons, which indicate the correct orientation of the primary flat. But in this case, alignment of the corners of hexagons is according to the misorientation of primary flat. The lateral position deviation between the two closest corners of the neighbouring hexagons indicates how close the hexagons are to the position that the <100> direction line passes. If the two corners are perfectly aligned, as shown figure 3.10 (a), the <100> direction line will pass through the center point of the two hexagons, On the other hand, if the top and bottom corners of one hexagon laterally deviate from the corners of its neighbouring hexagons with opposite direction but the same magnitude, the <100> direction line will pass through the center of the hexagons, as shown in figure 3.10 (b).

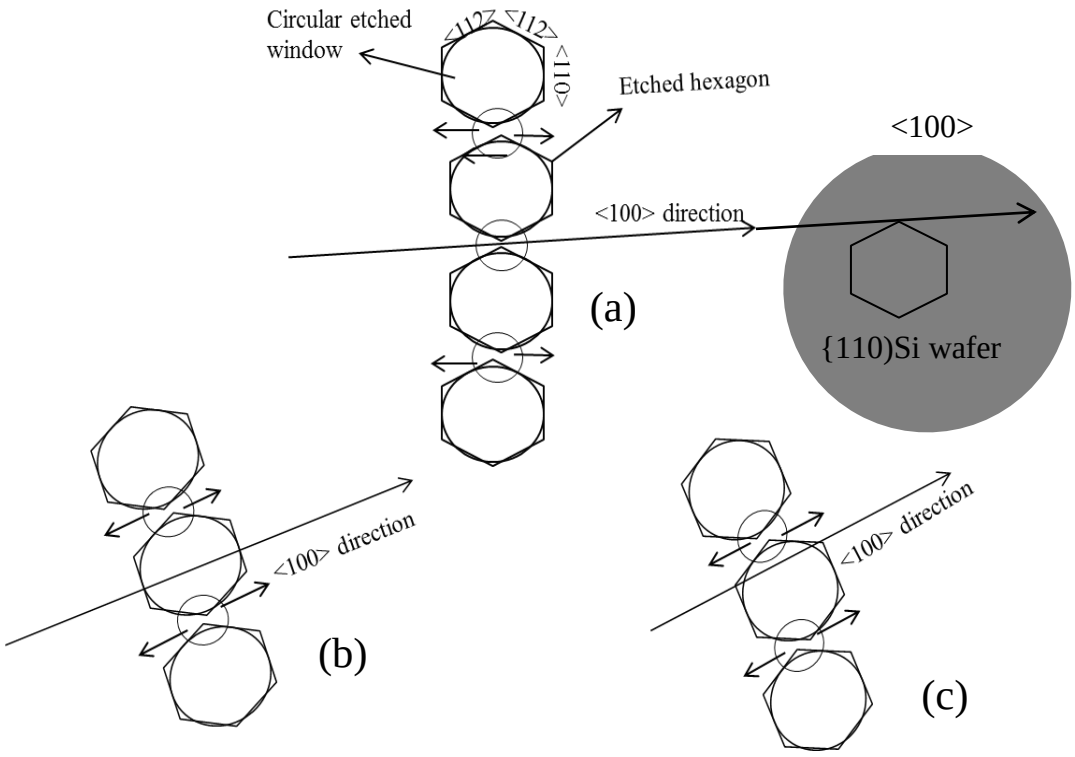
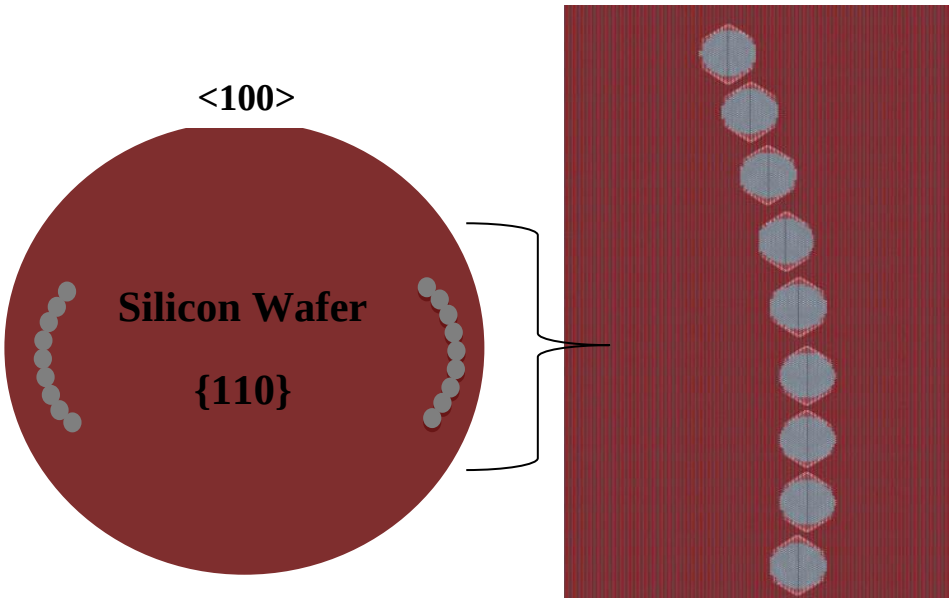


Figure 3.10: The determination of the <100> direction on the {110} silicon wafer: (a) the line passes through the center of the corners of two hexagons (b) through the center of the hexagons, and (c) between the above two extreme cases. (d) {110} Silicon wafer with primary flat is <100> direction.

Figure 3.10 (c) illustrates an intermediate case in which the <100> line passes through the point between the aforementioned two extreme cases, thus the deviation on the top corner is less than that of the bottom corner and has opposite direction. As a result, the <100> direction can be determined accurately from the connection of the pre-determined position indicated by the hexagons on the opposite sides of the wafer, as shown figure 3.1 [17]. The purpose of using of a pair of hexagons with symmetry location of the opposite side of the wafer is to increase the accuracy for correct orientation indication. The hexagons formed by the bulk etching on (110) silicon wafers are not right hexagons. They are surrounded by parallelogram with an angle of 109.5° at the larger corner. The relations between angle of

accuracy Φ, arc radius R, circle radius r, and the distance of the hexagons corner x can be express as

$$\frac{\phi}{360^{o}} \approx \frac{(\sqrt{6})r + x}{2\pi R}$$



(a) (b)

Figure 3.11: (a) Shows pattern on {110} silicon wafer after wet anisotropic etching. (b) Shows zoom portion of the etch pattern.

Above figure 3.11 (a) illustrate the neighboring etched pattern on the {110} silicon wafer before the masking layer is stripped off. Figure 3.11 (b) shows the zoomed part of one side of the wafer. In this figure, the misorientation of the primary flat can easily noticed. Figure 3.12 shows that the corners of the two hexagons are exactly aligned to each other. Similarly the two hexagons corners are aligned to each other on the other side of the wafer.

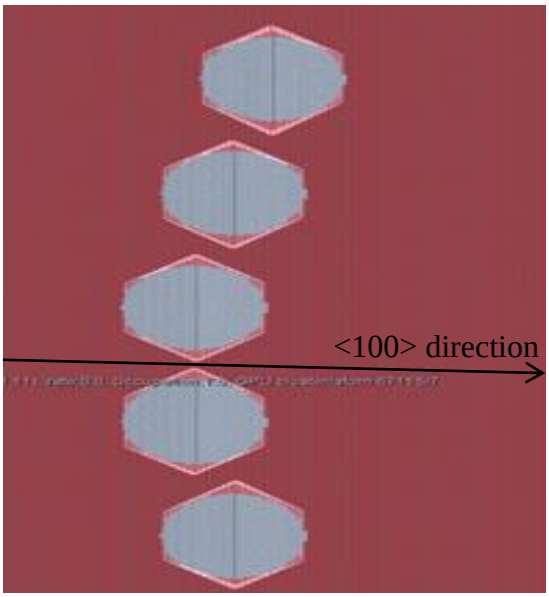


Figure 3.12: Shows that the corners of hexagons are perfectly aligned to each other. The line indicate <100> direction.

According to the figure 3.12 (a) the line along <100> direction on the silicon wafer passes between two corners which are aligned to each other from one side wafer to other side of wafer. For aligning the main device pattern, this line is used as a reference of <100> direction on (110) silicon wafer.

Chapter 4: Conclusions

A new pre-etching pattern capable of determining the <100> and <110> orientation on both {110} and {100} silicon wafer with good observability is proposed and verified. The procedure to align the subsequent photo mask after pre-etching process is also described in this thesis. The design concept and accuracy calculation have also been introduced and elaborated. The pre-etching alignment sets consist of circular windows with diameter 32 μm and center-to-center distance of two neighbouring circles is 48 μm. This pre-etching pattern after etching gives a different shape for different silicon wafers. These different shapes are successfully employed to easily determine the <110> and <100> crystal orientations on both silicon wafers. The accuracy of the correct orientation on the wafer varies according to arc radius of pre-etching pattern. This simple method can be used to indicate the crystal quickly and precisely on both (110) and (100) silicon wafers with minimal substrate damage. This pre etching pattern provides a valuable reference for all subsequent mask patterns for the formation of wet chemical based microstructures for applications in MEMS.

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Figure 3.11: (a) Shows pattern on {110} silicon wafer after wet anisotropic etching. (b) Shows zoom portion of the etch pattern.

Figure 3.12: Shows that the corners of hexagons are perfectly aligned to each other. And the line indicate correct <100> direction.

List of table

References

[1] An introduction to MEMS. PRIME Faradey Partnership, 2002.

[2] J. A. Pelesko, D. H. Bernstein. Modeling MEMS and NEMS. Chapman & Hall/CRC, 2003

[3] J. D. Plummer, M. D. Deal, P. B. Griffin. Silicon VLSI Technology: Fundamentals, Practice, and modeling. Pearson Education, Inc. 2001

[4] http://www.csa.com/discoveryguides/mems/overview.php

[5] F. Chollet, H. B. Liu. A short introduction to MEMS. 4th edition. Creative Commons, 2004.

[6] A. R. Jha. MEMS and Nanothechnology –Based Sensor and Devices for Communication, Medical, and Aerospace Application. Taylors & Francis Group, LLC, 2008.

[7] G. Ensell. Alignment of mask pattern to crystal orientation. Proc. 8th Int. Conf. on solid sensors and Actuators and Eurosensors IX (Stockholm) 1, (1995) 186-189.

[8] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel. Anisotropic etching of crystalline silicon in alkaline solution. J. Electrochem. Soc. 137, (1990) 3612.

[9] K. Bean. Anisotropic etching of silicon. IEEE Trans. Electron Devices, E-25, (1978) 1185-1193.

[10] O. Than, S. Büttgenbach. Simulation of anisotropic chemical etching of crystalline silicon using a cellular automata model. Sensors and Actuators A 45, (1994) 85-89.

[11] K. Bean. Anisotropic etching of silicon. IEEE Trans. Electron Devices, E-25, (1978) 1185-1193.

[12] T. D. James, G. Parish, K. J. Winchester, and C. A. Musca. A crystallographic alignment method in silicon for deep, long microchannel fabrication. J. Micromech. Microeng. 16, (2006) 2177-2182.

[13] W. H. Chang, and Y. C. Huang. A new pre-etching pattern to determine <110> crystallographic orientation on both (100) and (110) silicon wafers. Microsystem technologies 11, (2005) 117-128.

[14] G. Ensell. Alignment of mask pattern to crystal orientations. Sensor Actuators A 53, (1996) 345-8.

[15] M. Vangbo, and Y. Bäcklund. Precise mask alignment to the crystallographic orientation of the silicon wafers using wet anisotropic etching. J. Micromech. Microeng. 6, (1996) 279–284.

[16] J. M. Lai, W. H. Chieng, and Y. C. Huang. Precision alignment of mask etching with respect to crystal orientation J. Micromech. Microeng. 8, (1998) 327-9.

[17] Fang-Gang Tseng, and Kai Chen Chang. Precise [100] crystal orientations determinations on <110> -orientated silicon wafers. J Micromech. Microeng. 13, (2003) 47-52.