SMART TECHNOLOGY FOR EARLY CRACK DETECTION OF CONCRETE WALL

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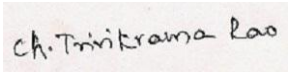

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This thesis is dedicated to my parents
for their love, endless support
and encouragement.

Abstract

Due to the ever growing human needs, many multi storied buildings, large sky scrapers and very large bridges are being developed. Due to some extreme environmental conditions there occur minute cracks inside the wall. These cracks, with time, protrude towards the end of pillar or wall, finally causing the buildings or bridges to collapse. Identifying these cracks in the very early stage (just after formation inside the pillar) can help us to get rid of disaster and as well as necessary measures.

So, there is a need to design a system in which a crack will be detected using crack detection sensors which are placed in the building or concrete walls. This information about crack will be communicated to outside world by wireless communication. All this processes require power supply which can supply continuously for tens of years. As, such a long power supply cannot be provided by any battery, we need to generate the power through energy harvesting. As the power generated through harvesting will be in micro scale range, the best communication technique (i.e. sending the information related to crack with minimum power) should be used. This will be achieved by using best frequency band for transmission at which the transmitted signal under goes minimum attenuation by losing minimum energy.

As a part of obtaining best frequency band, we need to know the wall parameters like permittivity and conductivity on which the attenuation of the signal depends. So, we developed an UWB pulse generator which generates a very short duration pulses which will be passed through a concrete wall and received at the other end. Then by analysing the transmitted signal frequency spectrum and received signal frequency spectrum, the parameters permittivity and conductivity can be obtained

A CMOS impulse generator was designed as a part of Ultra Wide Band (UWB) wireless communication system. An input square wave signal is delayed by using differential pairs and then XORed with the input signal to produce short duration pulses. An RLC circuit works as a Band Pass Filter (BPF) used to generate

Gaussian monopulse from the obtained short duration pulses. It operates with centre frequency at 4.782 GHz and -3dB band width of 20.36 GHz. The output peak to peak amplitude of the signal is 44.11 mV with pulse duration of 406 picoseconds. The complete circuit has been simulated in 0.18μm CMOS technology.

Contents

Chapter 1

Introduction

1.1 Introduction

Due to the ever growing human needs, many multi storied buildings, large sky scrapers and very large bridges are being developed. There is a serious need to check the sustainability and longevity of those buildings, bridges etc. Due to severe heat, cold and some extreme environmental conditions there occur minute cracks inside the wall. These cracks, with time, protrude towards the end of pillar or wall, finally causing the buildings or bridges to collapse. Identifying these cracks in the very early stage (just after formation inside the pillar) can help us to get rid of disaster and as well as necessary measures. Till now, many techniques were used to detect the cracks like pulse – echo testing [1], conventional manual ultrasonic methods [2], some acoustic methods [3]. These methods require manual operation and also couplants to transfer ultrasonic wave energy from transducers to parts being inspected [4]. There is a need to design a system in which no continuous monitoring and couplants are needed. This can achieve through a wireless communication. The detection of the small crack at early stage is not only sufficient, but it has to have been communicated reliably to outside world with an Integrated Circuit device. The power supply needed for this system can be provided by a battery but, it cannot sustain for more than 5 years. So, to detect the crack that may occur at indefinite time, a natural power source (piezoelectric or heat energy present in the pillar) is needed. This power will be extracted through energy harvesting. Therefore a proper choice of communication scheme (Frequency band, modulation technique etc.) and an efficient low-cost wireless transmit-receive architecture (essential for longer lifetime, as power is obtained through energy harvesting) is needed.

Pulsed UWB signals are used in similar form of applications like metal crack detection; see through wall applications (military usage) and in some medical implants [5]. Therefore, an UWB communication scheme seems to be preferable choice for inner wall crack-

detection. Moreover, to determine the system specifications of UWB-scheme, the characterization of wall parameters (like permittivity and conductivity) is essential. Even for this characterization, a UWB pulse generator is required and therefore the main focus of this paper is to design a tunable CMOS UWB pulse generator.

1.2 Aim and Motivation

Recent advancements in building technology and ever growing human needs resulted in multi-storied buildings, large bridge, sky scrapers etc. Inside the pillars of these large structures there gets the cracks and by the time they get to the surface the buildings will be already on verge of collapse. This causes severe damage to humans as well as economy.Identifying these cracks in the very early stage (just after crack formation inside the pillar) can help us to get rid of disaster and as well as necessary measures can be taken. The main objective of this project is to design a crack detection system in which number of crack detection sensors will be placed in a concrete wall (while building it). These sensors detect the cracks that originate from centre of the wall and send the information to the outside world. Through this information necessary safety measures can be taken.

1.3 Literature Review

Even though detection of wall cracks is necessary for safe livelihood, unfortunately no one researched in this area. As a part of UWB pulse generation, there are many ways of UWB signal generation. Some are generated through Step Recovery Diode (SRD) [6-9], combined SRD and schottky [10, 11] and MOS based circuits [12-15]. Quanmin Wang *et.al* [10] proposed a simple way of generating UWB pulse using step recovery diode, but this needs very high voltage in the order of few volts. A similar way of generation was proposed by Jeongwoo Han *et.al* [11] by using step recovery diode, schottky diode and transmission lines. But this technique also needs 7 volts of supply voltage. There are many techniques of UWB signal generation using MOS transistors for which power consumption and size is very less. Jeongwoo Han *et.al* [11] proposed a pulse combination technique through which Gaussian pulse of 450mV and pulse width of 300 picoseconds can be generated. This circuit can produce only fixed duration signal lacking the tunability feature whereas Haolu Xie *et.al* [14] proposed a similar way of UWB pulse generation with tunable feature. It can produce pulse with varying width of 240 ps to few nanoseconds. The main drawback is that by changing the pulse width, the amplitude level is not constant. The amplitude level also varies with varying pulse width. Jeong *et.al* [13] proposed a different way of producing UWB pulses by using a series of Delay blocks and a XOR block. Through this technique they are able to produce Gaussian monopulses of 27mVp-p with 3.7GHz bandwidth. They are also able to produce

variable pulse width of 0-36 picoseconds. Here, in this method even though the pulse width varies, the amplitude level does not vary but there is no mechanism for varying pulse duration. Generally these schemes generate UWB pulses of sub-nanosecond range, but they do not have desired tunable feature for pulse width. Since wall-parameters are vary largely from wall to wall (due to variation in construction material as well as thickness of wall), UWB pulse generator must be tunable in nature so that a single system can be used for different kinds of walls. On that regards, we have proposed a CMOS based tunable UWB short duration pulse generator having tenability feature in both pulse width and pulse duration. The tunability achieves through multiple delay cells and an encoder.

1.4 Thesis Organization

• **Chapter 1:** is the introduction describing the motivation behind the work, literature survey, objectives and contributions of the present work.

•**Chapter 2:** explores ultra-low power system and highlights the importance of energy harvesting for powering these devices.

• **Chapter 3:** describes solar energy and its properties. It discuss about solar cell and its parameters also.

• **Chapter 4:** describes ultra-low power MPPT concept and MPPT methods.

• **Chapter 5:** describes design and performance of charge pump circuits and analyses the losses in it.

• **Chapter 6:** describes design and performance of Hill climbing based MPPT method implementation and its draw backs.

• **Chapter 7:** describes design and performance of a novel feed forward technique for energy harvesting

Chapter 2

Crack Detection System

2.1 Introduction

Many large buildings, bridges and skyscrapers get collapsed due to the cracks that evolve with time in their pillars and large walls. This leads to death of many people and causes huge economical loss. This can be avoided by detecting the cracks at the initial stage itself and taking necessary safety measures. So, a system is needed to continuously monitor the cracks in the pillar and on detecting the crack, should send the information to outside world. In our crack detection system, we place number of crack detection sensors inside of a wall or a large pillar.

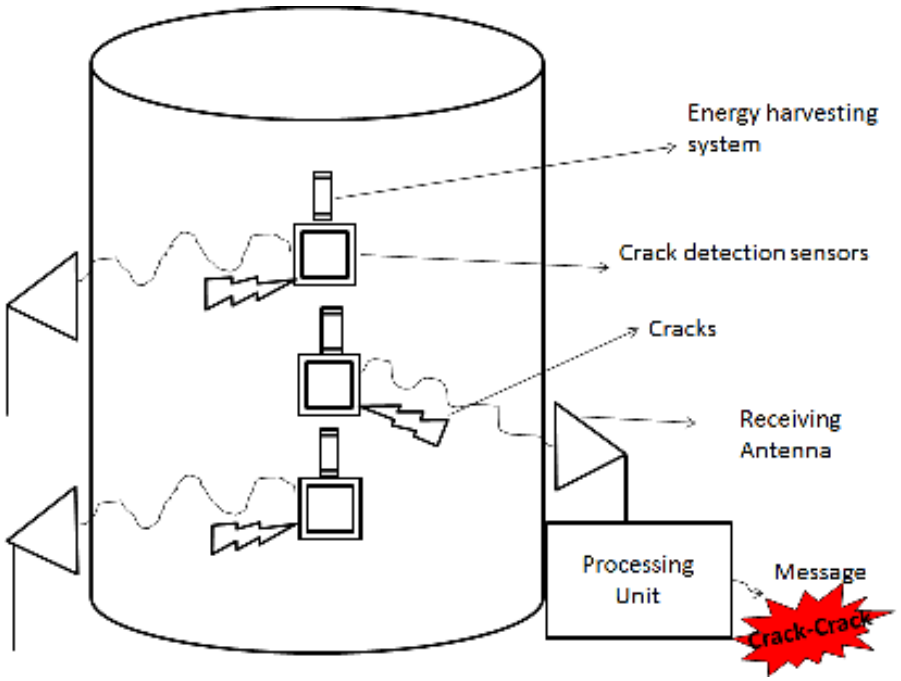

Fig. 2.1 Complete crack detection system

These sensors are capable of sensing minute cracks that occur inside the wall and protrude towards end of the wall. These sensors continuously monitor the pillar for the cracks. On detecting a crack, it sends the information about the crack to the outside world using wireless communication. This information is received by the receiving antennas and passes it to the processing system. The receiving system should be very sensitive in order to receive very low power electromagnetic signals coming from the sensor. The processing system on receiving the signal decodes the information in it and tells the details about the crack presence, location and intensity. Through this information necessary safety measures can be taken.

2.2 Cracks

A crack is a small break or a line along which something has split without breaking. Generally walls or pillars of buildings have cracks once or more in their life time. These cracks look very small in looking but these small cracks create a large havoc economically and for many lives causing large buildings and bridges to collapse unless proper care is taken to them. Generally there are two types of cracks that occur in building walls or bridge pillars. One type is the cracks that occur on the body of the walls and pillars i.e. they are visible to outside world and naked eye. These cracks are easy to detect manually as they are visible to naked eye. This type of cracks is not more dangerous as they are detectable, so necessary safety measures can be taken in time avoiding building collapse. The other kind of cracks is those that originate from the center of the wall and protrude towards the end of the wall. These cracks are not visible to naked eye at the time of origination as they originate from the center of the pillar or building wall. This type of cracks are more dangerous than the previous one as these cannot be easily detectable with naked eye, and when they protruded to the end of the wall, the building/wall will be at the verge of collapse leaving very less time to take necessary safety measures. Generally cracks occur due to the extreme environmental conditions like excess of heat and cold. The excessive temperatures and extreme coldness make the metals present in the pillar/wall to expand unevenly. This uneven expansion causes the cracks in the wall

2.3 Crack Detection Sensors

The name itself conveys it’s meaning that these sensors detect the cracks. Generally these sensors are capable of sensing very minute cracks that occur inside of a wall or pillars of large buildings. These sensors will be very minute in size. If the size of sensor is large, it will be difficult to place inside the pillar and also they may lead to additional cracks due to their placement. This sensor on detecting the crack sends that information to the outside world through wireless communication. If we use wired communication from center of the pillar to

outside of the pillar, the wire will cause additional problems like acting as another source of crack generation. So, wireless communication is used as means of communication for conveying information. The power needed to the sensor system is provided by the energy harvesting system

2.4 Energy Harvesting System

As the sensor needs power to detect the crack and send that information to outside of the pillar, some continuous power source is needed. Battery can be used as a power source for the sensor circuitry. But the longevity of the battery is only few years and the replacement of battery is not possible as entire setup is built in the pillar. So, a continuous power supply is needed other than a battery source. This is possible only through harvesting the available energy present in the wall/pillar. The possible energy that could be obtained in the pillar and can be harvested is piezoelectric energy and heat energy. By converting any form of this available energy to the power helps in continuous power supply. This entire work will be done by energy harvesting system. This system converts the available natural sources of energy to power. This system also preserves the power in a battery reserve as the continuous power supply cannot be provided because the sources of energy (piezoelectric, heat) may not be continuously. So, the preserved energy can be used as a continuous power supply for the sensor circuitry. This system should be very sensitive in nature because there will be very minute piezoelectric energy (vibrations that occur in the pillar) and the heat energy in the pillar/wall so, the system should sense these minute energy sources and convert into electric power. This system plays a major role in the entire crack detection system because it provides the power the entire system.

2.5 Receiving antenna

The receiving antenna receives the signal that is sent by the sensor system after detecting the crack in the pillar. The receiving antenna and the transmission part in the sensor system mutually helps in using minimum power for communicating the information. The more the receiving sensitivity for the receiving antenna, the less the power needed to transmit the information by the sensor circuitry. The receiving antenna is placed outside the pillar which could be at any place like nearer the pillar or farther the pillar depending upon the communication range and the safety. On receiving the signal from sensor, the receiving antenna sends it to the processing system.

2.6 Processing system

This system on receiving the information from the receiving antenna analyses it and makes a decision whether crack is present or not. This system decodes the signal and gives the

information regarding the presence of crack, location of crack and intensity of the crack. Through this information safety measures can be taken depending upon the intensity and location of crack.

Chapter 3

Literature Survey

3.1 UWB pulse generators

Till date there are many types of UWB pulse generators. People used different types of circuits for different purposes. Among all the UWB pulse generators, they can be categorized into certain categories depending upon some basic principles. They are

- Circuits using Step recovery Diode, Transmission lines
- Circuits using Step recovery diode, Schottky diode and Transmission lines
- Circuits using NAND and NOR gates
- Circuits using pulsed oscillator and RLC circuit
- Circuits using Differential amplifiers, Gilbert Cell and RLC circuit

Each of the type has their own pros and cons. The application decides which circuit is best suitable. Let us see these different types of circuits

Type1: These circuits step recovery diode and transmission lines to generate UWB pulses. The Step recovery Diode (SRD) is a semiconductor junction diode which is capable of producing short pulses. The main principle in SRD's is very less minority carrier life time. The SRD behaves normally during forward bias and in the reverse bias, due to very less minority carrier life time it produces a small pulse. The transmission lines are used to cancel the signal excluding the short pulse. These types of circuits also make use of schottky diodes for better precision.

Pros:

- Simple circuitry
- Easily understandable
- High output power

Cons:

- Relatively high pulse width
- High power consumption
- High power supply needed

Type2: This type of circuits use NAND and NOR gates to produce UWB pulses. The main principle of these circuits is the different delays observed in multiple inverters are passed through NAND and NOR gates to produce Gaussian pulses. These pulses on combining with great precision in time makes Gaussian pulses of the required number of derivative depending on the pulses combined. These types of circuits are easy to understand but very much care should be taken for combining the Gaussian pulses.

Pros:

- High output power can be observed
- Required number of derivative of Gaussian pulse can be obtained
- Very large pulse widths can be produced

Cons:

- On varying the pulse width, the amplitude level changes
- Difficult to join the pulses exactly
- Tuneability feature is absent

Type 3: This type of circuit uses pulsed oscillator which generates short duration pulses. These pulses are passed through RLC circuit which produces Gaussian pulses

Pros:

- Simple circuitry

Cons:

- No tuneability feature in pulse width is observed
- High power consumption due to RLC elements

Type 4: This type of circuits uses differential pairs to delay the input signal. Then the delayed input signal and the input signal are given to Gilbert cell top produce short pulses. These pulses further on giving to RLC circuit, produce UWB Gaussian pulses.

Pros:

- Tuneable feature for pulse width without varying the amplitude levels
- Low power consumption
- Very low pulse widths can be produced

Cons:

- Comparatively large circuitry

Among all these different types of circuits we chose the last type as it can vary the pulse width without varying the amplitude and it can produce the pulses having minimum pulse widths.

Chapter 4

Tunable UWB Pulse Generator

4.1 Need for Tunable UWB pulse generator

Till date many types of UWB pulse generators were developed. Each type of generator is having its own specific purpose. In our application for characterizing the wall parameters permittivity and conductivity of walls having different thicknesses, we need tunable UWB pulse generator. For finding the wall parameters permittivity and conductivity, we analyse the transmitted signal frequency spectrum and received signal frequency spectrum. If the transmitted signal frequency components are having higher power levels, then the received signal frequency components will be having higher power levels with less noise power helping for better parameter extraction. But there is compensation between power level and the bandwidth. The higher the power levels of frequency components, the lower the bandwidth of the pulse. Let us see diagrammatically the power levels and bandwidth.

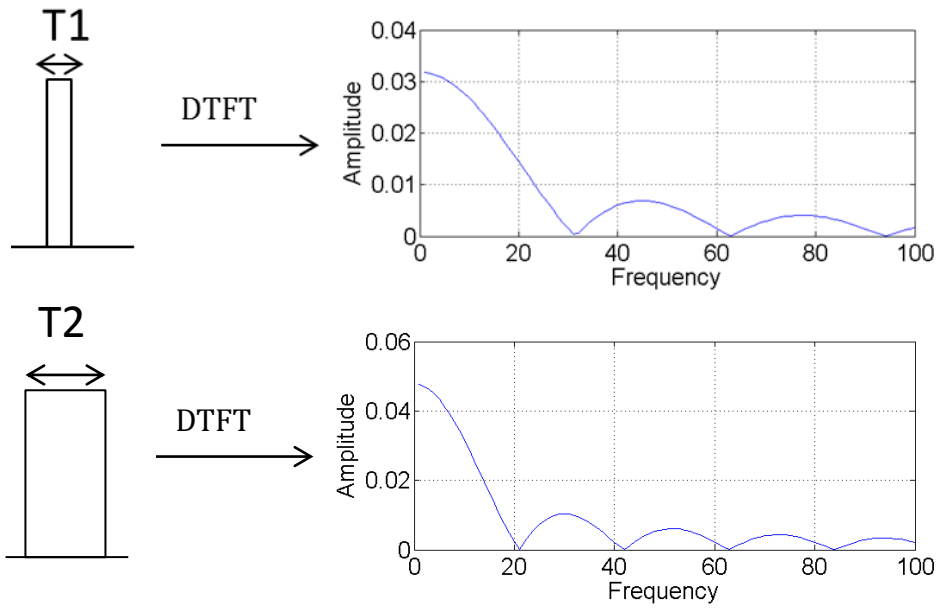

Fig.4.1. Discrete Time Fourier Transforms of two rectangular pulses having different widths

By comparing the Discrete Time Fourier Transforms of the rectangular pulses having widths of 'T1' and 'T2' from the figure 4.1, we can say that the pulse having less width (i.e. T1) having larger bandwidth and low amplitude levels compared to that of the pulse having more width (i.e. T2). In the first figure of Fig.4.1 the frequency components of at frequency unit 30 are near to zero i.e. not a good power level to analyze the transmitting and receiving signal frequency components around those frequencies. In the second figure of Fig.4.2 we can observe the amplitude levels of frequency components around frequency units 30 are higher compared to that of previous values. So, here second pulse is suitable for analyzing frequency components around 30 frequency units. Similarly for the frequency components below 20 units, first pulse is suitable as it is having more amplitude levels compared to the second one. So, a tunable UWB pulse generator is needed to get the wall parameters at different frequencies and for better extraction.

4.2 Introduction

Many CMOS based UWB pulse generator schemes were proposed till date. Some schemes use NAND and NOR gates [10], Voltage Controlled Ring Oscillator (VCRO) and pulse shaping circuit [8], Differential pairs and Gilbert cell [13]. Jeong *et al*. proposed an UWB pulse generator scheme which generates a sub-nanosecond pulse through differential pairs and a gilbert cell. Compared to other pulse generation schemes, the proposed scheme is capable of generating shorter duration UWB pulses and also having good scope to add tunability feature to pulse width. This can be achieved through adding the multiple delay cells (delay cell i.e. one block of the scheme proposed by Jeong) and an encoder.

4.3 UWB signal generation and shaping

The two major characteristics of Ultra Wide Band signal are wide band width and carrierlessness. Typical pulsed UWB system consists of a pulse generator and a filter. The Gaussian Mono-pulses provide better Bit Error Rate (BER) and less multipath fading among impulse signals. So, a filter with Band Pass (BP) nature is chosen as it can shape the input pulse train into train of Gaussian Mono-pulses through differentiation. The complete block diagram of mono-pulsed UWB system is shown in Fig.4.2. Here the pulse generator by making use of input clock signal produces a train of short duration rectangular pulses. The pulse shaping circuit in the following stage differentiates the incoming short rectangular pulses and generates Gaussian monopulses. The pulse shaping circuit uses RLC elements as

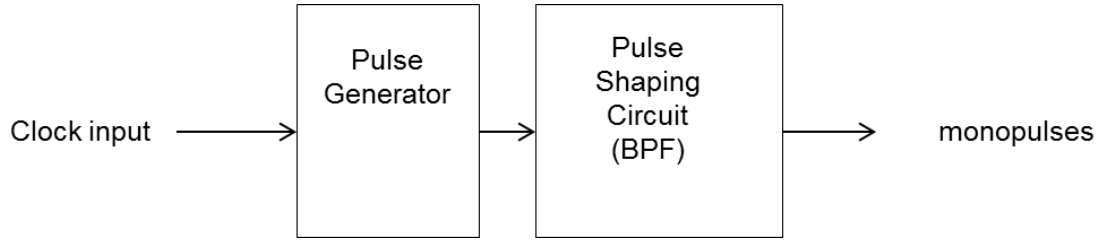

Fig.4.2Block diagram UWB Gaussian monopulse generator

Band pass filter through which each falling or rising edge of the rectangular pulse produces a Gaussian monopulse.

4.4 Tunable UWB pulse generator

The tunable UWB pulse generator is designed using four delay cells, an encoder, Gilbert cell and a pulse shaping circuit. The delay cell is the key block for pulse generation. It consists of differential pairs through which the input clock signal is delayed by certain picoseconds. By connecting four delay cells in series the delay of input clock signal can be increased to sub nanoseconds. These delayed signals through each delay cell are now given to an encoder.

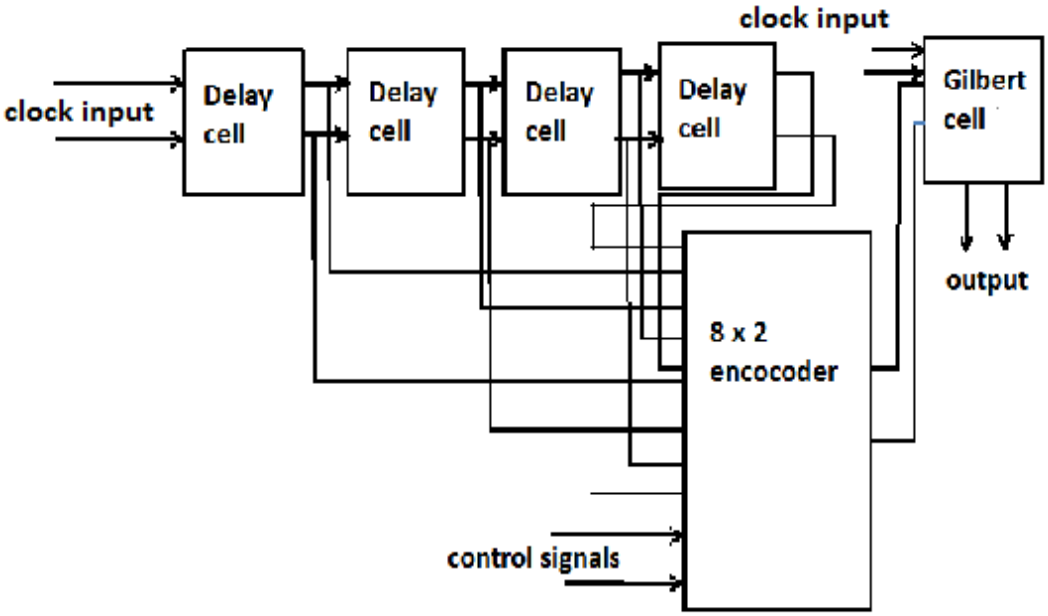

Fig.4.3. Block diagram of tunable UWB pulse generator

The encoder routes the signal from a particular delay cell by making use of control signals. Now this delayed signal through encoder and the input clock signal are given to the gilbert cell. Gilbert cell performs XOR operation on both of these signals and produces a train of short duration pulses [16, 17]. These short duration pulses are then differentiated using RLC circuit and thus producing Gaussian monopulses at each rising and falling edge of the

rectangular short duration pulse. Thus by using control voltages at the encoder, we can control the pulse width of short duration pulses. Now let us see each block in detail.

4.5 Delay cell

The delay cell is made up of differential pairs which are used to delay the input clock signal by certain picoseconds. This consists of three differential pairs of which two pairs (differential pairs 1 & 3) are connected in series and is referred as long path (B) and the other pair (differential pair 2) is referred as short path (A). As the signal traversing through the two differential pairs takes more time than that of the path having single differential pair, it is referred as long path and other as short path.

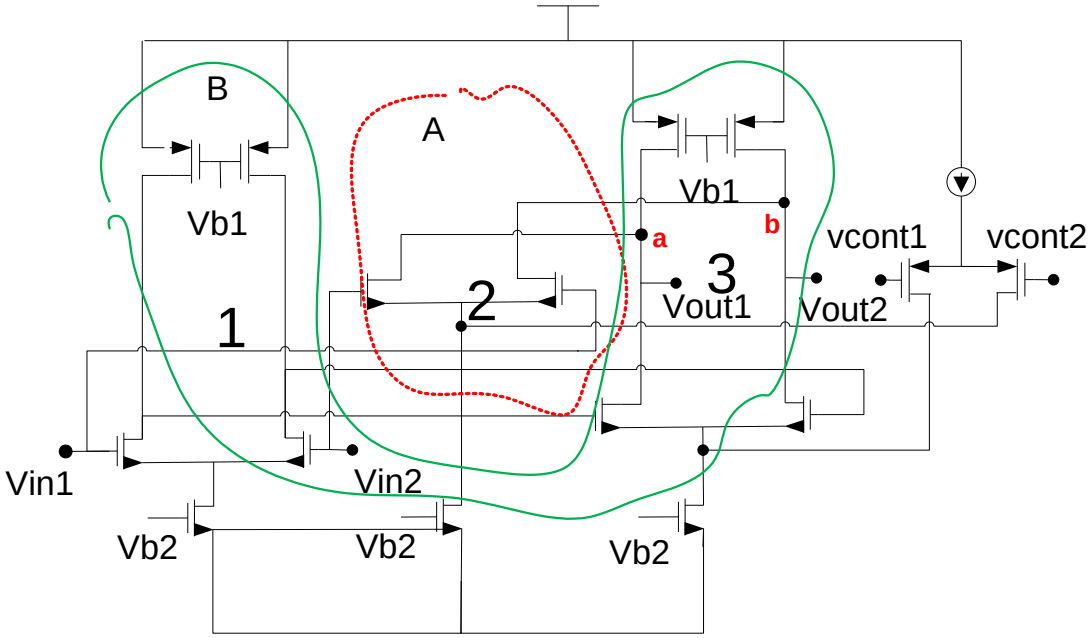

Fig.4.4 Circuit diagram of delay cell

The long path and the short paths are connected at the drain ends of 3rd differential pair i.e. at "a and b". As these two paths are connected at drain ends of 3rd differential pair, the output signals of both the paths are added in current domain.

The tail current of the differential pairs 2 and 3 is varied using the control voltage vcont1 and vcont2. The tail thus varied varies the voltage gain of the differential pair and thus effects the delay time. Thus the delay time of the input clock signal can be varied by controlling the control voltage vcont1 and vcont2. The higher the tail current in a differential pair, the higher the gain and so the higher the delay it offers to the input signal. By connecting the delay cells in series, the total delay can be increased further to sub nanoseconds. The required delay can be obtained by using an encoder which routes the signal from required delay cell.

4.6 8 x 2 Encoder

This encoder is used to route the two outputs of one in four delay cells depending upon the control signals. If the two control signals are low i.e. their magnitude is not enough to make the transistors ON, then the outputs of first delay cell are routed through it. The table for selecting the delay cell basing on control signals is given below in fig.4.5.

TABLE 4.1 delay cell selection basing on control signals

Control Voltages		Outputs of delay cell routed through
0V	0V	1
0V	1.8V	2
1.8V	0V	3
1.8V	1.8V	4

The high voltage is taken as 1.8V as it can make the transistor ON. Basing on the above controlling, a particular delay cell outputs can be routed. Here if the delay cell is selected, then the signal will be traversed through all the delay cells preceding it. It means the more the number of delay cell selected the more is the delay of the input signal. The 8 x 2 encoder is designed by using two 4 x 1 MUX's. Each 4 x 1 MUX is designed by using a 2 x 4 decoder and four pass transistors. Each pass transistor is made up of PMOS and NMOS transistors. Let us see the schematic of pass transistor.

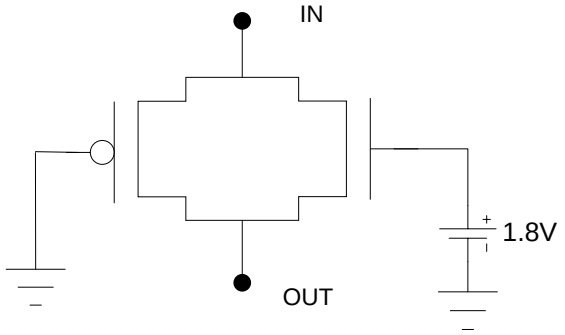

Fig.4.6 Pass transistor

As shown above the pass transistor is made up of PMOS and NMOS transistors for which drains and sources of two transistors are connected together and PMOS gate is connected to

ground and NMOS gate is connected to 1.8V supply. The delay between input and output is around 200 picoseconds. This pass transistor plays a key role in the whole encoder as it the thing which offers further delay to the input signal. These pass transistors along with 2 x 4 decoder forms 4 x 1 MUX. Let us see the gate level schematic of 2 x 4 decoder.

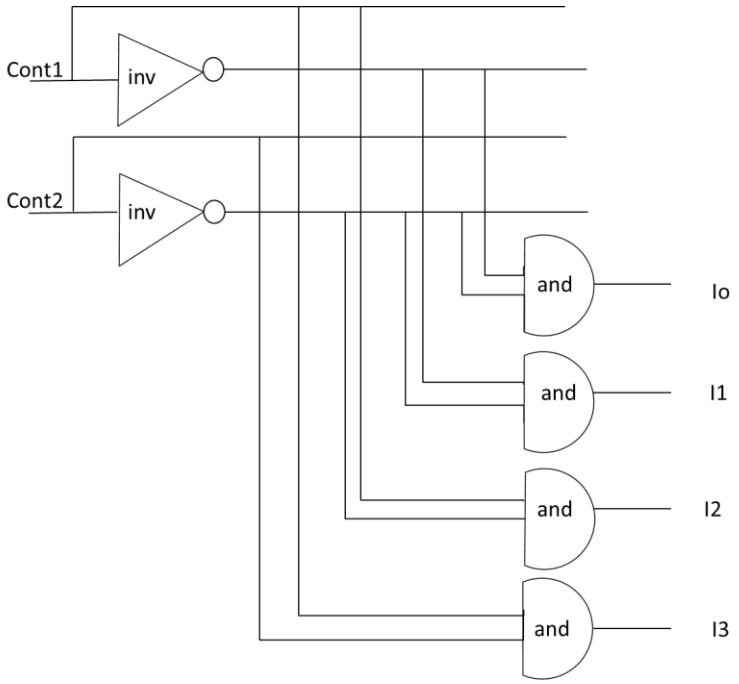

Fig.4.7 2 x 4 decoder

The 2 x 4 encoder is designed by using AND gates and inverters. The two control signals cont1 and cont2 decides for which AND gate output should go HIGH and LOW. These HIGH and LOW signals makes the pass transistors enable/disable. This encoder along with the pass transistors formed as 4 x 1 MUX. Let us see the block diagram of 4 x 1 MUX.

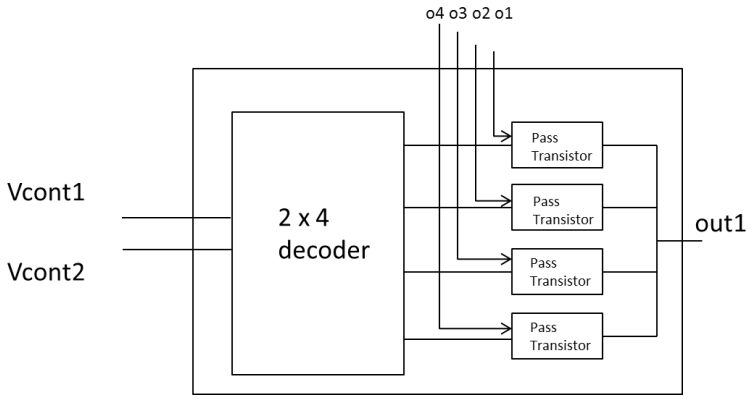

Fig.4.7 Block diagram of 4 x 1 MUX

As shown in above fig.4.7, the 4 x 1 MUX routes one of the four input signals through the it by using control signals cont1 and cont2. At any instant of time only one output of the 2 x 4

decoder is HIGH. So, only one pass transistor is enabled at any instant i.e. only one input signal is traversed through the pass transistor. As all the outputs of pass transistors are connected togetrher, only one input signal is traversed through the 4 x 1 MUX. Let us see the dependence of output of MUX on control signals given the inputs as o1, o2, o3 and o4.

TABLE 4.2 Output of 4 x 1 MUX basing on control signals

Vcont1	Vcont2	Output port high at deccoder	Output of MUX
0V	0V	1	O1
0V	1.8V	2	O2
1.8V	0V	3	O3
1.8V	1.8V	4	O4

The control signals of the 4 x 1 MUX are the inputs for the 2 x 4 decoder. The decoder, basing on control signals sends HIGH through one of its ports enabling only one pass transistor connected to it. This pass transistor passes the input signal connected to it to ouput with some delay added. This delay is around 200 picoseconds. Two 4 x 1 MUX's connected together to form 8 x 2 encoder. Let us see the block diagram of an 8 x 2 encoder.

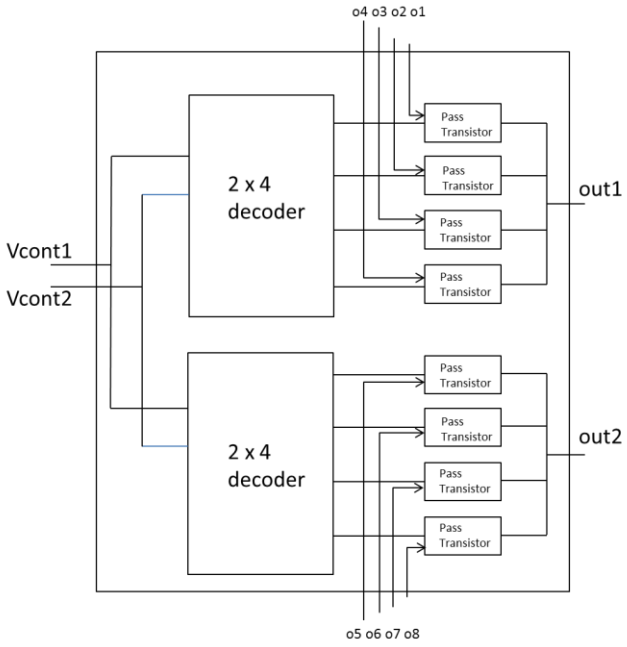

Fig.4.8 Block diagram of 8 x 2 encoder

An 8 x 2 encoder is shown in the fig.4.8. It consists of two 4 x 1 MUX's, eight inputs, two control signals and two outputs. The first four inputs to the encoder are the one rail outputs of

four delay cells and are named as o1, o2, o3, o4. The next four inputs are other rail outputs of the four delay cells and are named as o5, o6, o7, o8. The vcont1and vcont2 signals are connected to the top and bottom respectively pins of the two 4 x 1 MUX's. Finally by control voltages the two outputs of each delay cell can be routed through the encoder. Through this we can get the input signal delayed by the required amount. i.e in multiples of delay offered by a delay cell up to 4 times. Thus 8 x 2 encoder provides tuneability feature for pulse width as delay of the input clock signal indirectly causes the pulse width.

4.7 Gilbert Cell

Gilbert cell is used as a voltage gain amplifier (VGA) [18]. It is an amplifier in which the gain is varied using a control voltage. Here the voltage is applied between gates of 1, 2 and 3, 4 differential amplifiers. The drain ends of differential amplifiers 1, 3 and 2, 4 are connected together respectively and outputs are taken at these ends. The source ends of differential amplifiers 1, 4 and 2, 3 are connected together respectively. The control voltage vcont controls the gain of the amplifier.

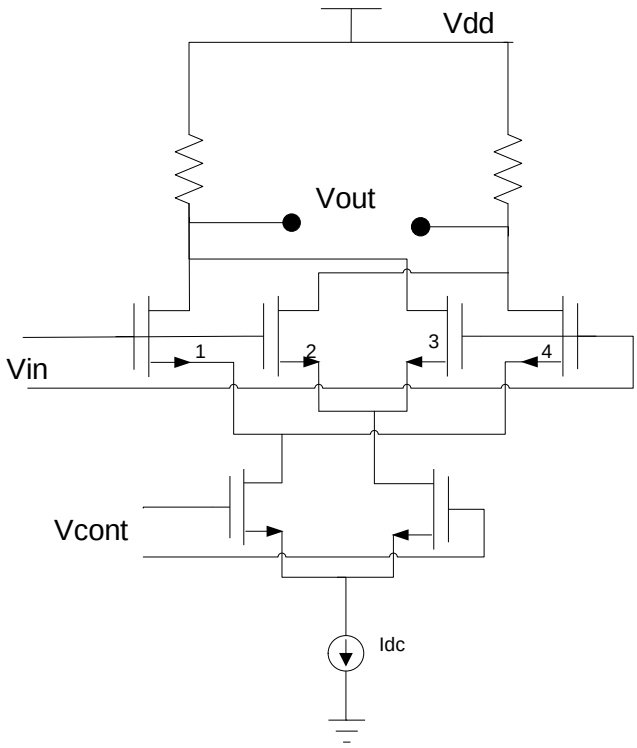

Fig.4.9 Gilbert Cell

The positive is the control voltage, the positive is the gain of the amplifier and the negative is the control voltage, the negative is the gain of the amplifier. Here the input clock pulse and its delayed signal coming from the encoder are applied to the control pins and at the input pins of the gilbert cell. One voltage acts as control voltage and other acts as input voltage. The

gain is having only two values i.e. either positive or negative with same magnitude. The input signal is amplified with positive gain when control voltage is HIGH and amplified with negative gain when control voltage is low. Let us see the function of gilbert cell diagrammatically.

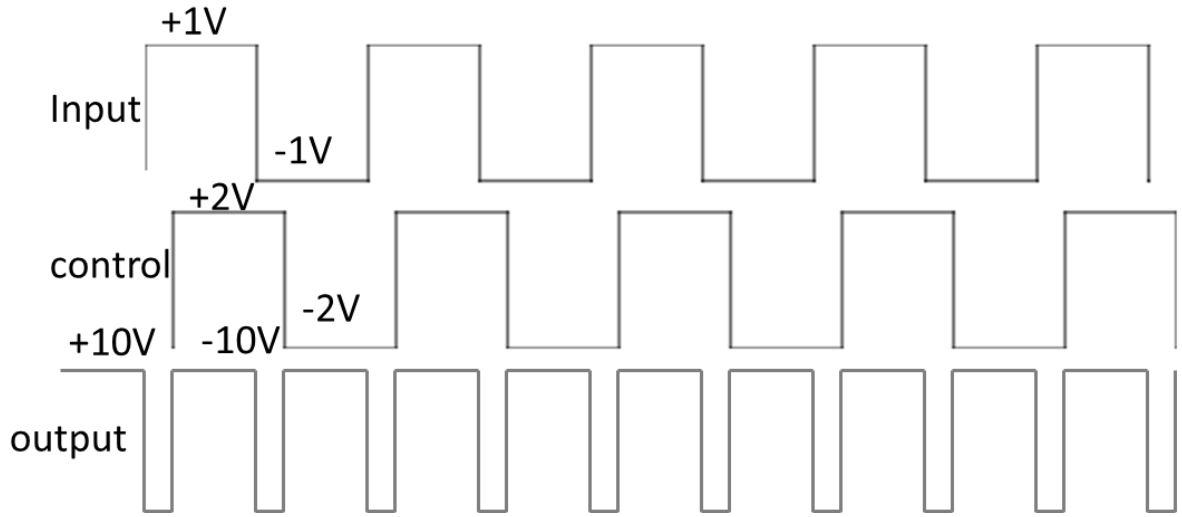

Fig.4.9. input, control and output voltages of Gilbert cell

Let the input signal be a square wave form alternating between +1V and -1V and the control voltage between +2V and -2V. Let the gain of the amplifier be 10. Now when control voltage is HIGH, it amplifies the input signal with positive gain i.e. +10 and when the control voltage is negative, it amplifies the input signal with negative gain i.e. -10. So the output voltage is alternating between +10V and -10V as shown in fig.4.9. Thus gilbert cell acting as a voltage multiplier producing short duration pulses by making use of the delay of input signal. These short duration pulses are further passed through a band pass filter to obtain Gaussian monopulses which will be fed to an antenna on further.

4.8 Pulse shaping circuit

Since the Gaussian Mono-pulses and Doublet provide the better Bit Error Rate (BER) and less multipath fading among impulse signals, the pulse shaping circuit should be Band Pass (BP) nature, as BPF can shape the pulse train to a Gaussian Mono-pulse through differentiation of the input pulse train. The designed pulse shaping circuit is in the form of BPF, generating Gaussian Mono-pulses. Gaussian monopulses are generated using 2^{nd} order RLC circuit. The parallel LC operates as a resonator and shapes impulses from the very-short pulses to damping sinusoidal signals.

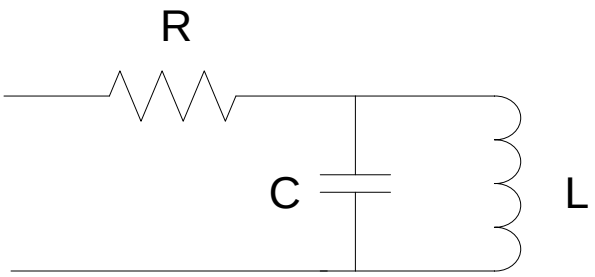

Fig.4.10. RLC circuit

The damping factor is chosen in such a way that the oscillations will become negligible with in a very short period of time and the signal resulting can be assumed as a Gaussian monopulse. The generated train of short duration pulses are the input to this circuit. For every transition i.e. from positive to negative or negative to positive, there occur damping oscillations. As the oscillations die very soon, the waveform is assumed to be Gaussian monopulse. This Gaussian monopulse is then fed to the antenna.

4.9 Simulation Results and Analysis

The input clock signal is taken as square signal with a period of 10ns and of pulse width of 5ns. The signal alternates between 0.6V and 1.2V. The two inputs are differential to each other. A single delay cell is amplifying the input signals and with certain delay is shown in fig.4.10.

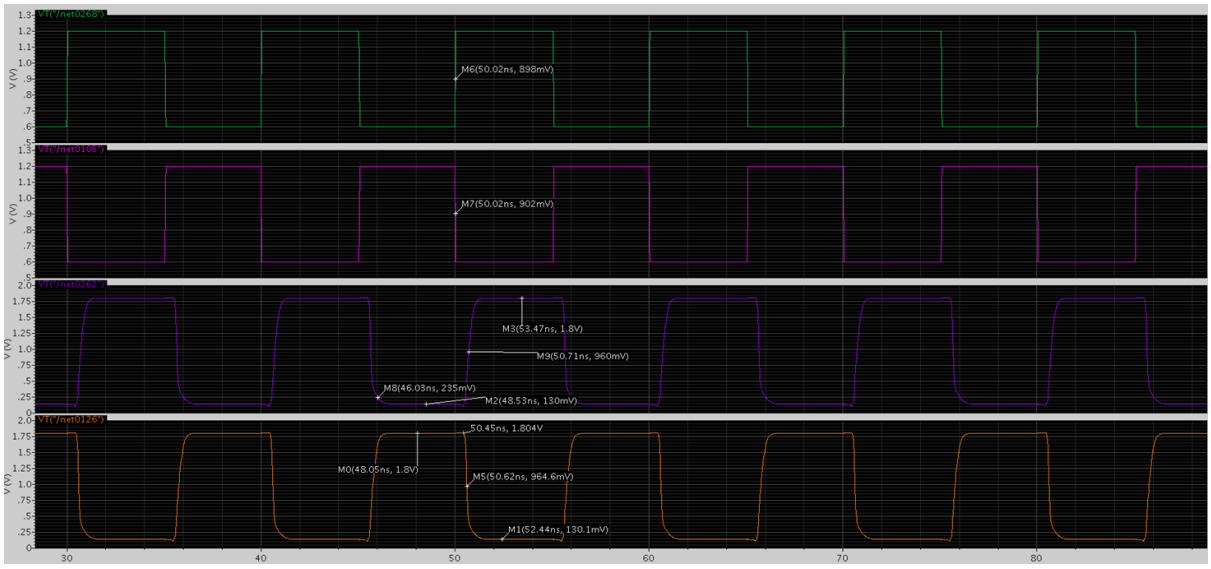

Fig 4.11 Two input signals of delay cell and their corresponding outputs

A single delay cell response to the input signal is shown in the below table

TABLE 4.3 Single Delay cell response to the input signals

Input low and high voltages	Output low and high voltages	Delay through cell
0.6V	1.722V	~70ps
1.2V	0.1123V	

The RLC circuit on filtering the short duration pulses produces Gaussian monopulses of 31.9mV$_{pp}$ and of width 300ps as shown in fig.4.11.

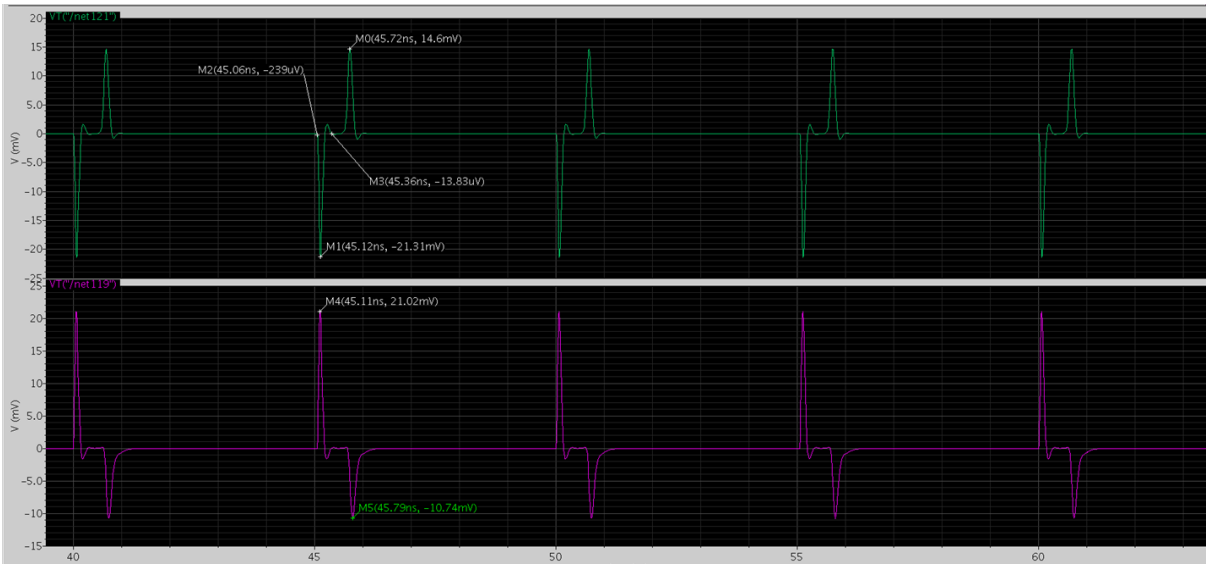

Fig 4.12 Two output signals of the RLC circuits

On varying the control signals in the differential amplifier, the width of the pulse is getting varied from 0 to 26 picoseconds keeping the amplitude constant. The varying pulse width is shown in fig.4.12.

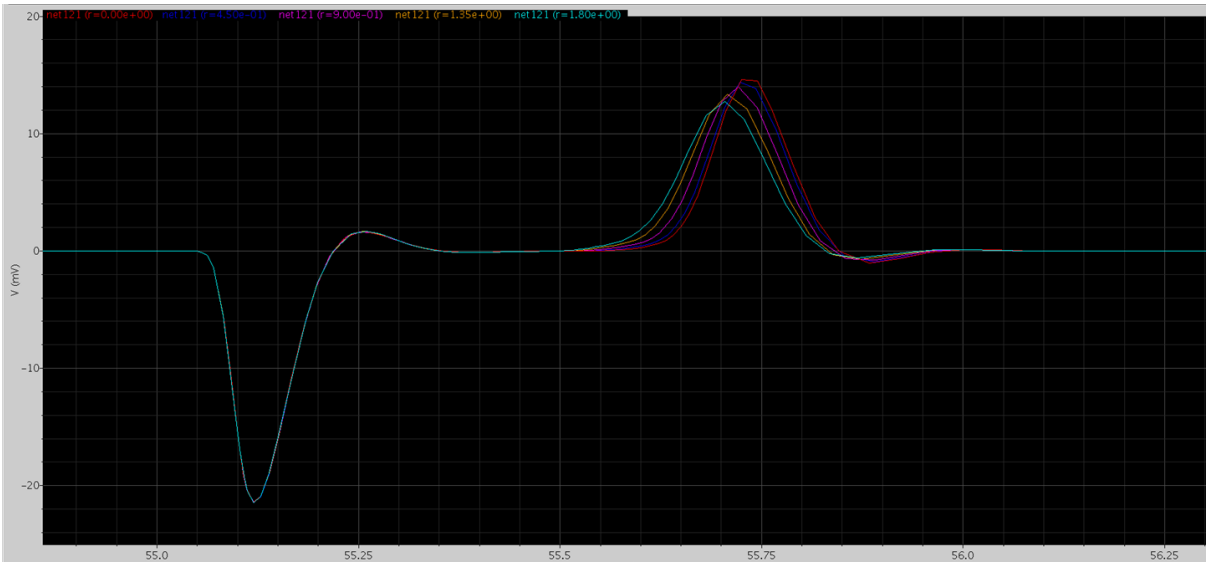

Fig 4.13 Varying pulse width at output of RLC filter with change in control voltage at differential amplifier

The designed UWB pulse generator consists of delay blocks and an XOR block for the pulse generation, and the BPF for the pulse shaping. The simulation was performed using Cadence Spectre with 0.18µm CMOS process. The combined circuit (delay cells, encoder and gilbert) produces a train of short pulses (rectangular in nature) as shown in Fig.4.12.

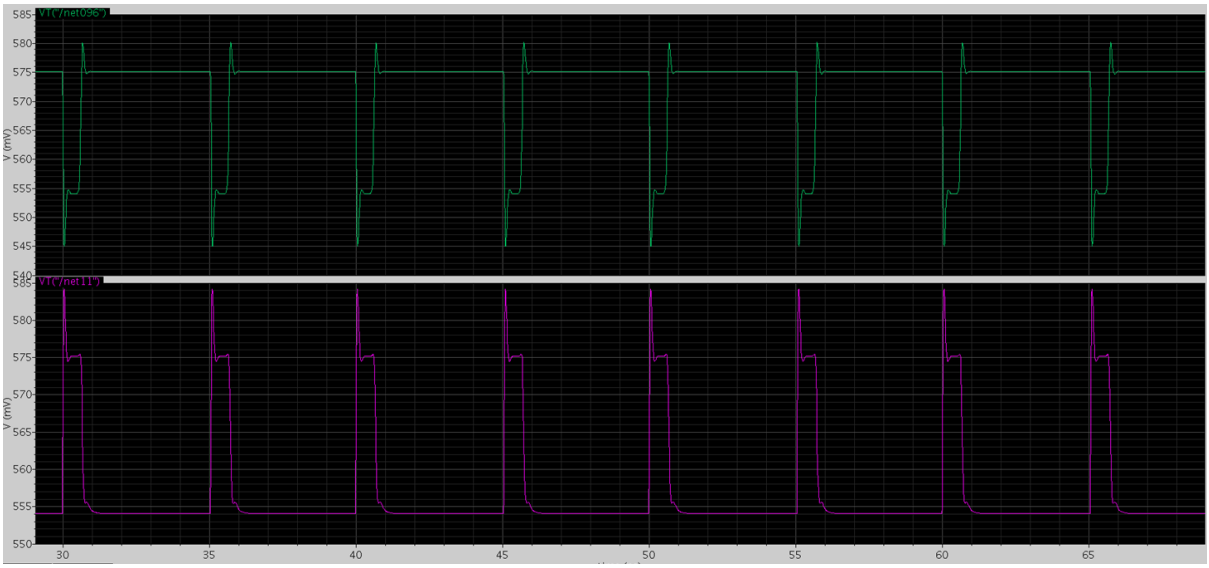

Fig 4.14 Output signals at the end of Gilbert cell

Each delay block is capable of delaying the input signal for tens of picoseconds, by connecting four delay cells, an encoder and a gilbert mixing, the delay is varied from 300ps to 860pS. Then, these pulses are passed through an RLC-BPF circuit resulting in Gaussian monopulses. To make the pulse shaping in UWB nature, a BPF is designed with a centre frequency 4.782GHz and -3dB BW 20.36GHz. The Gaussian Mono-pulses will be generated at every transition of the pulse of Fig.4.12. The pulse width of Gaussian monopulse is varied through the current in differential pairs. Through this, the output pulse width of Gaussian monopulse for each delay block can be varied from 1ps to 6.5ps with a control voltage range from 0 to 1.8V and by connecting 4 delay blocks in series will produce a total of 26ps tuneabilty in pulse width. The peak-to-peak amplitude of difference signal at the outputs of Gilbert cell is 63.82mV. The designed circuit produces variable pulse duration i.e. 300-860ps and variable pulse width 0-26ps, this wide range variability or tuneabilty in pulse width and pulse duration helps to change bandwidth and the power levels of the frequency components associated with UWB pulse. This helps in parameter extraction of concrete walls having different thicknesses

The results obtained from the designed system are compared with those of reference paper [9] is shown in Table 4.3

TABLE 4.4 Comparison between obtained results and the results in reference paper

	Reference paper [9]	Obtained results
Centre Frequency	3.6 GHz	4.782 GHz
-3 dB Band width	3.1 GHz	20.36 GHz
Output peak to peak voltage	26.75 mV	44.11 mV
Pulse width	36ps(variable)	26 ps(variable)
Pulse Duration	Fixed	Tuneable (300-860ps)

Here the main advantage in the designed system is tuneable pulse duration, increased output peak to peak voltage level, centre frequency and high bandwidth. The main drawback is that the pulse width of Gaussian monopulse can be varied up to 26 ps only. But, this tuneability is in the same order (0-36ps) of that of reference paper and it can be taken into account considering the other mentioned advantages.

Chapter 5

Delay time Formulation

5.1 Introduction

The main part of the tunable UWB pulse generator is the delay cell. The pulse width of the UWB pulse is obtained by the delay created by the delay cell. The delay in each delay cell is created by the differential pairs present in it. So, the main delay is created by the differential pairs. Now let us formulate the delay time of the differential pair present in the delay cell. Consider the basic delay cell. In the figure 4.2 consider the marked path A i.e. the basic differential pair.

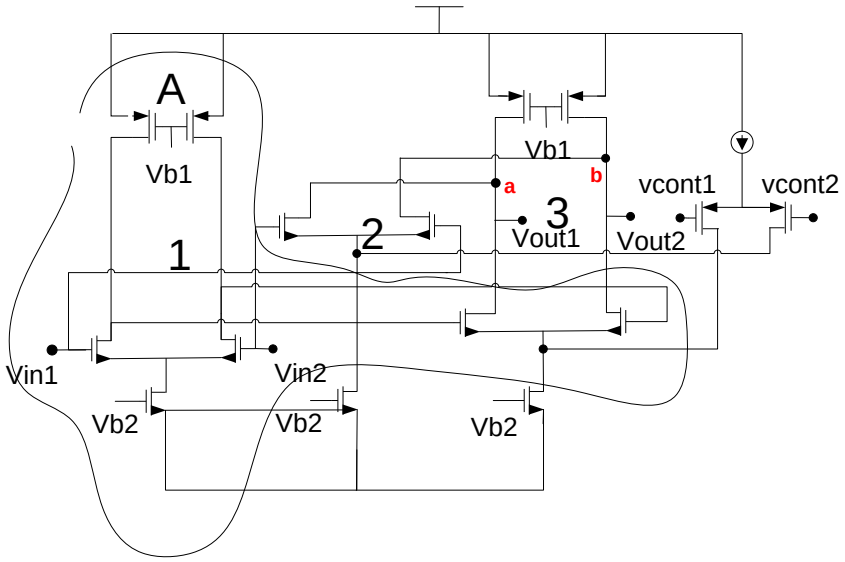

Fig 5.1 Basic Delay cell

Now let us find the delay of one differential pair. Consider the marked differential pair which is shown in Fig. 4.3. The propagation delay times τ_{PHL} and τ_{PLH} determine the input to output signal delay during the high-to-low and low-to-high transitions of the output respectively. By definition, τ_{PHL} is the time delay between the $V_{50\%}$-transition of the rising input voltage and the $V_{50\%}$ -transition of the falling output voltage. Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ -transition of the falling input voltage and the $V_{50\%}$-transition of the rising output voltage [19].

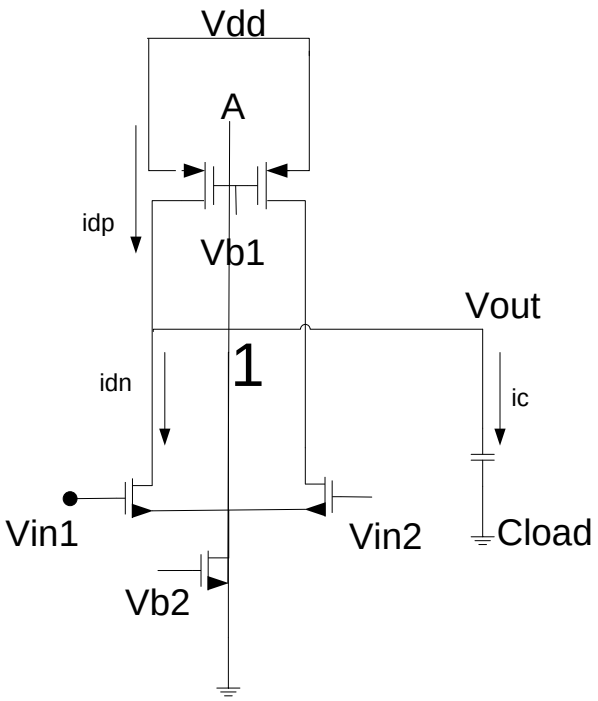

Fig 5.2 Basic Delay cell

Assume the capacitance offered by the second stage to the first stage is C_{load}. The current passing through the PMOS transistor and NMOS transistor is referred as i_{Dp} and i_{Dn} respectively. The current passing through the load capacitance C_{load} is i_c. If we consider the square wave as an input signal, then the delay times τ_{PHL} and τ_{PLH} are shown in Fig.4.3.

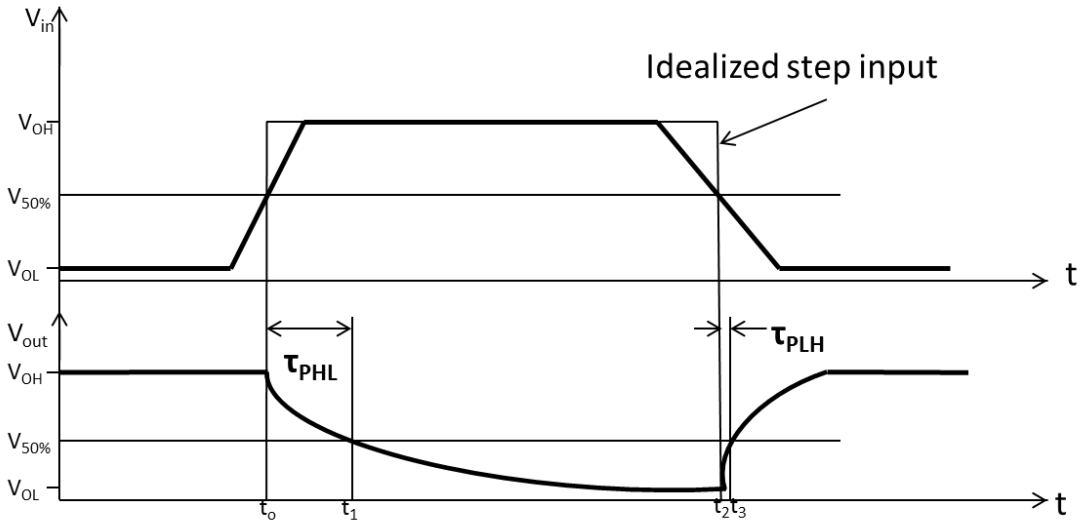

Fig.5.3. Input and output voltage waveforms of the delay cell and the definitions of propagation delay times. The input voltage waveform is idealized as a step pulse for simplicity.

5.2 Delay τ_{PHL} calculation

Consider the rising input square wave signal and assume initially the output i.e. V_{out} is at high voltage i.e. V_{OH}. When input signal transits from low to high , both PMOS and NMOS transistors will be in saturation region.

The currents i_{dp} and i_{dn} are

$$i_{dp} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[V_b - V_{out} - V_{tp}\right]^2$$

$$i_{dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{in} - V_{s2} - V_{tn}\right]^2$$

$$i_c = i_{dp} - i_{dn} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[V_b - V_{out} - V_{tp}\right]^2 - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{in} - V_{s2} - V_{tn}\right]^2$$

The, input and output voltage waveforms during this high-to-low transition are illustrated in Fig. 4.4. When the NMOS transistor starts conducting, it initially operates in the saturation region. When the output voltage falls below (V_{dd} - V_{th}), the NMOS transistor starts to conduct in the linear region. These two operating regions are also shown in Fig. 4.4.

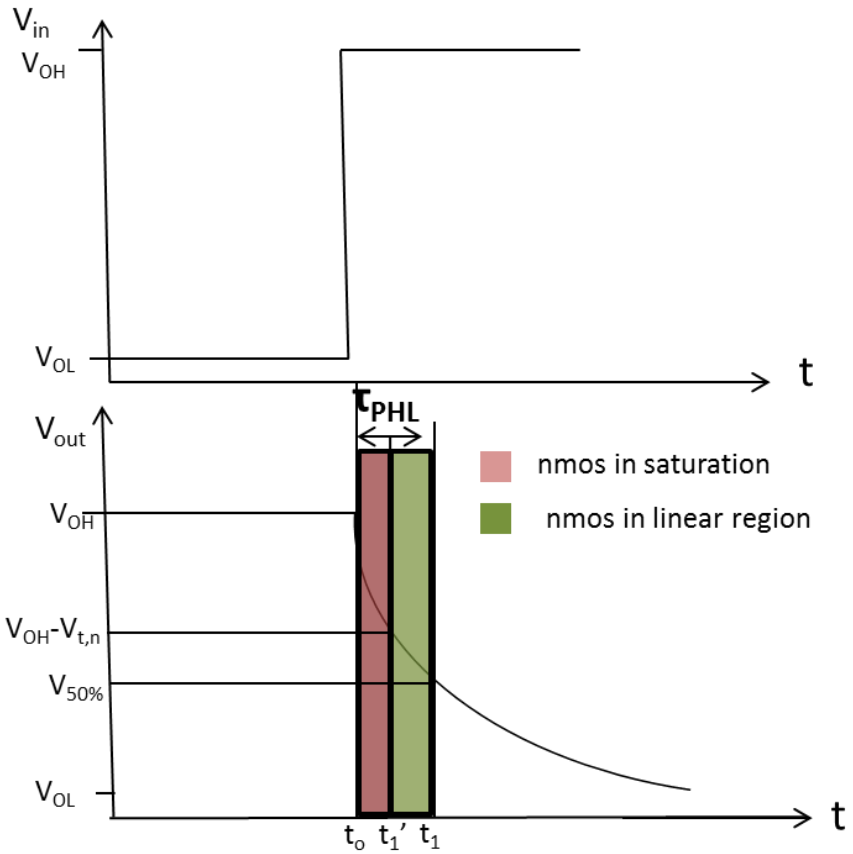

Fig.5.4 Input and Output voltages waveforms during high to low transitions

Consider

$$x = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}$$

$$y = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

$$a = V_b - V_{tp}$$

$$b = V_{in} - V_{s2} - V_{th}$$

Consider $i_c = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[V_b - V_{out} - V_{tp}\right]^2 - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{in} - V_{s2} - V_{tn}\right]^2$

$$i_c = x\left[a^2 + {V_{out}}^2 - 2aV_{out}\right] - yb^2$$

$$= xa^2 + x{V_{out}}^2 - 2axV_{out} - yb^2$$

$$= x{V_{out}}^2 - 2axV_{out} + xa^2 - yb^2$$

$$= x\left[{V_{out}}^2 - 2aV_{out} + \frac{xa^2 - yb^2}{x}\right]$$

We know that $i_c = \frac{d_{V_{out}}}{dt} = i_{dp} - i_{dn}$

$$C_{load}\int_{V_{OH}}^{V_{OH}-V_{th}} \frac{1}{i_{dp} - i_{dn}} dV_{out} = \int_{t_o}^{t_1^1} dt = t_1^1 - t_o$$

$$= C_{load}\int_{V_{OH}}^{V_{OH}-V_{th}} \frac{1}{i_c} dV_{out}$$

$$= \frac{C_{load}}{x}\int_{V_{OH}}^{V_{OH}-V_{th}} \frac{1}{{V_{out}}^2 - 2aV_{out} + \frac{xa^2 - yb^2}{x}} dV_{out}$$

Consider the equation ${V_{out}}^2 - 2aV_{out} + \frac{xa^2 - yb^2}{x}$ in denominator

$$= {V_{out}}^2 - 2aV_{out} + a^2 - \frac{yb^2}{x}$$

$$= (V_{out} - a)^2 - \left(\sqrt{\frac{yb^2}{x}}\right)^2$$

$$= \frac{C_{load}}{x}\int_{V_{OH}}^{V_{OH}-V_{th}} \frac{1}{(V_{out} - a)^2 - \left(\sqrt{\frac{yb^2}{x}}\right)^2} dV_{out}$$

Consider $t = \left(\sqrt{\frac{yb^2}{x}}\right)$

$$t_1^1 - t_o = \frac{C_{load}}{2xt}\left(ln\left[\frac{(V_{out} - a) - t}{(V_{out} - a) + t}\right] - ln\left[\frac{(V_{OH} - a) - t}{(V_{OH} - a) + t}\right]\right)_{V_{OH}}^{V_{OH}-V_{th}}$$

$$t_1^1 - t_o = \frac{C_{load}}{2xt}\left(ln\left[\frac{(V_{OH} - V_{th} - a) - t}{(V_{OH} - V_{th} - a) + t}\right] - ln\left[\frac{(V_{OH} - a) - t}{(V_{OH} - a) + t}\right]\right)$$

At $t = t_1^1$, output voltage will be $V_{OH} - V_{th}$ and NMOS transistor will be at Saturation-linear boundary region. Consider NMOS transistor is operating in linear region. The current passing through NMOS transistor in linear region is

$$i_{dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{s2} - V_{th})V_{out} - {V_{out}}^2\right] \text{ for } V_{out} \le V_{OH} - V_{th}$$

We know that $i_{c1} = C_{load}\frac{dV_{out}}{dt} = i_{dp} - i_{dn}$

$$C_{load}\int_{V_{OH}-V_{th}}^{V_{50\%}} \frac{1}{i_{dp} - i_{dn}} dV_{out} = \int_{t_1^1}^{t_1} dt = t_1 - t_1^1$$

$$= C_{load}\int_{V_{OH}-V_{th}}^{V_{50\%}} \frac{1}{i_{c1}} dV_{out}$$

$$\int_{t_1^1}^{t_1} dt$$

$$= C_{load}\int_{V_{OH}-V_{th}}^{V_{50\%}} \frac{dV_{out}}{\frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[V_b - V_{out} - V_{tp}\right]^2 - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{s2} - V_{th})V_{out} - {V_{out}}^2\right]}$$

Consider denominator

$$i_{c1} = x\left[a^2 + {V_{out}}^2 - 2aV_{out}\right] - y\left(2bV_{out} - {V_{out}}^2\right)$$

$$= xa^2 + x{V_{out}}^2 - 2axV_{out} - 2ybV_{out} + y{V_{out}}^2$$

$$= {V_{out}}^2(x + y) - 2V_{out}(ax + by) + xa^2$$

$$= {V_{out}}^2 - 2V_{out}\left(\frac{ax + by}{x + y}\right) + \frac{xa^2}{x + y}$$

$$= (x + y)\left\{\left[V_{out} - \frac{ax + by}{x + y}\right]^2 - \left[\sqrt{\frac{y^2b^2 - xya^2 + 2abxy}{(x + y)^2}}\right]^2\right\}$$

$$\int_{t_1^1}^{t_1} dt = \frac{C_{load}}{x + y}\int_{V_{OH}-V_{th}}^{V_{50\%}} \frac{dV_{out}}{\left[V_{out} - \frac{ax + by}{x + y}\right]^2 - \left[\sqrt{\frac{y^2b^2 - xya^2 + 2abxy}{(x + y)^2}}\right]^2}$$

$$t_1 - t_1^1 = \frac{C_{load}}{2(x+y)\sqrt{\frac{y^2b^2 - xya^2 + 2abxy}{(x+y)^2}}} ln \left[\frac{\left(V_{out} - \frac{ax+by}{x+y}\right) - p}{\left(V_{out} - \frac{ax+by}{x+y}\right) + p} \right]_{V_{OH}-V_{th}}^{V_{50\%}}$$

$$p = \sqrt{\frac{y^2b^2 - xya^2 + 2abxy}{(x+y)^2}}$$

$$t_1 - t_1^1 = \frac{C_{load}}{2(x+y)p} ln \left[\frac{\left(V_{50\%} - \frac{ax+by}{x+y}\right) - p}{\left(V_{50\%} - \frac{ax+by}{x+y}\right) + p} \right] - ln \left[\frac{\left(V_{OH} - V_{th} - \frac{ax+by}{x+y}\right) - p}{\left(V_{OH} - V_{th} - \frac{ax+by}{x+y}\right) + p} \right]$$

The total delay $\tau_{PHL} = (t_1 - t_1^1) + (t_1^1 - t_o) = t_1 - t_o$

$$\tau_{PHL} = \frac{C_{load}}{2xt} \left(ln \left[\frac{(V_{OH} - V_{th} - a) - t}{(V_{OH} - V_{th} - a) + t} \right] - ln \left[\frac{(V_{OH} - a) - t}{(V_{OH} - a) + t} \right] \right)$$
$$+ \frac{C_{load}}{2(x+y)p} ln \left[\frac{\left(V_{50\%} - \frac{ax+by}{x+y}\right) - p}{\left(V_{50\%} - \frac{ax+by}{x+y}\right) + p} \right]$$
$$- ln \left[\frac{\left(V_{OH} - V_{th} - \frac{ax+by}{x+y}\right) - p}{\left(V_{OH} - V_{th} - \frac{ax+by}{x+y}\right) + p} \right]$$

5.3 Delay τ_{PlH} calculation

When input voltage switches from high (V_{OH}) to low (V_{OL}), the NMOS transistor is in cutoff and the load capacitance is being charged up through the PMOS transistor

$$C_{load} \frac{dV_{out}}{dt} = i_{Dload(Vout)}$$

Note that the load device is initially in saturation, and enters the linear region when the output voltage rises above $V_{dd} + V_{tload}$ where $V_{tload} < 0$

$$i_{Dload} = x(|V_{tload}|)^2 \text{ for } V_{out} \leq V_{dd} - |V_{tload}|$$

$$i_{Dload} = x[2|V_{tload}|(V_{dd} - V_{out}) - (V_{dd} - V_{out})^2] \text{ for } V_{out} > V_{dd} - |V_{tload}|$$

The delay time τ_{PLH} can be found as follows

$$\tau_{PLH} = C_{load} \left[\int_{V_{OL}}^{V_{DD}-|V_{tload}|} \frac{dV_{out}}{i_{Dsatload}} + \int_{V_{DD}-|V_{tload}|}^{V_{50\%}} \frac{dV_{out}}{i_{Dload(linear)}} \right]$$

Consider the first term $C_{load} \int_{V_{OL}}^{V_{DD}-|V_{tload}|} \frac{dV_{out}}{i_{Dsatload}}$

$$= \frac{2C_{load}}{x(|V_{tload}|)^2}(V_{out})_{V_{OL}}^{V_{DD}-|V_{tload}|}$$

$$= \frac{2C_{load}}{x(|V_{tload}|)^2} V_{DD} - |V_{tload}| - V_{OL}$$

Consider the second term $C_{load}\int_{V_{DD}-|V_{tload}|}^{V_{50\%}} \frac{dV_{out}}{i_{Dload(linear)}}$

$$= \frac{2C_{load}}{x}\int_{V_{DD}-|V_{tload}|}^{V_{50\%}} \frac{dV_{out}}{2|V_{tload}| - {V_{out}}^2}$$

$$= \frac{C_{load}}{x|V_{tload}|} ln\left[\frac{V_{50\%}}{2|V_{tload}| - V_{out}}\right]_{V_{DD}-|V_{tload}|}^{V_{50\%}}$$

$$= \frac{C_{load}}{x|V_{tload}|} ln\left[\frac{V_{50\%}}{2|V_{tload}| - V_{50\%}}\right] - ln\left[\frac{V_{dd} - |V_{tload}|}{3|V_{tload}| - V_{dd}}\right]$$

The total delay τ_{PLH} is sum of above two terms i.e.

$$\tau_{PLH} = \frac{C_{load}}{x|V_{tload}|}\left[2(V_{DD} - |V_{tload}| - V_{OL}) + \frac{1}{V_{tload}}\left[ln\left[\frac{V_{50\%}}{2|V_{tload}| - V_{50\%}}\right] - ln\left[\frac{V_{dd} - |V_{tload}|}{3|V_{tload}| - V_{dd}}\right]\right]\right]$$

The total propagation delay of the input signal through the differential pair τ_D is

$$\tau_D = \frac{\tau_{PLH} + \tau_{PHL}}{2}$$

Chapter 6

Conclusion and Future work

6.1 Conclusion

A tuneable UWB CMOS pulse generator has been proposed for material characterisation of concrete walls. It is very essential for fixing proper communication scheme and system development for wireless monitoring of wall-cracks. Simulation results show the circuit ability to generate Gaussian monopulses with tuneable pulse width of 0-26ps and tuneable pulse duration of 300-860ps with peak to peak pulse magnitude of 63.82mV with supply voltage of 1.8V. These Gaussian monopulses are generated by combination of cascaded delay cells, an encoder and gilbert cell with a second order RLC differentiator network.

6.2 Future Work

This work can be further carried out as a future scope in order to develop a complete crack detection system

- Interfacing the circuit to the antenna and practically finding the wall parameters.
- Through these wall parameters and FDTD simulations, finding the best frequency for communication.
- Developing an energy harvesting system through which the energy available is converted to electrical power that can be used to the circuit
- Developing a crack detection sensor which should be so sensitive to detect a minute crack observed.

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