Femtosecond RMS timing jitter from 1 GHz InP on-chip mode-locked laser at 1550 nm

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Abstract: In this work, we analyze the timing stability of a 1 GHz InP on-chip monolithic mode-locked laser at 1550 nm. 504 fs RMS timing jitter is achieved by a hybrid mode-locking operation.

1. Introduction

Due to their compactness and ability to tune the emission wavelength, semiconductor mode-locked lasers (MLLs) are attractive sources for optical frequency comb generation [1]. The typical repetition-rates (RR) from these lasers are in the range of few tens of GHz up to THz. However, for applications where a modulation of a single frequency carrier is required, the need for lower RR (few hundreds of MHz) lasers remains. The most common approach for low RR semiconductor mode-locking laser would be to employ an external cavity laser geometry [2]. The drawback of complexity of the external cavity lasers gave the motivation to develop a stand-alone long resonator mode-locked laser chip. The investigated chip is identical to that in the work of Guzmán [3]. We focus in this work on the timing jitter analysis whilst the chip is operated in a hybrid mode-locking regime.

2. Laser chip

A microscopic image of the utilized chip can be seen in Figure 1. The effective waveguide has a total length of 41 mm and the laser gain is achieved by applying a forward current at the gain pads. The saturable absorber (SA) section, in contrast, is defined by an isolated contact in the middle of the gain section. The laser resonator is realised between the two multimode interference reflectors (MIR). The MIRs are etched deeply to reflect part of the light back by total internal reflection and couple out the rest. The laser output is obtained by the signal coupled out from MIR1. The signal coupled out from MIR2 is amplified through a booster and guided subsequently to realize an on-chip photodiode (PD). The chip is attached to a custom-designed printed circuit board (PCB). The PD’s pad is bonded to this PCB which features a Bias-Tee to investigate the RF signal by an electrical spectrum analyzer (ESA). Furthermore, the gain current is applied to the gain section through another Bias-Tee. In this way, the RF signal which corresponds to the laser cavities’ RR can be supplied through the Bias-Tee to operate the chip in hybrid mode-locking regime. Moreover, the PCB is mounted on a custom-designed aluminium holder and the temperature is set to 17 °C through a Peltier element.

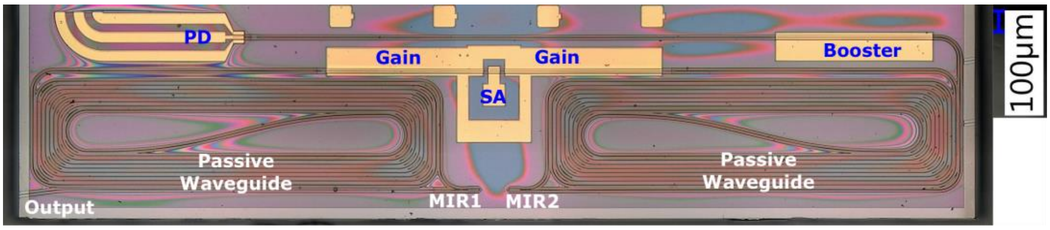

Figure 1: Microscope image of the investigated chip.

3. Experimental results

To realise the optical gain, a forward current is applied into the gain section of the chip. A reverse voltage is applied to the inbetween section to feature a SA. We varied the forward current from 30 to 200 mA in steps of 1 mA and the reverse voltage from 0 to -6 V in steps of 0.1 V. To characterise the chip, we obtained the electrical spectrum for each of the applied parameters. Figure 2 represents the peak power of the obtained spectra with respect to the applied gain current and reverse voltage. It can be clearly seen that there are few ranges where the peak power was strong and typical RF passive mode-locking spectra were realised in these ranges. Among these ranges, the best passive mode-locking stability performance is achieved for the current parameters from 130 to 150 mA with a step of 1 mA and voltage parameters from -4 to -6 V with a step of 0.1 V. For the foregoing range, we applied afterwards an RF signal from the synthesizer into the gain section to feature a hybrid mode-locking system. The best stability achievement is at a forward current of 143 mA and absorber reverse voltage of -5.8 V.

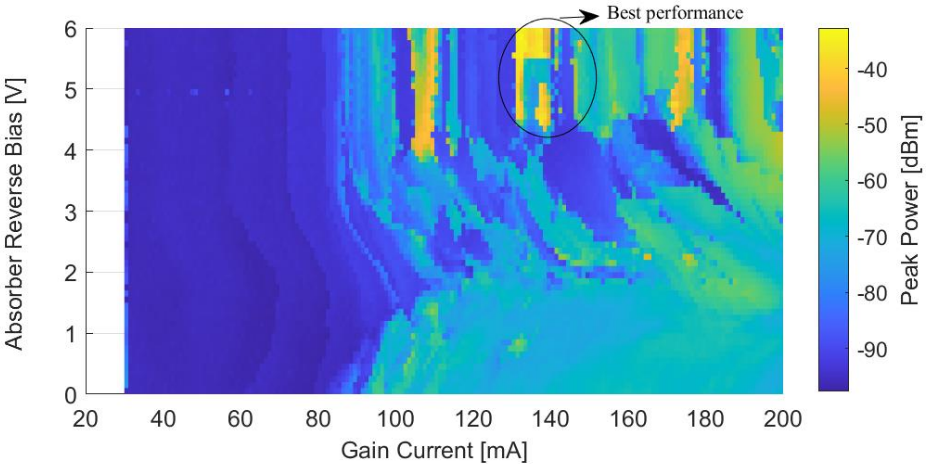

Figure 2: Peak Power for varied gain current and saturable absorber reverse voltage at the passive mode-locking operation.

The synthesizer frequencies are varied in the range from 800 MHz up to 960 MHz. The optimum stability is achieved for the locking range from 915 MHz to 925 MHz during hybrid mode-locking operation. Figure 3a and 3b show the fundamental frequency spectrum and phase noise at 922 MHz locking frequency, respectively. 504 fs RMS timing jitter is measured at this locking frequency for phase noise integration range from 20 kHz up to 100 kHz offset frequency. The measured RMS timing jitter from the synthesizer is 490 fs for the same phase noise offset frequency range. Additionally, we analyzed the amplitude noise performance. The measured relative high frequency amplitude noise is 0.036 %, extracted from the first seven harmonics [4].

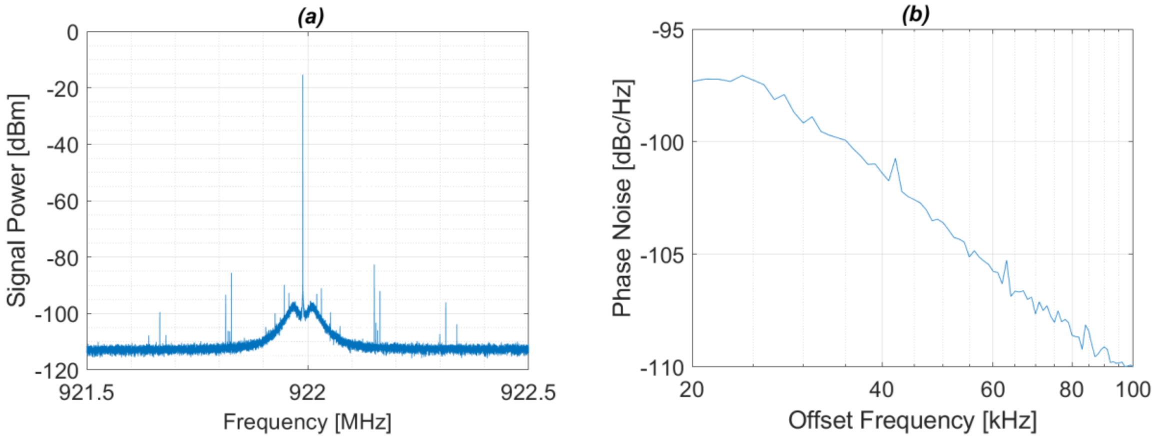

Figure 3: Electrical spectrum and phase noise for 922 MHz fundamental frequency during hybrid mode-locking operation.

4. Conclusion and outlook

In this work, we present an analysis of the noise performance of a 1 GHz InP on-chip monolithic hybrid mode-locked laser at 1550 nm wavelength. The measured RMS timing jitter is 504 fs for a phase noise integration range from 20 kHz to 100 kHz offset frequency. In future, we will investigate the pulse width and peak energy from this stand-alone on-chip mode-locked laser.

5. References

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