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Methodology to Improve Switching Speed of SiC MOSFETs in Hard Switching Applications

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To the Graduate Council:

I am submitting herewith a dissertation written by Handong Gui entitled "Methodology to Improve Switching Speed of SiC MOSFETs in Hard Switching Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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Methodology to Improve Switching Speed of SiC MOSFETs in Hard Switching Applications

A Dissertation Presented for the

Doctor of Philosophy

Degree

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Handong Gui

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Abstract

To meet the higher efficiency and power density requirement for power converters, the switching speed of power devices is preferred to increase. Thanks to silicon carbide (SiC) power MOSFETs, their intrinsic superior switching characteristics compared with silicon IGBTs makes it possible to run converters at faster switching speed in hard switching applications. Nevertheless, the switching speed is not only dependent on the device's characteristics, but also strongly related to the circuit like gate drive and parasitics. To fully utilize the potential of SiC MOSFETs, the impact factors limiting the switching speed are required to be understood. Specific solutions and methods need to be developed to mitigate the influence from these impact factors.

The characterization of the switching speed for SiC MOSFETs with different current ratings is conducted with double pulse test (DPT) first. Based on the result, the impact factors of switching speed are evaluated in detail.

According to the evaluation, the switching speed of SiC discrete devices with low current rating is mainly limited by the gate drive capability. A current source gate drive as well as a charge pump gate drive are proposed, which can provide higher current during the switching transient regardless of the low transconductance and large internal gate resistance of SiC discrete devices.

For SiC power modules with high current rating, the switching speed is mainly determined by the device drain-source overvoltage resulting from circuit parasitics. An analytical model for the multiple switching loops related overvoltage in 3L-ANPC converters is established. A simple modulation is developed to mitigate the effect of the non-linear device output capacitance, which helps reduce the overvoltage and enables higher switching speed operation of SiC power modules.

Furthermore, the layout design methodology for three-level converters concerning the multiple commutation loops is introduced. The development of a laminated busbar for a 500 kVA 3L-ANPC converter with SiC power modules is presented in detail.

Finally, a SiC based 1 MW inverter is built and tested to operate at cryogenic temperature. The proposed control and busbar above are utilized to increase the switching speed of the SiC power module.

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1 Introduction

This chapter starts with the illustration of the requirement and impact of the switching behavior of power semiconductor devices in hard switching applications from different aspects, which include the efficiency, power density, EMI and reliability. Then the background of silicon carbide (SiC) MOSFETs is introduced. The characteristics of the device are presented, and the benefits and challenges when applying SiC MOSFETs are examined. Finally, an outline for this dissertation is provided.

1.1 Requirement and Impact of Switching Speed in Hard Switching Applications

As a consequence of natural resources depletion and motivation to reduce carbon dioxide emission, electricity generated from renewable energy will see a four times increase by 2050 [1]. With such trend, power electronics conversion will play more and more important role in both the load and source side. The share of electricity flowing through power electronics was 30% in 2005, and this number is expected to rise to 80% by 2030 [2]. For instance, hybrid power generation and distributed propulsive power have been identified as candidate transformative aircraft configurations for future commercial transport vehicles with reduced fuel burn and harmful emissions [3].

From the performance point of view, the two key technical specifications for power electronics conversion are efficiency and power density. The National Aeronautics and Space Administration (NASA) has proposed a roadmap to achieve 25 kW/kg power density and 99.5% efficiency for inverters in aircraft electric propulsion drives [3]. The switching behavior of power devices has great influence on reaching these targets as the power devices are turned on and off with voltage and current across them. Passive components like inductors, transformers and

capacitors serve as energy buffers to smooth the power, and their size and performance are also significantly affected by the switching patterns controlled by the power devices. Thus, the requirement and impact of switching speed of power semiconductor devices in power converter systems, especially in hard switching applications, needs investigation.

Fig. 1-1 shows the typical hard switching transient with drain current, drain-source voltage in a typical phase-leg, and the generated energy loss of the lower device throughout each switching event (turn-on or turn-off). As non-ideal switches, it takes time (i.e., switching time t_{on} , t_{off}) to complete the switching transition, and a certain amount of loss is produced (i.e., switching loss E_{on} , E_{off}) along with the voltage and current change. which are the underlying reasons causing the non-ideal power conversion [4], [5]. Specifically, according to the aforementioned design targets of power converters, the impact of the switching performance in hard switching applications on efficiency, density, and EMI and reliability are evaluated as follows.

1.1.1 Efficiency

The loss dissipated by power converters primarily comes from three parts: power devices, passive components, and auxiliary circuits. Among them, the power device related loss occupies a large portion [6], [7]. For specific applications without magnetic components in their power stage such as motor drives, power devices are the main contributor to the total loss of the power converter.

Power device loss consists of conduction loss, switching loss and gate drive loss [4], [5]. In high power and hard switching applications, conduction loss and switching loss are dominant, while gate drive loss can be neglected. Although the characteristics of different power devices can affect the results, and the loss is dependent on voltage and load conditions, the switching loss is typically more than 50% of the total power device loss in an optimal converter design [8]. With

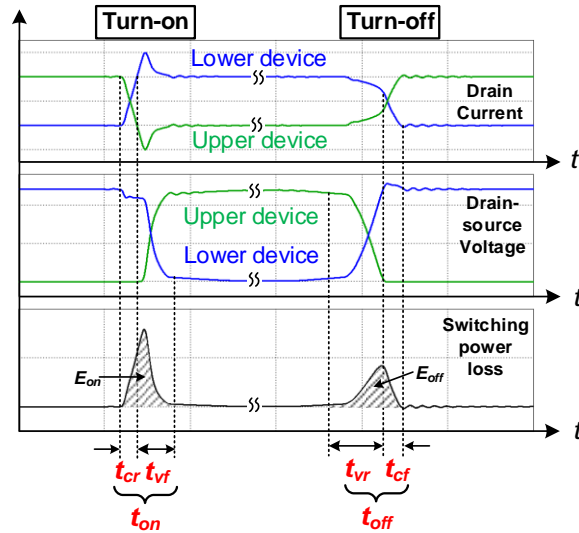


Fig. 1-1. Switching waveform of power devices indicating switching time and switching loss.

the same switching speed and switching energy in each switching event, the switching loss is proportional to the switching frequency. Thus, switching loss gets higher with higher switching frequency. To increase the switching frequency and avoid increasing the switching loss in hard switching applications, the only way is to reduce the dissipated energy in each switching event. Based on Fig. 1-1, the dissipated energy is caused by the overlap of device drain current and drain-source voltage. Hence, to achieve lower energy loss, the overlap area needs to be reduced. In other words, the device should switch faster to decrease the rise/fall time of the device current and voltage. In summary, increasing the power device switching speed is beneficial for improving the efficiency of the converter system.

Fig. 1-2 plots the calculated conduction and switching loss in a 500 kW inverter for aircraft application. Clearly, the switching loss is linear to the switching frequency, and higher switching speed with lower gate resistance leads to lower loss. To meet the target in [3], higher switching speed is preferred to reduce the switching loss.

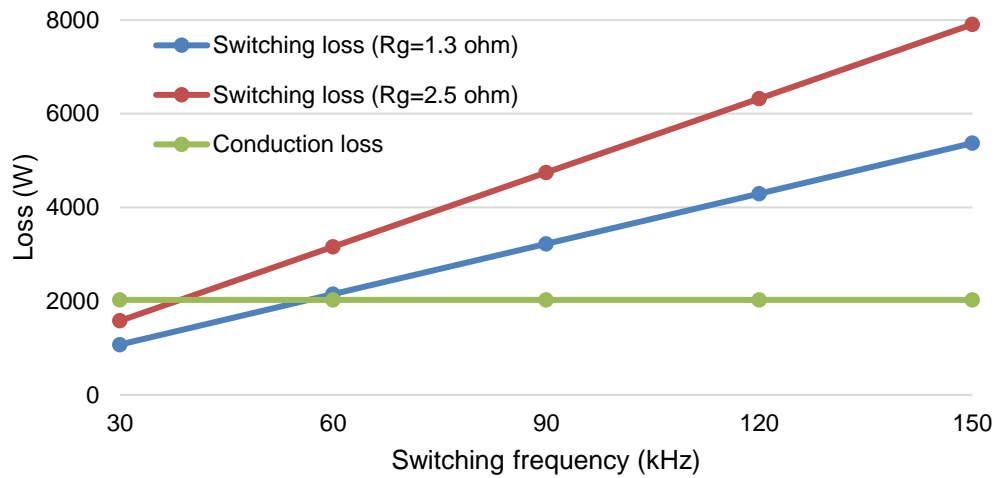


Fig. 1-2. Conduction and switching loss with different switching frequencies in a 500 kW inverter for aircraft application.

1.1.2 Power Density

Power devices, passive components, cooling systems, and auxiliary circuits are the main parts contributing to the size and weight of power converters. Among them, thermal management systems (e.g., heatsink and fan) and passive components (e.g., DC-link capacitor, transformer and filter) are most critical [9]. Fig. 1-3 illustrates the weight and volume breakdown of a 6.1 kW EV charger [10]. Notably, the heatsink occupies 16% of the weight and 25% of the volume, while the passive components (magnetics and dc-bus capacitors) account for 55% of the weight and 50% of the volume.

The device switching speed shows different impacts on the weight and size of thermal management systems and passive components. In general, higher loss produced by power devices results in larger and heavier cooling systems to dissipate the heat. Based on the explanation in the

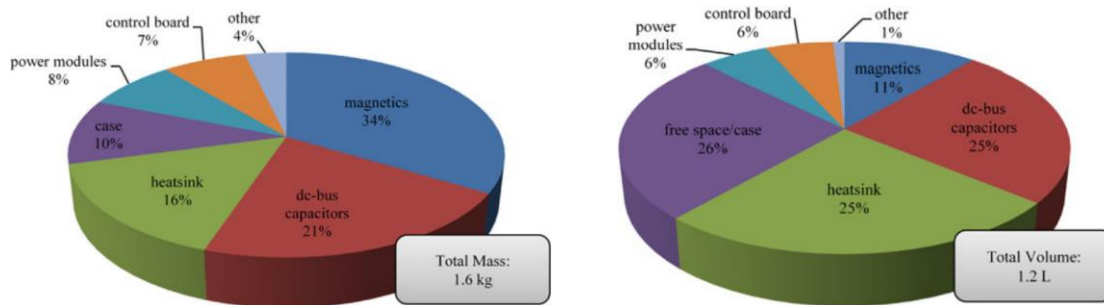


Fig. 1-3. Weight and volume breakdown of a 6.1 kW EV charger [10].

last section, increasing the switching speed of power devices can help reduce the switching loss, thus decrease the required weight and size of the thermal management system.

1.1.3 EMI and Reliability

According to the investigation of efficiency and power density, increasing power device switching speed can help achieve better performance. However, this is not the case for electromagnetic interference (EMI) and reliability.

EMI is a critical concern when developing power converters as it affects the operation reliability of neighboring equipment as well as the power converter itself. Equipment has to compile with several standards (e.g., IEC61800-3 Qp for motor drives, DO-160E for airborne equipment). To mitigate the EMI noise, filters are necessary to be implemented, which increases the size and weight of the converter system [11-14].

There are mainly three ways that the EMI noise can interfere with the external circuit: conductive coupling, radiated coupling, and near field coupling [15]. Among them, conductive coupling is usually the most significant EMI in power electronics systems and attracts more attention. Conducted EMI noise flows in both power lines and the ground. It is usually decoupled

to common mode (CM) and differential mode (DM) noise to conduct measurement and analysis more conveniently as shown in Fig. 1-4.

CM and DM noise is influenced by both the switching frequency and the switching speed of the power devices. The relationship between the switching frequency and the EMI filter weight/size is not necessarily linear because of the noise spectrum and varying standard requirement for different frequencies. Generally speaking, the lower corner frequency an EMI filter has, the better EMI noise attenuation it can provide. With the same EMI filter structure, the lower corner frequency calls for larger inductance and capacitance, which increases the weight and size. Fig. 1-5 depicts the results of designed inductance versus the switching frequency for CM and DM filters, respectively [16]. Although there is no monotonic relationship between filter inductance and switching frequency, the inductance value shows a general increasing trend with higher switching frequency.

The device switching speed mainly influences the CM noise. Faster switching speed introduces higher dv/dt across the parasitic capacitance and injects larger leakage current into the ground. However, it is found that the switching speed (dv/dt) of devices only influences the noise spectrum at high frequency range (>1 MHz) as shown in Fig. 1-6 [13]. Actually, this principle is well known in signal processing industry [17]. Thus, the switching speed has less significant influence on EMI noise than the switching frequency.

Another critical concern in reliability is the overvoltage induced by the resonance between parasitic inductance and capacitance during the switching transient. The parasitic inductances are mainly from the wiring structure of the power devices, the equivalent series inductance (ESL) of capacitors, and the PCB or busbar traces. The parasitic capacitances include the power device input

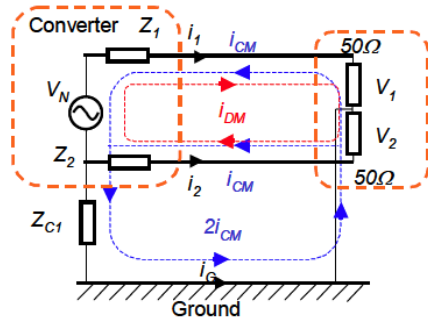


Fig. 1-4. Flow of CM and DM noise in a single-phase converter [15].

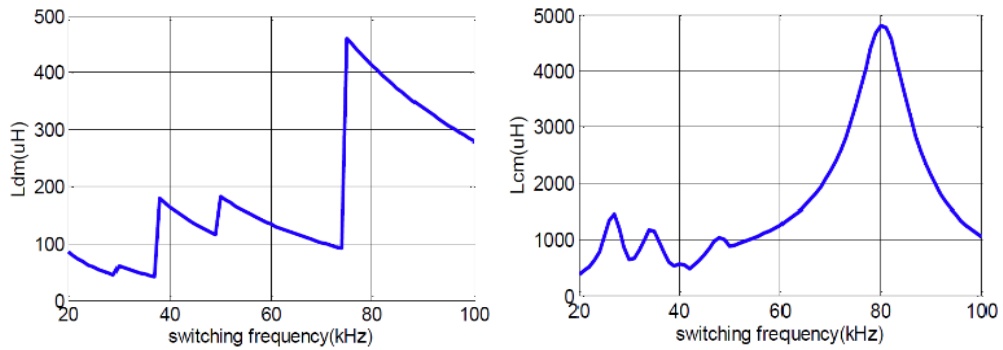


Fig. 1-5. Sweeping results of filter inductance versus the switching frequency [16].

Left: DM inductance. Right: CM inductance.

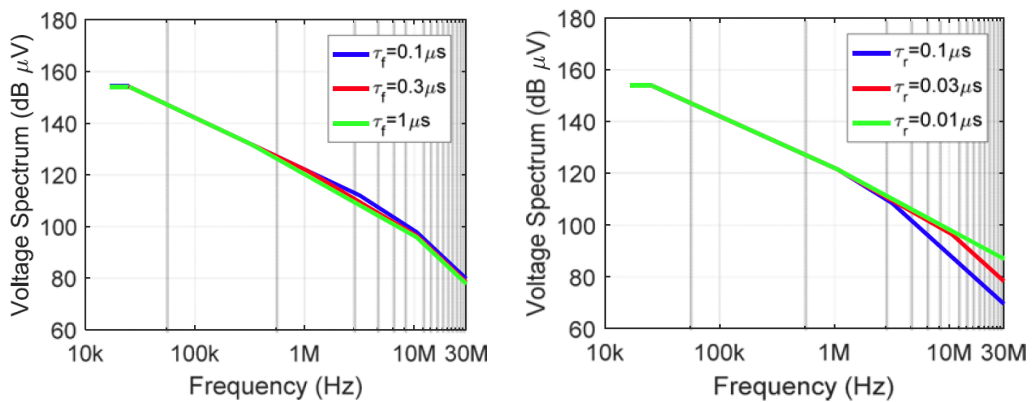


Fig. 1-6. CM bare noise spectral envelopes with different device voltage rise/fall time [13].

Left: voltage rise time. Right: voltage fall time.

and output capacitance, and the stray capacitance between two PCB or busbar layers. Generally, the higher dv/dt and di/dt with faster switching speed contribute to higher overvoltage [18]. Fig. 1-7 plots the peak device drain-source voltage versus dv/dt and di/dt [19]. As dv/dt and di/dt get higher ($k_{dv/dt}$ and $k_{di/dt}$ in the figure get larger), higher peak voltage occurs. If the overvoltage exceeds the device rating, the device lifetime can be significantly influenced, or the device can be directly damaged. Therefore, the overvoltage must be kept in an acceptable range when increasing the switching speed of power devices.

1.2 SiC MOSFETs

Power semiconductor devices are the fundamental components in power electronics converters. The characteristics of power semiconductor devices are the key points to determine the overall performance of a power converter. Conventionally, the power devices are mainly silicon (Si) based because of the maturity and low cost of the material. However, Si devices have exhibited limitations in conduction loss, switching speed and operating temperature [20], [21], and have reached close to the theoretical thermal and voltage handling limits [22]. Fortunately, the development of wide bandgap (WBG) devices brings a revolutionary change. Two representatives of WBG materials are silicon carbide (SiC) and gallium nitride (GaN) as they show promising characteristics in electrical, thermal and manufacturability. A comparison of properties between WBG and Si material is shown in Fig. 1-8. It is observed that from the aspects of voltage, switching frequency and thermal conductivity, WBG materials present superior characteristics [23].

Both SiC and GaN based power devices have distinct benefits for specific applications: SiC is regarded as a stronger candidate for power electronic applications above 1.2 kV, while GaN is ideal for high-frequency applications, and is regarded as highly competitive in applications below

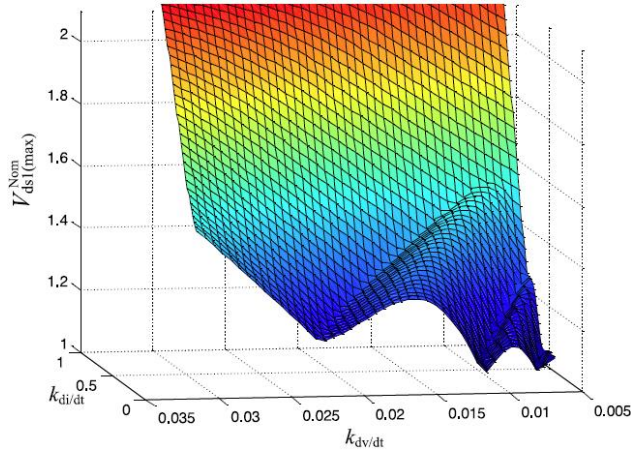


Fig. 1-7. Overvoltage under different dv/dt and di/dt [19].

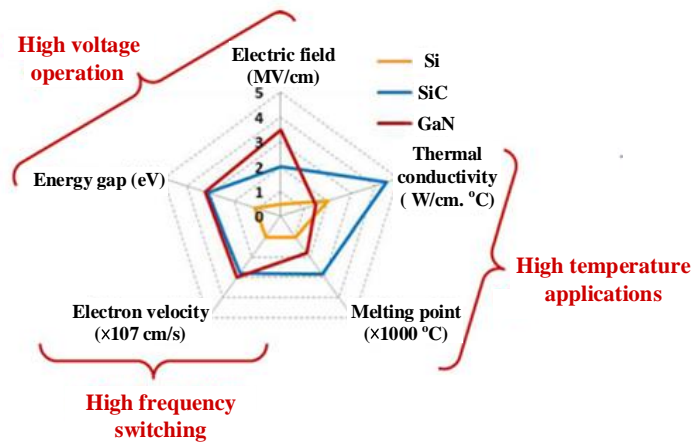


Fig. 1-8. Comparison of properties between WBG and Si material [23].

1.2 kV. In particular, device voltage rating between 650V and 1.2 kV is a competitive space that can be supported by either SiC or GaN technologies [24]. Thus, SiC devices are more suitable for high power high voltage applications. Today, SiC processing technologies are more mature and show higher reliability than GaN, which has resulted in SiC devices having a larger market share.

Fig. 1-9 shows the market breakdown of SiC devices from 2017 to 2023. The total SiC based device market is expected to grow steadily, reaching more than \$1.5 billion in 2023. Among all

the applications, the largest one is EV/HEV. This dissertation focuses on SiC devices, especially SiC MOSFETs, and the following sections will introduce the benefits and challenges of SiC utilization.

1.2.1 Benefits

SiC as a compound semiconductor material is formed by silicon (Si) and carbon (C). Currently, 4H-SiC is preferred for power devices primarily because of its high carrier mobility, particularly in the vertical c-axis direction [25]. Table 1-1 summarizes the physical property differences between Si and 4H-SiC [26]. As a rule of thumb, SiC has ten times the electric breakthrough field, allowing for thinner epitaxial layers to support the high blocking voltage in power devices. As an example, a 4.5 kV power device would require only a 40 μm -50 μm drift layer, as opposed to almost 500 μm in the case of silicon. The thinner and more highly doped drift layer leads to much lower drift resistance, hence, to low forward voltage and low conduction loss, while maintaining high blocking voltage. The velocity of minority carriers swept out of the depletion region is determined by saturation drift velocity. Hence, a higher saturated drift velocity of SiC will also increase the switching speed. Moreover, SiC thermal conductivity is 3.7 W/cm/K, allowing for efficient thermal management. With a high electric breakthrough field, SiC can be used especially for high-voltage unipolar devices such as MOSFETs and Schottky diodes, achieving low switching loss.

In today's power transistors, the Si IGBT is typically the preferred choice for high power high voltage applications. Moreover, the Si IGBT as a bipolar device has lower on-state losses than

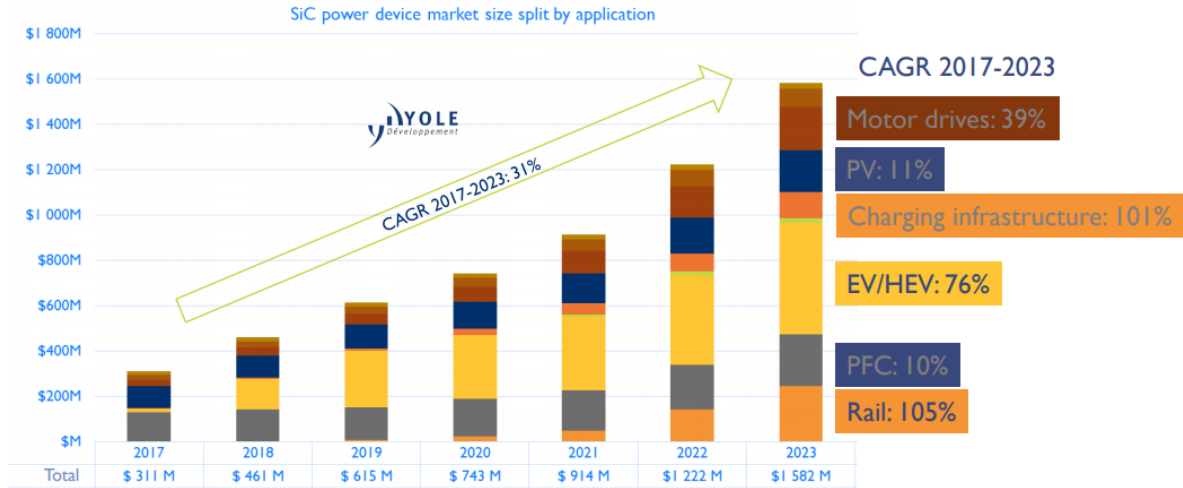


Fig. 1-9. SiC power devices market revenue from 2017 to 2023 [24].

Table 1-1. Comparison of physical properties of Si and 4H-SiC [12].

| Material Property | Si | 4H-SiC |
|----------------------------------|--------------------|-----------------|
| Energy bandgap (eV) | 1.12 | 3.23 |
| Breakdown field (MV/cm) | 0.25 | 2.5 |
| Thermal conductivity (W/cmK) | 1.5 | 3.7 |
| Saturation drift velocity (cm/s) | 1.05×10^7 | 2×10^7 |

high voltage Si MOSFET. However, a major drawback of Si IGBTs is that high switching speed operation is difficult due to the restricted dynamics of injected holes, resulting in significant switching loss by tail currents. Alternatively, the larger critical electric field for breakdown of SiC allows greatly reduced drift region resistance for the same breakdown voltage compared to the Si based devices. Furthermore, SiC MOSFETs have the intrinsic benefit of being unipolar devices, and thus enable faster switching than a Si IGBT, and better controllability of switching behavior. This makes the SiC MOSFET a more attractive device as shown in Fig. 1-10 [27].

Fig. 1-11 shows the comparison of the characteristics of a Si IGBT and a SiC MOSFET from Infineon with the same voltage and current ratings (1.2 kV, 50 A) at room temperature with the characteristics of SiC MOSFET normalized to 1. The SiC MOSFET shows significantly better properties in all aspects of switching time, switching loss, reverse recovery and gate charge.

1.2.2 Challenges

As described previously, due to the fast switching-speed capability, SiC MOSFETs offer a promising opportunity to significantly improve the overall performance of power conversion, such as increased power efficiency and density, as compared to Si IGBTs. However, it is the high switching-speed capability of SiC MOSFETs that makes their switching behavior become more susceptible to the parasitics and noise of the circuit especially in hard switching applications. As a result, the observed switching performance of SiC MOSFETs in real power converter systems cannot achieve the claimed number in manufacturer's datasheet. For example, the switching time of a SiC MOSFET based three-phase inductive motor drive was increased by a factor of 2, which induced 30% increase in switching loss compared with the test result of double pulse test under the same operating conditions because of the influence from the motor load [28]. On the other hand, the high speed switching transient introduces more oscillation and voltage spikes across the parasitics, which decrease the reliability of the components in the converter. Therefore, specific design is required to fully utilize SiC MOSFETs.

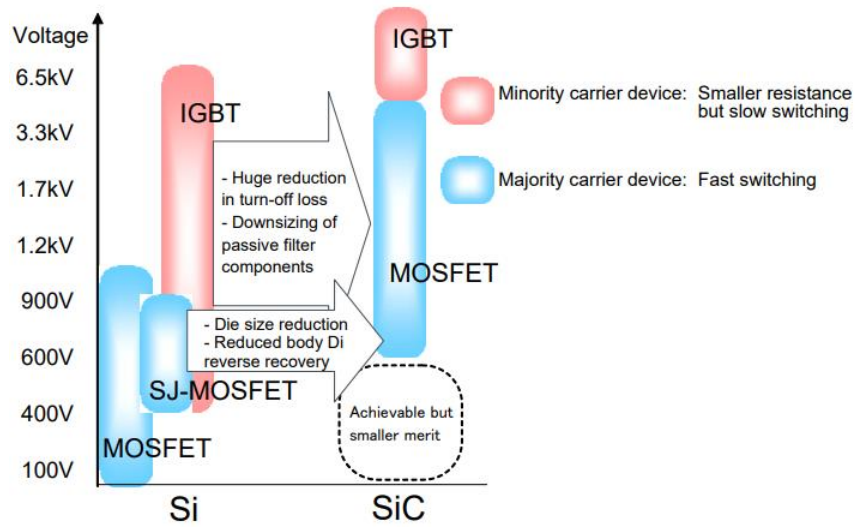


Fig. 1-10. Application of Si IGBT and SiC MOSFET [27].

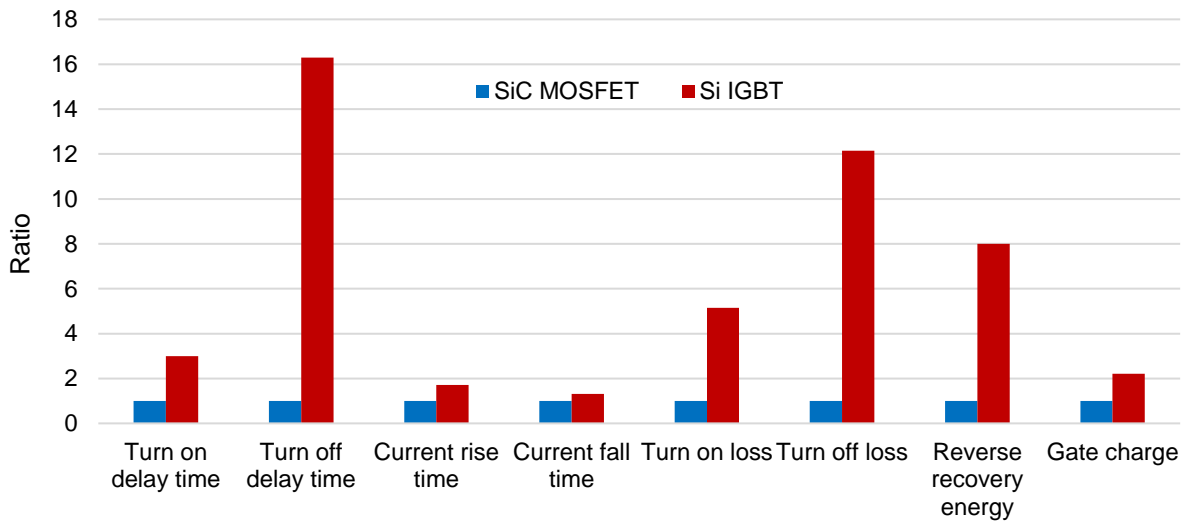


Fig. 1-11. Comparison of Si IGBT and SiC MOSFET with same voltage and current ratings.

1.3 Dissertation Outline

According to the above introduction, several conclusions can be drawn. 1) In hard switching applications, higher switching speed is beneficial for improving the converter efficiency and power density. EMI is not impacted much if the switching frequency is not changed, but the overvoltage

can be an issue to worsen the reliability. 2) SiC devices can provide superior switching characteristics that allow higher switching speed operation. Therefore, how to fully utilize the potential of the high switching speed capability of SiC MOSFETs, and to avoid the negative effect from increasing the switching speed is worth investigating. The research objectives of this dissertation are to 1) evaluate the key factors that limit the switching speed increase of SiC MOSFETs in hard switching applications with hardware testing; 2) develop solutions to avoid or suppress the negative effect of these factors, and improve the switching speed of SiC MOSFETs.

This dissertation is organized as follows:

Chapter 2 reviews the existing research in two areas. First, the commonly discussed impact factors of switching performance are summarized and reviewed one by one, which include gate drive technology, parasitics and layout, load, and heatsink. Second, the widely adopted methodology of switching performance characterization including double pulse test and calorimetric measurement is reviewed. Note that the reviewed literature in this chapter is not limited within the SiC research area.

Chapter 3 conducts the switching characterization with a SiC low current discrete MOSFET and a SiC high current MOSFET module. Based on the testing results, the impact factors that limit the switching speed of SiC MOSFETs are analyzed from the perspective of both device intrinsic characteristics and external circuits.

Chapter 4 proposes a current source gate drive for SiC discrete MOSFETs that can avoid the limitations of existing gate drive technologies. The detailed operating principle, parameter design, loss analysis, benefits and challenges are presented.

Chapter 5 proposes a charge pump gate drive with simpler structure and control to overcome the drawback of the current source gate drive. Similarly, the detailed operating principle, parameter design, loss analysis, benefits and challenges are illustrated.

Chapter 6 presents the modeling and mitigation of overvoltage in three-level active neutral point clamped converters. The multiple commutation loops issue is introduced, and the related overvoltage is modeled. With the model, the relationship between the overvoltage and the two commutation loops is evaluated. Moreover, a modified modulation is developed to mitigate the influence of the non-linear device output capacitance and reduce the overvoltage.

Chapter 7 introduces the design criteria of power stage layout for three-level converters to reduce the loop parasitic inductance. Based on the criteria, a detailed design example is provided for the laminated busbar layout of a 500 kVA SiC based three-level active neutral point clamped converter. The fabrication process of the designed busbar with aluminum is also presented.

Chapter 8 presents the design and testing of a 1 MW inverter for aircraft applications based on SiC power modules. The developed technologies in previous chapters are implemented. The design of sub-systems and the detailed switching loss analysis are included.

Chapter 9 gives the conclusion, main contribution and recommended future work.

2 Literature Review

Extensive work has been conducted to characterize and analyze the switching behavior of power semiconductor devices. Since the motivation of this dissertation is to evaluate the impact factors of the SiC MOSFET switching speed, the existing work in this area should be reviewed and summarized. In the meantime, the methodology of characterizing the device switching behavior is also critical, especially for high switching speed conditions. In this chapter, literature in the above two areas is reviewed. Note that not only SiC devices are concentrated, but also Si MOSFETs, Si IGBTs and GaN devices are included.

2.1 Impact Factors of Switching Speed in Hard Switching Applications

Phase-leg configuration is the basic cell of most hard switching converters and is commonly selected to evaluate device switching performance. Fig. 2-1 plots the configuration of a phase-leg switching cell with the main components highlighted, which include power semiconductor devices, gate drives, parasitics and load current. According to [29], there are four main factors impacting the switching speed of WBG power devices, namely gate drives, parasitics, inductive loads, and heatsinks.

2.1.1 Gate Drives

As shown in Fig. 2-1, a typical gate drive mainly consists of gate drive circuit, signal isolator, and isolated power supply. Among them, gate drive circuit directly provides the required gate voltage and current to the power devices, and greatly influences the switching performance of power devices. In addition, if the signal isolator and isolated power supply cannot operate properly during the fast switching transient, the PWM signals' transmission from controller to gate drive can be interfered, and the switching operation of the power device can be affected [30].

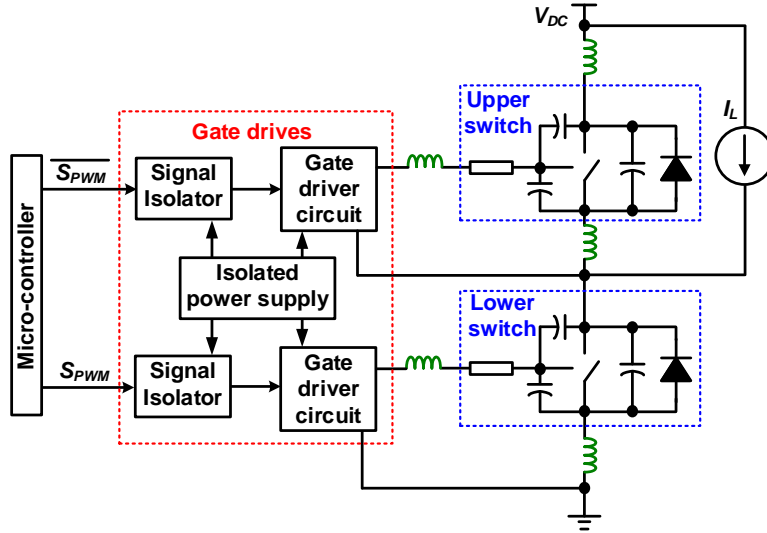


Fig. 2-1. Configuration of phase-leg with gate drivers and parasitics.

In terms of the technology of a gate drive circuit, it can be grouped into three fundamental categories: voltage source gate drives (VSGs), current source gate drives (CSGs), and resonant gate drives (RGs) [31], [32]. The advantage of the RG is its ability to reduce the gate drive loss [33-35]. However, for SiC MOSFETs in high voltage and high power applications, the gate drive loss is small compared to other losses due to their superior intrinsic gate charge characteristic, which makes RGs less attractive because of its more complicated structure.

The VSG is the most common technology for semiconductor power devices because of its simple structure and control. Fig. 2-2 shows a phase-leg with a typical VSG. The VSG circuit can be simplified to a half bridge phase leg that connects the gate drive power supply. The typical switching waveform during the switching transient of the lower switch is shown in Fig. 2-3. During turn-on transient, the gate drive output voltage increases from zero to V_{dr_L} in t_r . The total turn-on switching time t_{on} is the sum of current rise time t_{cr} and the voltage fall time t_{vf} . The turn-off transient is similar to turn-on. In a proper gate drive circuit design or selection for SiC MOSFETs

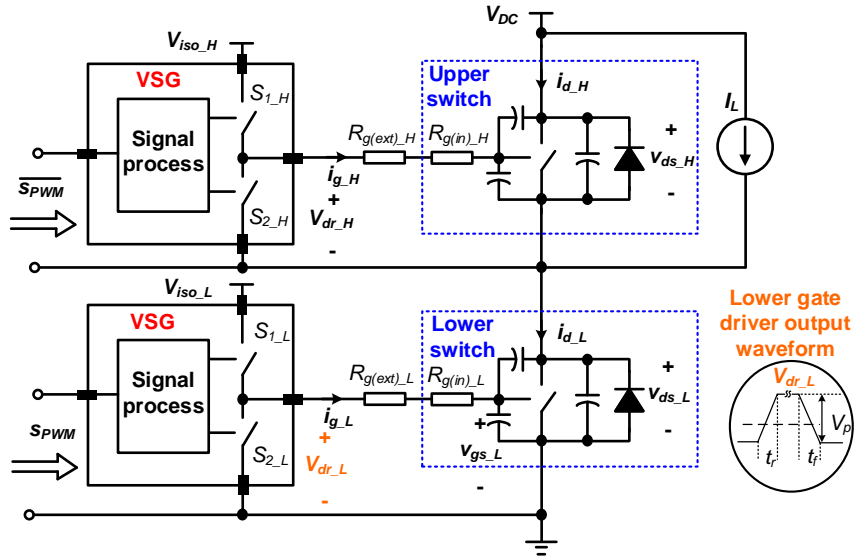


Fig. 2-2. Phase-leg with VSG.

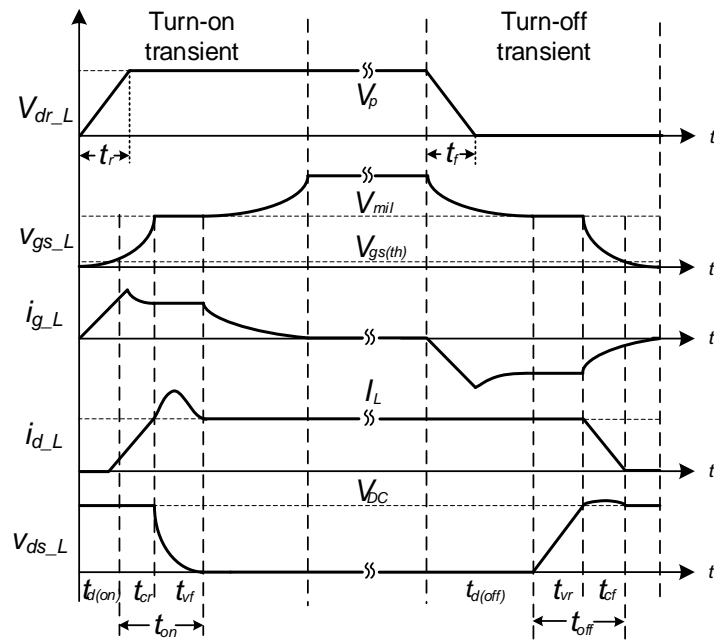


Fig. 2-3. Typical waveforms during switching transient with VSG.

in hard switching applications, t_r is much lower than t_{on} and does not have great influence on the switching transient.

For SiC MOSFETs, some manufacturers provide guidance about the design of VSG [27], [36], and researchers have proposed more advanced controls and topologies to improve the performance of VSGs, which mainly includes crosstalk and overvoltage suppression [37-41], current and voltage balancing [42-45], and dynamic gate impedance control [46-50]. However, it is still not clear whether the switching speed of the SiC discrete devices and power modules have been maximized with the existing VSG technology.

If the VSG is not sufficient to fully utilize the switching speed of SiC MOSFETs, the CSG can be a candidate in spite of its more complex hardware circuit and control strategy. The basic switching transient with CSGs is similar to that with VSGs. The main difference between VSGs and CSGs is the gate current. For VSGs, the gate current is proportional to the difference between gate drive supply voltage and the device gate voltage. As gate voltage increases in switching transients, the gate current keeps decreasing. In contrast, the gate current provided by CSGs can be independent from the gate drive supply voltage. Thus, with the same gate charge, the required charging/discharging time with CSGs can be reduced. Fig. 2-4 presents a typical CSG for Si MOSFET with an inductor [51].

Not much research has been conducted to develop CSGs for SiC MOSFETs, and most of them are based on linear circuits, which are difficult for applications requiring large gate current [52], [53]. More CSGs have been proposed for Si MOSFETs and Si IGBTs. In [51], [54-57], CSGs with inductors are adopted for low voltage Si MOSFETs in voltage regulator applications to reduce the gate drive loss. In [58-62], CSGs based on voltage controlled current source with BJTs are used to adaptively tune the dv/dt and di/dt and improve the switching loss of Si IGBTs. Nevertheless, these

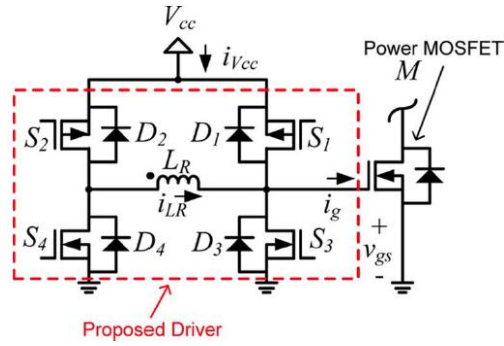


Fig. 2-4. CSG proposed in [51].

CSGs are not designed for SiC MOSFETs. Compared to Si MOSFETs and Si IGBTs, there are some unique characteristics of SiC MOSFETs like lower gate source voltage rating, lower transconductance, and higher internal gate resistance. Therefore, existing CSGs may not be suitable for SiC MOSFETs.

In addition to gate driver circuit, signal isolator and isolated power supply also show influence on the switching speed of power devices. As shown in Fig. 2-2, the source of the upper side switch is the middle point of the phase-leg, and it jumps between the DC bus voltage and the lower side ground at switching frequency. This high frequency dv/dt can result in CM current from secondary to primary side of the isolator through the coupling capacitance [63]. This current can interfere with the PWM signals generated from the micro-controller. In consequence, abnormal PWM signals are transmitted to the gate drive, and the power devices are falsely turned-on or off. Thus, special attention should be paid to the common mode transient immunity (CMTI) of the signal isolator and the coupling capacitance of the isolated power supply.

2.1.2 Parasitics and Layout

Fig. 2-5 shows the primary parasitics in the phase-leg configuration, including three parasitic inductances, three parasitic capacitances, and one internal gate resistance of power devices. These parasitics influence the transients of two loops: the gate loop and the power loop. The parasitics involved in the gate loop are gate loop inductance L_{gs} , common source inductance L_{cm} , transfer capacitance C_{gd} , input capacitance C_{gs} , and internal gate resistance $R_{g(int)}$. The power loop mainly includes power loop inductance L_{ds} , common source inductance L_{cm} , transfer capacitance C_{gd} , and output capacitance C_{ds} . Note that L_{cm} and C_{gd} are shared by both loops.

The influence of parasitics on the gate loop is first reviewed. According to the equivalent circuit of the gate loop, a LCR resonant network is formed by L_{gs} , L_{cm} , C_{gd} , C_{gs} and $R_{g(int)}$ [64]. Therefore, an oscillation can occur across the device gate-source terminal if the parasitic inductance is large enough. In extreme cases where the oscillation is high enough to exceed the device rating, the gate of the device can be damaged. An external gate resistance can be added to mitigate the oscillation, but the device switching speed is slowed down. For SiC MOSFETs, they normally have larger internal gate resistance than conventional Si devices, which is beneficial for lowering the gate loop oscillation. Generally, the influence of the parasitics on the gate loop is limited as long as the loop layout is carefully designed.

Compared to the gate loop, the more critical concern comes from the power loop. The mechanism of the power loop oscillation is due to the resonance between the power loop inductance L_{ds} and device output capacitance C_{ds} . Many papers have discussed the modeling and mitigation of the oscillation issue [65-70], and most of them were focused on the turn-off overvoltage. However, several studies have shown that the turn-on overvoltage is normally higher than the turn-off case in WBG devices [18], [19], [71]. The mechanism of turn-off and turn-on

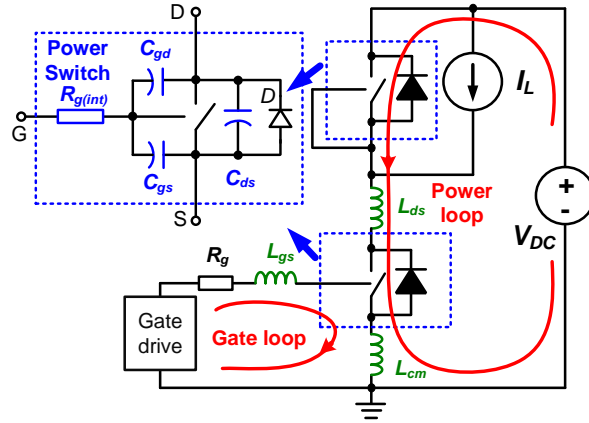


Fig. 2-5. Parasitics in the switching commutation loop.

overvoltage is different. Fig. 2-6 shows the equivalent circuits of the turn-on and turn-off transients [29]. The turn-on transient is mainly affected by dv/dt , while di/dt has larger influence on the turn-off. Nevertheless, di/dt also has significant influence on the turn-on transition [18]. To guarantee that the overvoltage is not high enough to damage the device, snubber circuits are usually added to absorb the oscillation energy [72], [73]. However, these snubbers not only increase the loss, but also increase the complexity of the power stage, which deteriorate the reliability of the converter.

Most of the research on power device overvoltage is based on two-level phase-leg. However, the overvoltage issue can even be more severe and complicated in multi-level topologies since they have multiple commutation loops. Several studies focused on switching loops in three-level converters [74-77]. Two modulations for three-level active neutral point clamped (3L-ANPC) converters are compared in [74] to evaluate the loss distribution with different switching loops. The multi-loop influence on loss, harmonics and overvoltage in commonly used three-level converters is analyzed in [75]. The overvoltage issue in the 3L-ANPC converter and its causes are investigated in [76], while [77] provides a solution for the overvoltage mitigation. However, there



Fig. 2-6. Equivalent circuits of turn-on and turn-off transients [29].

Left: turn-on. Right: turn-off.

is still the lack of an analytical model that can explain the coupling effect among different commutation loops and build the relationship between the overvoltage and the parasitics for multi-level converters.

Last but not least, the mutual influence between the gate and power loop should also be evaluated. The shared parasitics by the two loops are the common source inductance L_{cm} and transfer capacitance C_{gd} . During the turn-on transient, the increase of drain current introduces a positive di/dt across L_{cm} . In consequence, a positive voltage drop occurs on L_{cm} , which reduces the real voltage applied to the gate-source of the device. A similar situation happens during the turn-off transient. The absolute value of the applied gate voltage is reduced due to a negative voltage across L_{cm} . Therefore, the switching speed is reduced [78]. Fortunately, this issue can be strongly attenuated by using the Kelvin connection for device packaging [79], and many manufacturers have already had products for the SiC MOSFET [80], [81].

Compared to L_{cm} , the so called “cross-talk” phenomenon caused by C_{gd} is more severe. The mechanism of cross-talk during turn-on and turn-off switching transients is shown in Fig. 2-7 [37]. Taking turn-on transient as an example, the rise of the drain-source voltage of the upper switch generates the current flowing through the transfer capacitance C_{gd_H} . This current then introduces a positive voltage across the gate resistance. If the current is large enough and the induced voltage

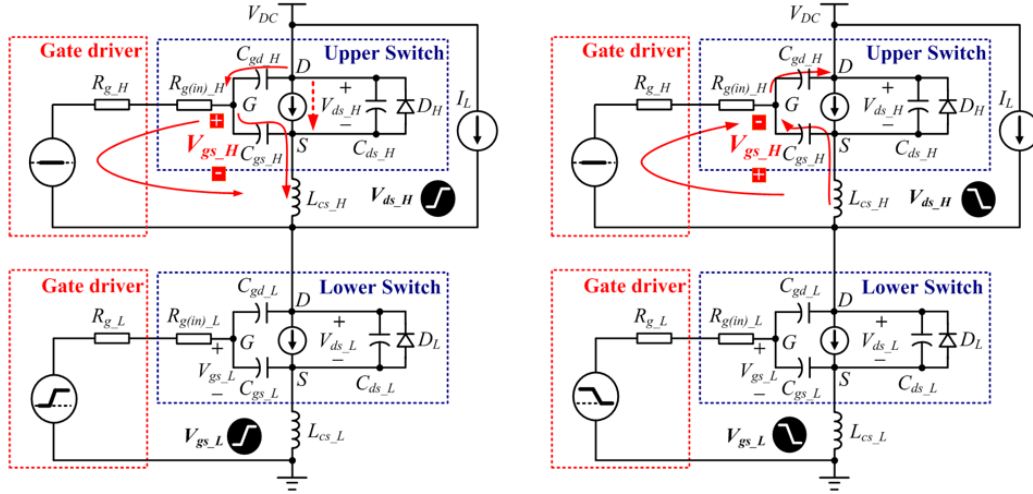


Fig. 2-7. Mechanism of cross-talk [37]. Left: turn-on. Right: turn-off.

exceeds the threshold voltage of the power device, the upper switch is falsely turned-on. Since the lower switch has already been turned-on at this moment, a shoot-through current occurs from DC bus to the ground, which not only generates extra loss, but also can cause device damage if the shoot-through time lasts long enough. Although the cross-talk during the turn-off transient creates a negative spurious voltage and does not cause false turn-on, the gate may degrade if the negative voltage is lower than the minimum allowed gate rating. Apparently, higher switching speed results in higher current on C_{gd} , leading to more severe cross-talk. To avoid or suppress the cross-talk, auxiliary circuits have been developed to regulate the impedance of the device gate, which should be effective in most cases [37-39], [82-85].

From the above survey on parasitic influence, it can be concluded that parasitics bring about negative effect for high switching speed operation. To further improve the device switching speed, the parasitics are desired to be reduced. Among the aforementioned parasitics, the capacitances and the internal gate resistance are the intrinsic parameters of the device, which are not changeable. So the parasitics that can be decreased are the inductances. Since the power loop can introduce

more serious issues, and the common source inductance can be improved by using Kelvin connection, the power loop inductance is the critical element. The most straightforward way to reduce this inductance is optimizing the circuit layout. Methodology and guidance of power loop layout have been studied for both PCB design [86-91] and busbar design [92-97]. There are two main types of layout design for the power loop design. As shown in the left side of Fig. 2-8, the power loop of lateral layout is paralleled with the PCB layer. Shielding layers can be added to the inner PCB layers to screen the magnetic field. The loop of vertical layout is perpendicular to the PCB layers and utilize multiple layers to complete the loop, as shown in the right side of Fig. 2-8. Considering that the PCB board thickness is relatively small, the power loop inductance of vertical layout is normally lower than that of lateral loop because of the smaller loop area [86]. Thus, vertical layout is recommended for power loop design of a two-level phase leg.

However, most previous work focused only on low power two-level converters based on PCBs and did not pay much attention to the high power busbar design for multi-level converters. Actually, noise issue is even more serious in high power hard switching converters because of the higher voltage and current stress. Moreover, the multiple commutation loops in multi-level converters make the loop layout more complicated. In [98-104], busbars are designed specifically for three-level converters such as NPC-type and T-type converters. However, the loop inductance is normally higher than 100 nH, which still limits the switching speed of SiC MOSFETs due to introduced voltage overshoot. Thus, methodology should be developed for low inductance layout design of three-level converters.

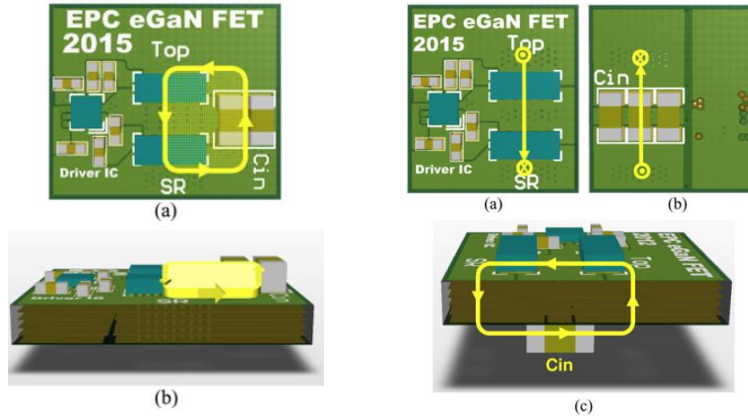


Fig. 2-8. Two types of layout for power loop [86]. Left: lateral. Right: vertical.

2.1.3 Loads

In motor drive applications, one of the problems with the device fast switching is the motor overvoltage resulting from reflected wave phenomenon. The reason of this issue is the high dv/dt of the power devices and surge impedance mismatch between the cable and motor [105]. If the output line-to-line voltage is not filtered, the peak voltage at the motor side can be much higher than the DC bus voltage [106].

Recently, it has been found that the load also has impact on the switching speed and loss of the power devices [28], [107-112]. The equivalent circuit of a three-phase two-level inverter with motor load is depicted in Fig. 2-9. It is observed that the load is equivalently paralleled with the power device. During the switching transient, the impedance of the device is dominated by its output capacitance. If the equivalent impedance of the load paralleling with the device is much larger than the impedance of the output capacitance, then the switching performance of the device is not affected. Fig. 2-10 draws the impedance curves with different loads. For SiC MOSFETs, the typical frequencies of interest during the switching transient is several MHz. It is clear that the

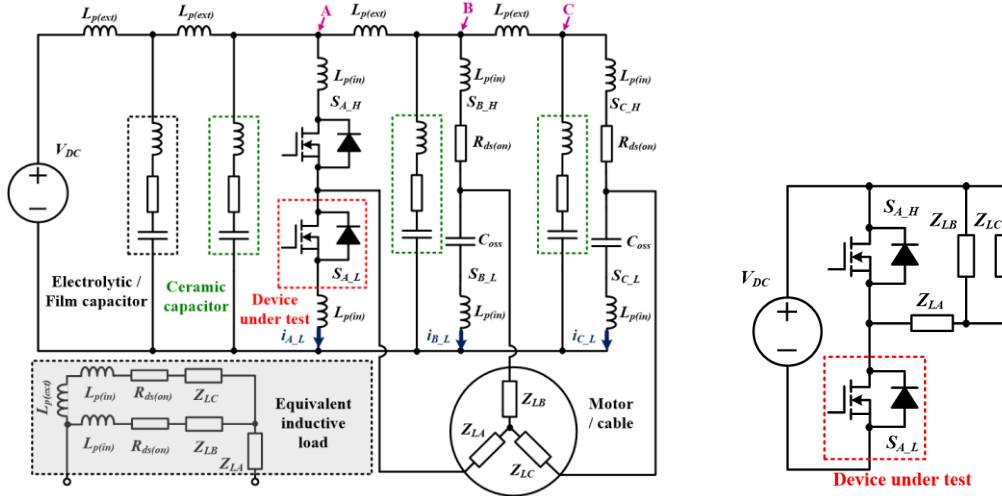


Fig. 2-9. Equivalent circuit of three-phase inverter with motor load [28].

Left: converter system. Right: single phase-leg.

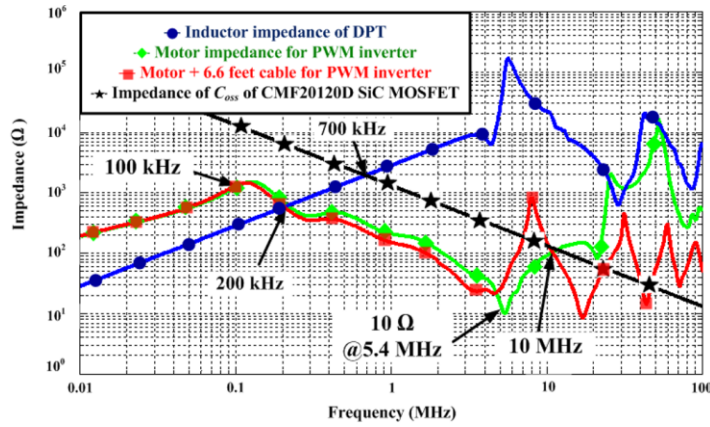


Fig. 2-10. Impedance curves with different loads [28].

motor load has lower or similar impedance compared to the device output capacitance in that specific frequency range. In consequence, both the switching time and loss of the power device is increased.

2.1.4 Heatsinks

In high power applications, heatsinks and coldplates are widely implemented to maintain the temperature of the power devices. Power devices are mounted to the heatsink with a thin layer of thermal insulation material like thermal pad or thermal grease. Thus, as shown in Fig. 2-11, parasitic capacitances are introduced between the drain of the power devices and the heatsink plate [113], [114]. As a result, extra capacitances are paralleled with drain-source of the devices, which slow down the switching speed. If the heatsink is grounded, an extra path is generated. CM current flows through this path during the fast switching transient and results in higher EMI.

2.2 Methodology for Characterization of Device Switching Performance

Although different models and simulation tools have been developed [66], [115-119], the most straightforward and effective way to evaluate the switching performance of a power device is still the real hardware testing. Nowadays, there are two main kinds of methods to implement the switching characterization: double pulse test and calorimetric measurement.

2.2.1 Double Pulse Test

The most widely adopted way for the switching characterization is the double pulse test (DPT) [120-126]. Fig. 2-12 plots the typical configuration and waveforms of the DPT for a phase-leg. Two pulses with different width are generated for the gate of the lower switch, which is the device under test (DUT). The upper switch keeps off and the body diode provides the freewheeling path. When the lower switch is on, the DC bus voltage is applied across the load inductor L , and the drain current i_d increases linearly. By turning off and on of the lower switch, the device voltage and current during the turn-off and turn-on transients can be captured with the help of an

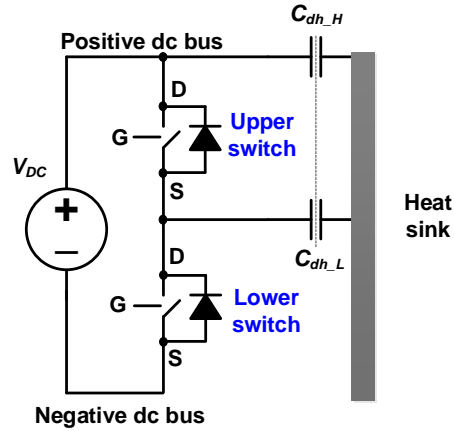


Fig. 2-11. Capacitive coupling between devices and heatsink.

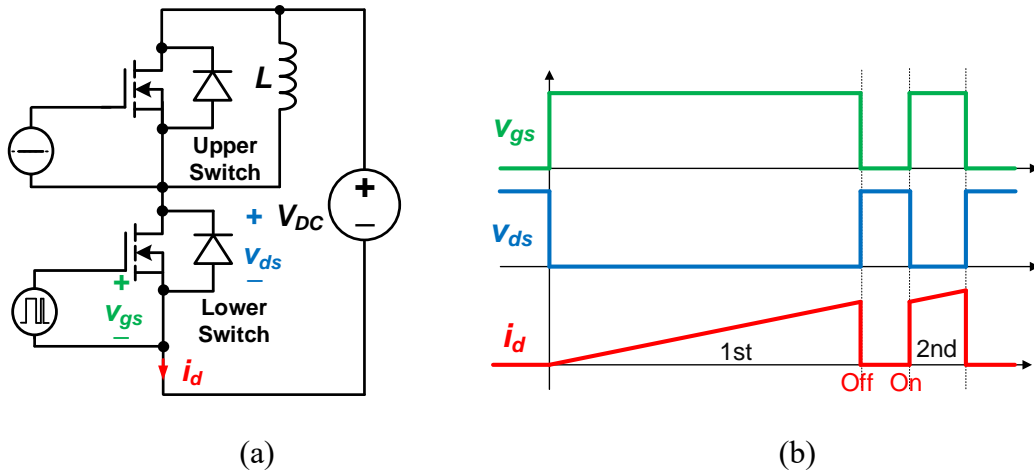


Fig. 2-12. Typical DPT for phase-leg. (a) Configuration. (b) Waveforms.

oscilloscope. After the data processing, the switching time and loss can be calculated. The fundamental elements in a DPT are drawn in Fig. 2-13.

According to the above introduction, the key point of the DPT is to capture the waveforms during the device switching transients. Because the switching time of WBG devices is usually

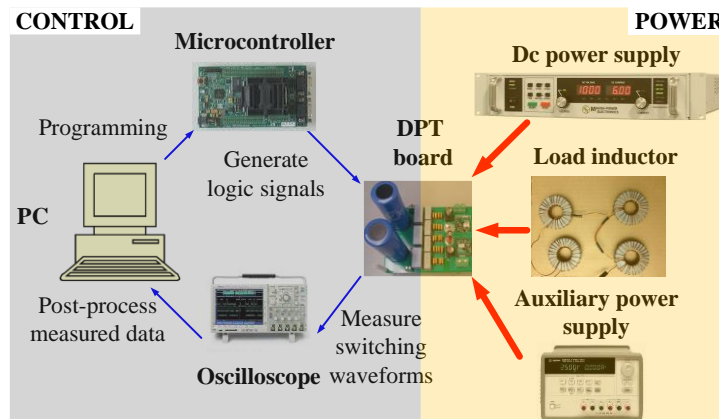


Fig. 2-13. Elements in a typical DPT [126].

short, namely tens of or even several nanoseconds, it is required to pay special attention to the selection and usage of probes and oscilloscopes.

It has been concluded in [126] that high bandwidth passive probes are preferred for voltage measurement, while coaxial shunt is more suitable for current measurement. Moreover, probe-tip adaptors are recommended to shorten the grounding lead, which helps reduce noise due to the loop inductance [127].

Another critical issue is the voltage-current alignment. Since the DPT uses the overlap between the captured voltage and current waveforms to calculate the switching loss, the propagation delay mismatch in voltage and current measurement can result in serious inaccuracy. As shown in Fig. 2-14, a 2-ns misalignment leads to more than 100% error in switching loss estimation [126]. Therefore, it is important to deskew the probes by using the deskew function in the oscilloscope or the deskew fixture to align the voltage and current measurement.

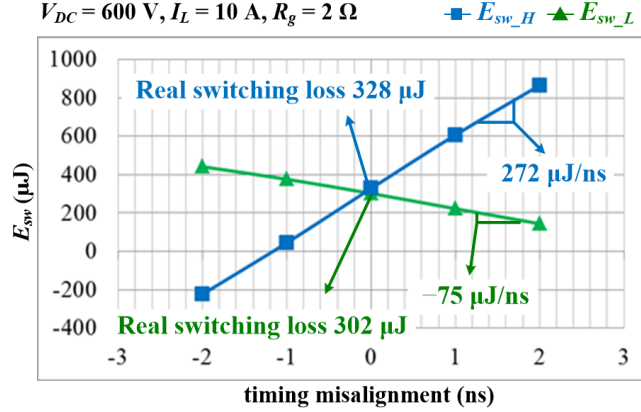


Fig. 2-14. Relationship between calculated switching loss and V-I alignment [126].

2.2.2 Calorimetric Measurement

Another popular method to characterize the device switching performance is the calorimetric measurement [128-133]. Different from the DPT using electric waveforms, calorimetric measurement utilizes heat dissipated during the operation of the device to get the switching loss. Fig. 2-15 illustrates the configuration and testing setup of a typical calorimetric measurement [130]. The DUT is located inside a box with thermal insulation, and temperature sensors are attached to the DUT or the heatsink close to the DUT. By monitoring the temperature of the device, the switching loss can be calculated.

With the temperature stabilized, the total dissipated power of a device is

$$P_{sw} = \frac{T_c - T_a}{R_{th}} \quad (2-1)$$

where T_c and T_a are monitored device and ambient temperature inside the box, while R_{th} is the thermal resistance from device case to the ambient.

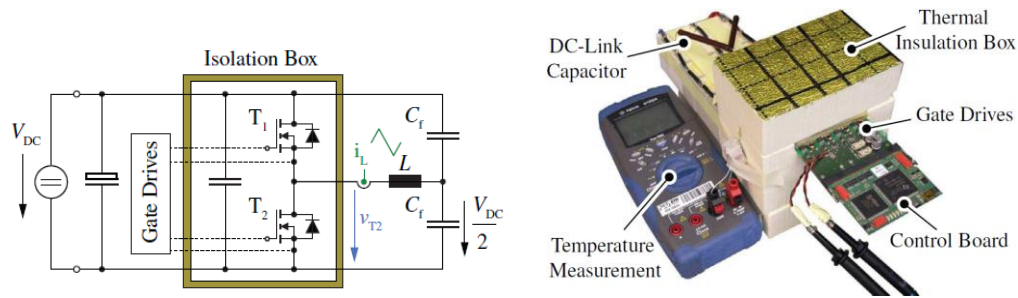


Fig. 2-15. Calorimetric measurement for device loss [130].

Left: configuration. Right: testing setup.

Since the total loss includes both the switching and conduction loss, the switching loss can be calculated by deducting the conduction loss. When calculating the conduction loss, the on-resistance can be obtained based on the monitored temperature and the temperature dependent curve from the device datasheet.

From the last section, the DPT requires careful alignment to obtain accurate switching information, which increases the difficulty of implementation especially in very high switching speed applications. In general, the calorimetric measurement can provide more accurate loss results. However, the calorimetric measurement is only effective to obtain the loss of a power device. For example, it is very difficult to identify the turn-on and turn-off loss, not to mention the switching time and transient overshoot information. Thus, the DPT is more applicable for cases where details of the switching process are needed, while the calorimetric measurement is preferred when accurate total switching loss is needed.

2.3 Summary

This chapter presents the review of two areas that are closely related to the switching performance of power devices.

First, the impact factors that limit the switching speed of power devices in hard switching applications is reviewed. Four elements are included: gate drive technologies, parasitics and layout design, loads, and heatsinks. For gate drive technologies, voltage source gate drives (VSG) are most widely implemented, while current source gate drives (CSG) can also be the candidate. However, it is not clear if the existing gate drives can fully utilize the switching speed capability of SiC MOSFETs. Parasitics mainly introduce overvoltage and influence the reliability of power devices. PCB and busbar layout should be optimized to reduce the parasitics, especially the loop inductance. For loads and heatsinks, they both introduce extra parasitics to the circuit, and can deteriorate the switching performance and increase EMI of the converter.

Second, two main methods of characterizing device switching performance are summarized: double pulse test (DPT) and calorimetric measurement. For DPT, the selection and usage of measurement tools is critical because the waveforms during the fast switching transient should be captured. For calorimetric measurement, high accurate switching loss can be obtained. These two methods have advantages and drawbacks, and are suitable for different applications.

3 Characterization of Switching Speed of SiC MOSFETs

This chapter studies the limitation and impact factors of switching speed of SiC devices in hard switching applications. As has been pointed out, both the device intrinsic characteristics and the external circuit have significant influence on the switching performance. Therefore, both are evaluated with double pulse tests in this chapter.

SiC MOSFETs with various current ratings should be evaluated because they have different intrinsic characteristics, and the parasitics exhibit significantly different influence when di/dt and dv/dt change. Fig. 3-1 plots the comparison between some SiC discrete devices and power modules from different manufacturers. Generally, power modules with multiple SiC dies in parallel have higher current rating. Therefore, a SiC discrete device and a SiC power module are selected for testing. Specific design concerns are introduced in detail for high power module characterization.

With the conducted test above, the switching transients in different cases are analyzed and compared. The impact factors that limit the switching speed of SiC MOSFETs are described, which serve as the reference for proposing solutions to improve the switching speed.

This part of work is published or accepted in the journal and conference papers [134], [135].

3.1 Switching Transient Analysis

3.1.1 Typical Switching Transient and Impact Factors of Switching Speed

A typical phase-leg configuration with two MOSFETs as well as the parasitics are plotted in Fig. 3-2. The parameters and parasitics are defined as in Table 3-1. The load current flows into the switching node, so the lower side MOSFET is the active switch, while the upper side MOSFET is the synchronous switch.

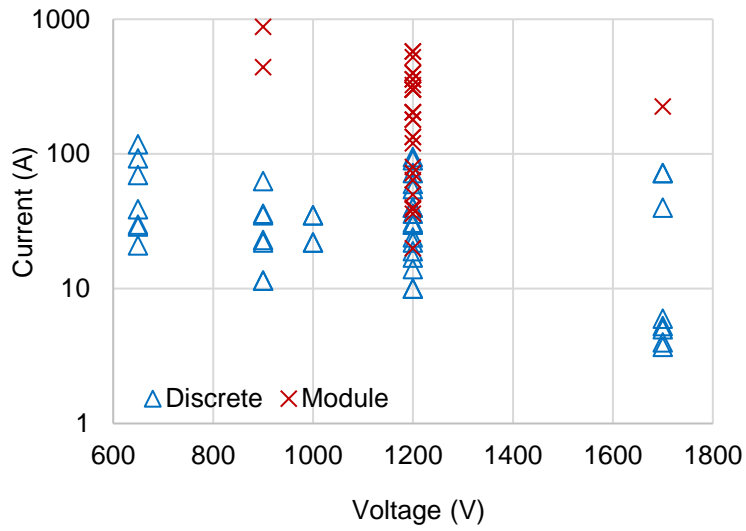


Fig. 3-1. Voltage and current ratings of SiC discrete devices and power modules from several manufacturers.

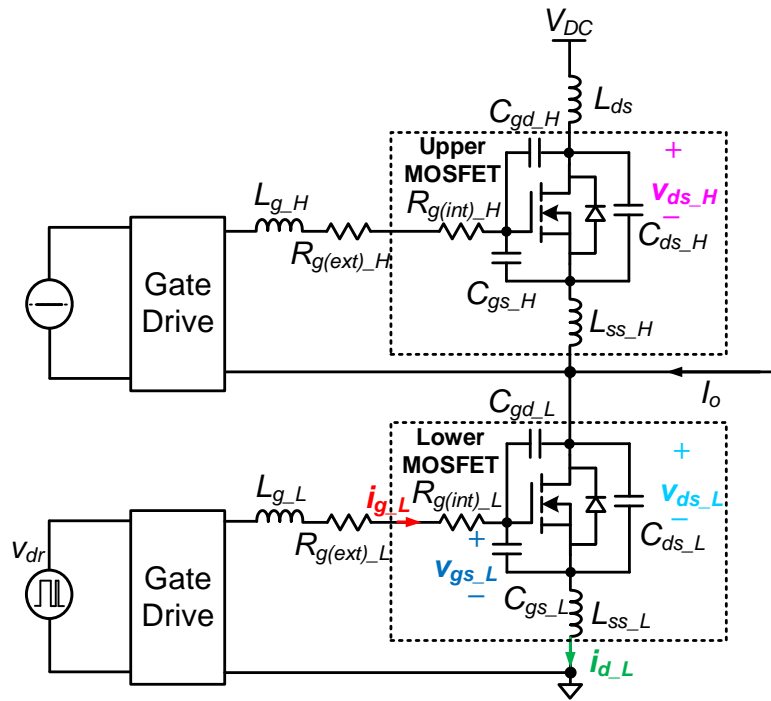


Fig. 3-2. Phase-leg configuration of FET/FET structure including switches and circuit parasitics.

Table 3-1. Parameters and parasitics definition in Fig. 3-2

| Parameters | Description |
|-------------------------------|--|
| I_o | Load current |
| V_{DC} | DC bus voltage |
| V_{dr} | Gate drive supply voltage |
| i_{g_L} | Gate current of lower switch |
| i_{d_L} | Drain current of lower switch |
| v_{gs_L} | Gate-source voltage of lower switch |
| v_{ds_H}/v_{ds_L} | Drain-source voltage of upper/lower switch |
| $R_{g(ext)_H}/R_{g(ext)_L}$ | External gate resistance of upper/lower switch |
| $R_{g(int)_H}/R_{g(int)_L}$ | Internal gate resistance of upper/lower switch |
| C_{gs_H}/C_{gs_L} | Gate input capacitance of upper/lower switch |
| C_{gd_H}/C_{gd_L} | Transfer capacitance of upper/lower switch |
| C_{ds_H}/C_{ds_L} | Output capacitance of upper/lower switch |
| L_{g_H}/L_{g_L} | Gate loop inductance of upper/lower switch |
| L_{ss_H}/L_{ss_L} | Common source inductance of upper/lower switch |
| L_{ds} | Total power loop inductance |

Fig. 3-3 plots the typical waveforms during the switching transient, and the different modes during the switching transient are briefly explained as follows.

1) Mode 1: turn-on signal is applied to the gate drive of the lower MOSFET, and the gate-source voltage v_{gs_L} starts to increase. The drain-source voltage v_{ds_L} of the lower MOSFET remains at the bus voltage V_{DC} , and the drain current i_{d_L} is zero until v_{gs_L} reaches the threshold voltage V_{th} . In this mode, the lower MOSFET operates in the cutoff region.

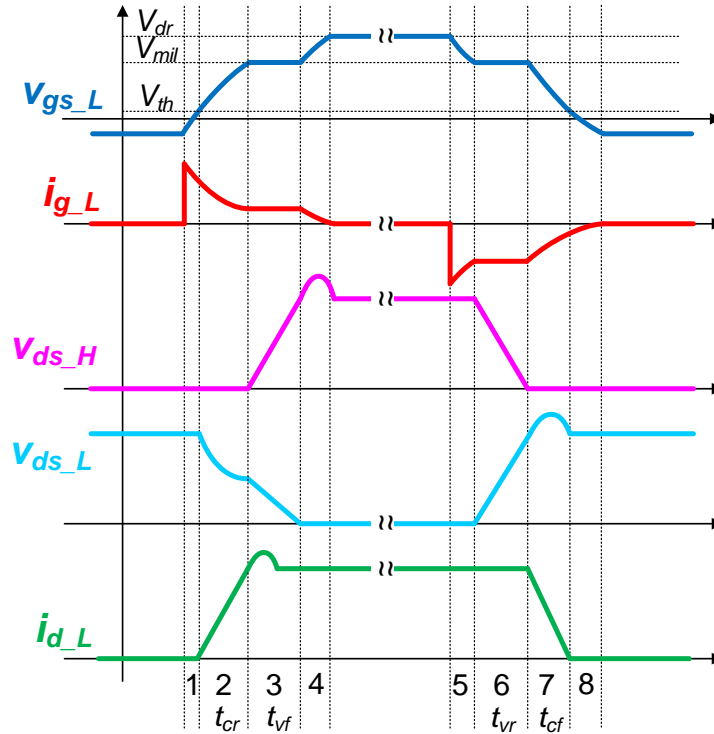


Fig. 3-3. Typical switching transient waveforms.

2) Mode 2: after v_{gs_L} reaches V_{th} , the lower MOSFET starts to turn on and the load current starts to commutate from the body diode of the upper MOSFET to the channel of the lower MOSFET. v_{ds_L} does not drop because the body diode of the upper MOSFET still conducts and v_{ds_L} is clamped at the bus voltage. During this process, the lower MOSFET operates in the saturation region, and the drain current can be expressed as

$$i_{d_L}(t) = g_m (v_{gs_L}(t) - V_{th}) \quad (3-1)$$

where g_m is the transconductance of the MOSFET.

This mode ends when the drain current reaches the load current I_o . At the end of this mode, the gate-source voltage reaches the Miller voltage, which is expressed as

$$V_{mil} = V_{th} + \frac{I_o}{g_m} \quad (3-2)$$

The current rise time can be calculated as

$$t_{cr} = t(V_{mil}) - t(V_{th}) = (R_{g(ext)_L} + R_{g(int)_L}) C_{gs_L} \ln \frac{V_{dr} - V_{th}}{V_{dr} - V_{th} - \frac{I_o}{g_m}} \quad (3-3)$$

3) Mode 3: the current completes the commutation, and the body diode of the upper MOSFET is off. The drain-source voltage of the lower MOSFET starts to decrease while that of upper device increases. The gate current i_{g_L} is mainly used to charge the transfer capacitance C_{gd_L} so the gate-source voltage keeps constant, which equals to V_{mil} . During the process, the drain-source voltage of the lower MOSFET v_{ds_L} is

$$v_{ds_L}(t) = V_{DC} - \frac{V_{dr} - V_{mil}}{(R_{g(ext)_L} + R_{g(int)_L}) C_{gd_L}} t \quad (3-4)$$

This mode ends when v_{ds_L} drops to zero. The voltage fall time is expressed as

$$t_{vf} = \frac{C_{gd_L} V_{DC}}{I_{g_L}} = \frac{(R_{g(ext)_L} + R_{g(int)_L}) C_{gd_L} V_{DC}}{V_{dr} - V_{th} - \frac{I_o}{g_m}} \quad (3-5)$$

4) Mode 4: C_{gs_L} is further charged until v_{gs_L} reaches V_{dr} while v_{ds_L} and i_{d_L} go into steady state.

The turn-off transient from mode 5 to 8 in Fig. 3-3 is similar to the turn-on. The detailed analysis will not be covered in this dissertation.

As mentioned above, the switching speed mainly influences the switching loss. In hard switching applications, the current-voltage overlap loss is the dominant loss. From Fig. 3-3, it is

observed that the current-voltage overlap only occurs on the lower MOSFET, which is the active switch. Therefore, the overlap loss during turn-on transient can be written as

$$E_{on} = \int_0^{t_{ov}} i_{d_L} v_{ds_L} dt \quad (3-6)$$

where t_{ov} is the overlap time of drain current and drain-source voltage. During the turn-on transient, it equals to the sum of t_{cr} and t_{vf} . Eq. (3-6) can be simplified if the voltage and current are regarded as changing linearly:

$$E_{on} = \frac{1}{2} I_o V_{DC} (t_{cr} + t_{vf}) \quad (3-7)$$

Thus, it is necessary to evaluate the impact factors on t_{cr} and t_{vf} so that the switching loss is better understood.

From (3-3), the current rise time is influenced by $R_{g(ext)_L}$, $R_{g(int)_L}$, C_{gs_L} , V_{dr} , V_{th} , g_m and I_o . From (3-5), the impact factors for voltage fall time are $R_{g(ext)_L}$, $R_{g(int)_L}$, C_{gd_L} , V_{dr} , V_{DC} , g_m and I_o . Table 3-2 summarizes the trend of t_{cr} and t_{vf} when these factors increase. Remarkably, among these factors, I_o , V_{DC} , V_{dr} and $R_{g(ext)}$ are determined by the external circuit and are tunable. The remaining factors are purely determined by the device itself.

To improve the switching loss, the overlap time needs to be reduced. However, the parasitics, especially the loop inductance, limit the ability for enhancing the switching speed.

As has been mentioned in Section 2.1.2, the di/dt and dv/dt of the MOSFET during switching transient increase when the switching speed increases. As a result, the overvoltage across the switch gets higher owing to the influence from the device parasitic capacitance and the loop inductance.

Table 3-2. Factors that influence the switching time

| Factor | Trend when the factor increases | |
|----------------|---------------------------------|-----------|
| | t_{cr} | t_{vf} |
| I_o | Increase | Increase |
| V_{DC} | No change | Increase |
| V_{dr} | Decrease | Decrease |
| $R_{g(ext)_L}$ | Increase | Increase |
| $R_{g(int)_L}$ | Increase | Increase |
| C_{gs_L} | Increase | No change |
| C_{gd_L} | No change | Increase |
| V_{th} | Increase | Increase |
| g_m | Decrease | Decrease |

For the device gate loop, the cross-talk occurs due to the displacement current flowing through gate resistance caused by the drain-gate dv/dt during the switching transient. Fortunately, several methods have been proposed to attenuate the phenomenon according to the review in Section 2.1.2. Simple auxiliary circuits can be implemented with low cost and easy control.

The drain-source overvoltage is a more severe and challenging issue that prevent an increase of switching speed. To prevent the switch from damage, snubbers have to be added or the switching speed has to be slowed. In terms of snubbers, it not only increases the loss but also makes the power stage more complicated and less reliable. In Fig. 3-3, it is observed that the overvoltage occurs on v_{ds_H} when the lower MOSFET is turned on, and on v_{ds_L} when the lower MOSFET is turned off. According to the review in Section 2.1.2, the turn-on overvoltage on v_{ds_H} and the turn-

off overvoltage on v_{ds_L} have different mechanisms. However, both of these two types of overvoltage are strongly dependent on the di/dt and dv/dt of the switch [18], [66].

3.1.2 Influence of Different Current Ratings

The switching performance of the devices with the same semiconductor technology but different current ratings can be different. Assuming a low current rating discrete device and a high current rating power module use the same die technology, the module can be ideally regarded as paralleling N discrete devices as shown in Fig. 3-4, and has N times higher rated current.

Fig. 3-5 shows the comparison of di/dt and dv/dt between the discrete device and the power module. If the applied gate drives have enough driving capability in both cases, the gate current for each die in the module should be the same as for the discrete device. Thus, the current rise time of the discrete device and the power module is identical at rated current condition. As a result, the power module shows N times higher di/dt than the discrete device. On the other hand, if the applied bus voltage is the same, the power module has the same dv/dt as the discrete device because both the gate current and the transfer capacitance is N times higher. This di/dt difference brings about significantly different parasitic effect. Generally, it is more difficult for the power module with higher power rating and higher di/dt to increase the switching speed. Characterization of SiC Discrete Device and Power Module

3.1.3 Testing Setup

Since the body diode reverse recovery is not significant for SiC MOSFETs, FET/FET cell configuration is used for characterizing the devices with the same die technology but different current ratings. One discrete device and one power module utilizing the state-of-the-art die and packaging technology are selected to test, and the parameters are listed in Table 3-3. As shown,

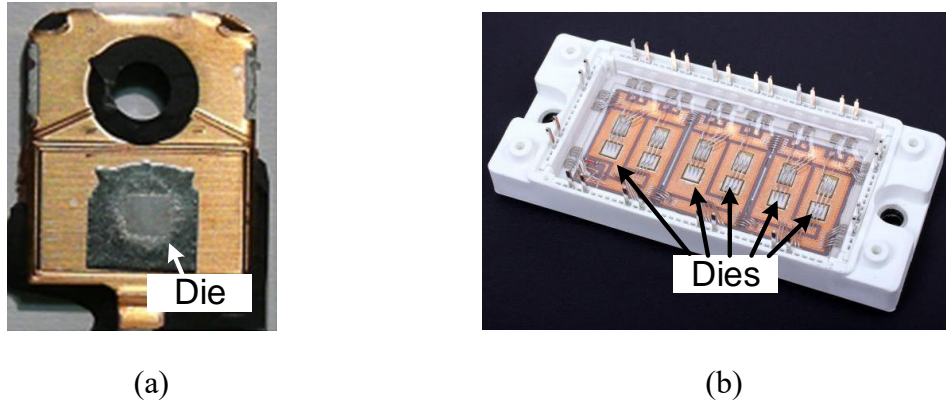


Fig. 3-4. Dies in discrete device and power modules. (a) Discrete device. (b) Power module.

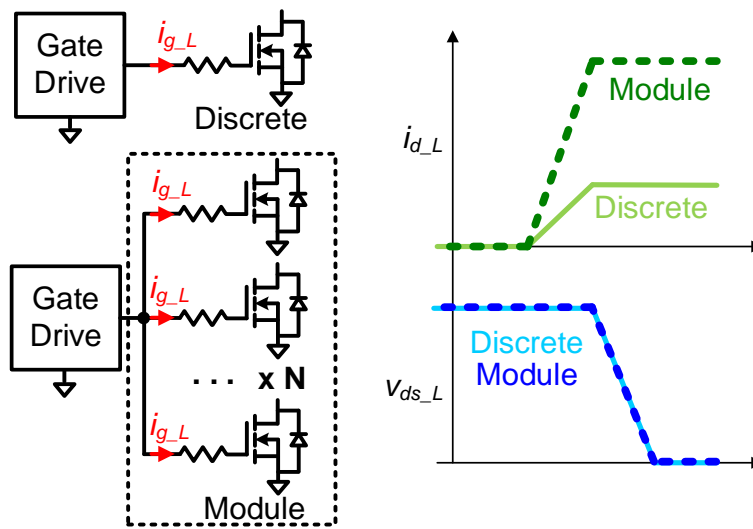


Fig. 3-5. Ideal di/dt and dv/dt comparison between discrete device and power module.

the power module has much higher current rating as well as lower on-resistance and internal gate resistance. Because of the current rating and packaging variation, different testing setups have to be adopted. For both setups, 500 V is used as the DC bus voltage.

Table 3-3. Parameters of tested discrete device and power module

| | Discrete | Module |
|----------------------------|---------------------|------------------------|
| Manufacturer | Wolfspeed | Wolfspeed |
| Packaging | TO-247 4pin | High Performance 62 mm |
| Die | 3 rd Gen | 3 rd Gen |
| V_{br} (V) | 1200 | 900 |
| I_d (A) | 30 | 880 |
| $R_{ds(on)}$ (m Ω) | 75 | 1.25 |
| $R_{g(int)}$ (Ω) | 10.5 | 0.2 |
| C_{oss} (pF) @500 V | 65 | 2800 |

3.1.3.1 Discrete Device

Fig. 3-6 demonstrates the DPT board for discrete devices. Note that the bulky DC-link capacitors are located on a dedicated board and connected with the device under test (DUT) through short wires so that one capacitor board can be used to test multiple switching cells. Fig. 3-7 shows the established testing platform.

3.1.3.2 Power Module

The module used here is illustrated in Fig. 3-8, which has a half bridge structure containing two MOSFETs. Since the peak current of the module is more than 800 A, the current shunt used in discrete device case is no longer suitable due to the high loss. Among different current measurement methods, Rogowski coil is a good candidate without introducing extra loss or PCB size increase [136]. The Rogowski coil from CWT can provide 30 MHz bandwidth with 35 ns rise time capture capability, which is sufficient for the current measurement here [137]. From Fig. 3-8,

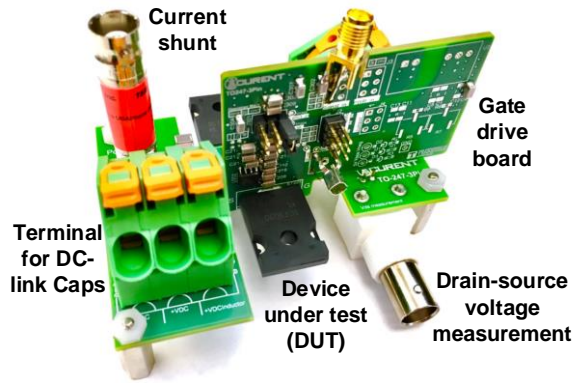


Fig. 3-6. Double pulse testing board.

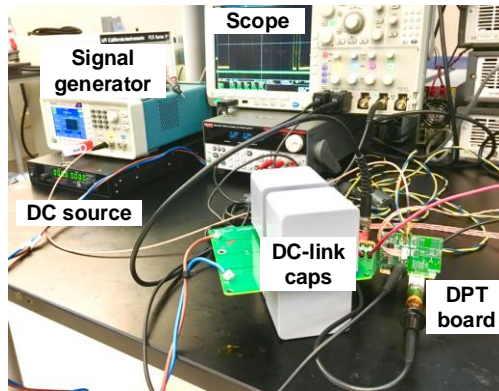


Fig. 3-7. Testing platform of double pulse test.



Fig. 3-8. Tested power module.

there are three screw holes for each switch terminal. Thus, three Rogowski coils are implemented to measure the total current of the module.

To achieve thermal balance and avoid dynamic overshoot, the current distribution should be balanced among the paralleling dies inside the module. Fig. 3-9 draws two types of layout design of the DPT. With Fig. 3-9(a), the DC-link capacitors are located at one side of the module.

The testing setup and current waveforms from the three Rogowski coils are shown in Fig. 3-10 and Fig. 3-11, respectively. Remarkably, there is large current unbalance among the three Rogowski coils, which indicates that the drain current is not evenly distributed inside the module.

Fig. 3-12 and Fig. 3-13 show the DPT boards and the testing platform following the layout 2 in Fig. 3-9(b). The DC-link capacitors are placed symmetric to the power module, which helps achieve the current balance. Fig. 3-14 shows the tested drain currents. Compared to Fig. 3-11, the current balance is significantly improved. The tested inductance of the DPT power loop is 10 nH.

3.1.4 Experimental Results

Fig. 3-15 illustrates the tested switching waveforms of the discrete device at 30 A with no external gate resistance. The overvoltage of the upper MOSFET during turn-on is 106 V above the DC bus voltage (500 V) while that of the lower MOSFET during turn-off is 101 V. Since the voltage rating of the device is 1.2 kV, it means that even with the lowest external gate resistance, there is still large room to accelerate the switching speed without exceeding the breakdown voltage of the tested SiC MOSFET.

On the other hand, it is shown in Fig. 3-16 that with 1.4 Ω external gate resistance, the overvoltage is much larger for the power module, namely 438 V for the upper MOSFET and 362 V for the lower MOSFET when the load current is 800 A. In such case, the drain-source voltage

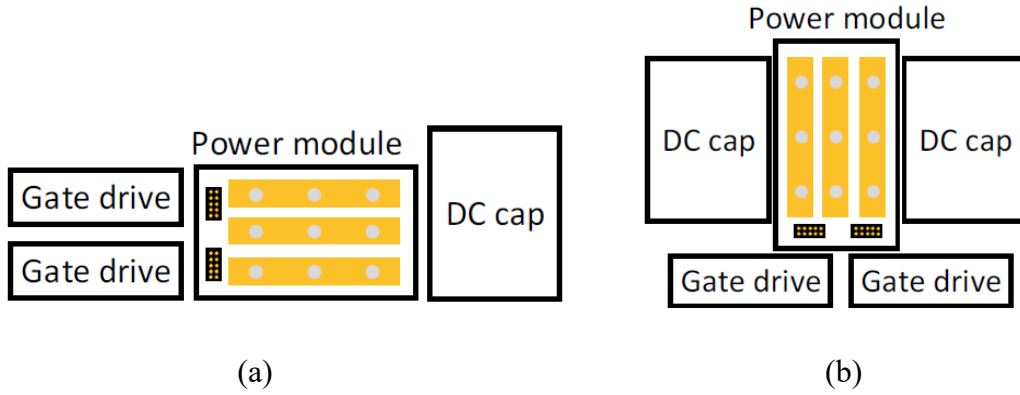


Fig. 3-9. DPT layout for power module. (a) Layout 1. (b) Layout 2.

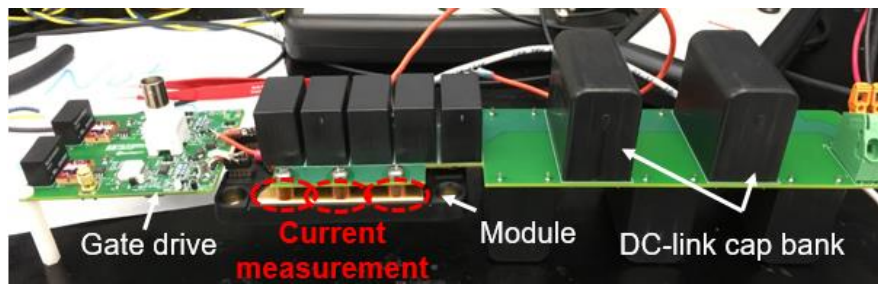


Fig. 3-10. Testing setup with layout 1.

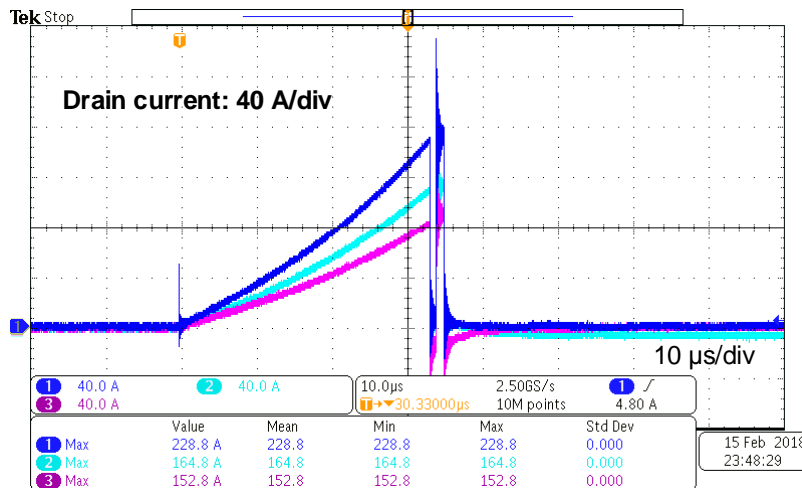


Fig. 3-11. Drain current distribution with layout 1.

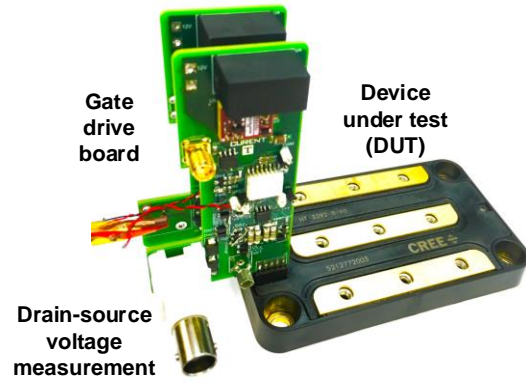


Fig. 3-12. Gate drive for power module.

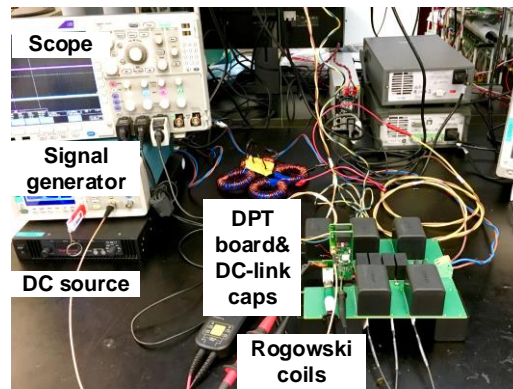


Fig. 3-13. Testing setup with layout 2.

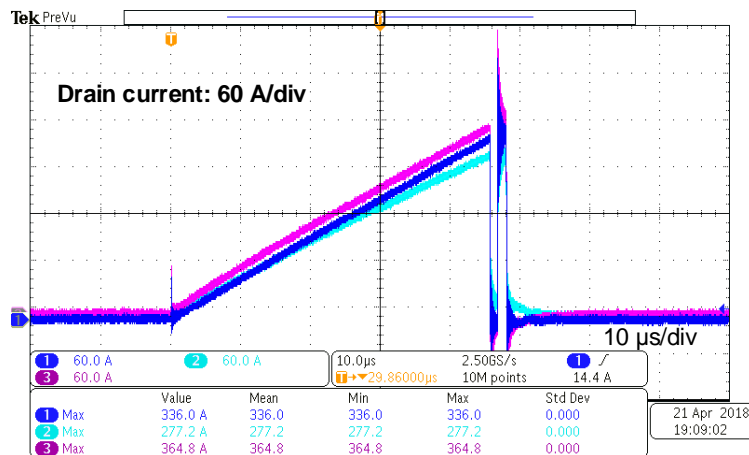


Fig. 3-14. Drain current distribution with layout 2.

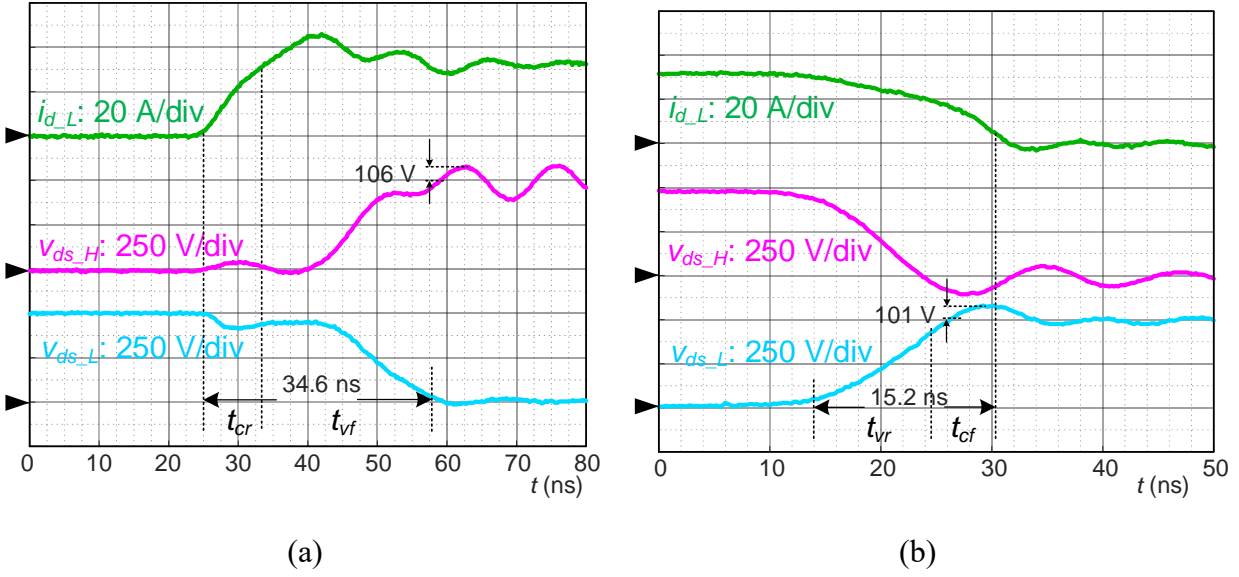


Fig. 3-15. Tested switching waveforms of discrete device when $V_{DC}=500$ V, $I_o=30$ A and $R_{g(ext)_L}=0$ Ω . (a) Turn-on. (b) Turn-off.

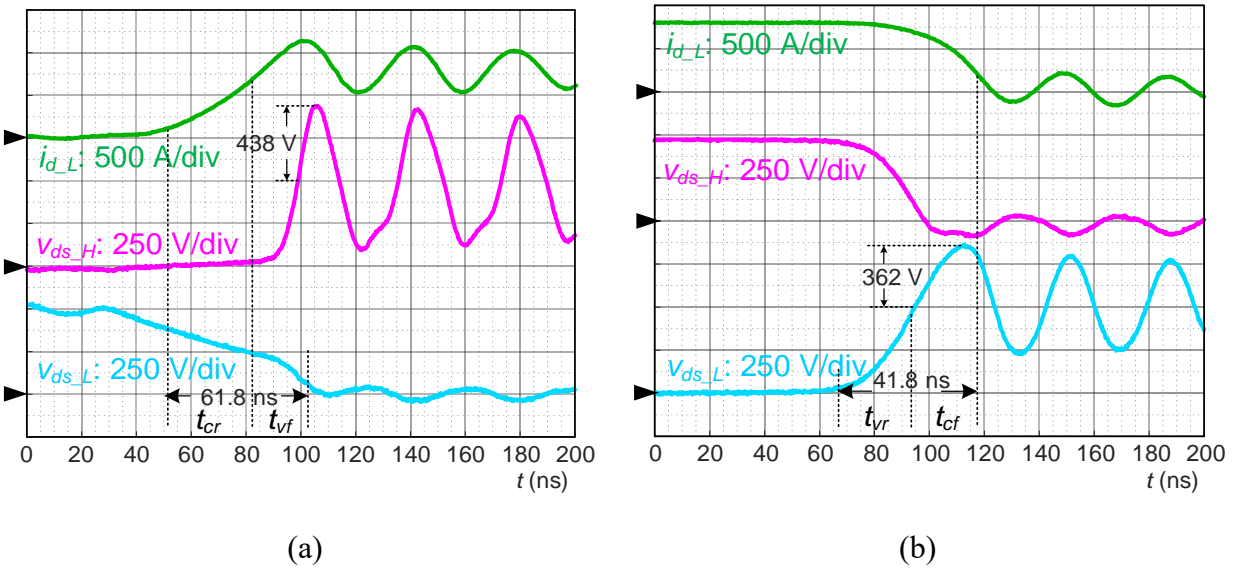


Fig. 3-16. Tested switching waveforms of power module when $V_{DC}=500$ V, $I_o=800$ A and $R_{g(ext)_L}=1.4$ Ω . (a) Turn-on. (b) Turn-off.

of the MOSFETs already approaches their voltage rating (900 V). Therefore, the switching speed cannot be further increased.

Fig. 3-17 plots the relationship between the overvoltage during the switching transient and the applied external gate resistance of the discrete device and the power module at full load condition. Clearly, the power module shows higher overvoltage for both the upper and lower MOSFETs. As the external gate resistance decreases, the overvoltage of the power module increases more rapidly, which is due to its lower internal gate resistance.

Fig. 3-18 and Fig. 3-19 illustrate di/dt and dv/dt versus the applied external gate resistance of the discrete device and the power module at full load condition. The power module exhibits a much higher di/dt that contributes to the higher overvoltage. The dv/dt of the discrete device and power module are similar, which matches with the previous analysis in Section 3.1.2.

3.1.5 Analysis and Discussion

3.1.5.1 Discrete Devices

From the above testing results, there is still much room to increase the switching speed of the discrete device. It is desired to understand the inherent bottleneck for further increasing the switching speed during the switching transient.

In Fig. 3-15, it is observed that the turn-on switching time is 34.6 ns while the turn-off switching time is 15.2 ns at full load condition. From the turn-on waveforms in Fig. 3-15(a), the voltage fall time is dominant and accounts for 3/4 of the total turn-on time. Thus, the voltage falling process is worth analyzing in detail.

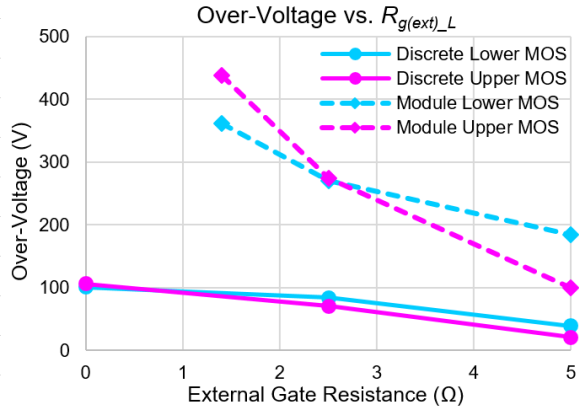


Fig. 3-17. Comparison of tested overvoltage between discrete device and power module.

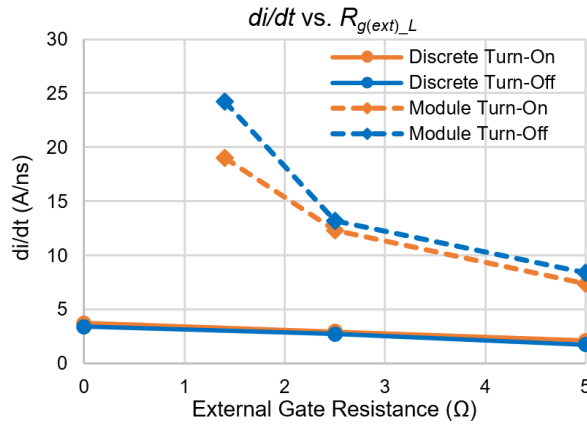


Fig. 3-18. Comparison of tested di/dt between discrete device and power module.

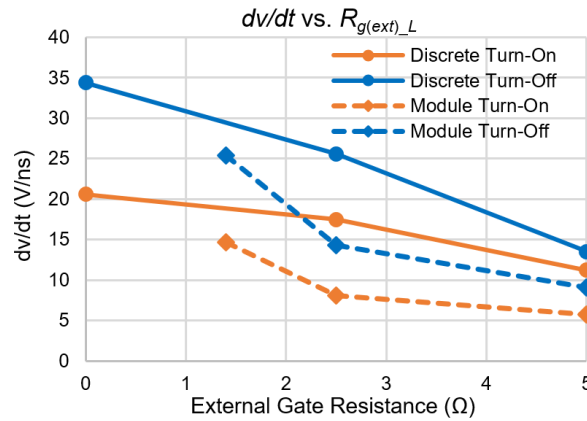


Fig. 3-19. Comparison of tested dv/dt between discrete device and power module.

According to (3-5), for a certain device, the voltage fall time is mainly impacted by the gate current during the Miller plateau. Based on the analysis in Section 3.1.1, the gate current during Miller plateau is expressed as

$$I_{g-L} = \frac{V_{dr} - V_{th} - \frac{I_o}{g_m}}{R_{g(int)-L} + R_{g(ext)-L}} \quad (3-8)$$

Fig. 3-20 presents the tested transfer characteristics of the two devices with 500 V DC bus voltage. Lower transconductance contributes to higher Miller voltage, which is 9 V for the SiC MOSFET and 4.5 V for the Si CoolMOS when the load current is 30 A as shown in Fig. 3-20. As a result, the discharging current for the transfer capacitance is much smaller in the SiC MOSFET.

In addition, the internal gate resistance of discrete SiC devices is usually large due to the gate oxide reliability issue. Low g_m and high $R_{g(int)-L}$ contributes to low gate current during the Miller plateau. In consequence, the voltage across the transfer capacitance drops slowly with this gate current even without any external gate resistance, and the voltage fall time dominates the turn-on time. Therefore, the key point to improve the switching speed of the SiC discrete devices is to enhance the gate current provided by the gate drive.

3.1.5.2 Power Modules

From the testing results in Fig. 3-16 the switching speed of the power module with high current rating is limited by the drain-source overvoltage resulting from the higher di/dt and the parasitics in the switching loop. Without further improving the layout and achieving lower parasitics, the existing VSG technology is sufficient to maximize the switching speed of power modules with large current rating. Thus, the main focus of increasing the switching speed of the

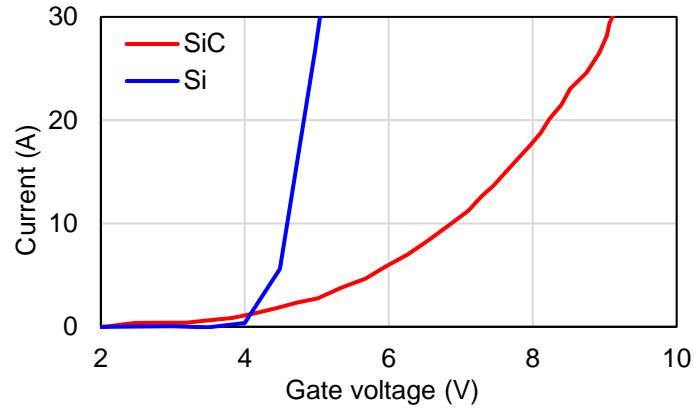


Fig. 3-20. Tested transfer characteristics when $V_{ds}=500$ V.

SiC power module is to reduce the voltage overshoot by introducing some advanced control strategies or optimizing the layout design.

3.2 Conclusion

To understand the key impact factors that limit the switching speed of SiC MOSFETs in hard switching applications, switching characterization is conducted and evaluated with double pulse tests.

First, two switching cell configurations are investigated to compare the switching transients of a SiC MOSFET and a Si CoolMOS with same voltage and current ratings. The testing results show that if the reverse recovery of device body diode can be neglected, the SiC MOSFET has higher switching loss and longer switching time with the same applied gate drive circuits. The turn-on time is longer than the turn-off time, and the voltage fall time is dominant during the turn-on transient. This is mainly due to the lower intrinsic transconductance of SiC MOSFETs and the consequential lower gate current to discharge the transfer capacitance and change the drain-source voltage of the device.

Second, the switching transients of a low current SiC discrete device and a high current SiC power module are tested. For the high current power module, detailed design including the testing setup layout, de-sat protection, and cross-talk suppression circuits are introduced. The results show that the constraints limiting the switching speed for the discrete device and the power module are different. There is still plenty of room to improve the switching speed for the discrete device even when the external gate resistance is reduced to zero, which means the conventional voltage source gate drive cannot maximize the switching speed. The reason is still the low transconductance and the limited gate current. Therefore, gate drives with stronger gate current capability are required to further improve the switching speed of the SiC discrete devices. On the other hand, the power module suffers from high overvoltage caused by the loop parasitics due to higher di/dt . Thus, the key points to enhance the switching speed of the SiC power module are developing control strategies to mitigate the device overvoltage and optimizing the power loop layout to reduce parasitic inductances.

4 Current Source Gate Drive

This chapter presents a current source gate drive (CSG) designed for SiC discrete MOSFETs that can increase the switching speed and reduce the switching loss. First, the limitation of the existing voltage source gate drives (VSG) and CSG are analyzed, and the requirements of the gate drive technology for SiC discrete devices are concluded. Based on the requirements, a CSG dedicated for SiC discrete MOSFETs that can avoid the influence from the large internal gate resistance is proposed, and its operation principle is analyzed in detail. Both the switching and gate drive loss calculations are presented and compared with the conventional VSG to show the superiority of the CSG, and the key parameters design procedure is given. Moreover, the benefits as well as the challenges of applying the proposed CSG is summarized. The effectiveness of the CSG is verified with experimental results.

This part of work is published or accepted in the journal and conference papers [135], [138].

4.1 Limitations of Existing Gate Drives

According to the analysis of Section 3.1.5.1, the key factor that limits the switching speed of SiC discrete devices is the relatively low gate current during the voltage fall time, which results from the low transconductance and high internal gate resistance. Therefore, a gate drive with stronger gate current ability is needed. In this section, VSG is first evaluated to see if it can improve the switching speed since it is the most widely adopted gate drive technology. Then CSG is also analyzed as an alternative candidate.

4.1.1 Voltage Source Gate Drive

From (3-8), the only two factors that can be manually tuned are the gate drive supply voltage V_{dr} and the external gate resistance $R_{g(ext)_L}$. Unfortunately, V_{dr} is limited by the SiC MOSFET gate

voltage rating, which is typically around 20 V. On the other hand, even though $R_{g(ext)_L}$ is reduced to be zero, the large internal gate resistance still exists. As a result, it is difficult to increase the gate current during Miller plateau with conventional VSGs. Therefore, CSG is a better candidate because of its ability to enhance the gate current independently. With the same gate charge, CSGs can provide constant current during the switching transient and hence reduce the switching time, especially the voltage fall time.

4.1.2 Current Source Gate Drive

As shown in Fig. 4-1, the required CSG should be able to provide constant current during the switching transient, especially during voltage fall time to reduce the gate charging/discharging time. Nevertheless, the existing CSG topologies cannot necessarily provide a constant current for discrete SiC devices with large internal gate resistance. When the gate current flows, large voltage drop occurs across the internal gate resistance. According to (3-2), the gate-source Miller voltage is only related to threshold voltage V_{th} , transconductance g_m and load current I_o . Thus, the gate-source voltage during the Miller plateau does not change with a CSG and is still relatively high. As a result, to keep the current constant, the external gate voltage $v_{gs(ext)}$ is likely to be higher than the gate drive supply voltage V_{dr} . For the existing CSGs containing a constant current source (CCS) as shown in Fig. 4-2, there always exists a MOSFET or BJT between the gate drive supply voltage and the gate external voltage. In consequence, $v_{gs(ext)}$ is clamped by V_{dr} and the CSG will lose current control.

For example, a typical CSG topology in [51] is used to simulate for a SiC MOSFET with 5 Ω internal gate resistance, and the result is shown in Fig. 4-3. The constant current ends when the external gate voltage approaches to V_{dr} and before v_{ds} starts to drop. Then the CSG becomes a classical VSG. With such a CSG, the reduction of switching time is significantly limited, which is

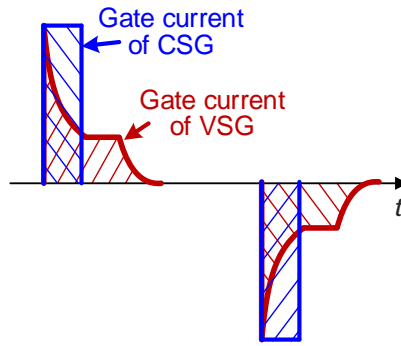


Fig. 4-1. Comparison of gate current between CSG and VSG.

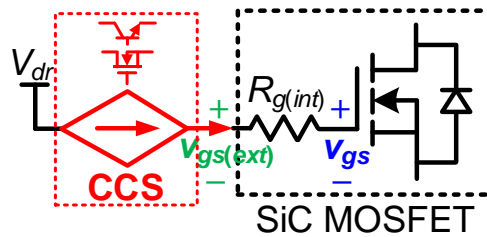


Fig. 4-2. Configuration of CSG with constant gate current.

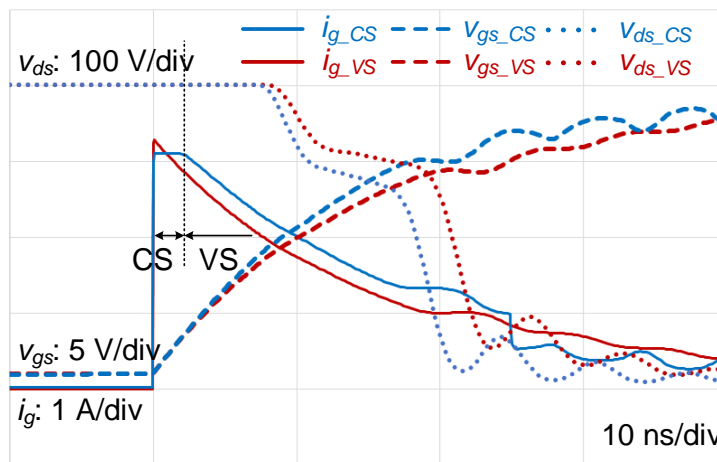


Fig. 4-3. Simulation waveforms of switching transient with existing CSG and VSG.

only 2.5 ns in Fig. 4-3. Therefore, it is desired to develop a CSG that can keep constant gate current during the switching process regardless of the large internal gate resistance for discrete SiC devices.

In conclusion, the basic requirements for the desired CSG should have two key functions. 1) During the switching transient, the CSG can keep CCS regardless of large internal gate resistance. External gate voltage can be higher than gate drive supply voltage. 2) After the switching transient ends, the CSG can actively change to VSG to protect the gate voltage from over-charging/discharging.

4.2 Proposed Current Source Gate Drive

4.2.1 Topology and Operating Principles

Based on the requirements summarized above, Fig. 4-4 shows the proposed CSG for SiC discrete devices [138]. One P-channel MOSFET S_1 , one N-channel MOSFET S_4 , two bidirectional switches S_2 & S_3 and one inductor L are included in the gate drive. Note that S_1 - S_4 are low voltage switches and have small footprints.

During one typical switching period, there are eight modes. The key waveforms are illustrated in Fig. 4-5, which include the gate signals of switches S_1 - S_4 , the inductor current i_L , the gate current i_g , the external and real gate-source voltage $v_{gs(ext)}$ and v_{gs} , the drain-source voltage v_{ds} , and drain current i_d . The equivalent circuit in each mode during the turn-on transient is plotted in Fig. 4-6, and the modes are briefly explained as follows.

1) Subinterval 1 (t_0 - t_1): *Pre-charging state*. Before t_0 , only S_2 is on, and the SiC MOSFET is in the off state. At t_0 , the P-channel MOSFET S_1 is turned-on so the inductor is charged by V_{dr} , and the inductor current i_L increases linearly. This mode aims to build the current required for charging the gate, and the current at t_1 is

$$I_L(t_1) = \frac{V_{dr}}{L}(t_1 - t_0) \quad (4-1)$$

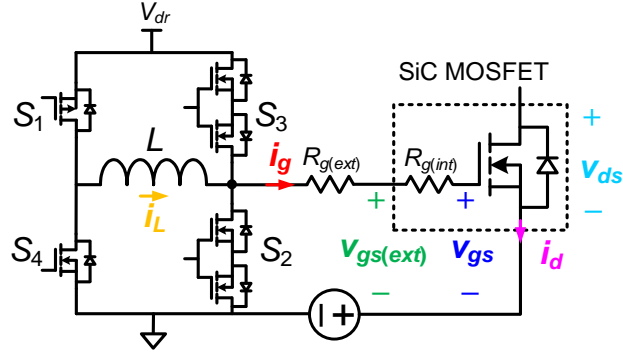


Fig. 4-4. Circuit of proposed CSG for discrete device.

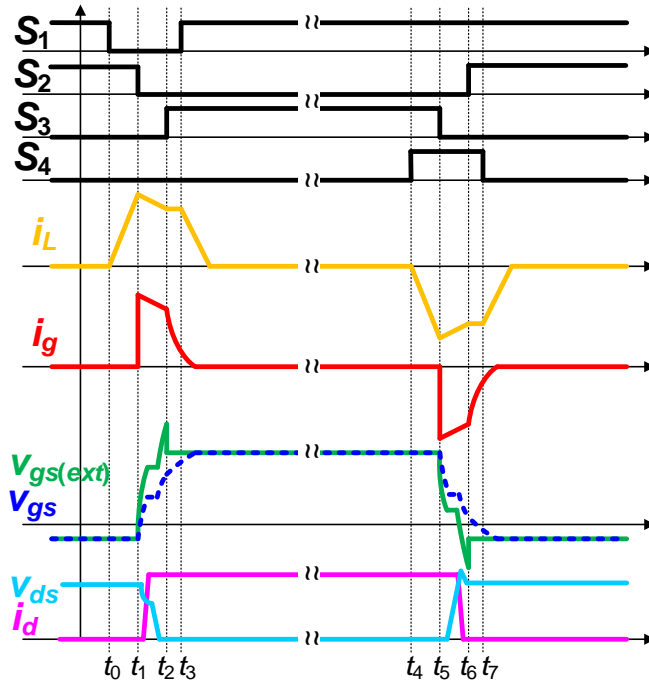


Fig. 4-5. Operation waveforms of proposed CSG.

Therefore, the initial gate current can be tuned by changing t_1 and selecting the proper inductance for L .

2) Subinterval 2 (t_1 - t_2): *Gate charging state*. At t_1 , the bi-directional switch S_2 is turned-off so the inductor current flows through the gate resistance and charges the gate capacitance C_{gs} of the

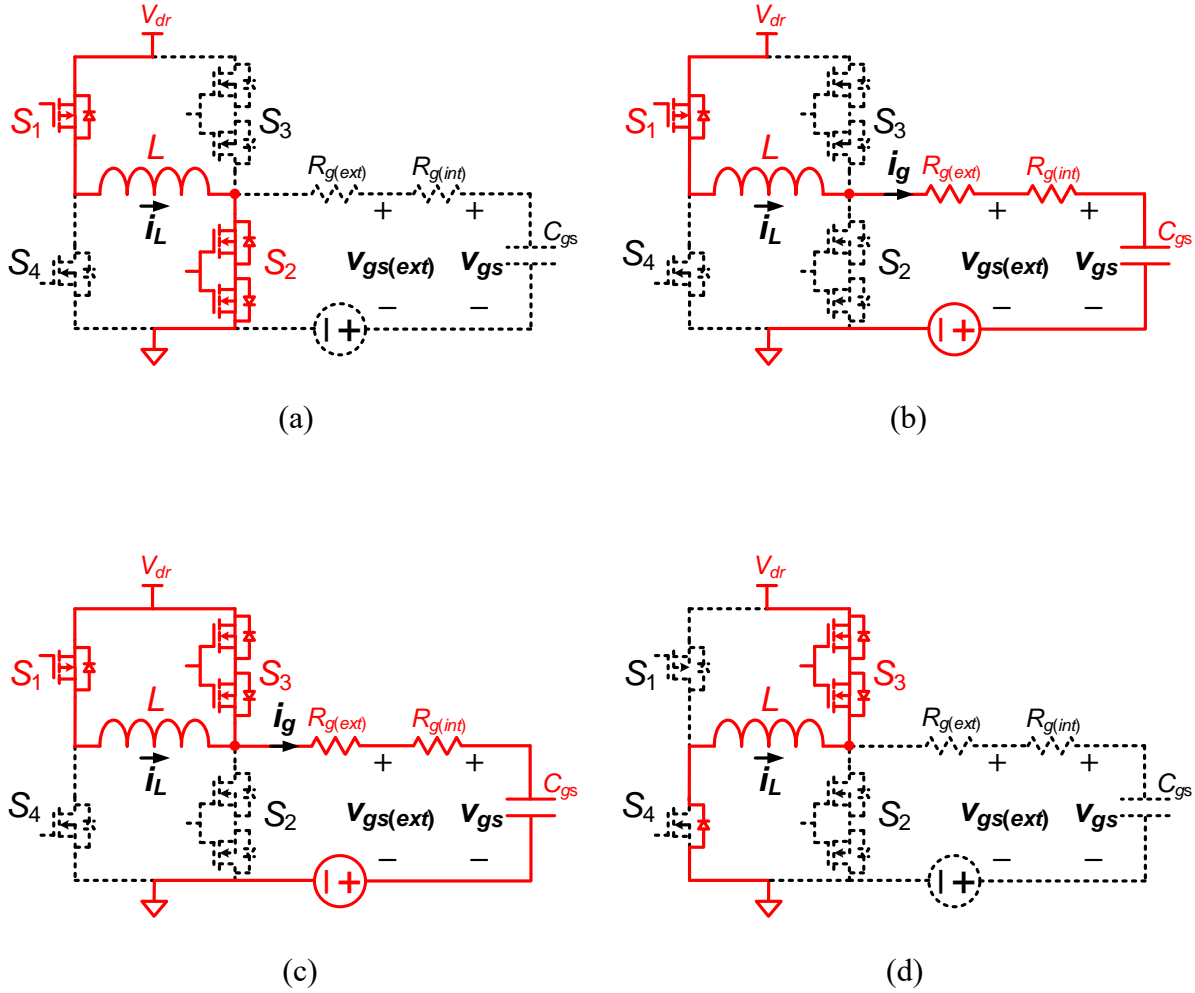


Fig. 4-6. Equivalent circuits in different operation subintervals of proposed CSG.

(a) Subinterval 1. (b) Subinterval 2. (c) Subinterval 3. (d) Subinterval 4.

SiC MOSFET. L , $R_{g(ext)}$, $R_{g(int)}$ and C_{gs} form an LCR resonant network. During the short time interval of this mode, the inductor current i_L does not change much so the gate can be regarded as charged by a current source. The switching transient of the SiC MOSFET completes in this mode so the switching time, especially the voltage fall time, is reduced compared to a conventional VSG.

Note that due to the internal gate resistance, the external gate voltage $v_{gs(ext)}$ is always higher than the real gate voltage v_{gs} . In order to keep the current source during this mode, the bi-directional

switch S_3 should be in off state so that $v_{gs(ext)}$ can be higher than V_{dr} . If a simple N-channel MOSFET is adopted for S_3 , the body diode of S_3 conducts when $v_{gs(ext)}$ approaches to V_{dr} and $v_{gs(ext)}$ is clamped. In such case, the gate drive automatically changes to be a VSG, and the gate current decreases rapidly like Fig. 4-3. Therefore, a bi-directional switch is necessary for keeping the current source. The relationship between external and real gate voltage is

$$v_{gs} = v_{gs(ext)} - i_g (R_{g(ext)} + R_{g(int)}) \quad (4-2)$$

3) Subinterval 3 (t_2 - t_3): *Free-wheeling state*. At t_2 , the bi-directional switch S_3 is turned-on, and $v_{gs(ext)}$ is pulled down to be V_{dr} . Then, the gate drive turns to be a conventional voltage source, and i_g reduces until the real gate voltage reaches V_{dr} . Note that the time to turn on S_3 is critical. If t_2 is too early, the transient has not finished, and the switching loss increases as i_g drops. Otherwise, if t_2 is too late, the constant current keeps charging and the gate voltage would be higher than the maximum rating, which damages the device. Therefore, the timing of turning on S_3 should be carefully selected, which is one of the challenges to implement this CSG. In this mode, i_L free-wheels through S_1 and S_3 and keeps constant. Since i_L in this mode contributes to nothing but loss, the time interval should be controlled to be as short as possible.

4) Subinterval 4 (t_3 - t_4): *Discharging state*. At t_3 , the P-channel MOSFET S_1 is turned-off and i_L flows through S_3 and the body diode of S_4 . The inductor is discharged by V_{dr} and i_L decreases linearly to zero, which means that the stored energy in L returns to the power supply of the gate drive without being wasted.

From t_4 , the turn-off transition starts, and the operation principle is similar to the turn-on transition.

4.2.2 Loss Analysis

The switching loss is the main target to reduce, and it is directly related to the switching time. So calculating the switching time based on the equations in Chapter 3 can indicate the switching loss. In addition, the gate drive loss should also be addressed.

4.2.2.1 Switching Loss

The basic switching time and loss calculation for the conventional VSG is analyzed in Section 3.1.1. The current rise time t_{cr} and voltage fall time t_{vf} are given by (3-3) and (3-5), respectively.

For the proposed CSG, assuming the gate current is constant, the current rise time can be expressed as

$$t_{cr(CSG)} = C_{gs} \frac{I_o}{g_m I_g} \quad (4-3)$$

The voltage fall time is

$$t_{vf(CSG)} = C_{gd} \frac{V_{DC}}{I_g} \quad (4-4)$$

Based on the above analysis, the turn-on time of a typical 1.2 kV, 30 A SiC MOSFET with 10.5 Ω internal gate resistance is plotted in Fig. 4-7. With the same initial gate current, it is observed that the current rise time and the voltage fall time with the proposed CSG decreases compared to the conventional VSG. Remarkably, the voltage fall time with the proposed CSG is independent of the load, while higher load current leads to longer voltage fall time for the conventional VSG. Therefore, the heavier the load is, the more turn-on time can be reduced. At full load condition, the total overlap time can be reduced by half, leading to significant switching loss reduction.

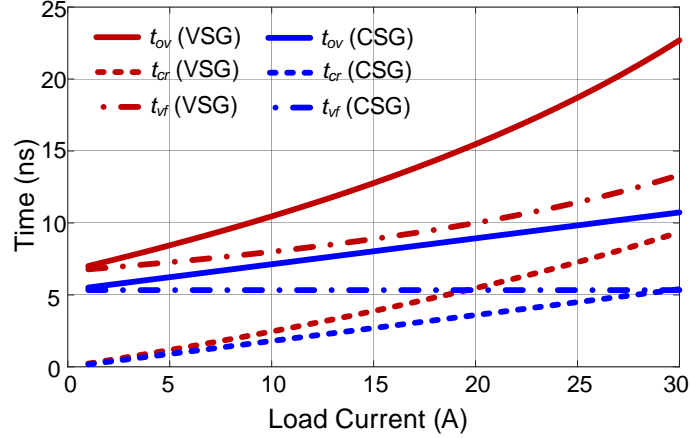


Fig. 4-7. Switching time comparison between VSG and CSG at different load conditions.

4.2.2.2 Gate Drive Loss

For the conventional VSG, the gate drive energy loss of each switching cycle is

$$E_{g(VSG)} = V_{dr} Q_g \quad (4-5)$$

where Q_g is the gate charge.

Since the gate current is discontinuous in one switching period and the switches S_1 - S_4 and inductor L in the CSG have low parasitics, the conduction loss, switching loss of the switches and the core loss of the inductor is negligible. Therefore, the gate drive energy loss of the proposed CSG is derived as

$$E_{g(CSG)} = \frac{1}{2} V_{dr} Q_g + (R_{g(ext)} + R_{g(int)}) I_g Q_g \quad (4-6)$$

With the same SiC MOSFET as in Fig. 4-7, the relationship between gate drive loss during one switching cycle and external gate resistance $R_{g(ext)}$ is plotted in Fig. 4-8. Due to the large internal gate resistance, the proposed CSG shows higher gate drive loss than the VSG. However, because of the superior intrinsic gate charge characteristic of SiC MOSFETs, the gate drive loss is

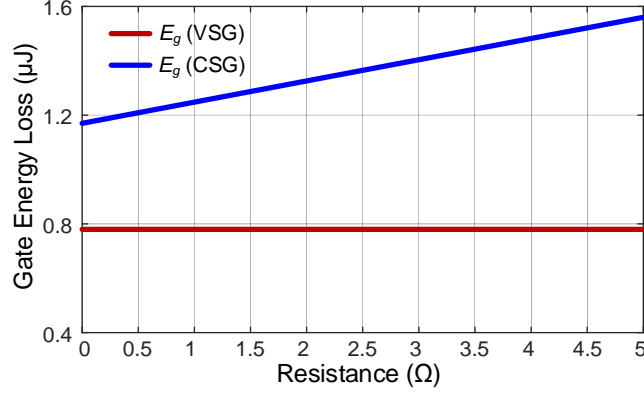


Fig. 4-8. Gate drive energy loss comparison between VSG and CSG with different external gate resistance.

much lower than the switching loss. So the higher gate drive loss of the proposed CSG does not impact the overall loss reduction.

4.2.3 Parameter Design

The key components in the proposed CSG circuit are the inductor L and the external gate resistor $R_{g(ext)}$. In terms of the control, the critical parameters are the inductor charging time t_{ic} (from t_0 to t_1 in Fig. 4-5) and the gate charging time t_{gc} (from t_1 to t_2 in Fig. 4-5).

As mentioned above, the CSG should keep constant current during the switching transient of the device. The gate charging time t_{gc} consists of two periods. From the start of the gate charging at t_1 in Fig. 4-5 to the end of the current rise, the equivalent circuit this period is illustrated in Fig. 4-9, which is a typical RLC series tank.

For such a typical second order system, the response of current can be written as

$$i_g(t) = \begin{cases} A_1 e^{-\alpha_0(\zeta + \sqrt{\zeta^2 - 1})t} + A_2 e^{-\alpha_0(\zeta - \sqrt{\zeta^2 - 1})t} & \zeta \geq 1 \\ B_1 e^{-\alpha t} \cos(\omega_d t) + B_2 e^{-\alpha t} \sin(\omega_d t) & \zeta < 1 \end{cases} \quad (4-7)$$

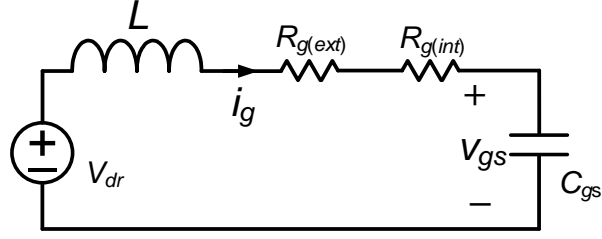


Fig. 4-9. Equivalent circuit of proposed CSG during gate charging.

where A_1 , A_2 , B_1 and B_2 are the coefficients related to the initial state. The damping ratio ζ , time constant α , angular resonance frequency ω_0 , and damped resonance frequency ω_d are:

$$\begin{aligned}\zeta &= \frac{R_{g(ext)} + R_{g(int)}}{2} \sqrt{\frac{C_{gs}}{L}} \\ \alpha &= \frac{R_{g(ext)} + R_{g(int)}}{2L} \\ \omega_0 &= \frac{1}{\sqrt{LC_{gs}}} \\ \omega_d &= \omega_0 \sqrt{1 - \zeta^2}\end{aligned}\tag{4-8}$$

Considering the over-damped case where L is small, the circuit is like a RC first order system. The RC time constant without external gate resistance is 89 ns for the discrete device in Table 3-3, which is too long for the gate charging time. Therefore, the RLC network should operate at under-damped condition where ζ is smaller than 1. The gate current can be derived as

$$i_g(t) = I_{g0} e^{-\alpha t} \cos(\omega_d t) + \frac{1}{\omega_d L} \left(V_{dr} - \frac{R_{g(ext)} + R_{g(int)}}{2} I_{g0} \right) e^{-\alpha t} \sin(\omega_d t)\tag{4-9}$$

where I_{g0} is the initial gate current.

When the drain current of the SiC MOSFET reaches the load current, the drain-source voltage begins to decrease. The gate voltage v_{gs} is clamped to the Miller voltage V_{mil} . In this period, the circuit becomes a RL first order system, and the gate current response can be derived as

$$i_g(t) = \left(I_{g1} - \frac{V_{dr} - V_{mil}}{R_{g(ext)} + R_{g(int)}} \right) e^{-2\alpha(t-t_{cr})} + \frac{V_{dr} - V_{mil}}{R_{g(ext)} + R_{g(int)}} \quad (4-10)$$

where I_{g1} is the gate current at the beginning of the voltage falling stage. When the drain-source voltage of the MOSFET drops to zero at t_2 , the switching transient ends and the proposed CSG should be changed to VSG. The inductor is shorted and the equivalent circuit becomes a RC first order system until the gate is fully charged.

The discrete SiC MOSFET in Table 3-3 is used to evaluate the parameter selection. The input capacitance C_{gs} is 1.35 nF. Still, the DC bus voltage is 500 V and the load current is 30 A. The gate drive supply voltage V_{dr} is 15 V and 5 Ω external gate resistance is adopted. According to Fig. 3-20, the Miller voltage V_{mil} is 9 V. With certain gate current, the current rise time and voltage fall time can be estimated by (3-3) and (3-5).

Assuming the required gate current is 1.5 A, the calculated gate currents during the switching transient with different inductance values are illustrated in Fig. 4-10. Higher inductance leads to lower current drop and is better from the perspective of maintaining constant current. However, higher inductance not only results in larger size, but also makes it more difficult to build the required initial gate current.

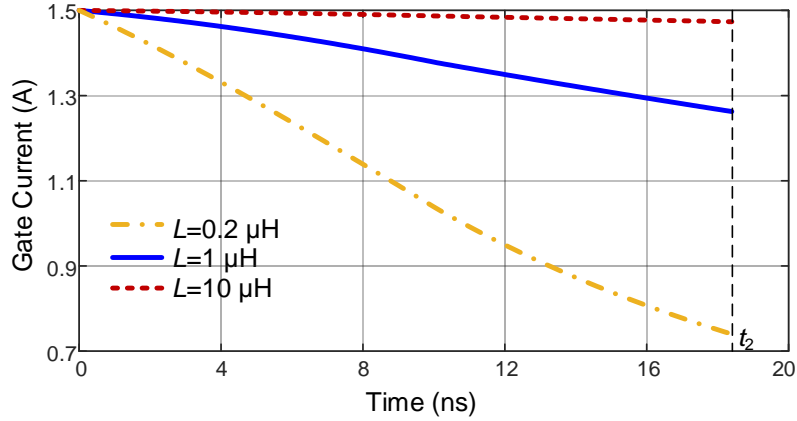


Fig. 4-10. Calculated gate current with different inductances.

Based on (4-1), with certain gate drive supply voltage, the required time to build the current is proportional to the inductance. As a result, the higher the inductance is, the longer it takes to initialize the gate current. Since the MOSFET cannot be turned on before the current reaches the required value, there is a maximum duty cycle limit for the proposed CSG. For the initial current of 1.5 A with the gate drive supply voltage of 15 V, assuming the maximum duty cycle is 0.95, the relationship between the allowed highest switching frequency and the inductance is demonstrated in Fig. 4-11. Notably, the allowed maximum switching frequency is lower than 100 kHz when the inductance is higher than 5 μH , while the frequency is lower than 50 kHz when the inductance is higher than 10 μH . Hence, lower inductance value is preferred for high switching frequency operation.

Considering the trade-off between keeping the current source and achieving high switching frequency, a moderate inductance should be selected for different applications. In this dissertation, the allowed current drop by the end of the switching transient is set to be less than 20%. Based on Fig. 4-10, a 1 μH inductor is chosen to provide 1.5 A gate current for the tested discrete SiC MOSFET.

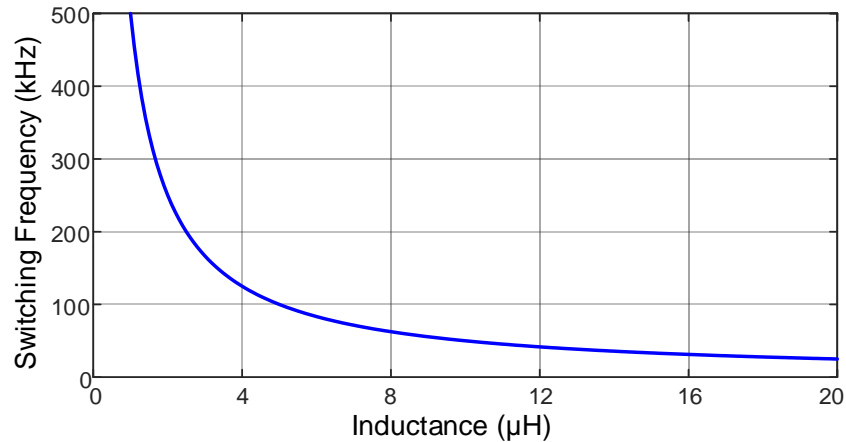


Fig. 4-11. Relationship between allowed maximum switching frequency and inductance.

4.2.4 Benefits and Challenges

Benefits: 1) The current source keeps the gate current at relatively high level during the switching transient. It shortens the long voltage fall/ rise time caused by the small transconductance and high Miller voltage of the SiC MOSFET with conventional VSG. As a result, the switching loss is significantly reduced.

2) The utilization of bi-directional switches enables constant current source during the whole switching transient and is suitable for discrete SiC MOSFETs with large internal gate resistance.

3) The gate current can be tuned by changing the pre-charging time. It provides the potential for more flexible and intelligent control strategies like di/dt and dv/dt control to better utilize and protect the SiC MOSFET.

4) The control of the switches turns the gate drive from current source to voltage source after the switching transient of the SiC MOSFET. The inductor and gate current keep at zero in steady state to eliminate circulating current and extra loss.

5) The stored energy in the inductor can return to the source of the gate drive after the switching transient, which avoids increasing the gate drive loss.

Challenges: 1) The introduction of the bi-directional switches disables the automatic change from CSG to VSG after the switching transient. Thus, the proposed CSG requires accurate time control to turn it to be VSG so that the gate is not over-charged/ discharged at different DC bus voltage and load conditions.

2) With the increased dv/dt , the overvoltage and cross-talk of the MOSFET during a switching transient increases. In addition, higher dv/dt can lead to higher noise and increase EMC. Therefore, the trade-off between switching speed, device reliability and noise should be balanced for real applications.

4.3 Experimental Results

The discrete SiC MOSFET from Wolfspeed in Table 3-3 is selected to test the proposed CSG. A conventional VSG is also tested with the same SiC MOSFET for comparison. The internal gate resistance of the MOSFET is 10.5Ω . To make a fair comparison, the power supply of both gate drives is $+15/-4 \text{ V}$. Zero external gate resistance is applied for the conventional VSG, and the gate current of the proposed CSG is set to be 1.4 A so that both gate drives have similar initial gate current.

Fig. 4-12 demonstrates the picture of the proposed CSG. It can be seen that the inductor is small and does not impact the size of the gate drive. A DPT is implemented to evaluate the switching performance of both gate drives, and a similar platform is adopted as shown in Fig. 3-7.

The tested gate-source voltage of S_1 to S_4 and gate inductor current i_L in the proposed CSG is plotted in Fig. 4-13. Compared with Fig. 4-5, it can match well with the theoretical analysis.

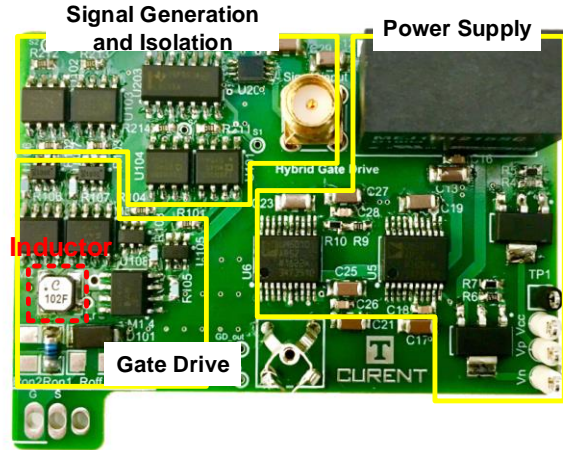


Fig. 4-12. Prototype of proposed CSG.

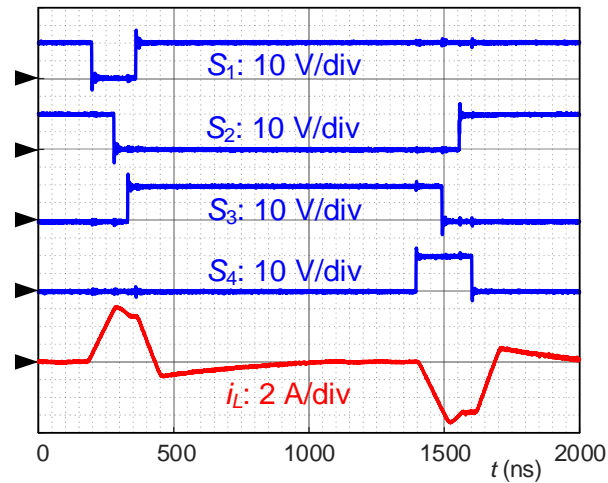


Fig. 4-13. Tested control signals of CSG.

Fig. 4-14 and Fig. 4-15 illustrate the tested switching waveforms of the instantaneous power, drain current and drain-source voltage with both gate drives at 500 V bus voltage and 30 A load current condition. Clearly, the switching time decreases with the proposed CSG during turn-on transient, and voltage fall time reduces significantly. From the shaded area of the instantaneous power, the turn-on loss has great improvement. The penalty is that because of the higher dv/dt , the overvoltage of the upper MOSFET increases from 106 V to 375 V. The turn-off loss and time also

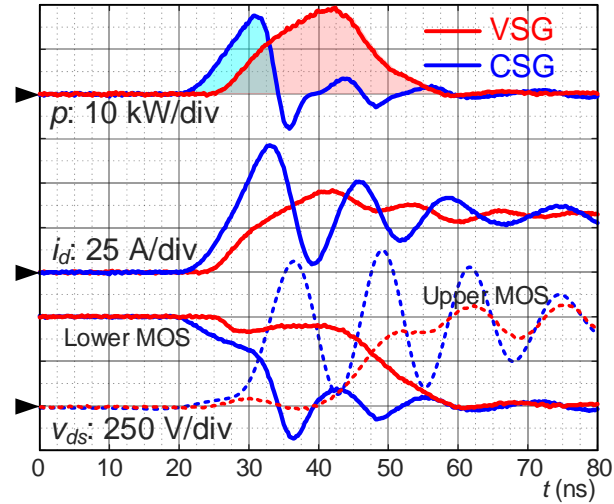


Fig. 4-14. Tested turn-on waveform of v_{ds} and i_d at 500 V, 30 A.

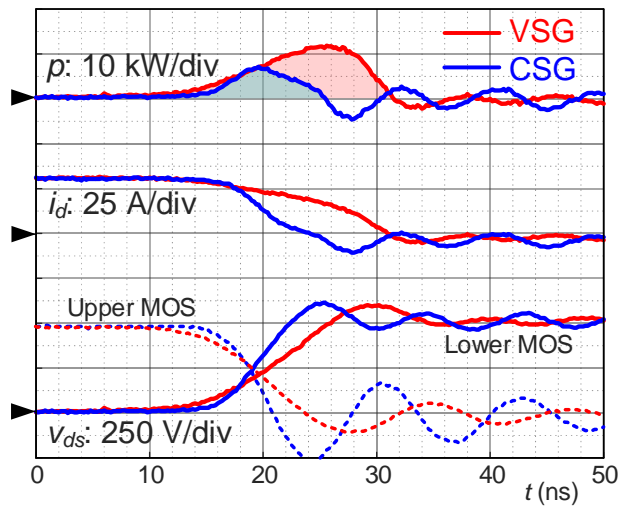


Fig. 4-15. Tested turn-off waveform of v_{ds} and i_d at 500 V, 30 A.

decrease with the proposed CSG but the overvoltage of the lower MOSFET does not increase. This is mainly because the displacement current during turn-off cannot exceed the load current. Thus, the voltage rise time is limited by the load current rather than the gate drive capability, which prevents the drain-source voltage from increasing.

The gate voltage and current waveform at 500 V bus voltage and 30 A load current condition with the proposed CSG is shown in Fig. 4-16. Due to the large internal gate resistance, the real gate voltage cannot be directly monitored. With the measured external gate voltage $v_{gs(ext)}$ and the gate current i_g , the real gate voltage can be calculated by (4-2) and is drawn as a blue dashed line. The inductor current i_L is also plotted for reference. Although the external gate voltage exceeds the maximum gate voltage of the MOSFET (+19/-8 V), the real gate voltage is beneath the limitation. However, the margin of gate voltage is very small due to the parasitic ringing. How to avoid the gate overvoltage, accurately control the gate drive to turn to voltage source, and protect the MOSFET can be an issue and requires more attention for the CSG.

Fig. 4-17 shows the tested switching time with the conventional VSG and the proposed CSG at different load conditions. From Fig. 4-17(a), the voltage fall time at full load with the proposed CSG is 6.8 ns while that with the conventional VSG is 25.6 ns. The total turn-on switching time decreases from 34.6 ns to 11.4 ns with the proposed CSG. In addition, Fig. 4-17(a) can match with the trend in Fig. 4-7, which verifies the theoretical analysis.

In Fig. 4-17(b), the turn-off switching time decreases from 15.2 ns to 7.6 ns at full load with the proposed CSG. Comparing the turn-on and turn-off time, the improvement in turn-on time is better due to two main reasons.

First, a negative voltage (e.g. -4 V) is supplied to the gate of the device during turn-off. Since the Miller voltage is relatively high as previously discussed, the gate current during the turn-off transient is higher than during the turn-on with the conventional VSG, which makes the turn-off process faster than the turn-on process.

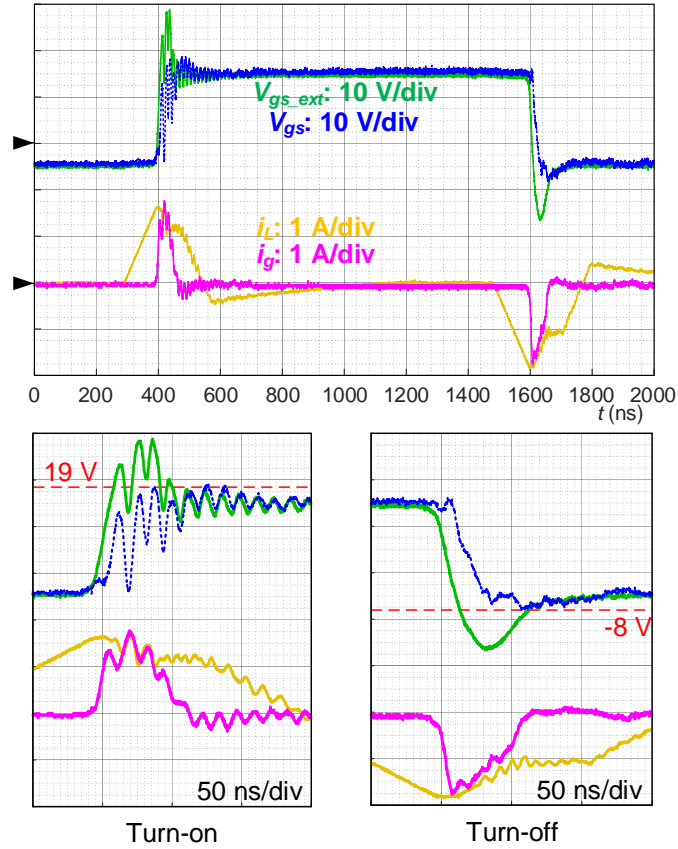


Fig. 4-16. Waveform of gate voltage and current with proposed CSG at 500 V, 30 A.

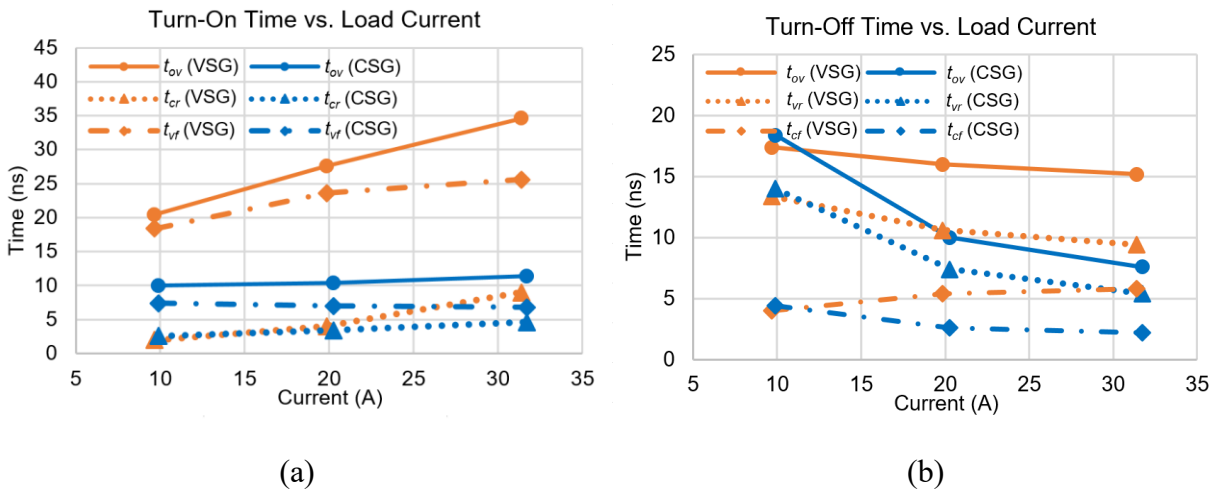


Fig. 4-17. Comparison of tested switching time at different load conditions.

(a) Turn-on. (b) Turn-off.

Second, the voltage rise time during the turn-off transient is influenced by not only the gate current charging the transfer capacitance, but also the load current charging the output capacitance. At light load condition, the voltage rise time is dominated by the load current instead of the gate current, so both drive technologies show similar voltage rise time in Fig. 4-17(b). As the load current increases, the voltage rise time with the conventional VSG is determined by the gate drive current. But for the proposed CSG with much higher gate current, the voltage rise time is still dominated by the load current. On the contrary, the voltage fall time during turn-on is independent of the load current with the proposed CSG, which is verified in Fig. 4-17(a) and can help to achieve larger turn-on time reduction. As a result, increasing gate current has more significant improvement for turn-on time than turn-off time.

Fig. 4-18 plots the switching loss at different load conditions. The switching loss with the proposed CSG at full load is $148 \mu\text{J}$, which is less than one third of the loss with the conventional VSG. The trend can match with the switching time curve in Fig. 4-17. Note that the switching loss with the proposed CSG can be further reduced by increasing the gate current as long as the overvoltage is within an acceptable range.

Fig. 4-19 presents the overall performance comparison between the conventional VSG and the proposed CSG. The smaller area means better overall performance, and the characteristics of the proposed CSG are normalized to 1. The proposed CSG can provide significantly shorter switching time and lower switching loss. The only drawback is the higher overvoltage especially on the upper MOSFET, which is the common trade-off to pursue higher switching speed in hard switching applications.

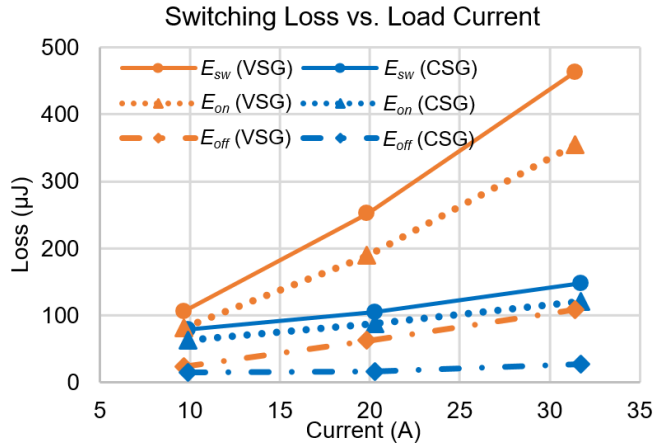


Fig. 4-18. Comparison of tested switching loss at different load conditions.

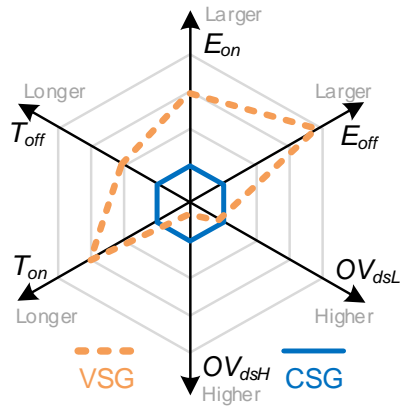


Fig. 4-19. Performance comparison between conventional VSG and proposed CSG.

4.4 Conclusion

To increase the switching speed of SiC discrete MOSFETs, it is desired to increase the gate current during the switching transient. However, due to the high Miller voltage and internal gate resistance of the discrete device, the gate current with the conventional VSG and existing CSG is limited, and the voltage fall time during turn-on transient is dominant.

By introducing a bi-directional switch to the gate drive circuit, a CSG is proposed that can achieve constant gate current during the whole switching transient regardless of the influence by the large gate resistance. The external gate voltage can be higher than the gate drive supply voltage without being clamped. After the switching transient, the CSG is controlled to turn to VSG to avoid the gate over-charge and discharge. The detailed operating principles and the design of parameters, especially the inductance, are discussed. There is a trade-off between keeping the constant gate current and realizing the fast response time of the CSG, and the parameters should be selected based on the application requirements.

A comparison is made between the conventional VSG and proposed CSG with double pulse tests. The results show that the turn-on and turn-off times are shortened by 67% and 50%, respectively, with the proposed CSG at full load condition. A switching loss reduction of 68% is achieved by the proposed CSG in comparison with the conventional VSG.

5 Charge Pump Gate Drive

This chapter presents a charge pump gate drive (CPG) designed for SiC discrete MOSFETs that can increase the turn-on switching speed and loss. First, the limitations of the proposed CSG in the last chapter are analyzed. The derivation of the proposed CPG is introduced in detail, and the operation principles are evaluated. The design procedure is given, and the switching and gate drive loss calculation is presented and compared with the conventional VSG to show the superiority of the CPG. In addition, the benefits as well as the challenges of applying the proposed CPG is summarized. The effectiveness of the CPG is verified with experimental results.

This part of work is published in the conference paper [139].

5.1 Limitation of Current Source Gate Drive

In the last chapter, a CSG that can keep the gate current constant throughout the switching transient is proposed. Nevertheless, it has the following constraints, which limits its implementation in real applications.

- 1) It requires accurate timing control to avoid the overcharging issue. In real applications, the switching time is influenced by the load current and bus voltage. As a result, the time to turn the CSG back to VSG has to be tuned, which is difficult to realize.

- 2) The CSG relies on an inductor to generate the required gate current. Although the inductor does not occupy much space on the PCB, it is difficult to be integrated into gate drive chips.

- 3) The required bi-directional switches as well as the inductor in the circuit make the gate drive complicated and difficult to be integrated.

In general, although the proposed CSG achieves considerable switching loss reduction, it is still desired to develop a gate drive circuit that can meet the compact, reliable and low cost requirements of the gate drives for SiC MOSFETs, especially for discrete devices. From device datasheets and the reported testing results, the turn-on loss is the dominant part in switching loss [52], [81], [128], [135], [140]. Therefore, turn-on loss is the main target to be reduced compared with the turn-off loss.

5.2 Proposed Charge Pump Gate Drive

5.2.1 Topology Derivation

Considering the switching process, there are two main requirements for the gate drive. First, it should provide sufficient gate current during the switching transient to shrink the switching time. Second, the gate voltage should be kept under the rating of the MOSFET in both transient and steady state. As mentioned above, the gate drive supply voltage cannot be too high mainly due to the second requirement. However, as shown in Fig. 5-1, the dynamic supply voltage v_p can be higher than the gate voltage rating during the switching transient since it takes time for gate voltage v_{gs} to increase. As long as v_p drops back to the normal value V_{dr} (lower than the gate voltage rating) before v_{gs} approaches V_{dr} , there is no risk of overcharging the gate.

In [37], [39], [141], [142], four-level gate drives (4LG) were adopted to achieve such function. A typical 4LG as well as its operating waveform are shown in Fig. 5-2. Two power supplies and two half-bridges provide four different gate drive voltages, namely V_p , $V_p - V_n$, 0 and $-V_n$. During the turn-on switching transient, V_p is used to enhance the turn-on speed. In steady state, the voltage drops to $(V_p - V_n)$.

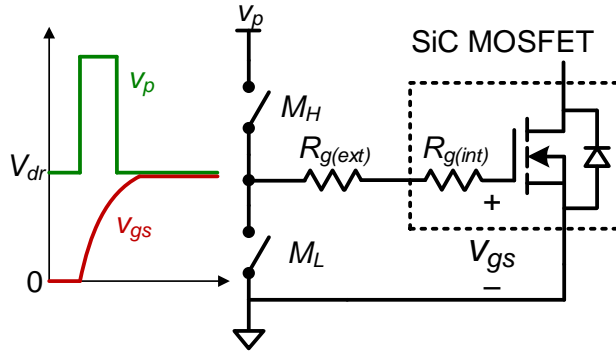


Fig. 5-1. Ideal supply voltage of gate drive.

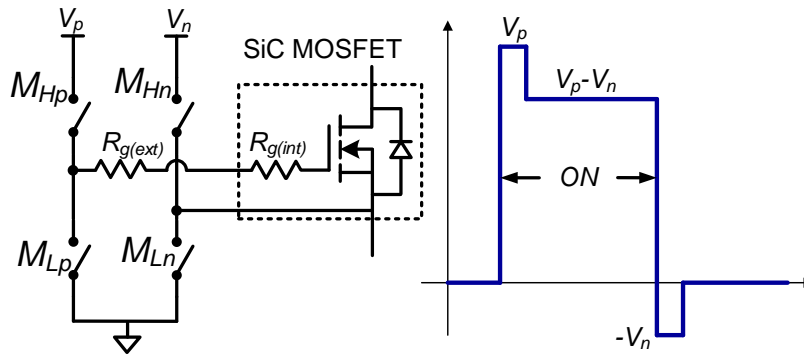


Fig. 5-2. Four-level gate drive circuit and operating waveform.

However, such 4LG has two drawbacks. First, due to the limited negative gate voltage rating, V_n (e.g. 5 V) is usually much lower than V_p (e.g. 20 V). As a consequence, the voltage enhancement during the turn-on transient is limited. To further increase the voltage, additional power supplies or transformers are required [39], which significantly increase the complexity and cost of the gate drive.

Second, the voltage shift from V_p to $(V_p - V_n)$ requires an accurate control signal to avoid gate overvoltage, which not only increases the complexity of the circuit, but also cannot adaptively fit for different load and bus voltage conditions, where the switching transient time changes.

Therefore, the required gate drive should have the ability to automatically change the voltage level and guarantee that the gate voltage is always lower than the rating.

With the aforementioned idea and requirements, Fig. 5-3 shows the proposed charge pump gate drive. It consists of two main parts: a charge pump circuit and a typical voltage source gate drive. The charge pump utilizes the flying capacitor structure, which consists of a pair of MOSFETs M_1 and M_2 , two diodes D_1 and D_2 , and two capacitors C_f and C_p . C_f is the flying capacitor while C_p is the charge-storage capacitor. The VSG is a totem-pole bridge including two MOSFETs M_H and M_L . $R_{g(ext)}$ is the external gate resistance, while $R_{g(int)}$ is the internal gate resistance. v_p is the voltage across C_p , which is also the gate drive output voltage. The power supply V_{dr} is connected with M_1 and M_2 . Another power supply V_n provides the required negative voltage across the gate-source during the OFF state.

5.2.2 Operating Principle

During one typical turn-on switching period, there are five modes, and the key waveforms are illustrated in Fig. 5-4, which includes the charge pump control signal S_c , gate drive output control signal S_g , the flying capacitor voltage v_f , the pump capacitor voltage v_p , the gate current i_g , the external and real gate-source voltage v_{gse} and v_{gs} . The equivalent circuit in each subinterval is plotted in Fig. 5-5, and the operation during the turn-on transient is briefly explained as follows.

1) Subinterval 1 (t_0 - t_1): *OFF steady state*. Before t_1 , both S_c and S_g are in low level, and M_2 and M_L are in ON state. In this state, both v_f and v_p equal to V_{dr} and do not change if the forward voltage drop of D_1 and D_2 is neglected. The gate drive output is low to keep the SiC MOSFET in OFF state.

2) Subinterval 2 (t_1 - t_2): *voltage pump state*. At t_1 , S_c changes to high level, and M_1 is turned on. As a result, D_1 conducts while D_2 is off. The flying capacitor C_f transfers energy to the charge-

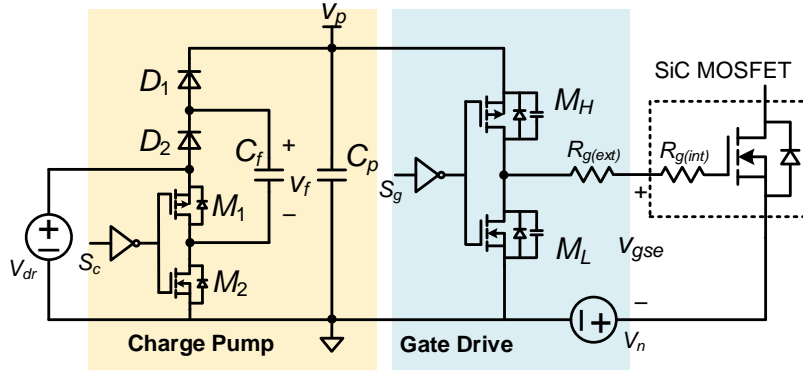


Fig. 5-3. Circuit of proposed CPG.

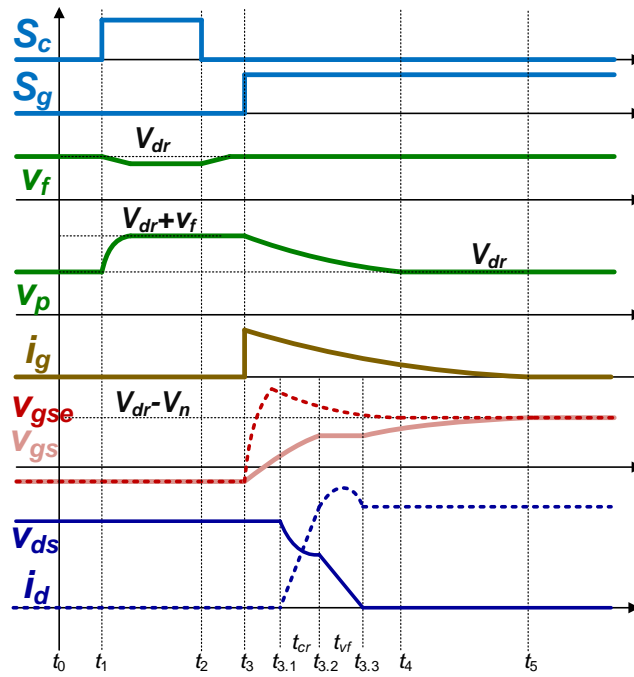


Fig. 5-4. Operation waveforms of proposed CPG.

storage capacitor C_p . Assuming the energy transfer is lossless, the relationship between v_p and v_f at t_2 can be expressed as:

$$\begin{cases} v_p(t_2) = v_f(t_2) + V_{dr} \\ C_f v_f^2(t_2) + C_p v_p^2(t_2) = (C_f + C_p) V_{dr}^2 \end{cases} \quad (5-1)$$

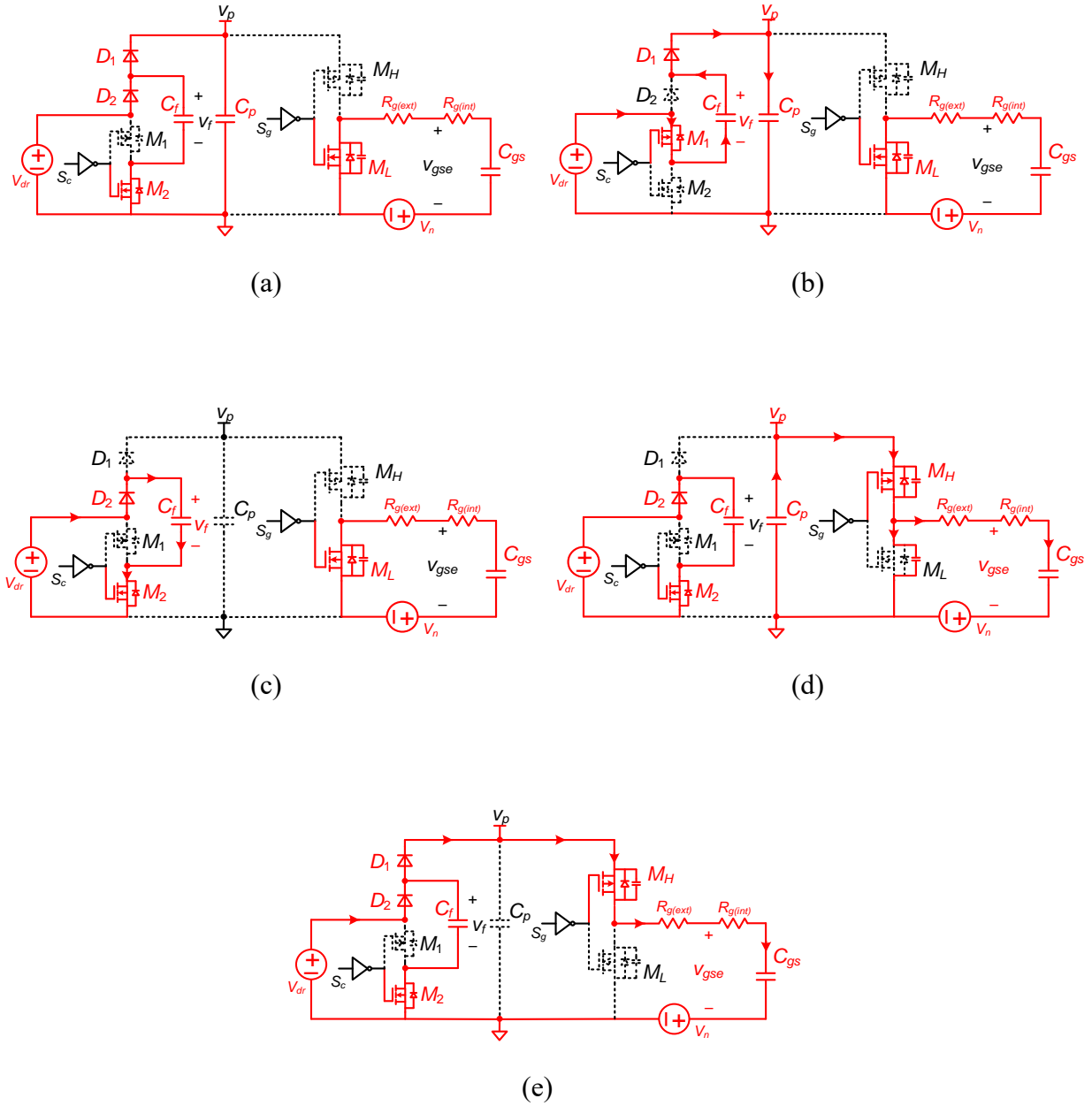


Fig. 5-5. Equivalent circuits in different subintervals of proposed CPG.

(a) Subinterval 1. (b) Subinterval 2. (c) Subinterval 3. (d) Subinterval 4. (e) Subinterval 5.

If the capacitance C_f is much higher than C_p , the voltage drop on v_f can be neglected, and $v_p(t_2)$ is pumped to $2V_{dr}$. Note that since the energy directly flows from one capacitor to the other, this

time period can be very short. By the end of this subinterval, the required high supply voltage is established.

3) Subinterval 3 (t_2-t_3): *standby state*. At t_2 , S_c is pulled down to turn on M_2 and turn off M_1 . In such case, D_1 is off as v_p is higher than v_f . Because part of the energy on C_f is given to C_p , D_2 conducts and the power supply V_{dr} charges C_f . In this state, C_p is disconnected from C_f , and v_p remains constant at high voltage level. Note that this subinterval can also be very short as long as D_1 is off before the gate drive output signal S_g becomes high. The gate drive output is still low, and the SiC MOSFET is in OFF state.

4) Subinterval 4 (t_3-t_4): *gate-charging state I*. At t_3 , S_g turns to high, and the gate drive starts to provide current to charge the SiC MOSFET gate capacitance. Because v_p approximately equals to $2V_{dr}$ at the beginning of this state, the gate current can be enhanced compared with the conventional VSG. The gate voltage v_{gse} starts to increase from $-V_n$, and the SiC MOSFET is turned on when the gate threshold voltage V_{th} is reached. As C_p is disconnected with C_f and V_{dr} , there is no source to provide energy to charge C_p . Therefore, v_p keeps decreasing during the charging process, and the gate voltage approaches to v_p in the end. By tuning the external gate resistance $R_{g(ext)}$, the decreasing rate of v_p can be regulated, which enables the change of switching speed like a typical VSG.

The key point of this CPG is that the capacitance C_p should be selected to guarantee that v_p can finally reach V_{dr} . If C_p is too large and has too much stored energy, the steady state v_p after the gate charging process can be higher than V_{dr} , which results in overcharging. The detailed analysis of C_p calculation is provided in Section V. It should be noted that the external gate-source voltage v_{gse} can be dynamically higher than $(V_{dr}-V_n)$ because of the internal gate resistance of the SiC MOSFETs. However, the real gate-source voltage keeps increasing and does not exceed $(V_{dr}-V_n)$.

5) Subinterval 5 (t_4 - t_5): *gate-charging state II*. v_p reaches V_{dr} at t_4 , and the gate voltage is still increasing. D_1 conducts to connect C_p with V_{dr} . Hence, V_{dr} directly provides energy to charge the gate, and the gate drive becomes a typical VSG throughout the rest of the MOSFET ON state.

The turn-off process of the proposed CPG is the same as a typical VSG since the turn-off loss is not as large as the turn-on loss. However, the same circuit can also be adopted to reduce the turn-off loss.

5.2.3 Benefits and Challenges

Benefits: 1) the pumped gate drive output voltage enables higher gate current that charges the gate capacitance during the turn-on switching transient compared with the conventional VSG. As a result, the turn-on switching loss is reduced.

2) The pumped voltage naturally drops back to normal gate supply voltage without any additional control, which avoids overcharging and has a simple gate drive structure at the same time.

3) The proposed CPG is still a voltage source based gate drive, and the implementation is the same as a typical VSG for the end-user. The SiC MOSFET turn-on switching speed can be easily tuned by changing the external gate resistance. Thus, it is convenient to replace the conventional VSG in power converters with the proposed CPG.

4) The energy transfer time is short between capacitors, resulting in a short charge pump time. Therefore, the time delay between PWM signal and device turn-on is reduced.

5) No extra power supply is required compared with a conventional VSG, which keeps costs low.

6) No inductor is required, which makes the proposed CPG easy for integration.

7) The control signals of the transistors share the same ground, which avoids complex level shifters or floating drives.

Challenges: 1) the drop of the gate drive output voltage is determined by the charge-storage capacitor value C_p . Thus, C_p needs to be carefully selected considering the gate capacitance C_{gs} . If C_p is too large, the pumped voltage cannot decrease to the normal voltage V_{dr} , which can introduce overcharging. Otherwise, if C_p is too small, the pumped voltage reduces too quickly during the switching transient, which deteriorates the switching speed improvement.

2) The increased turn-on speed results in higher dv/dt , leading to more significant influence from parasitics. For example, higher drain-source overvoltage and cross-talk phenomenon can occur on the synchronous device, and EMI can become worse. These side effects from increasing the switching speed should be taken into consideration when applying the proposed CPG.

5.2.4 Parameter Design and Selection

5.2.4.1 Capacitance Design

As mentioned above, the key point in designing the proposed CPG is to select the proper capacitance C_p . Fig. 5-6 shows the waveforms of the pumped voltage v_p and the external gate to ground voltage ($v_{gse}+V_n$) with different C_p . The equivalent circuit after the SiC MOSFET turns on is also plotted. During the turn-on transient, C_p transfers charge to C_{gs} . In the end, the voltage across the two capacitances is the same. The main difference is whether v_p can drop to V_{dr} to conduct D_1 and D_2 , and it is determined by the relationship between C_p and C_{gs} .

If C_p is too small, as shown by the blue line in Fig. 5-6, there is not sufficient stored charge for C_{gs} . As a result, v_p decreases quickly and reaches V_{dr} even when ($v_{gse}+V_n$) is still low. Then the

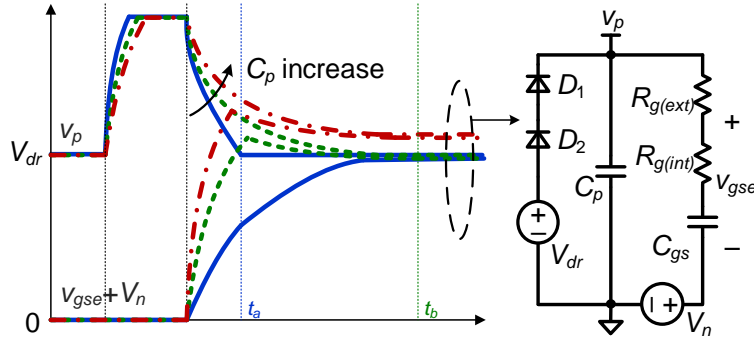


Fig. 5-6. Voltage waveforms during turn-on transient and equivalent circuit with different C_p .

required charge is provided by V_{dr} , and the gate drive is the same as the conventional VSG. In this case, the switching speed improvement is limited.

On the other hand, oversized C_p can have severe consequences. As shown by the red line, v_p drops slowly as C_p has more stored charge. In the end, $(v_{gs}+V_n)$ rises higher than V_{dr} , which results in overcharging and can cause reliability issues for the gate of the SiC MOSFET.

The ideal case is shown by the green line. v_p reduces to V_{dr} at the same time when $(v_{gs}+V_n)$ reaches v_p . Under this circumstance, no overcharging occurs, and the switching speed improvement is maximized. The following calculation presents how to select such proper C_p .

Once M_H is turned on, part of the charge stored in C_p is used to charge the output capacitance of M_L , which is represented as C_{ossL} . Then the output of the gate drive becomes high level, and C_p provides charge to the gate capacitance C_{gs} to turn on the SiC MOSFET. After the drain current of the SiC MOSFET rises to the load current, the gate current discharges the transfer capacitance C_{gd} of the SiC MOSFET and decreases the drain-source voltage. Therefore, if D_1 and D_2 do not conduct, and V_{dr} does not provide energy to C_p , the charge in C_p is transferred to the gate capacitance C_{gs} , the transfer capacitance C_{gd} of the SiC MOSFET, and the output capacitance C_{ossL} of M_L :

$$Q_p = Q_{gs} + Q_{gd} + Q_{ossL} \quad (5-2)$$

where Q_p is the lost charge in C_p , Q_{gs} and Q_{gd} are the gate-to-source charge and gate-to-drain charge of the SiC MOSFET, and Q_{ossL} is the received charge of C_{ossL} during the turn-on transient.

When the gate voltage goes into steady state at t_b in Fig. 5-6, the relationship between v_p and the gate voltage is:

$$v_p(t_b) = v_{gs}(t_b) + V_n = V_{dr} \quad (5-3)$$

Therefore, the charge transfer during the turn-on transient is derived as:

$$\left\{ \begin{array}{l} V_{p0} - \frac{Q_p}{C_p} = \frac{Q_{ossL}}{C_{ossL}} = V_n + \frac{Q_{gs}}{C_{gs}} = V_{dr} \\ \frac{Q_{gd}}{C_{gd_Q}} = V_{dc} \end{array} \right. \quad (5-4)$$

where V_{p0} is the initial voltage of v_p , which is approximately $2V_{dr}$. V_{dc} is the DC bus voltage, and C_{gd_Q} is the charge equivalent transfer capacitance of the SiC MOSFET at V_{dc} . Thus, the required C_p can be calculated as:

$$C_p = \frac{C_{gs}(V_{dr} - V_n) + C_{gd_Q}V_{dc} + C_{oss}V_{dr}}{V_{dr}} \quad (5-5)$$

Note that this is the maximum C_p that can be used to avoid overcharging. To leave some margin, the selected C_p should be a little lower than the calculated value from (5-5).

In terms of C_f in Fig. 5-3, as mentioned in above, it should be much higher than C_p . In practice, choosing a C_f that is 50 times higher than C_p should be enough.

5.2.4.2 Signal Generation

The proposed CPG only needs two control signals, and they can be easily realized with one PWM input signal and some logic gates.

The realization of the logic signals to control the proposed CPG is shown in Fig. 5-7. The delay units can be simply implemented with RC filters with different values. Two logic integrated circuits are used to generate the required signals. Thus, the control signal generation is simple, and the units can be easily integrated. The logic waveforms for the control signals are illustrated in Fig. 5-8.

5.2.5 Loss Analysis

5.2.5.1 Switching Loss

To simplify the loss analysis, the drain current and the drain-source voltage during the switching transient can be approximately regarded as linearly increasing or decreasing. Therefore, the switching loss can be indicated by comparing t_{cr} and t_{vf} with different gate drives.

The turn-on transient starts at t_3 in Fig. 5-4. From t_3 to $t_{3.2}$, v_p decreases while v_{gs} increases, and the equivalent circuit is plotted in Fig. 5-9(a). The initial voltage of v_p and v_{gs} is $2V_{dr}$ and $-V_n$, respectively. The voltage relationship in the gate loop can be written as:

$$2V_{dr} - \frac{1}{C_p} \int_0^t i_g(t) dt = R_g i_g(t) + \frac{1}{C_{gs}} \int_0^t i_g(t) dt \quad (5-6)$$

where R_g is the sum of $R_{g(ext)}$ and $R_{g(int)}$.

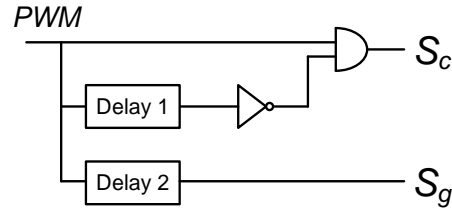


Fig. 5-7. Control logic implementation.

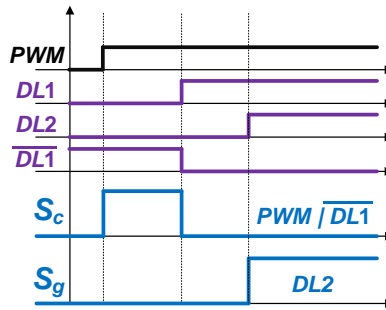


Fig. 5-8. Control logic waveforms.

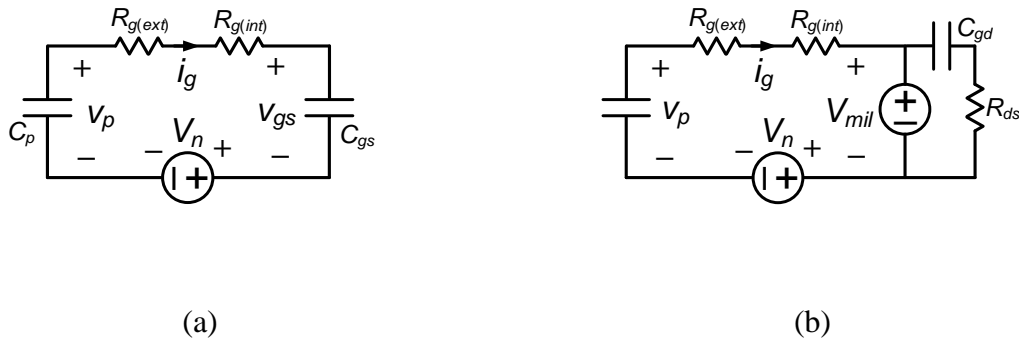


Fig. 5-9. Equivalent circuit of gate loop during turn-on transient. (a) t_3 to $t_{3.2}$. (b) $t_{3.2}$ to $t_{3.3}$.

The gate current can be calculated as:

$$i_g(t) = \frac{2V_{dr}}{R_g} \exp\left(-\frac{1}{R_g C_e} t\right) \quad (5-7)$$

where C_e is the equivalent capacitance in the gate loop:

$$\frac{1}{C_e} = \frac{1}{C_p} + \frac{1}{C_{gs}} \quad (5-8)$$

v_p and v_{gs} during the charging are:

$$v_p(t) = 2V_{dr} - \frac{1}{C_p} \int_0^t i_g(t) dt = 2V_{dr} - \frac{2V_{dr}C_e}{C_p} \left[1 - \exp\left(-\frac{1}{R_g C_e} t\right) \right] \quad (5-9)$$

$$v_{gs}(t) = \frac{1}{C_{gs}} \int_0^t i_g(t) dt - V_n = \frac{2V_{dr}C_e}{C_{gs}} \left[1 - \exp\left(-\frac{1}{R_g C_e} t\right) \right] - V_n \quad (5-10)$$

The current rise time t_{cr} is from $t_{3.1}$ to $t_{3.2}$. At $t_{3.1}$, v_{gs} equals to the threshold voltage V_{th} . At $t_{3.2}$, v_{gs} equals to the Miller voltage V_{mil} . With (5-10), the time interval from $t_{3.1}$ to $t_{3.2}$ can be calculated as:

$$t_{cr(CPG)} = t_{3.2} - t_{3.1} = R_g C_e \ln \left[\frac{2V_{dr}C_e - (V_{th} + V_n)C_{gs}}{2V_{dr}C_e - (V_{mil} + V_n)C_{gs}} \right] \quad (5-11)$$

where V_{mil} is related to the load current I_L and the transconductance of the SiC MOSFET g_m :

$$V_{mil} = V_{th} + \frac{I_L}{g_m} \quad (5-12)$$

Starting from $t_{3.2}$, the gate current discharges the transfer capacitance C_{gd} , and the gate voltage is clamped at V_{mil} . The equivalent circuit changes to Fig. 5-9(b). The voltage relationship is:

$$v_p(t_{3.2}) - \frac{1}{C_p} \int_0^t i_g(t) dt = R_g i_g(t) + V_{mil} + V_n \quad (5-13)$$

The initial voltage of v_p at $t_{3.2}$ can be calculated by (5-9):

$$v_p(t_{3.2}) = 2V_{dr} - \frac{(V_{mil} + V_n)C_{gs}}{C_p} \quad (5-14)$$

The gate current is derived as:

$$i_g(t) = \frac{V_0}{R_g} \exp\left(-\frac{1}{R_g C_p} t\right) \quad (5-15)$$

where $V_0 = v_p(t_{3.2}) - V_{mil} - V_n$.

The gate drive output voltage v_p is:

$$v_p(t) = v_p(t_{3.2}) - \frac{1}{C_p} \int_0^t i_g(t) dt = v_p(t_{3.2}) \exp\left(-\frac{1}{R_g C_p} t\right) \quad (5-16)$$

During the voltage fall time t_{vf} from $t_{3.2}$ to $t_{3.3}$, the voltage across the transfer capacitance decreases from V_{dc} to around zero. The process is expressed as:

$$\frac{1}{C_{gd}} \int_0^{t_{vf}} i_g(t) dt = V_{dc} \quad (5-17)$$

Substituting (5-15) into (5-17), the voltage fall time can be calculated:

$$t_{vf(CPG)} = R_g C_p \ln\left(\frac{V_0 C_p}{V_0 C_p - V_{dc} C_{gd}}\right) \quad (5-18)$$

In terms of the conventional VSG, the current rise time t_{cr} and voltage fall time t_{vf} are given by (3-3) and (3-5), respectively.

Based on the calculation above, the turn-on switching time is calculated for a 1.2 kV, 30 A SiC MOSFET [140] with zero external gate resistance, and the results at different load conditions are plotted in Fig. 5-10. Both the current rise time and voltage fall time achieve significant improvement especially at high load currents. Compared with the conventional VSG, the total turn-on switching time is reduced by 60% at full load with the proposed CPG. Thus, lower turn-on switching loss is achieved.

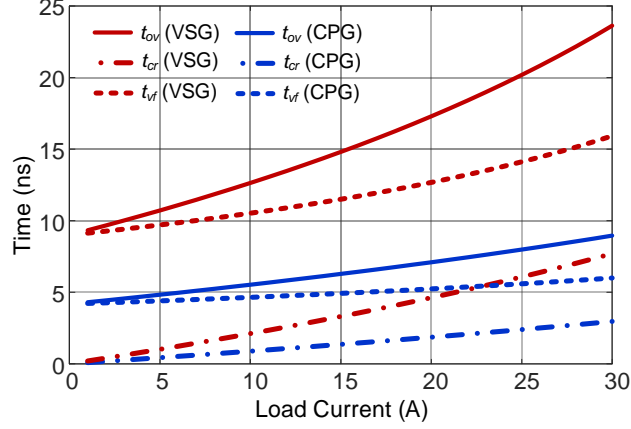


Fig. 5-10. Turn-on switching time comparison between conventional VSG and proposed CPG under different loads.

5.2.5.2 Gate Drive Loss

The gate drive loss of the proposed CPG is mainly generated in two intervals. First, energy is lost when C_p is pumped up by the flying capacitor C_f . Second, during the turn-on transient, all the transferred energy from C_p to C_{gs} , C_{gd} , and C_{ossL} is dissipated.

Assuming C_f is much larger than C_p , during the charge pump state from t_1 to t_2 in Fig. 5-4, v_p increases from V_{dr} to $2V_{dr}$. C_f can be regarded as a constant voltage source, and v_f does not change. According to the energy transfer theory, the amount of energy transferred to the capacitor equals to the amount of energy dissipated in the circuit. Thus, the energy loss during this period is written as:

$$E_{g1} = \frac{1}{2}C_p(2V_{dr})^2 - \frac{1}{2}C_pV_{dr}^2 = \frac{3}{2}C_pV_{dr}^2 \quad (5-19)$$

During the turn-on transient, the initial and final voltage of v_p is $2V_{dr}$ and V_{dr} , respectively. Therefore, the energy loss E_{g2} is the same as E_{g1} . Neglecting the loss in other parts of the CPG, the total gate drive loss during one switching period is:

$$E_{g(CPG)} = 3C_p V_{dr}^2 \quad (5-20)$$

In terms of the conventional VSG, the gate drive loss is calculated by:

$$E_{g(VSG)} = V_{dr} Q_g \quad (5-21)$$

where Q_g is the total gate charge of the SiC MOSFET, which usually can be obtained from the device datasheet.

With the same SiC MOSFET used in Fig. 5-10, the gate drive loss of the proposed CPG is calculated to be 1.7 μJ , while that of the conventional VSG is 1.0 μJ . Therefore, the gate drive loss increases with the proposed CPG. However, the typical switching loss of the SiC MOSFET is higher than 100 μJ . Thus, the increased gate drive loss can be neglected compared to the reduction of the turn-on switching loss with the proposed CPG.

5.3 Experimental Results

The proposed CPG is developed, and the components and parameters used for the gate drive are listed in Table 5-1. The prototype is shown in Fig. 5-11. Note that the charge pump part only accounts for a small portion of the PCB. The CPG can change to a conventional VSG by disabling the signal S_c . Thus, comparison experiments can be conducted for both the proposed CPG and conventional VSG on the same gate drive board. Double pulse test (DPT) is implemented to evaluate the performance of the SiC MOSFETs with the proposed CPG. Fig. 5-12 illustrates the testing platform of the DPT.

To comprehensively investigate the performance of the proposed CPG, two SiC MOSFETs from different manufacturers are tested. The device parameters are listed in Table 5-2. To leave enough margin for the drain-source voltage and avoid the influence of cross-talk from the upper

Table 5-1. Components and parameters of CPG.

| | | | |
|------------|--|------------|--|
| M_1, M_2 | SI4599 P and N channel MOSFETs, Vishay, 40 V, 5 A | M_H, M_L | SI4559 P and N channel MOSFETs, Vishay, 60 V, 4 A |
| D_1, D_2 | SS24 Schottky diode, ONsemi, 40 V, 2 A | C_p | Calculated with (5-5) |
| | | C_f | Around 50 x C_p |

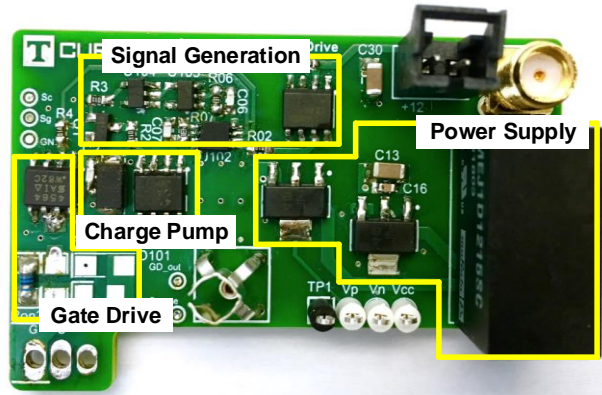


Fig. 5-11. Prototype of proposed CPG.

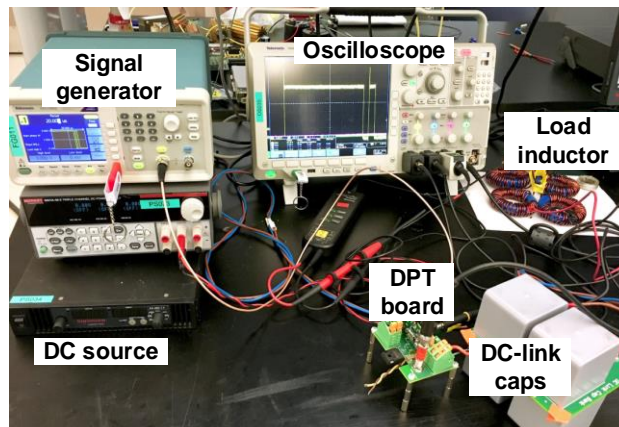


Fig. 5-12. Testing platform.

Table 5-2. Parameters of tested SiC MOSFETs.

| | Device A | Device B |
|--------------|---------------|-------------|
| Part No. | C3M0075120K | SCT3030KL |
| Manufacturer | Wofspeed | Rohm |
| Packaging | TO-247 4pin | TO-247 3pin |
| Voltage | 1.2 kV | 1.2 kV |
| Current | 30 A | 72 A |
| $R_{g(int)}$ | 10.5 Ω | 5 Ω |
| C_{gs} | 1.4 nF | 2.2 nF |
| C_{gd_Q} | 8.7 pF | 98 pF |
| V_{dr} | 19 V | 18 V |
| V_n | 4 V | 0 |

device, a 1.7 kV SiC Schottky diode (C3D25170H from Wolfspeed) is used as the upper device (synchronous switch).

The basic charge pump function of the proposed CPG is evaluated first. Based on the calculation from (5-5), C_p should be 1.7 nF for the tested SiC MOSFET. Fig. 5-13 shows the tested pumped voltage and external gate voltage with different C_p values for Device A, which has 1.4 nF gate capacitance. When C_p is 370 pF, v_p decreases quickly while $(v_{gse}+V_n)$ rises slowly, resulting in higher switching loss. When C_p is 3.4 nF, the final static gate-source voltage v_{gse} is 21 V, which exceeds the gate voltage rating of the tested SiC MOSFET (19 V). When C_p is 1.8 nF, however, the final static voltage is the same as the blue curve, which equals to V_{dr} , and the gate voltage rises much more rapidly than the blue curve. Note that $(v_{gse}+V_n)$ can be higher than v_p because the SiC MOSFET has 10.5 Ω internal gate resistance, while the external gate resistance is zero. The capacitance value in this case is slightly higher than the calculation result (1.7 nF) from (5-5). It is

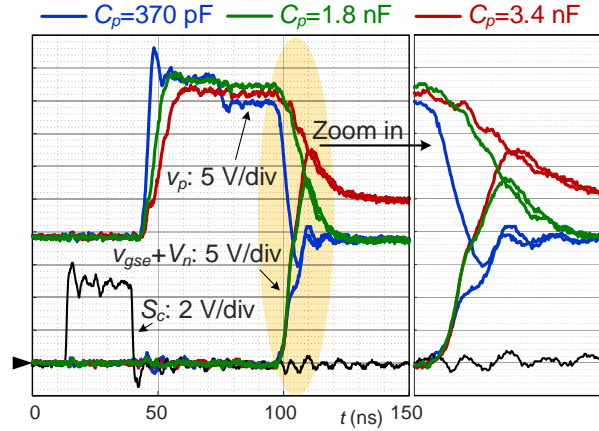


Fig. 5-13. Tested waveforms of pumped voltage and external gate voltage with different C_p .

mainly because the calculation neglects the energy loss during the charge transfer. Generally, the testing result can match well with the analysis in Fig. 5-6.

The switching speed of the SiC MOSFET can be tuned by changing the external gate resistance. Fig. 5-14 illustrates the tested pumped voltage and external gate voltage with different $R_{g(ext)}$ when C_p is 1.8 nF. The gate voltage rises slower with larger $R_{g(ext)}$. Therefore, the usage of the CPG is the same as a conventional VSG, and the switching speed can be easily regulated. Remarkably, the steady state v_p is independent of $R_{g(ext)}$, and it always approaches to V_{dr} .

The tested turn-on transient waveforms with the proposed CPG and the conventional VSG for Device A are plotted in Fig. 5-15(a). Both gate drives utilize zero external gate resistance. Clearly, both the current rise time and voltage fall time are greatly reduced, which indicates much faster switching speed with the proposed CPG. The shaded area of the instantaneous power suggests that the turn-on switching loss is also significantly decreased. Fig. 5-15(b) demonstrates the transient waveforms of the proposed CPG with different external gate resistances. By increasing the resistance, the switching speed is slowed. Detailed data analysis will be presented in next subsection.

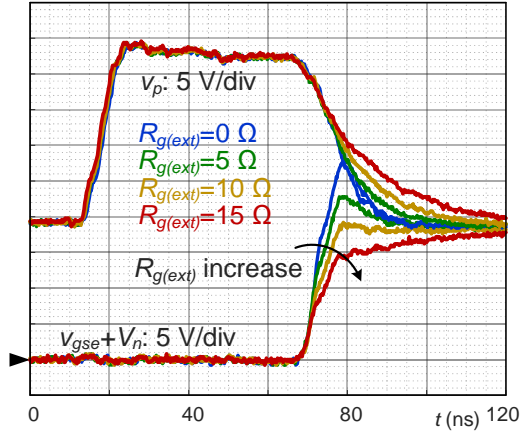


Fig. 5-14. Tested waveforms of pumped voltage and external gate voltage with different $R_{g(ext)}$.

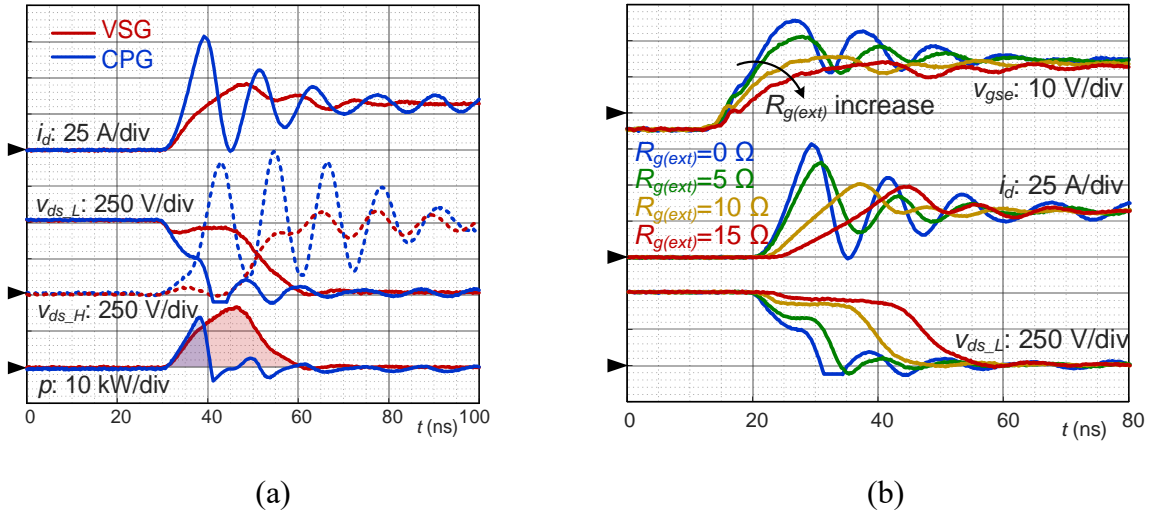


Fig. 5-15. Tested turn-on transient waveforms for Device A at 500 V, 30 A.

(a) Comparison between CPG and VSG with zero $R_{g(ext)}$. (b) CPG with different $R_{g(ext)}$.

Fig. 5-16(a) and (b) show the tested waveforms for Device B. Similar to the result for Device A, the proposed CPG can achieve much higher switching speed.

The comparison of the turn-on time and loss for Device A is given in Fig. 5-17. The proposed CPG with various $R_{g(ext)}$ and the conventional VSG with zero $R_{g(ext)}$ are illustrated. In addition, the

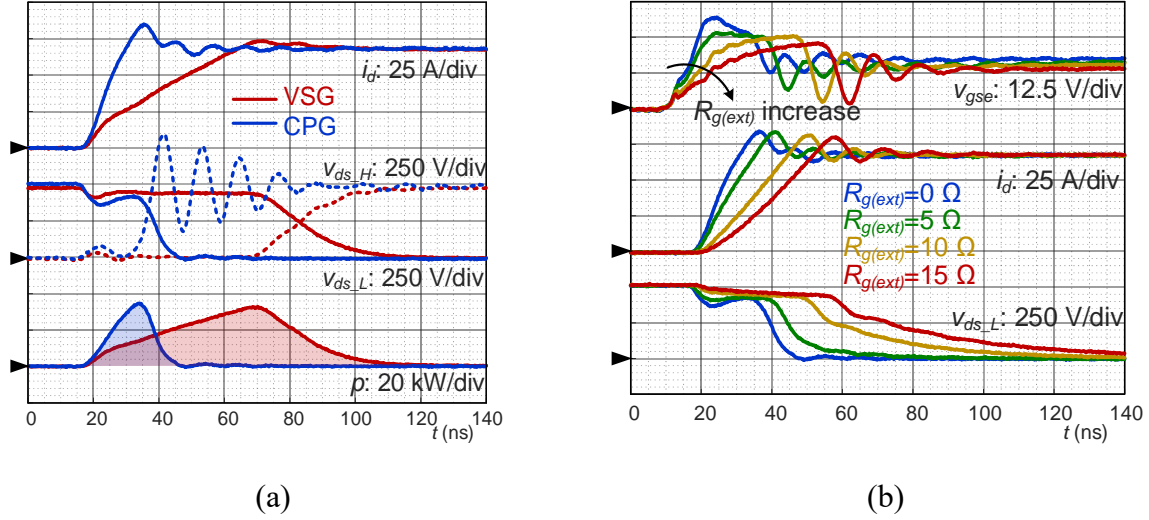


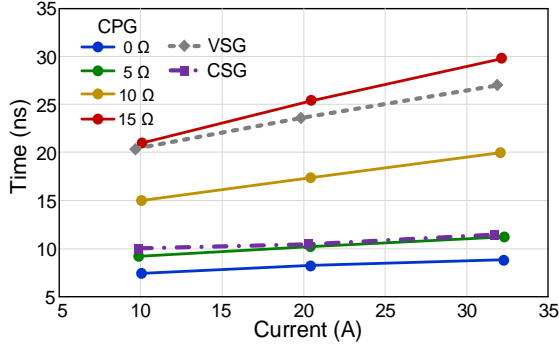
Fig. 5-16. Tested turn-on transient waveforms for Device B at 500 V, 65 A.

(a) Comparison between CPG and VSG with zero $R_{g(ext)}$. (b) CPG with different $R_{g(ext)}$.

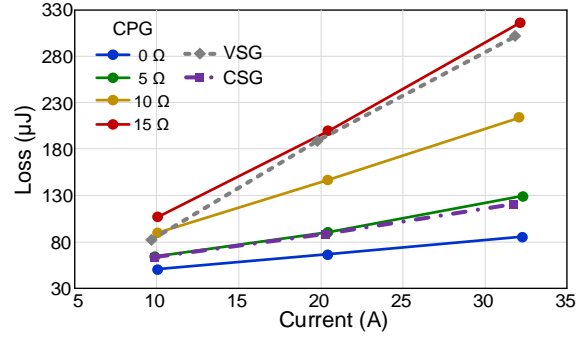
result with the current source gate drive (CSG) in last chapter is included since it is tested with the same SiC MOSFET and under the same operating conditions. From Fig. 5-17(a), with zero $R_{g(ext)}$, the proposed CPG can achieve 67.4% reduction in turn-on switching time comparing with VSG. Moreover, the turn-on time of the CPG is even less than that of the CSG, where constant gate current is provided. As the external gate resistance increases, the switching time of the CPG increases. Nevertheless, until $R_{g(ext)}$ reaches 15 Ω , the turn-on time of the CPG is lower than the VSG with zero $R_{g(ext)}$.

The turn-on loss exhibits a similar trend. At full load and with zero $R_{g(ext)}$, the CPG has a 71.7% reduction in turn-on loss compared with the VSG, and a 29.4% reduction compared with the CSG.

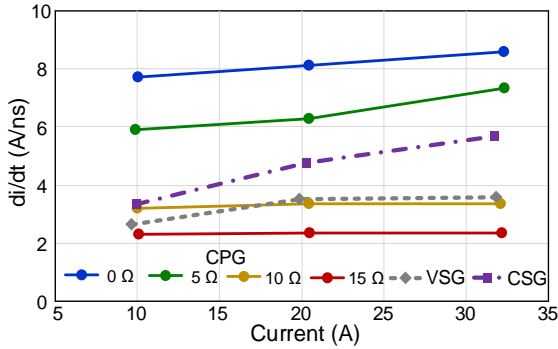
The average di/dt and dv/dt during the switching transient are plotted in Fig. 5-17(c) and (d). The di/dt with zero $R_{g(ext)}$ at full load condition is 2.4 times of the VSG, and the achieved maximum di/dt is 8.6 A/ns. The dv/dt is 3.0 times higher than the VSG with a maximum value of 63.2 V/ns.



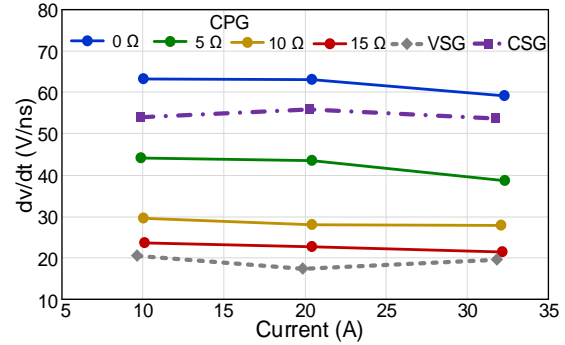
(a)



(b)



(c)



(d)

Fig. 5-17. Performance comparison of proposed CPG with different $R_{g(ext)}$, VSG and CSG for Device A. (a) Turn-on time. (b) Turn-on loss. (c) Average di/dt . (d) Average dv/dt .

Similarly, significant improvement is shown with Device B, as illustrated in Fig. 5-18. The proposed CPG achieves 69.5% decrease of the turn-on time and 67.9% decrease of the turn-on loss at full load and with zero $R_{g(ext)}$. The corresponding di/dt and dv/dt is 4.0 and 2.6 times higher than the VSG, and the maximum value is 12.3 A/ns and 28.7 V/ns, respectively.

Despite the higher switching speed, there are also challenges when utilizing the proposed CPG. As can be observed from Fig. 5-15(a) and Fig. 5-16(a), the turn-on drain-source overvoltage across

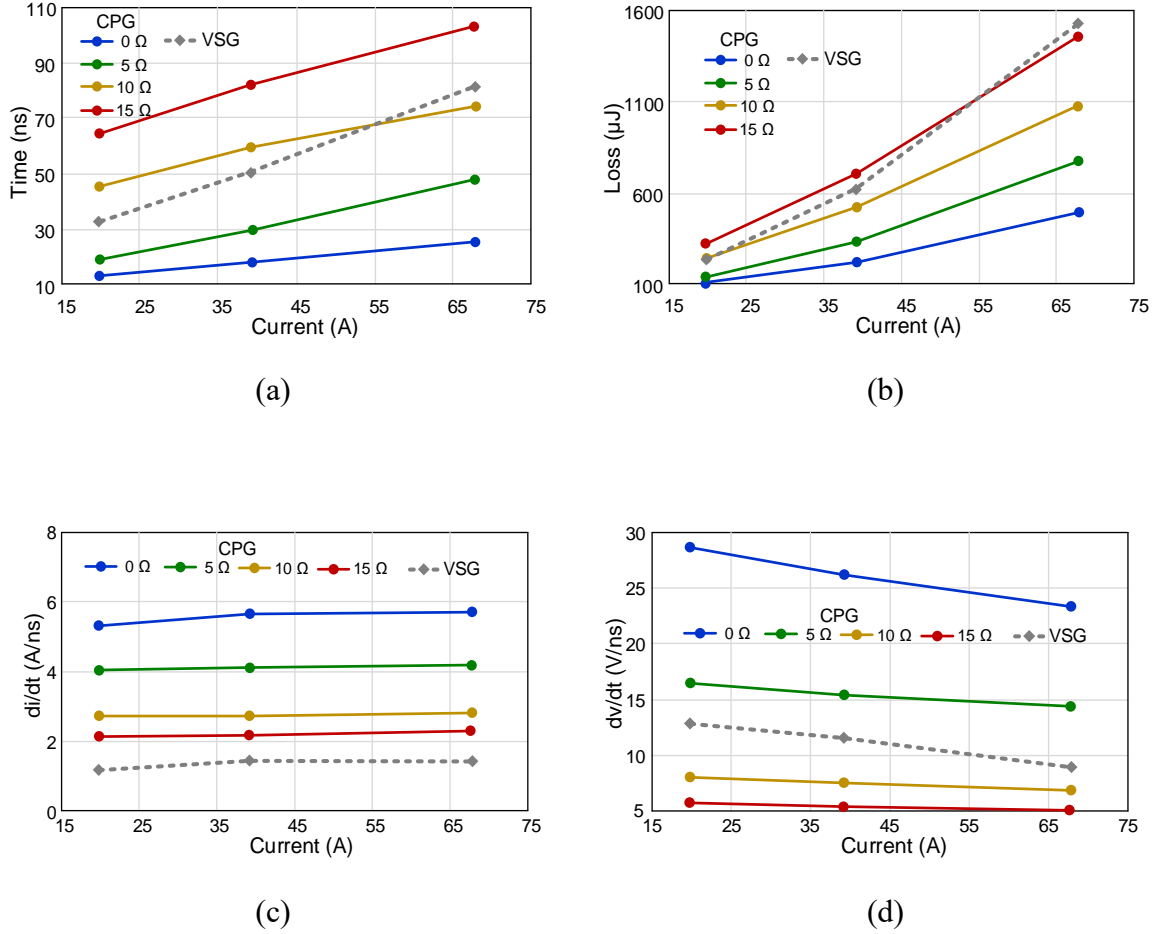


Fig. 5-18. Performance comparison of proposed CPG with different $R_{g(ext)}$, VSG and CSG for Device B. (a) Turn-on time. (b) Turn-on loss. (c) Average di/dt . (d) Average dv/dt .

the upper devices (synchronous switch) is significantly increased because of the high switching speed.

The overvoltage with different gate resistances is shown in Fig. 5-19. With zero $R_{g(ext)}$, the overvoltage is 492 V with Device A, and 384 V with Device B. In hard switching applications, there is always trade-off between higher switching speed and the side effect resulting from parasitics. However, since the synchronous switch turns off with zero current, the voltage overshoot does not increase the overall switching loss.

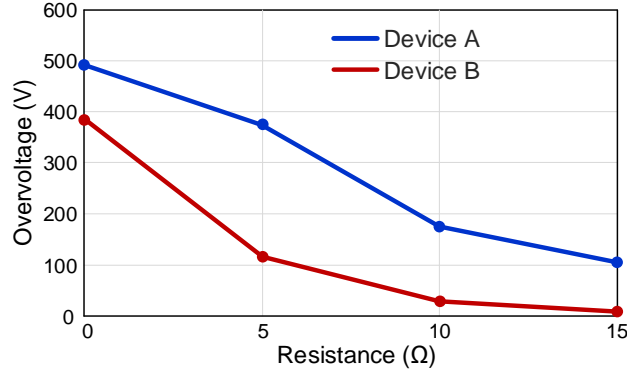


Fig. 5-19. Turn-on drain-source overvoltage of synchronous switch with different $R_{g(ext)}$.

Another issue caused by the higher switching speed and parasitics is the cross-talk in a FET-FET phase-leg architecture. To evaluate the cross-talk with the proposed CPG, the upper device is changed to a SiC MOSFET, which is the same as the lower device. The upper device operates as the active switch, and the gate voltage of the lower device is monitored. As shown in Fig. 5-20, with zero $R_{g(ext)}$, the gate voltage of the lower device increases to 2 V during the turn-on transient when DC voltage is 200 V, which has the potential to cause shoot-through. With higher $R_{g(ext)}$, the gate voltage decreases and keeps under the threshold voltage. Thus, the proposed CPG can achieve higher switching speed without causing shoot-through in most cases.

In extreme cases that require ultra-fast switching speed such that zero $R_{g(ext)}$ is required, anti-cross-talk auxiliary circuits [37], [39], [143], [144] can be adopted to mitigate the issue. It is worth noting that the proposed CPG can also be implemented to dynamically decrease the gate voltage of the synchronous switch during the turn-on transient, so that the device is more difficult to be falsely turned on.

Generally, higher overvoltage and worse cross-talk is the intrinsic penalty of the switching speed increase. However, the value of the proposed CPG is not deteriorated by these side effects.

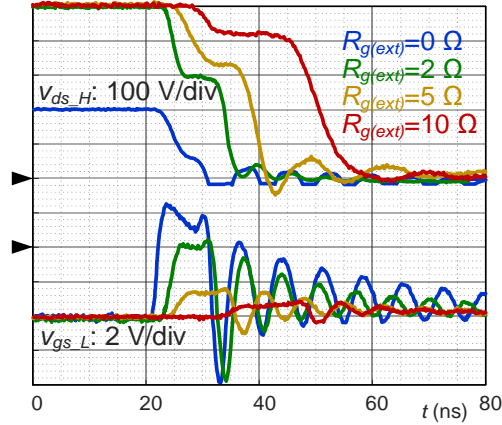


Fig. 5-20. Tested cross-talk waveform for Device A with different $R_{g(ext)}$.

From Fig. 5-15 and Fig. 5-16, even though the gate resistance of the proposed CPG increases to 10Ω , the switching loss is still much lower than the conventional VSG. With such higher resistance, the overvoltage is within the acceptable range, and the cross-talk does not cause shoot-through according to Fig. 5-19 and Fig. 5-20.

In real applications, it is up to the designer to decide the proper switching speed to achieve good balance in different aspects of converter performance, which is the same way in the conventional VSG implementation. The proposed CPG provides the potential to further increase the switching speed and reduce the switching loss of the SiC MOSFET, which is difficult to achieve with the conventional VSG.

5.4 Conclusion

To further simplify the structure and control of the gate drive, a charge pump gate drive (CPG) utilizing the charge transfer is proposed in this chapter, which can dynamically increase the gate drive output voltage during the turn-on switching transient to increase the switching speed. With the proper capacitance selection for the proposed CPG, the gate drive voltage can automatically

drop back to the normal value without additional control, which avoids the overcharging issue and keeps the structure simple.

The function of the proposed CPG is verified with double pulse tests with different load and external gate resistances. Two SiC MOSFETs from different manufacturers are tested and compared to the results with the conventional VSG. Under full load condition, the turn-on switching time of the CPG is decreased by 67.4% and 69.5% for the two MOSFETs, while the turn-on switching loss is reduced by 71.7% and 67.9%, respectively. The challenge of implementing the proposed CPG is the larger parasitic influence such as the overvoltage and cross-talk caused by the higher di/dt and dv/dt with the increased switching speed. The end-user can tune the external gate resistance to adjust the switching speed, which is the same as a conventional VSG.

6 Modeling and Control of Overvoltage in Three-Level Active Neutral Point Clamped Converters

The main hurdle to increase the switching speed in high current SiC power modules is the overvoltage induced by circuit parasitics. This chapter presents the analytical model for the device drain-source overvoltage related to the two commutation loops in three-level active neutral point clamped (3L-ANPC) converters. State space analysis is implemented to build the model. Based on the model, the overvoltage of both the high and line switching frequency devices is analyzed and discussed in detail. Furthermore, a modified modulation is developed to mitigate the influence of the non-linear output capacitance and thus reduce the overvoltage. The model as well as the modified modulation is verified with the experimental results based on a 500 kVA 3L-ANPC converter.

This part of work is published or accepted in the journal and conference papers [77], [145], [146].

6.1 Introduction of 3L-ANPC Converter

6.1.1 Topology and Merits

Compared to the conventional two-level (2L) converters, three-level (3L) converters own the merits of lower device voltage rating, better harmonic spectrum, lower EMI noise, higher switching speed capability, and better dynamic response [147], [148]. Among the 3L converter topologies, the neutral point clamped (NPC) converter is one of the popular candidates for medium voltage and high power applications such as grid tied solar inverters, motor drives, and electric transportation systems. In applications requiring higher efficiency or flexible control, the active neutral point clamped (ANPC) converter is proposed by replacing the diodes in the NPC converter

with the active switches like MOSFETs or IGBTs [149-151]. The topology of a 3L ANPC converter is plotted in Fig. 6-1.

6.1.2 Modulation Schemes

According to the switch states transition, there are two main types of fundamental modulation schemes for a 3L-ANPC converter single phase leg. For the modulation 1 in Fig. 6-2(a), during half line period, the outer switch (S_{1L}) and the clamping switch (S_{3L}) operate complementarily at high switching frequency. The inner switches (S_{2H} and S_{2L}) also operate complementarily but at line switching frequency [74], [152-156]. As a result, the high switching speed commutation occurs between the outer and clamping switches (S_{3L} and S_{1L}), and the commutation loop only includes these two switches. Compared with the other modulation scheme, it involves fewer switches and has a shorter loop length. Therefore, the loop in modulation 1 is called the short loop. Note that in the other half phase leg, the non-active clamping switch (S_{3H} in Fig. 6-2) is kept in ON state to provide constant potential for the non-active outer and inner switches (S_{1H} and S_{2H} in Fig. 6-2).

The other modulation scheme (modulation 2) is drawn in Fig. 6-2(b). In contrast with the modulation 1, the inner switches continuously operate at high switching frequency, while the outer and clamping switches operate at line frequency [149], [157-159]. The commutation loop contains four switches (S_{3H} , S_{2H} , S_{2L} and S_{1L} in Fig. 6-2(b)), and is called the long loop. There are also some hybrid modulations that combine these two basic schemes together but with higher complexity [160], [161].

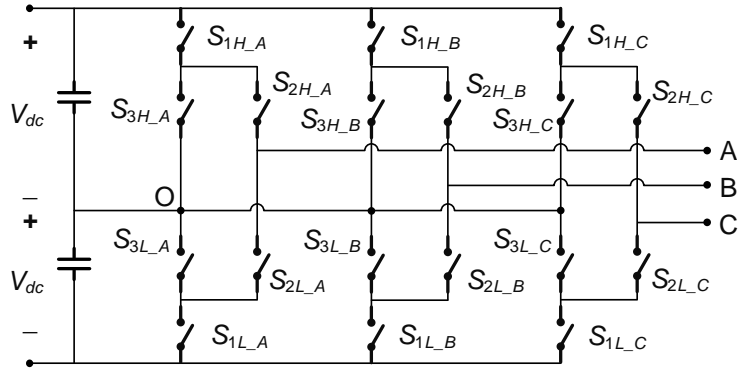
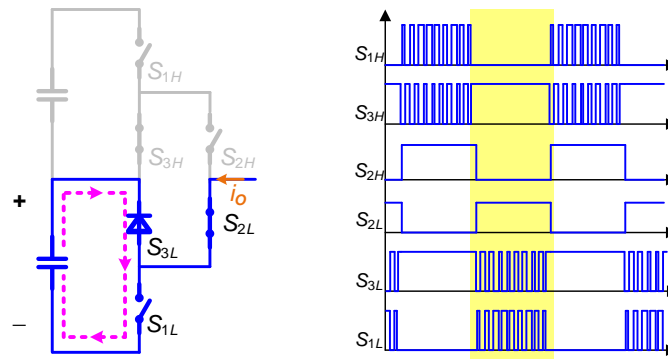
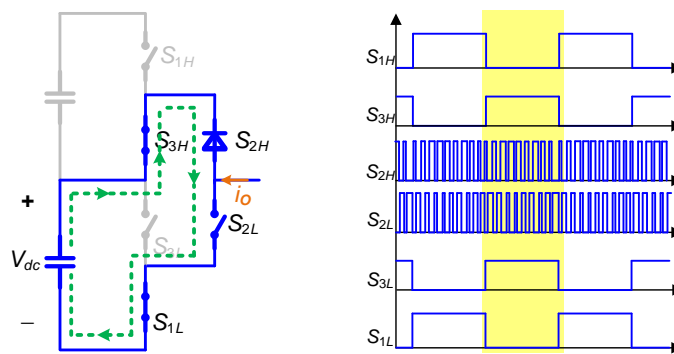


Fig. 6-1. Topology of 3L-ANPC converter.



(a)



(b)

Fig. 6-2. Modulation schemes for 3L-ANPC converter phase leg.

(a) Modulation 1. (b) Modulation 2.

Conventionally, modulation 2 has wider implementation as only two switches operate at high switching frequency. However, with the increase of switching speed by SiC MOSFETs, modulation 1 is adopted more and more frequently because of the following reasons.

1) Modulation 2 has longer commutation loop, which introduces more parasitic inductance. At the same switching speed, more inductance results in higher overvoltage across the switch. To avoid damaging the power device and reduce EMI noise, the switching speed has to be reduced, leading to higher loss.

2) In high power applications, power modules with half bridge structure are popular for bridge-type topologies. With modulation 1, it is easier to achieve loss balance among three modules if S_{1H} and S_{3H} , S_{1L} and S_{3L} , S_{2H} and S_{2L} are paired. On the contrary, it is difficult to achieve such balance in modulation 2 because S_{2H} and S_{2L} always operate at high switching frequency and these devices bear most of the switching loss.

6.2 Modeling of Drain-Source Overvoltage

As shown in the analysis above, modulation 1 is more suitable for high switching frequency applications due to the shorter commutation loop and better loss balancing. However, as has been pointed out in [75-77], there is multi-commutation loop issue in 3L-ANPC converters.

6.2.1 Loop Analysis and Equivalent Circuit

The equivalent circuit of a phase leg in the 3L-ANPC converter is illustrated in Fig. 6-3. Different connecting bars and parasitic inductances are highlighted. Since S_{2L} and S_{3H} are on, S_{2H} is equivalently paralleled with S_{3L} . The detailed switching waveform is plotted in Fig. 6-4. Note that S_{2H} is a non-active switch during a half line cycle. When the active switch S_{3L} commutates with S_{1L} , the drain-source voltage of S_{2H} follows that of S_{3L} . The parasitic inductance resonates

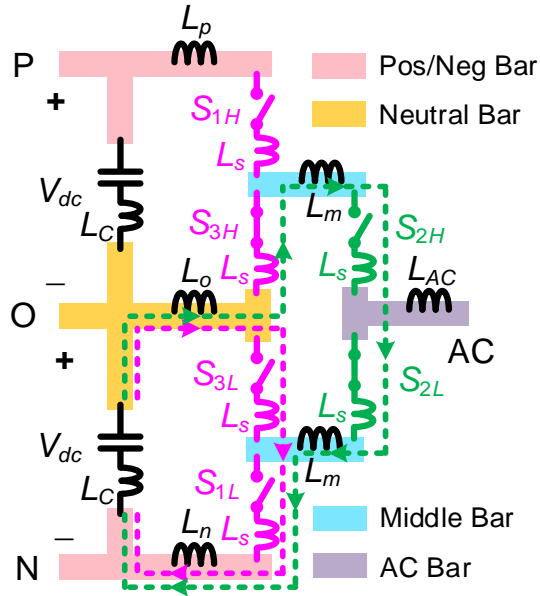


Fig. 6-3. 3L-ANPC converter single phase considering layout and parasitics.

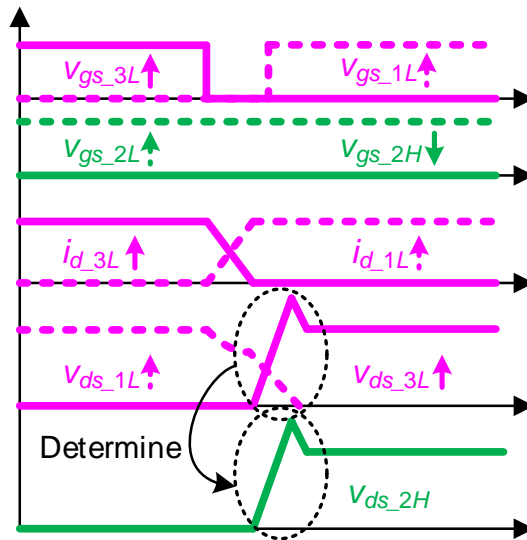


Fig. 6-4. Ideal switching transient waveforms when S_{1L} is active switch.

with the output capacitance of S_{2H} . So the resonance of v_{ds_2H} is excited by the operation of S_{3L} , which differs from modulation 2, where S_{2H} is an active switch and the resonance is independent

of S_{3L} . Therefore, both the short and long commutation loops exist, and there is coupled influence between S_{3L} and S_{2H} .

Assume each busbar part is independent and is not coupled with other busbar parts, and each switch has the same stray inductance. The two loops share the neutral busbar, positive/negative busbar, the switch S_{1L} and the DC-link capacitor. The short loop contains the switch S_{3L} while the longer loop includes two pieces of middle busbar as well as the switches S_{3H} , S_{2H} and S_{2L} . When the load current flows into the phase leg and S_{1L} is the active switch, the equivalent circuit of the phase leg can be drawn in Fig. 6-5. Generally, the overvoltage during turn-on is higher than during turn-off [19], [29], so here the turn-on overvoltage during the transient of the active switch S_{1L} is analyzed. L_1 is the shared loop inductance by two loops and equals to the sum of capacitor ESL L_C , neutral busbar inductance L_o , negative busbar inductance L_n , and one switch stray inductance L_s . L_2 is the sum of two middle busbar inductance $2L_m$ and three switch stray inductance $3L_s$. L_3 equals to one switch stray inductance L_s . The short loop inductance L_{st} is L_1+L_3 while the long loop inductance L_{lg} is L_1+L_2 . R_1 , R_2 and R_3 are the loop parasitic resistances. C_{3L} and C_{2H} are the output capacitances of S_{3L} and S_{2H} . i_3 and i_2 are the currents through S_{3L} and S_{2H} . S_{1L} is represented as a controlled voltage source.

Based on Fig. 6-5, assuming the output capacitance of the switch has a constant value, the gain of the drain-source voltage across two switches can be expressed as

$$\begin{aligned} G_{2H}(s) &= \frac{v_{ds_2H}}{V_{dc} - v_{ds_1L}} = \frac{s^2 C_{3L} L_3 + s C_{3L} R_3 + 1}{H(s)} \\ G_{3L}(s) &= \frac{v_{ds_3L}}{V_{dc} - v_{ds_1L}} = \frac{s^2 C_{2H} L_2 + s C_{2H} R_2 + 1}{H(s)} \end{aligned} \quad (6-1)$$

where

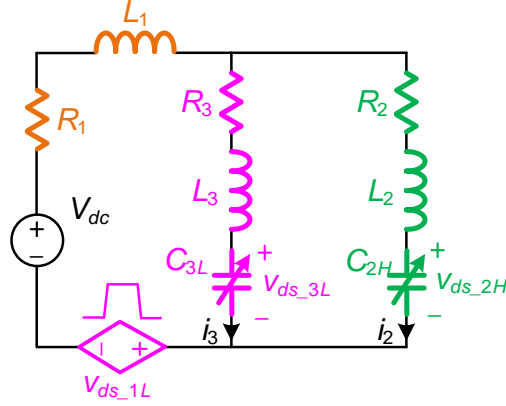


Fig. 6-5. Equivalent circuit of phase leg during negative half line cycle.

$$\begin{aligned}
 H(s) = & s^4 (L_1 L_2 + L_1 L_3 + L_2 L_3) C_{2H} C_{3L} \\
 & + s^3 (L_1 R_2 + L_1 R_3 + L_2 R_1 + L_2 R_3 + L_3 R_1 + L_3 R_2) C_{2H} C_{3L} \\
 & + s^2 [(L_1 + L_2) C_{2H} + (L_1 + L_3) C_{3L} + (R_1 R_2 + R_1 R_3 + R_2 R_3) C_{2H} C_{3L}] \\
 & + s [(R_1 + R_2) C_{2H} + (R_1 + R_3) C_{3L}] + 1
 \end{aligned} \tag{6-2}$$

The bode plots of the voltage gain G_{2H} and G_{3L} are shown in Fig. 6-6. For reference, G_{3L} in a conventional 2L phase leg without the long commutation loop is also illustrated. The parameters are as follows: $L_1=4$ nH, $L_2=15$ nH, $L_3=1.5$ nH, $C_{3L}=C_{2H}=3.8$ nF.

It is observed that there are two resonant frequencies in the 3L phase leg: f_{r1} and f_{r2} . The effect of the resonant frequencies can be observed in Fig. 6-7. For the high switching frequency device S_{3L} , the dominant resonant frequency of the drain-source voltage is f_{r2} , which is also close to the resonant frequency in a 2L phase leg. For the line switching frequency device S_{2H} , the dominant resonant frequency is f_{r1} . Generally, the line switching frequency device has lower resonant frequency than the high switching frequency device does.

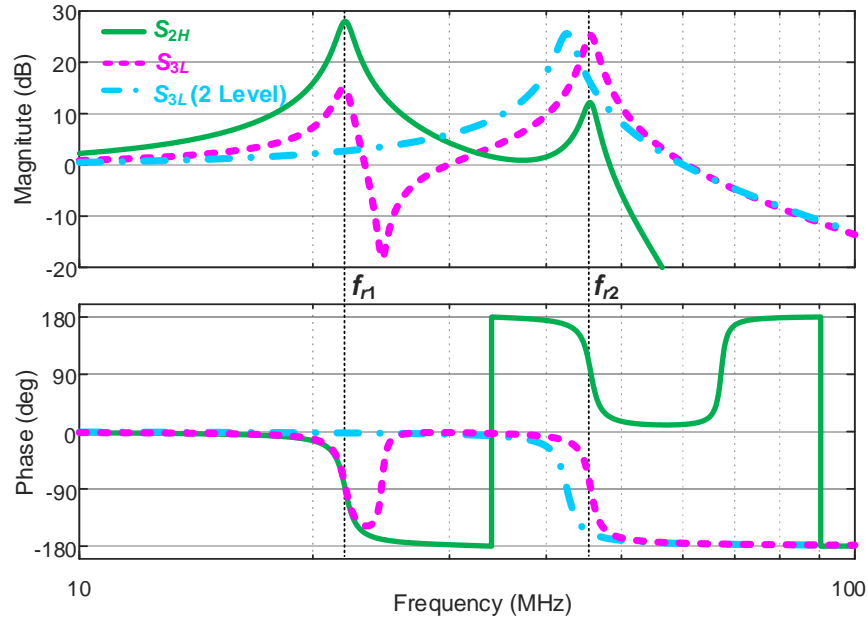


Fig. 6-6. Voltage gain of line and high switching frequency devices in 3L and 2L phase leg.

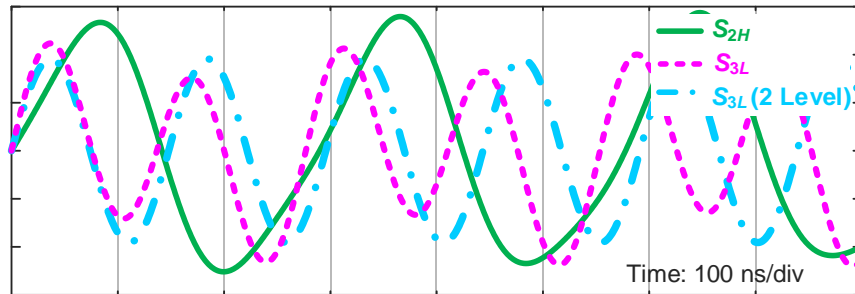


Fig. 6-7. Voltage response at resonant frequencies in 3L and 2L phase leg.

6.2.2 Overvoltage Model Considering Non-Linear Output Capacitance

For semiconductor power devices like MOSFETs and IGBTs, the output capacitance is non-linear and is dependent on the drain-source voltage. Based on different semiconductor material and device structure, the output capacitance at low voltage can be 10-500 times higher than that at high voltage [162]. According to [77], the non-linearity of the output capacitance is one of the largest impact factor for the overvoltage.

Since the output capacitance is non-linear and voltage dependent, it is difficult to directly derive the voltage response in frequency domain like in (6-1). Here, the state space analysis is implemented to build the analytical voltage response model in time domain.

First, the instantaneous voltage and current relationship in Fig. 6-5 can be derived based on KVL and KCL:

$$\begin{cases} V_{dc} = L_3 \frac{di_3}{dt} + v_{ds_3L} + (R_1 + R_3)i_3 + R_1 i_2 + L_1 \left(\frac{di_3}{dt} + \frac{di_2}{dt} \right) + v_{ds_1L} \\ V_{dc} = L_2 \frac{di_2}{dt} + v_{ds_2H} + (R_1 + R_2)i_2 + R_1 i_3 + L_1 \left(\frac{di_3}{dt} + \frac{di_2}{dt} \right) + v_{ds_1L} \\ L_3 \frac{di_3}{dt} + v_{ds_3L} + R_3 i_3 = L_2 \frac{di_2}{dt} + v_{ds_2H} + R_2 i_2 \\ C_{3L} \frac{dv_{ds_3L}}{dt} = i_3 \\ C_{2H} \frac{dv_{ds_2H}}{dt} = i_2 \end{cases} \quad (6-3)$$

By applying the state space, (6-3) can be written in the format of

$$\dot{X}(t) = AX(t) + BU(t) \quad (6-4)$$

$X = [i_3 \ i_2 \ v_{ds_3L} \ v_{ds_2H}]^T$ is the state vector. The analysis begins when the current commutation finishes and v_{ds_1L} starts to drop. At this moment, $i_3 = i_2 = 0$ and $v_{ds_3L} = v_{ds_2H} = 0$. So the initial state $X_0 = [0 \ 0 \ 0 \ 0]^T$.

$U = V_{dc} - v_{ds_1L}$ is the input vector. Here, v_{ds_1L} is assumed to drop linearly during turn-on

$$v_{ds_1L}(t) = \begin{cases} V_{ds_1L_0} \left(1 - \frac{t}{t_{vf_1L}} \right) & t \leq t_{vf_1L} \\ 0 & t > t_{vf_1L} \end{cases} \quad (6-5)$$

where $V_{ds_1L_0}$ is the initial voltage of S_{1L} and is expressed as

$$V_{ds_{-1L_0}} = V_{dc} - (L_1 + L_3) \frac{di_{1L}}{dt} \quad (6-6)$$

where i_{1L} is the current flowing through S_{1L} .

A and B are state and input matrix and they can be derived as

$$A = \begin{bmatrix} \frac{(R_1 + R_3)L_2 + R_3L_1}{KL_2L_3} & \frac{R_1L_2 - R_2L_1}{KL_2L_3} & \frac{L_1 + L_2}{KL_2L_3} & \frac{L_1}{KL_2L_3} \\ \frac{R_1L_3 - R_3L_1}{KL_2L_3} & \frac{(R_2 + R_3)L_3 + R_2L_1}{KL_2L_3} & \frac{L_1}{KL_2L_3} & \frac{L_1 + L_3}{KL_2L_3} \\ \frac{1}{C_{3L}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{2H}} & 0 & 0 \end{bmatrix} \quad (6-7)$$

$$B = \begin{bmatrix} \frac{1}{KL_3} & \frac{1}{KL_2} & 0 & 0 \end{bmatrix}^T$$

where

$$K = 1 + \frac{L_1}{L_2} + \frac{L_1}{L_3} \quad (6-8)$$

The voltage dependent output capacitance is modeled with the equation [163]

$$C(v) = C_{hv} + \frac{1}{\frac{1}{C_{0v}} + \frac{v^x}{C_j}} \quad (6-9)$$

where C_{0v} and C_{hv} are the low-voltage and high-voltage capacitances while x and C_j are curve fitting coefficients.

Fig. 6-8 compares the derived analytical voltage transient waveforms between constant and non-linear output capacitances. The constant capacitance uses the time related effective value based on the device datasheet. Obviously, the overvoltage with non-linear capacitance is much

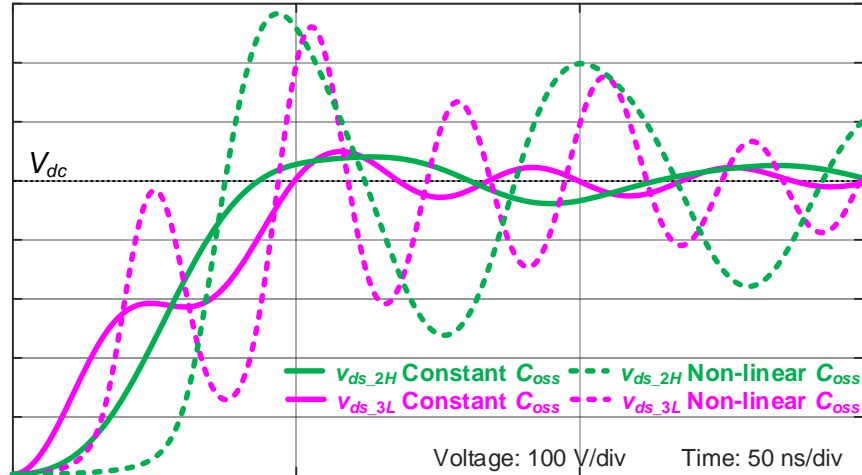


Fig. 6-8. Transient waveforms with constant and non-linear capacitance based on established model.

higher than the constant capacitance case. To predict the real condition during switching transient, voltage dependent non-linear capacitance has to be taken into consideration in the model.

6.2.3 Analysis of Overvoltage with Established Model

Based on the analytical model built above, the overvoltage of both high and line switching frequency switches can be evaluated. Fig. 6-9 illustrates the transient waveforms of 3L and 2L phase leg. Despite the influence of the non-linear capacitance, the basic trend of resonant frequencies analyzed in Fig. 6-6 and Fig. 6-7 is still valid. The resonant frequency of the high switching frequency device is close to that in a typical 2L phase leg, and is higher than the line switching frequency device.

The overvoltage on both the high and line switching frequency devices should be investigated to understand the relationship between overvoltage and loop inductance. The overvoltage percentage $OV(\%)$ is defined to simplify the analysis

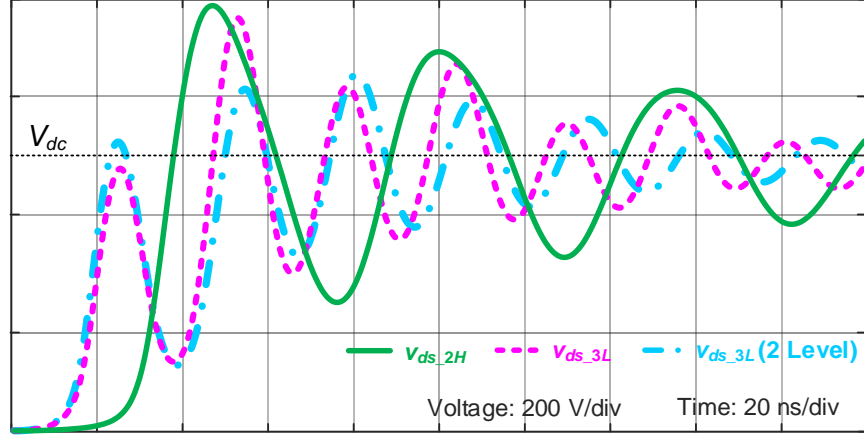


Fig. 6-9. Transient waveforms with 3L and 2L phase leg based on established model.

$$OV(\%) = \frac{V_{ds_pk} - V_{dc}}{V_{dc}} \times 100\% \quad (6-10)$$

Based on the analytical model, the relationship among the short loop inductance L_{st} , the ratio between long and short loop inductances L_{lg}/L_{st} , and $OV(\%)$ is shown in Fig. 6-10. From the plot, the following conclusions can be made.

1) With the same inductance ratio of short and long loops, the increase of inductance leads to higher overvoltage for both the high and line switching frequency devices.

2) Keeping the same short loop inductance, the larger long loop inductance results in higher overvoltage across the line switching frequency device. However, the overvoltage of the high switching frequency device reaches its peak when L_{lg}/L_{st} is 3-4. Further increasing the long loop inductance does not cause higher overvoltage. This can be explained that the increased L_{lg} decouples C_{3L} and C_{2H} . The voltage rise on C_{3L} is the excitation of the resonance on C_{2H} . Larger L_{lg} prevents v_{ds_2H} following the trend of v_{ds_3L} , and v_{ds_2H} in turn shows less influence on v_{ds_3L} .

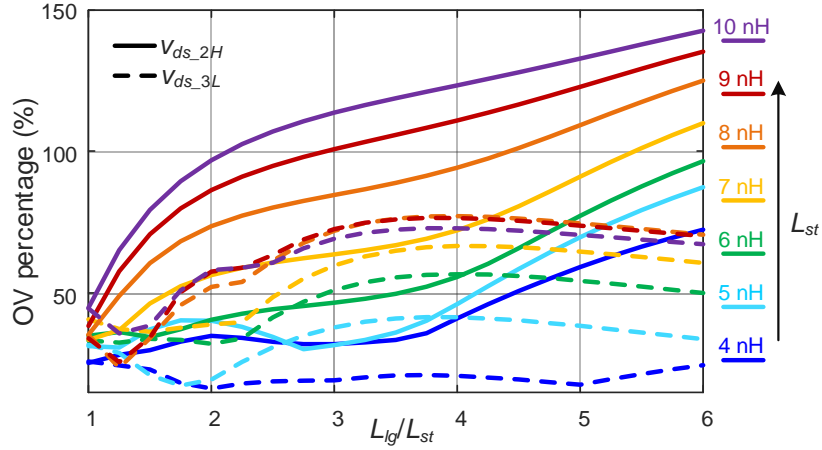


Fig. 6-10. Overvoltage ratio of high and line switching frequency devices under different L_{st} and L_{lg}/L_{st} ratio.

3) When $L_{lg}/L_{st} = 1$, the two devices have the same overvoltage, which is easy to understand. Generally speaking, the line frequency device exhibits higher overvoltage compared to the high switching frequency device especially with large L_{st} and inductance ratio. The only exception is when L_{st} is small (lower than 5 nH) and L_{lg}/L_{st} is 2.5-4.

In terms of the coupling effect between the high and line frequency devices, it is also important to know the influence of the long loop on the switching speed of the high switching device. Fig. 6-11 shows the voltage rise time of the high switching frequency device in 3L and 2L phase legs with different loop inductance ratios. The closer the two loop inductances are, the longer voltage rise time appears for the high switching frequency device in a 3L phase leg. The two loops have the strongest coupling when they have the same loop inductance value, leading to the largest influence on the rising speed of the voltage across the switch. From Fig. 6-11, when the loop inductance ratio is larger than 2.2, the voltage rise time difference between 3L and 2L phase leg is smaller than 10%. Considering the 3L-ANPC converter, it is common that the long loop has much larger parasitic inductance than the short loop does. Therefore, in most cases, the switching speed

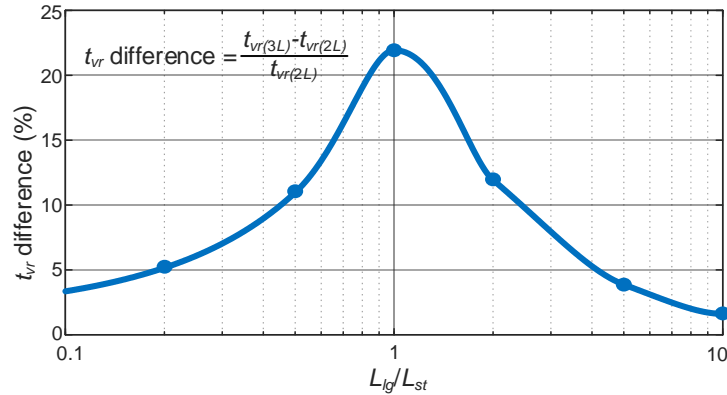


Fig. 6-11. Voltage rise time difference of high switching frequency devices between 3L and 2L single phase.

of the high switching frequency device in a 3L phase leg is not slowed down much compared with a 2L phase leg.

The detailed analytical transient waveform comparison under the same short loop inductance is provided in Fig. 6-12. For a 2L phase leg, the voltage rise time is 15 ns. In a 3L phase leg, when the two loops have the same inductance, the voltage rise time is 18.5 ns, which indicates a 23 % increase. Meanwhile, when the long loop inductance is five times higher than the short loop inductance, the voltage rise time increase is less than 1 ns.

From Fig. 6-10 to Fig. 6-12, it can be summarized that the overvoltage on the line frequency device is normally more severe, and the switching speed of the high switching frequency device is not impacted. Thus, the line switching frequency device deserves more analysis.

Fig. 6-13 shows the relationship between the overvoltage on the line switching frequency device and the voltage fall time of the v_{ds_1L} as well as the long loop inductance L_{lg} . Although the relationship is not purely monotonic, generally larger L_{lg} and lower t_{vf_1L} result in higher overvoltage.

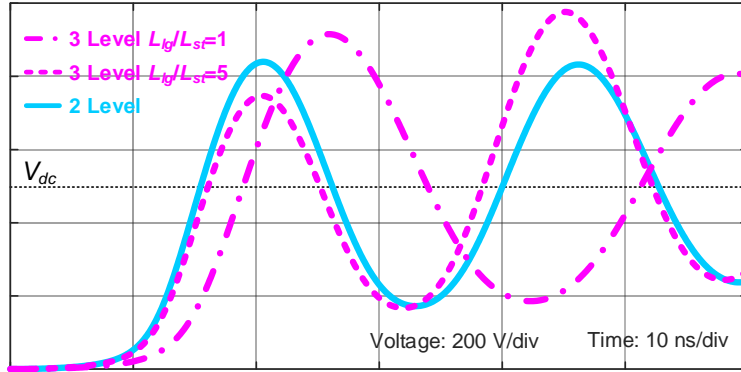


Fig. 6-12. Voltage transient waveforms with different L_{lg}/L_{st} and same L_{st} based on established model.

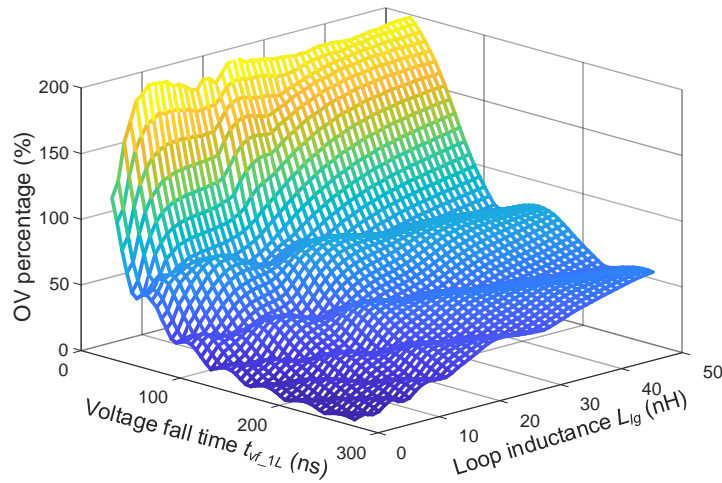


Fig. 6-13. Overvoltage of line switching frequency device under different L_{lg} and t_{vf_1L} .

6.3 Control and Modeling with Modified Modulation

6.3.1 Modified Modulation

As shown in the analysis of Section 6.2.2, one of the sources for the high overvoltage is the non-linear output capacitance. For a typical power device, the output capacitance shown in Fig. 6-14 can be approximately divided into two regions [66]. When the drain-source voltage is low,

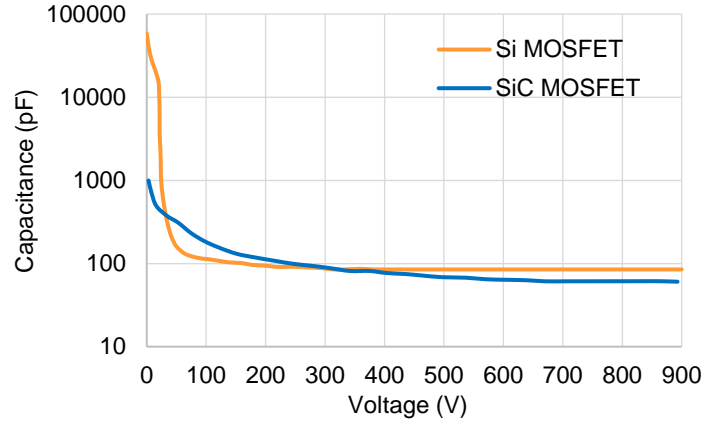


Fig. 6-14. Non-linear output capacitance of 900 V Si and SiC MOSFET.

the capacitance decreases rapidly as the voltage increases, and this is the main non-linear region. On the other hand, the capacitance does not change much after the voltage reaches a certain threshold (normally less than 1/10 of the voltage rating). Therefore, if there is an initial voltage across the drain-source of the switch and it is higher than the threshold, the effect of the capacitance non-linearity can be significantly mitigated. The ideal state trajectory of the resonance between the output capacitance and the loop inductance is drawn in Fig. 6-15. Without the initial voltage, the device drain-source voltage resonates from zero to the peak value higher than $2V_{dc}$. Meanwhile, the trajectory becomes smaller and the peak voltage reduces with the initial voltage at the beginning of the resonance. In addition, the shape of the trajectory is more circular, which indicates that the capacitance is more constant.

The required initial voltage across the device drain-source can be realized with a simple modification based on the conventional modulation. Table 6-1 highlights the change of the operation states for the switches in a phase leg with the modified modulation. Compared with the conventional one, the only change is turning off the non-active clamping switches (S_{3H} and S_{3L}) instead of keeping them on.

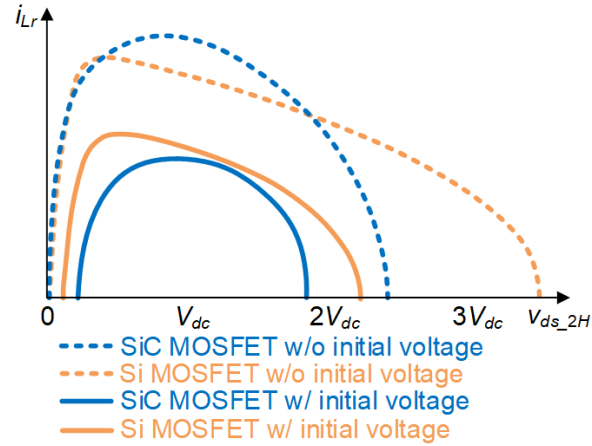


Fig. 6-15. State trajectory of parasitic resonance during switching transient.

Table 6-1. Change of switch states with modified modulation compared to conventional modulation.

| State | S_{1H} | S_{2H} | S_{3H} | S_{3L} | S_{2L} | S_{1L} |
|----------------|----------|----------|----------|----------|----------|----------|
| P | On | On | Off | On→Off | Off | Off |
| O ⁺ | Off | On | On | On→Off | Off | Off |
| O ⁻ | Off | Off | On→Off | On | On | Off |
| N | Off | Off | On→Off | Off | On | On |

6.3.2 Loop Analysis and Equivalent Circuit

For the modified modulation, all of the three non-active switches (S_{1H} - S_{3H} in Fig. 6-2) are off during the half line cycle. This makes the analysis more complicated because the voltage distribution on these switches are changing with the commutating of S_{1L} and S_{3L} . As a result, not only the dynamic overvoltage, but also the steady state voltage within a switching cycle should be evaluated.

Similar to Fig. 6-5, the equivalent circuit with the modified modulation in the negative half line cycle is plotted in Fig. 6-16. In addition to the non-active line switching frequency device S_{2H} , both the output capacitances of the non-active high switching frequency devices S_{1H} and S_{3H} are also involved.

6.3.3 Overvoltage Model

The state space analysis is adopted to build the analytical voltage response model. The instantaneous voltage and current relationship is derived as

$$\left\{ \begin{array}{l} V_{dc} = L_3 \frac{di_{1H}}{dt} + v_{ds_1H} + R_3 i_{1H} + L_3 \frac{di_{3H}}{dt} + v_{ds_3H} + R_3 i_{3H} + L_1 \left(\frac{di_{3H}}{dt} - \frac{di_{3L}}{dt} \right) + R_1 (i_{3H} - i_{3L}) \\ V_{dc} = L_3 \frac{di_{3L}}{dt} + v_{ds_3L} + R_3 i_{3L} + v_{ds_1L} + L_1 \left(\frac{di_{3L}}{dt} - \frac{di_{3H}}{dt} \right) + R_1 (i_{3L} - i_{3H}) \\ L_3 \frac{di_{3L}}{dt} + v_{ds_3L} + R_3 i_{3L} + L_3 \frac{di_{3H}}{dt} + v_{ds_3H} + R_3 i_{3H} = L_2 \left(\frac{di_{1H}}{dt} - \frac{di_{3H}}{dt} \right) + v_{ds_2H} + R_2 (i_{1H} - i_{3H}) \\ C_{1H} \frac{dv_{ds_1H}}{dt} = i_{1H} \\ C_{2H} \frac{dv_{ds_2H}}{dt} = i_{1H} - i_{3H} \\ C_{3H} \frac{dv_{ds_3H}}{dt} = i_{3H} \\ C_{3L} \frac{dv_{ds_3L}}{dt} = i_{3L} \end{array} \right. \quad (6-11)$$

$X = [i_{1H} \ i_{3H} \ i_{3L} \ v_{ds_1H} \ v_{ds_2H} \ v_{ds_3H} \ v_{ds_3L}]^T$ is the state vector. $U = [V_{dc} \ v_{ds_1L}]^T$ is the input vector.

v_{ds_1L} is still assumed to drop linearly during turn-on as in (6-5).

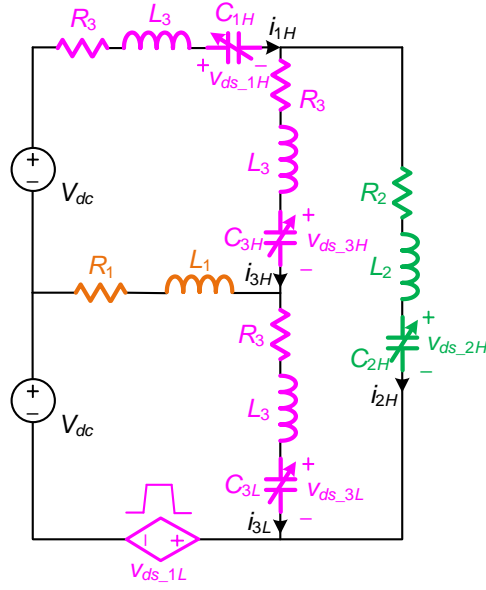


Fig. 6-16. Equivalent circuit of phase leg during half line cycle with modified modulation.

The state and input matrixes A and B are

$$A = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & -\frac{2L_1L_3 + L_3^2}{M} & -\frac{L_1L_2 + L_2L_3}{M} & -\frac{L_1L_2}{M} \\ a_{21} & a_{22} & a_{23} & -\frac{L_1L_2 + L_2L_3}{M} & \frac{L_1L_3 + L_3^2}{M} & a_{26} & -\frac{L_1L_2 + L_1L_3}{M} \\ a_{31} & a_{32} & a_{33} & -\frac{L_1L_2}{M} & \frac{L_1}{M} & -\frac{L_1L_2 + L_1L_3}{M} & a_{37} \\ \frac{1}{C_{1H}} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{2H}} & -\frac{1}{C_{2H}} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{3H}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{3L}} & 0 & 0 & 0 & 0 \end{bmatrix} \quad (6-12)$$

$$B = \begin{bmatrix} \frac{2L_1L_2 + 4L_1L_3 + L_2L_3 + 2L_3^2}{M} & \frac{2L_1L_2 + L_2L_3 - L_3^2}{M} & \frac{2L_1L_2 + 2L_2L_3 + L_3^2}{M} & 0 & 0 & 0 & 0 \\ -\frac{L_1L_2 + 2L_1L_3 + L_3^2}{M} & -\frac{L_1L_2 - L_3^2}{M} & -\frac{L_1L_2 + 2L_2L_3 + L_3^2}{M} & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad (6-13)$$

where

$$\begin{aligned} a_{11} &= -\frac{R_2(2L_1L_3 + L_3^2) + R_3(L_1L_2 + 2L_1L_3 + L_2L_3 + L_3^2)}{M} \\ a_{12} &= -\frac{R_1L_2L_3 - R_2(2L_1L_3 + L_3^2) + R_3(L_1L_2 + L_2L_3)}{M} \\ a_{13} &= \frac{R_1L_2L_3 - R_3L_1L_2}{M} \\ a_{14} &= -\frac{L_1L_2 + 2L_1L_3 + L_2L_3 + L_3^2}{M} \\ a_{21} &= -\frac{R_2(L_1L_3 + L_3^2) - R_3(L_1L_2 + L_2L_3)}{M} \\ a_{22} &= -\frac{R_1(L_2L_3 + L_3^2) + R_2(L_1L_3 + L_3^2) + R_3(L_1L_2 + L_1L_3 + L_2L_3 + L_3^2)}{M} \\ a_{23} &= -\frac{R_1(L_2L_3 + L_3^2) - R_3(L_1L_2 + L_1L_3)}{M} \\ a_{26} &= -\frac{L_1L_2 + L_1L_3 + L_2L_3 + L_3^2}{M} \\ a_{31} &= -\frac{R_2L_1L_3 + R_3L_1L_2}{M} \\ a_{32} &= \frac{R_1(2L_2L_3 + L_3^2) - R_2L_1L_3 - R_3(L_1L_2 + L_1L_3)}{M} \\ a_{33} &= -\frac{R_1(2L_2L_3 + L_3^2) + R_3(L_1L_2 + L_1L_3 + 2L_2L_3 + L_3^2)}{M} \\ a_{37} &= -\frac{L_1L_2 + L_1L_3 + 2L_2L_3 + L_3^2}{M} \\ M &= L_3(3L_1L_2 + 2L_1L_3 + 2L_2L_3 + L_3^2) \end{aligned} \quad (6-14)$$

6.3.4 Analysis of Overvoltage with Established Model

From Fig. 6-16, the line switching frequency device S_{2H} is no longer equivalently paralleled with S_{3L} . When S_{3L} is on, there is initial voltage across the drain-source of S_{2H} .

The switching transient waveforms based on the established model is illustrated in Fig. 6-17. The initial voltage on S_{2H} is 120 V. Compared to the waveform with the conventional modulation, the overvoltage of the high and line switching frequency devices with the modified modulation achieve a reduction of 124 V and 188 V, respectively.

6.3.5 Analysis of Steady State Voltage

Since there is voltage distribution among the non-active switches, this distribution is worth investigating because the steady state voltage in different switching states can introduce extra loss and increase the stress of steady state. Moreover, the reduction of the dynamic overvoltage is highly dependent on the initial voltage of the line switching frequency device.

To simplify the analysis, the loop inductances are neglected as they only affect the dynamic transient. The drain-source voltage of S_{3L} is modeled as a trapezoidal pulse with overvoltage. The equivalent circuit is plotted in Fig. 6-18.

In addition, the non-linear output capacitance is expressed as two discrete values [66]:

$$C_{oss} = \begin{cases} nC & 0 \leq v_{ds} \leq \frac{V_{dc}}{m} \\ C & v_{ds} > \frac{V_{dc}}{m} \end{cases} \quad (n, m > 1) \quad (6-15)$$

where m and n are the coefficients that determine the intrinsic threshold and the non-linearity of the capacitance, which can be obtained from the device's datasheet.

The operating waveforms are shown in Fig. 6-19. Assuming the voltage across S_{3L} , S_{2H} and S_{3H} is zero at t_0 . From t_0 to t_1 , v_{ds_3L} rises from 0 to V_{pk1} , which includes the overvoltage caused by the loop inductance. v_{ds_2H} follows v_{ds_3L} and increases to its peak value while v_{ds_3H} keeps at zero. At t_1 , C_{2H} and C_{3H} equal to C and nC .

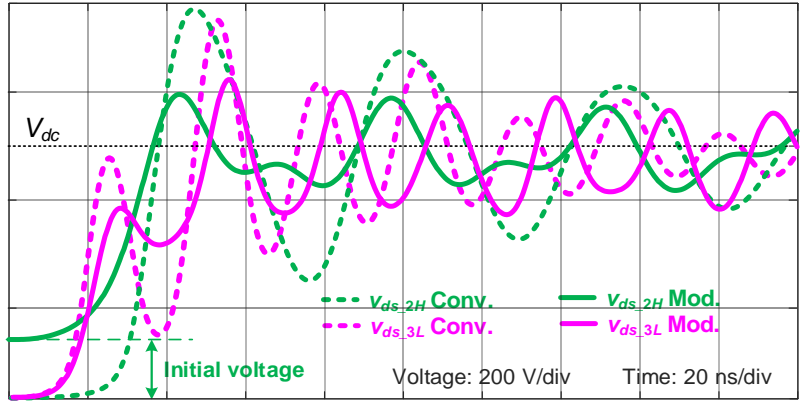


Fig. 6-17. Transient waveforms with different modulations based on established model.

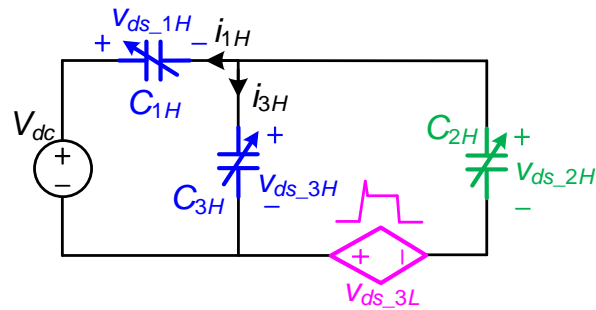


Fig. 6-18. Equivalent circuit of phase leg with modified modulation for steady state analysis.

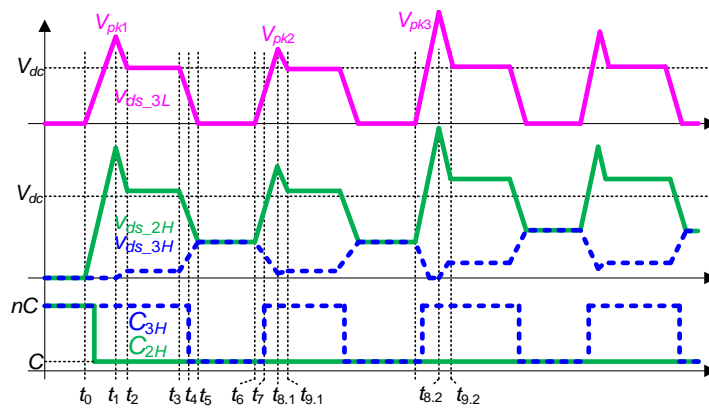


Fig. 6-19. Conceptual operating waveforms with modified modulation.

From t_1 to t_2 , v_{ds_3L} finishes the dynamic resonance and drops back to V_{dc} . The relationship between v_{ds_3H} and v_{ds_2H} can be expressed as

$$v_{ds_3H}(t_2) = \frac{1}{nC} \int_{t_1}^{t_2} i_{3H} dt = v_{ds_2H}(t_2) - V_{dc} = V_{pk1} - V_{dc} - \frac{n+1}{nC} \int_{t_1}^{t_2} i_{3H} dt \quad (6-16)$$

Assuming $V_{pk1} = (k_1+1)V_{dc}$ and $0 < k_1 < 1$, v_{ds_3H} and v_{ds_2H} at t_2 can be calculated by

$$\begin{cases} v_{ds_3H}(t_2) = \frac{1}{nC} \int_{t_1}^{t_2} i_{3H} dt = \frac{k_1}{n+2} V_{dc} \\ v_{ds_2H}(t_2) = v_{ds_3H}(t_2) + V_{dc} = \left(1 + \frac{k_1}{n+2}\right) V_{dc} \end{cases} \quad (6-17)$$

The voltage distribution at t_3 equals to that at t_2 . From t_3 , v_{ds_3L} and v_{ds_2H} decrease, while v_{ds_3H} increases. At t_4 , v_{ds_3H} increases to V_{dc}/m , where C_{3H} changes from nC to C .

$$v_{ds_3H}(t_2) + \frac{1}{nC} \int_{t_3}^{t_4} i_{3H} dt = \frac{V_{dc}}{m} \quad (6-18)$$

v_{ds_3H} and v_{ds_2H} at t_4 are

$$\begin{cases} v_{ds_3H}(t_4) = \frac{1}{m} V_{dc} \\ v_{ds_2H}(t_4) = v_{ds_2H}(t_2) - \frac{n+1}{nC} \int_{t_3}^{t_4} i_{3H} dt = \frac{m(k_1+1) - n - 1}{m} V_{dc} \end{cases} \quad (6-19)$$

At t_5 , v_{ds_3L} decreases to 0. S_{2H} and S_{3H} are in parallel, and $v_{ds_2H} = v_{ds_3H}$.

$$v_{ds_3H}(t_4) + \frac{1}{C} \int_{t_4}^{t_5} i_{3H} dt = v_{ds_2H}(t_4) - \frac{2}{C} \int_{t_4}^{t_5} i_{3H} dt \quad (6-20)$$

$$v_{ds_3H}(t_5) = v_{ds_2H}(t_5) = \frac{m(k_1+1) - n + 1}{3m} V_{dc} \quad (6-21)$$

At t_6 , v_{ds_3L} rises again. At t_7 , v_{ds_3H} drops to V_{dc}/m , where C_{3H} changes from C to nC .

$$v_{ds_3H}(t_5) - \frac{1}{C} \int_{t_6}^{t_7} i_{3H} dt = \frac{V_{dc}}{m} \quad (6-22)$$

v_{ds_3H} and v_{ds_2H} at t_7 are

$$\begin{cases} v_{ds_3H}(t_7) = \frac{1}{m} V_{dc} \\ v_{ds_2H}(t_7) = v_{ds_2H}(t_5) + \frac{2}{C} \int_{t_6}^{t_7} i_{3H} dt = \frac{m(k_1+1) - n - 1}{m} V_{dc} \end{cases} \quad (6-23)$$

Because of the initial voltage, the overvoltage across S_{3L} and S_{2H} are lower than the previous switching cycle. Assuming $V_{pk2} = (k_2+1)V_{dc}$ and $0 < k_2 < k_1 < 1$, v_{ds_3H} and v_{ds_2H} at $t_{8.1}$ are

$$\begin{cases} v_{ds_3H}(t_{8.1}) = v_{ds_3H}(t_7) - \frac{1}{nC} \int_{t_7}^{t_{8.1}} i_{3H} dt = \frac{k_1 - k_2}{n+2} V_{dc} \\ v_{ds_2H}(t_{8.1}) = v_{ds_3H}(t_{8.1}) + V_{pk2} = \frac{m(k_1+1) + (n+1)(k_2+1)}{n+2} V_{dc} \end{cases} \quad (6-24)$$

After v_{ds_3L} and v_{ds_2H} recover from the dynamic peak at $t_{9.1}$, v_{ds_3H} and v_{ds_2H} are

$$\begin{cases} v_{ds_3H}(t_{9.1}) = v_{ds_3H}(t_{8.1}) + \frac{1}{nC} \int_{t_{8.1}}^{t_{9.1}} i_{3H} dt = \frac{k_1}{n+2} V_{dc} \\ v_{ds_2H}(t_{9.1}) = v_{ds_3H}(t_{9.1}) + V_{dc} = \left(1 + \frac{k_1}{n+2}\right) V_{dc} \end{cases} \quad (6-25)$$

If the overvoltage of S_{3H} increases during the load change, v_{ds_3H} drops to 0 before v_{ds_3L} and v_{ds_2H} rise to their peak value at $t_{8.2}$. As a result, the condition at $t_{8.2}$ is the same as t_1 except for the voltage peak value. Assuming $V_{pk3} = (k_3+1)V_{dc}$ and $0 < k_1 < k_3 < 1$, v_{ds_3H} and v_{ds_2H} from $t_{8.2}$ to $t_{9.2}$ follow the process during t_1 and t_2 .

$$\begin{cases} v_{ds_3H}(t_{9.2}) = \frac{1}{nC} \int_{t_{8.2}}^{t_{9.2}} i_{3H} dt = \frac{k_3}{n+2} V_{dc} \\ v_{ds_2H}(t_{9.2}) = v_{ds_3H}(t_{9.2}) + V_{dc} = \left(1 + \frac{k_3}{n+2}\right) V_{dc} \end{cases} \quad (6-26)$$

Comparing (6-15), (6-25) and (6-26), it is observed that the steady state v_{ds_3H} and v_{ds_2H} are only dependent on the highest peak v_{ds_3L} that occurs before. Higher peak v_{ds_3L} results in higher steady state v_{ds_3H} and v_{ds_2H} while lower peak v_{ds_3L} does not change steady state v_{ds_3H} and v_{ds_2H} .

The relationship between the steady state v_{ds_2H} and the overvoltage coefficient k_1 for two kinds of devices is plotted in Fig. 6-20. The initial voltage across S_{2H} when S_{3L} is ON (t_5-t_6) is always higher than V_{dc}/m , which indicates that the modified modulation can help avoid the non-linear region and reduce the overvoltage. Moreover, the steady state v_{ds_2H} when S_{3L} is off does not exceed 1.2 times of the DC voltage. Therefore, the steady state voltage stress on the device is not increased significantly.

Fig. 6-21 plots the waveforms based on the analytical model in section 6.3.5. The overvoltage at t_b is lower than t_a , but the steady state v_{ds_3H} and v_{ds_2H} does not change after t_b . On the other hand, the switching speed is manually increased at t_c and the overvoltage increases, leading to higher steady state v_{ds_3H} and v_{ds_2H} after t_c .

6.4 Experimental Results

A 500 kVA 3L-ANPC converter based on SiC MOSFETs is built to verify the analytical model. The DC bus voltage V_{dc} is 500 V, and the line-to-line output voltage RMS value is 600 V. The switching frequency of the SiC MOSFETs is 30 kHz, and the output line frequency is 3 kHz. The 900 V HT-3000 series SiC MOSFET module from Wolfspeed is used. The single phase leg of the converter prototype is shown in Fig. 6-22, and the testing platform is shown in Fig. 6-23.

The conventional modulation is implemented first and the voltage waveforms of the SiC MOSFETs in one line cycle as well as the zoom in switching transient are illustrated in Fig. 6-24. The applied gate resistance is 2.5 Ω , with which the dv/dt of v_{ds_1L} is 10 V/ns. The peak voltage of

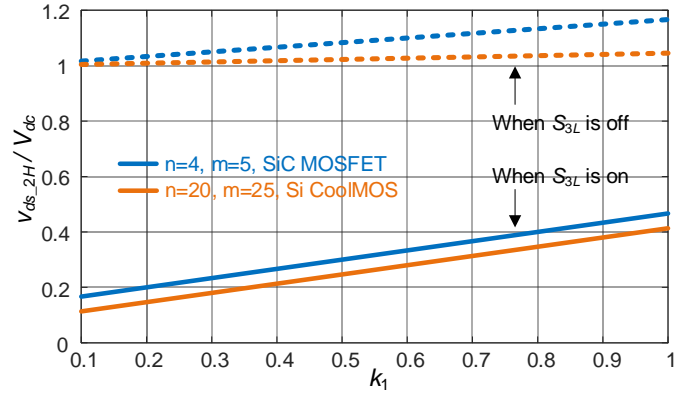


Fig. 6-20. Relationship between steady state v_{ds_2H} and k_1 with different devices.

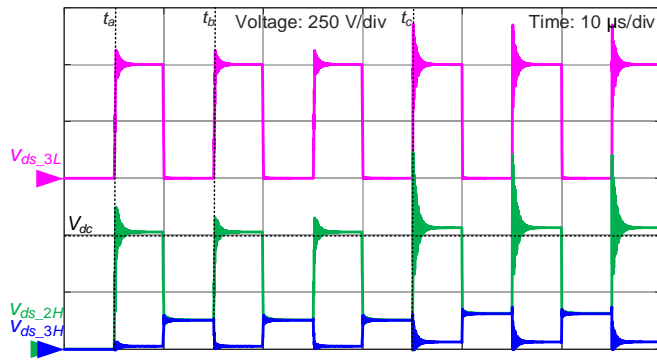


Fig. 6-21. Waveforms with modified modulation based on established model.

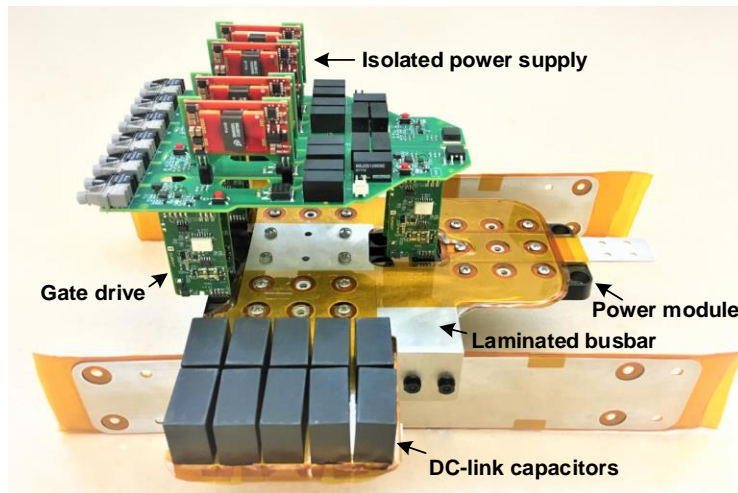


Fig. 6-22. Prototype of 3L-ANPC converter phase leg.

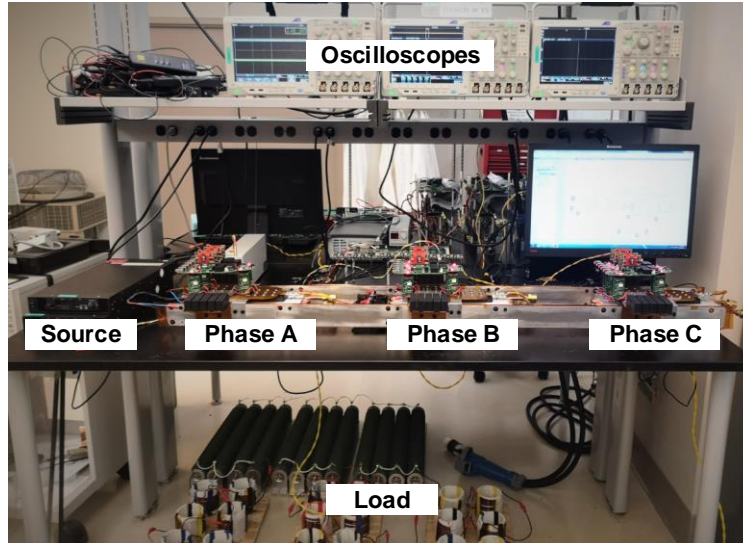


Fig. 6-23. Testing platform of 3L-ANPC converter.

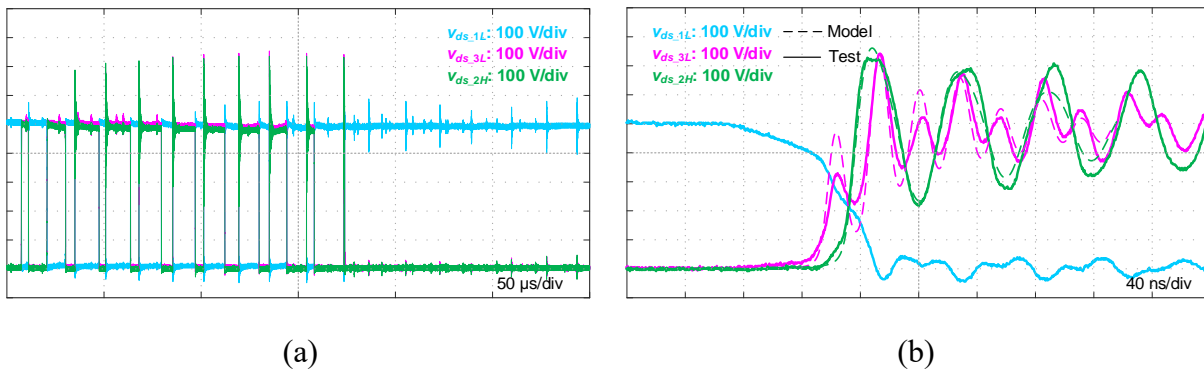


Fig. 6-24. Tested switching waveforms with conventional modulation.

(a) One line cycle. (b) Switching transient.

the high switching frequency device S_{3L} is 754 V, while that of the line switching frequency device S_{2H} is 736 V. Considering the device voltage rating of 900 V, there is not much margin to further increase the switching speed.

Fig. 6-25 plots the waveforms with the modified modulation. The peak voltage of S_{3L} and S_{2H} are 592 V and 560 V, respectively. Comparing the tested results of the conventional modulation with the same switching speed and parasitic inductances, the overvoltage is significantly reduced, which validates the attenuation of the non-linear capacitance influence analyzed in Section 6.2.2.

With the modified modulation, it is possible to increase the switching speed. Fig. 6-26 shows the tested waveforms when the gate resistance is reduced from 2.5 Ω to 1.3 Ω . The peak voltage of the two devices are 702 V and 806 V, which are still lower than the 900 V voltage rating. The envelope of the peak voltage and steady state voltage of S_{2H} is highlighted in Fig. 6-26(a). As the peak voltage increases, the steady state voltage also increases, which matches with the analysis in Section 6.3.5. The dv/dt of v_{ds_1L} achieves 18 V/ns.

From Fig. 6-24(b) to Fig. 6-26(b), the tested waveforms are compared with the analytical model results. Fig. 6-27 plots the error of device drain-source peak voltage between the model and tested results with different gate resistances. Generally, they can match with each other. The mismatch is mainly caused by three reasons:

- 1) The excitation is assumed to have an ideal trapezoidal shape in the model. However, the actual voltage rise and drop is not linear, as shown in v_{ds_1L} of Fig. 6-24(b) and Fig. 6-25(b).

- 2) The coupling between different busbar parts is complicated, and it leads to errors when using a single inductance value to represent the inductance of each part.

- 3) The model of high frequency AC resistance is not accurate when the power modules and capacitors are included, which makes the prediction of the amplitude after the first peak pulse to be less accurate. Nevertheless, the analytical model is good enough to show the trend of the overvoltage.

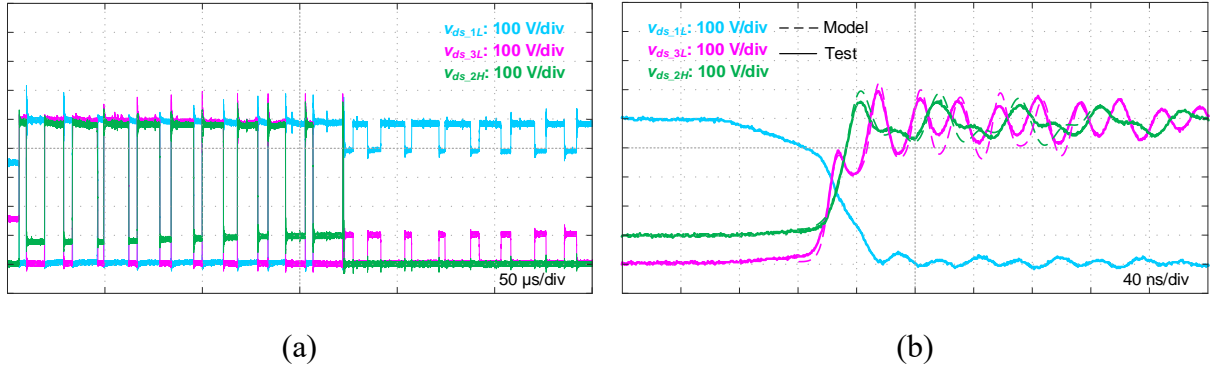


Fig. 6-25. Tested switching waveforms with modified modulation.

(a) One line cycle. (b) Switching transient.

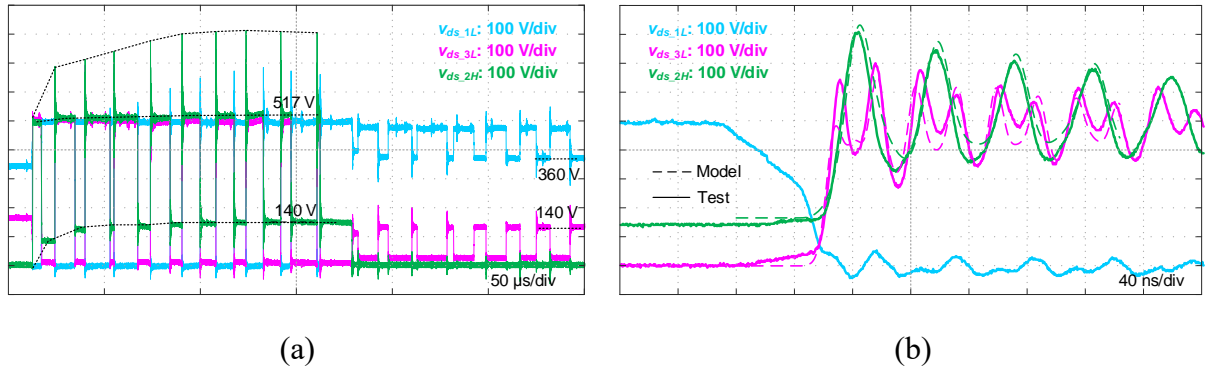


Fig. 6-26. Tested switching waveforms with modified modulation and with lower gate resistance.

(a) One line cycle. (b) Switching transient.

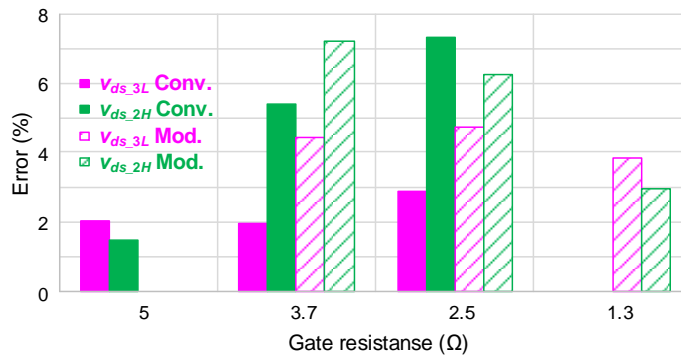


Fig. 6-27. Error of drain-source peak voltage between model estimation and tested results with different gate resistance.

6.5 Conclusion

This chapter develops the analytical model for the device drain-source overvoltage in 3L-ANPC converters. Two commutation loops exist during the switching transient, which results in coupling effect between the high and line switching frequency devices. According to the investigation with the established model, several conclusions can be drawn. 1) The non-linearity of the device output capacitance shows significant influence on the device overvoltage. 2) The line switching frequency device usually has higher overvoltage than the high switching frequency device. 3) The resonant frequency of the line switching frequency device is lower than the high switching frequency device. 4) The switching speed of the high switching frequency device is not impacted by the coupling effect of the line switching frequency device when the long loop inductance is much larger than the short loop inductance.

By turning off the non-active clamping switch, a modified modulation is developed to reduce the overvoltage. Initial voltage is built across the line switching frequency device, which helps the device output capacitance avoid the non-linear region and the overvoltage is decreased. Because of this initial voltage, the steady state drain-source voltage distribution among the non-active switches is also analyzed. Extra output capacitance loss is introduced due to the initial voltage, but it can be neglected compared to the reduced switching loss with the modified modulation.

A 500 kVA 3L-ANPC converter with 30 kHz switching frequency based on SiC MOSFET power modules is built and tested. The overvoltage model of the conventional and modified modulations are verified. With the modified modulation, 162 V and 176 V overvoltage reduction is achieved for the high and line switching frequency devices.

7 Layout Design and Realization for Three-Level Converters

In addition to modeling the device overvoltage and reducing it with control strategies, the more straightforward solution to decrease the overvoltage is to shrink the parasitics, especially the loop inductance of the power loop. For three-level converters, the power loop layout is more complicated due to the existence of multiple commutation loops. This chapter first briefly introduces the basic theories of magnetic cancellation. Then based on the loop analysis, the design criteria of two main types of three-level converters is provided. The detailed design examples are given for both the PCB and busbar layout of the three-level active neutral point clamped (3L-ANPC) converter. Moreover, the procedure of building a laminated busbar for a high power 3L-ANPC converter is presented, which includes material selection, cutting, insulation implementation and soldering.

This part of work is published in the conference paper [164].

7.1 Basic Theories

For a closed electric loop, the current always follows the path with lowest impedance [17]. The resistance is dominant at low frequency, so the return current tends to follow the shortest geometric path on a plane as shown in Fig. 7-1. However, at high frequency, the inductance is dominant and the current follows the path with lowest inductance. As shown in Fig. 7-1, the current return path lies directly beneath the outgoing path instead of the shortest geometric path. This phenomenon is related to the magnetic cancellation effect.

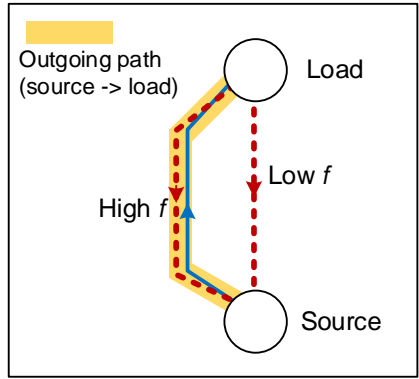


Fig. 7-1. Current flow path at low and high frequency.

With Ampere's law, the curl of the magnetic field \mathbf{B} is equal to the product of the permeability μ and current density \mathbf{J} :

$$\nabla \times \mathbf{B} = \mu \mathbf{J} \quad (7-1)$$

With Faraday's law, the curl of the electric field \mathbf{E} is equal to the partial derivative of the magnetic field \mathbf{B} :

$$\nabla \times \mathbf{E} = -\frac{\partial}{\partial t} \mathbf{B} \quad (7-2)$$

According to the definition of inductance:

$$v = L \frac{di}{dt} \quad (7-3)$$

the magnetic field gives rise to the inductance. Thus, the direct way to reduce the inductance is to cancel the magnetic field.

For a current loop with outgoing and returning paths, there are two typical ways for layout. The first one is to laterally place the two paths side by side in the same plane, which is shown in Fig. 7-2(a). The other one shown in Fig. 7-2(b) is to stack the paths in two planes in two horizontal

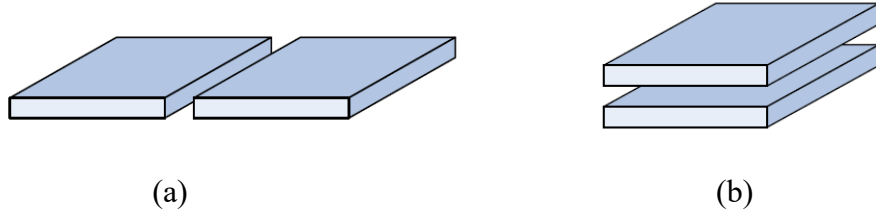


Fig. 7-2. Typical ways of layout. (a) Lateral placement. (b) Vertical placement.

planes. From the perspective of magnetic cancellation, the vertical placement can achieve better performance. As shown in Fig. 7-3, with opposite current directions on two plates, the generated magnetic fields also have opposite directions, which cancel with each other. Considering the overlap of the magnetic fields, the vertical placement can apparently achieve more cancellation.

For a current loop with two plates like Fig. 7-2, the parasitic inductance of one plate includes two parts: self-inductance and mutual inductance.

The self-inductance L of one plate can be calculated with the equation from [92], [165]

$$L = \frac{\mu_0 \mu_r l}{\pi} \left(\frac{1}{8} + \frac{2h}{h+w} \right) \quad (d \ll h \parallel d+h \ll w) \quad (7-4)$$

where μ_0 and μ_r are the vacuum permeability and the relative permeability of the insulation material; l , w and h are the length, width and thickness of the plate; d is the distance between two adjacent plates.

The mutual inductance M between two plates is calculated as [92], [165]

$$M = \frac{\mu_0 \mu_r l h}{\pi \sqrt{4(d+h)^2 + kw^2}} \cos \varphi \quad (7-5)$$

where k is the correction coefficient and φ is the angle between the current direction of two plates.

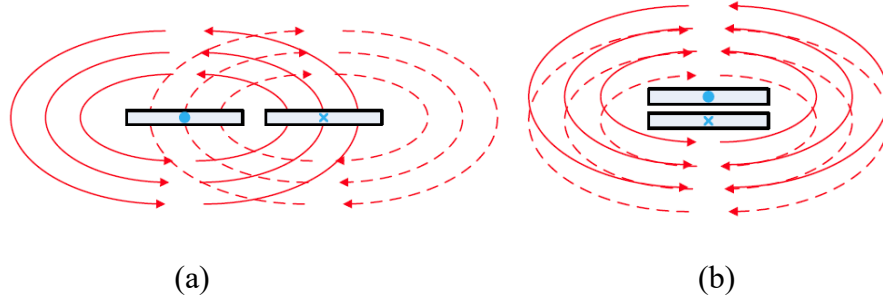


Fig. 7-3. Magnetic field distribution. (a) Lateral placement. (b) Vertical placement.

If the two plates have the same shape and the current directions are opposite, the magnetic fields generated by the currents on the two plates have a cancelling effect. In such case, the total parasitic inductance of the busbar is

$$L_{sum} = \frac{\mu_0 \mu_r l}{\pi} \left(\frac{1}{4} + \frac{4h}{h+w} - \frac{2h}{\sqrt{4(d+h)^2 + kw^2}} \right) \quad (7-6)$$

From (7-6), to minimize the parasitic inductance, it is preferred to increase the mutual inductance between two adjacent busbar layers. The method is to decrease the distance, and increase the overlap area of the two plates, which can match with the observation from Fig. 7-2. Also, this explains the reason why the returning path lies directly beneath the outgoing path at high frequency in Fig. 7-1, as the loop inductance is minimized due to the magnetic cancelling effect.

7.2 Layout Design Methodology for Three-Level Converters

Multiple commutation loops exist in 3L converters and it requires special attention to optimize the layout design. According to the structure of the topology, 3L converters can be categorized into two main groups: converters with symmetric and asymmetric commutation loops.

7.2.1 Converter with Symmetric Commutation Loops

A typical example of the 3L converter with symmetric commutation loops is the 3L T-type converter. Fig. 7-4 plots the configuration of a single phase leg of the 3L T-type converter with commutation loops highlighted. The phase leg contains two high frequency commutation loops. It is noted that from the schematic point of view, the two loops have identical and symmetric structure, and the sources of the two loops are different decoupling capacitors. For such configuration, the layout criteria and procedure are as follows.

1) Determine the available paths. From Fig. 7-4, there are four paths in total for layout: Path 1 connects the upper side decoupling capacitor with the drain of upper side switch S_H . Path 2 connects the lower side decoupling capacitor with the source of lower side switch S_L . Path 3 connects the common source switch S_N with the other two switches. Path 4 connects the decoupling capacitors with S_N .

2) Find the shared paths by two loops and select them as the returning path. Path 3 and 4 are shared by both commutation loops. Thus, they can be located in one plane to serve as the returning path for both loops.

3) Locate the rest of the paths in one plane and place them laterally. Path 1 and 2 belongs to two different loops so they should be placed side by side in one plane. The layout of Path 1 and 2 should be identical so that the parasitics are the same for two loops.

4) Increase the area of the returning path to fully overlap with both outgoing paths. Based on the above analysis, the outgoing and returning path should be overlapped to maximize the magnetic cancellation.

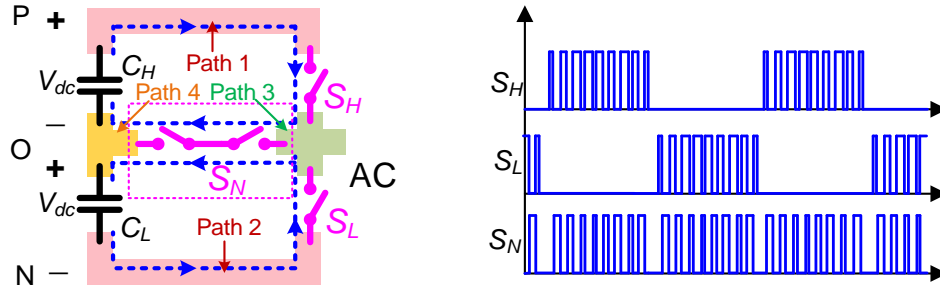


Fig. 7-4. Phase leg of 3L T-type converter and the corresponding modulation.

Based on the criteria, the layout configuration of 3L T-type converter phase leg is drawn in Fig. 7-5. Note that the criteria only provide the general guidance, and the layout in a real case should be modified with different voltage/current ratings and device packaging.

7.2.2 Converter with Asymmetric Commutation Loops

For 3L converters with asymmetric commutation loops, a typical example is the 3L-ANPC converter. The loop analysis has already been presented in Section 6.2.1. The phase leg of the 3L-ANPC converter is plotted in Fig. 7-6 again and two commutation loops are included. Different from the converter with symmetric loops, here the two loops have different length and are no longer symmetric, which makes the layout more complicated. In addition, the two loops share the same decoupling capacitor as the source.

In such structure, the basic criteria still follow the aforementioned rules in symmetric loops. However, special attention should be paid to the longer loop design as it includes more paths and devices. Detailed design examples for both PCB and busbar layout are presented below.

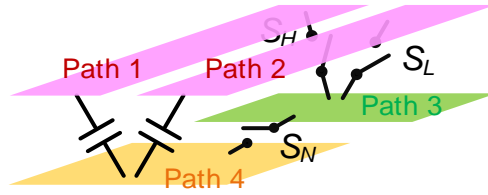


Fig. 7-5. Layout configuration of 3L T-type converter phase leg.

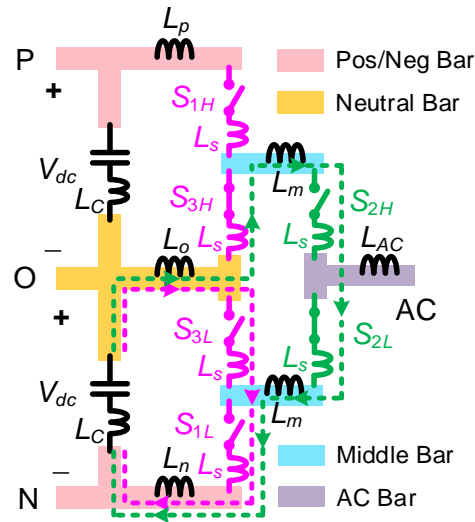


Fig. 7-6. 3L-ANPC converter single phase considering layout and parasitics.

7.3 PCB Layout with Discrete Devices for 3L-ANPC Converter

This section mainly compares the lateral and vertical layout for 3L-ANPC converter phase leg in PCB design. The detailed layout optimization will be provided in busbar design in the next section.

7.3.1 Lateral Loop Design

Fig. 7-7 presents the example of lateral layout design for a 20 kW SiC MOSFET based 3L-ANPC converter phase leg. Generally, the placement of the power devices follows the circuit

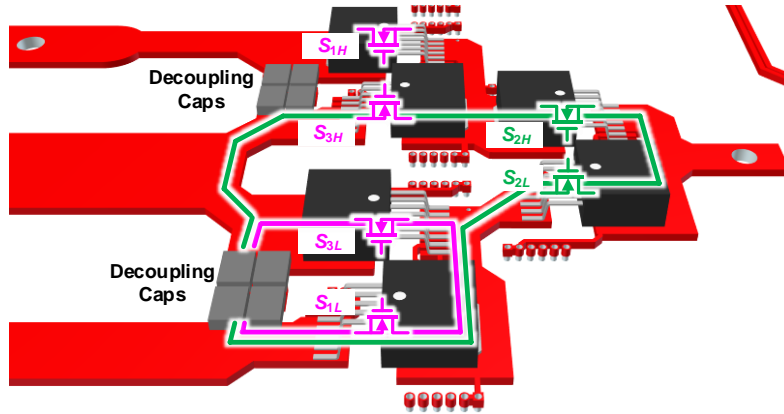


Fig. 7-7. Lateral layout PCB design for 3L-ANPC phase leg.

schematic drawing, where two line switching frequency devices are next to the four high switching frequency devices. This layout is straightforward and can utilize multiple copper layers to conduct current in parallel. However, the penalty is that the whole loop is at one layer and unavoidably generates a large area.

7.3.2 Vertical Loop Design

For the vertical layout in Fig. 7-8, all six devices are located in a line and the loops are vertical to the PCB layers. With such design, the outgoing and returning paths are overlapped, and the magnetic cancellation between the PCB layers is maximized for both commutation loops. Based on the simulation in Ansys Q3D, the loop inductance of the long loop with the lateral layout is 57 nH, while that in the vertical layout is 12 nH, which indicates the superiority of the vertical layout.

7.4 Busbar Layout with Power Modules for 3L-ANPC Converter

In high power applications, power modules are normally implemented and busbars are the main connectors between different components. Extensive work has been conducted for busbars

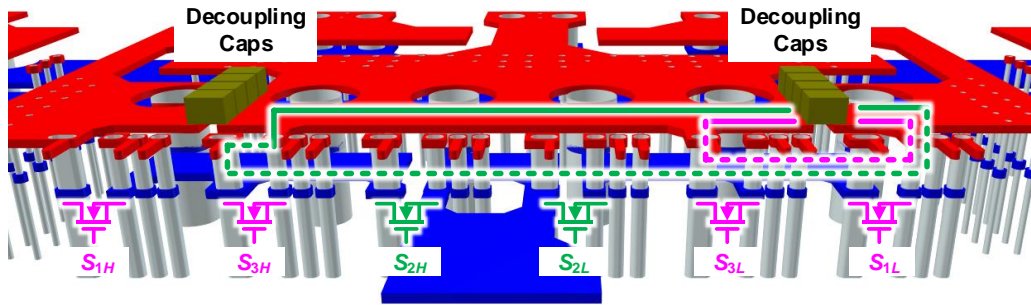


Fig. 7-8. Vertical layout PCB design for 3L-ANPC phase leg.

design, and laminated structure is usually used [94], [95]. An example of designing a two-layer busbar for a 3L-ANPC converter phase leg is given below.

7.4.1 Busbar Layout Considering Multi-Loops in 3L-ANPC Converter

According to (7-5) and (7-6), it is preferred to increase the mutual inductance between two adjacent busbar layers. In other words, two busbar parts with opposite current directions in Fig. 7-9 should be overlapped to form the laminated architecture. To simplify the design and reduce the cost, here a two-layer laminated structure is adopted for the required busbar.

In terms of the short commutation loop, it only includes two busbar parts: the neutral busbar and the negative (or positive) busbar. So the two parts should be laminated in two layers.

The long commutation loop is more complicated and critical. The design criteria in Section 7.2 is followed.

1) Four busbar parts are included in the loop shown in Fig. 7-6: the neutral busbar (yellow), negative busbar (red) and two middle busbars (blue).

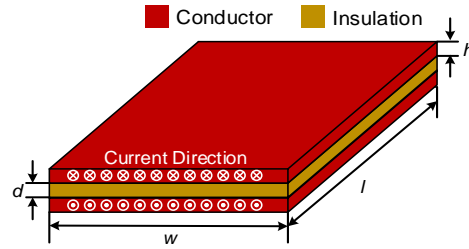


Fig. 7-9. Typical structure of two-layer busbar.

2) The shared loop is chosen as the returning path. Here, the neutral and negative busbar are shared by both loops. The neutral busbar is selected as the returning path because it is also the shared path for the other two commutation loops in the upper side of the phase leg.

3) The other busbar parts should be located in the other layer.

4) The neutral busbar should cover the area of all the other busbar parts.

Considering the overall system layout including the placement of SiC MOSFET power modules and the capacitors, Fig. 7-10 plots the conceptual 3D view of the busbar layout for the long commutation loop. The middle busbars (blue) and the negative (orange) busbar are placed in the same layer. The neutral busbar (yellow) is a whole plate and serves as the returning path of the commutation loop. With such design, the busbar parts are coupled and the magnetic field can be canceled with the opposite current flowing direction, resulting in lower loop inductance.

The equivalent circuits of the commutation loops considering the busbar structure are illustrated in Fig. 7-11. For the short commutation loop, the negative and neutral busbar are coupled and the mutual inductance is M_{on} . For the long loop, the negative and middle busbars are coupled with the neutral busbars. The mutual inductance between middle and neutral busbars is M_{om} . Note that the effective self-inductance of the neutral busbar in the short loop (L_{o1}) is smaller than that in the long loop ($L_o=L_{o1}+L_{o2}+L_{o3}$).

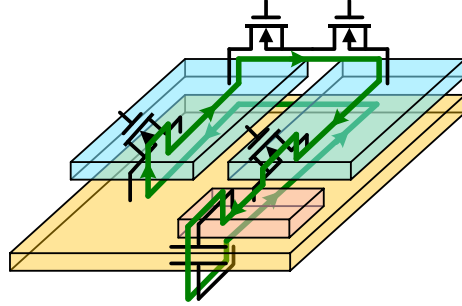


Fig. 7-10. 3D view of busbar layout with long commutation loop.

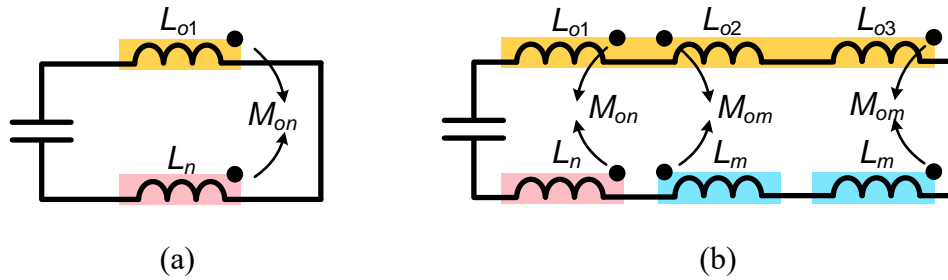


Fig. 7-11. Equivalent circuits of commutation loops. (a) Short loop. (b) Long loop.

Based on Fig. 7-11, the loop inductances of short loop L_{st} and long loop L_{lg} can be written as

$$\begin{cases} L_{st} = L_C + L_{o1} + L_n - 2M_{on} + 2L_s \\ L_{lg} = L_C + L_o + L_n + 2L_m - 2M_{on} - 4M_{om} + 4L_s \end{cases} \quad (7-7)$$

where L_C is the ESL of decoupling capacitors, L_s is the power module stray inductance, and L_n is the negative busbar self-inductance.

7.4.2 DC-Link Capacitor Selection and Placement

Film capacitors should be used for the DC-link capacitor due to their low ESL. There are two options for the capacitor selection. One is to choose a single bulky capacitor, and the other is to use multiple capacitors in parallel.

Table 7-1 shows the comparison of the examples of the two options. To achieve 100 μF capacitance value, ten smaller capacitors need to be paralleled. However, considering the ESL, weight and price, paralleling capacitors is a better choice. The challenge is to carefully place the capacitors to reach minimized inductance and good current balancing. Ideally, no extra decoupling capacitor is needed as the overall inductance of the paralleled capacitors is low enough.



As recommended in [166], the adjacent two paralleled capacitors are placed oppositely. Fig. 7-12 sketches the top view of the placement of the capacitors on the busbar plate. The red line represents the current on the top layer (positive/negative busbar), and the yellow dotted line is the current on the bottom layer (neutral busbar), while the dark dashed line is the current inside the capacitors. For the left side capacitor, the current flows into the capacitor on the bottom layer, while the current flows out of the right side capacitor through the top layer. Therefore, current on two laminated plates is in opposite directions, which helps the magnetic field cancellation and reduces the total inductance.

Fig. 7-13 shows the designed busbar plate for DC-link capacitors. There are ten capacitors in two rows. The orange plate is the negative/positive busbar while the yellow one is the neutral busbar. The finalized busbar design for single phase is shown in Fig. 7-14.

7.5 Busbar Fabrication with Aluminum

After the design is determined, busbar manufacturers can help build the busbar. However, it usually takes long lead time and the price can be expensive. To reduce the risk, it would be better to fabricate the busbar prototype in the lab and verify its function before sending it to manufacturers. This section discusses the procedure of making laminated busbars with aluminum.

Table 7-1. Comparison of DC-link capacitors.

| | Part | Capacitance | ESL | Weight | Price | Required Qty |
|---|------------------|-------------|-------|--------|--------|--------------|
|  | FFVE6K0107K | 100 μ F | 25 nH | 350 g | \$ 60 | 1 |
|  | MKP1848C61060JK2 | 10 μ F | 15 nH | 15 g | \$ 4.2 | 10 |

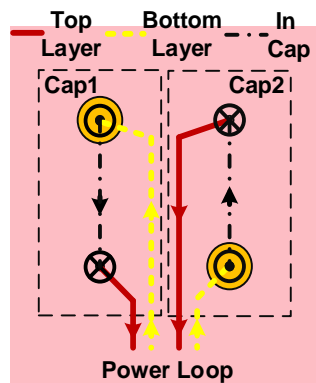


Fig. 7-12. Top view of busbar with capacitors placement and current flowing directions.

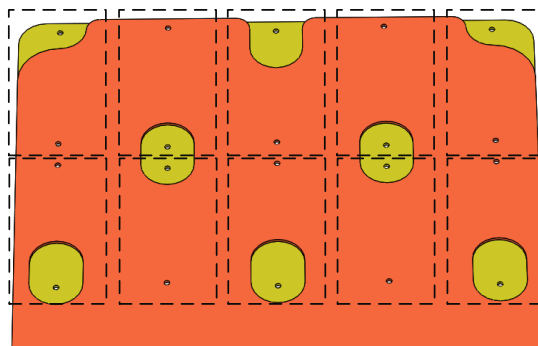


Fig. 7-13. Designed plate for capacitors.

Note that the fabrication with copper is similar or even simpler because soldering on aluminum is tricky and requires special attention, which will be introduced in Section 7.5.3.

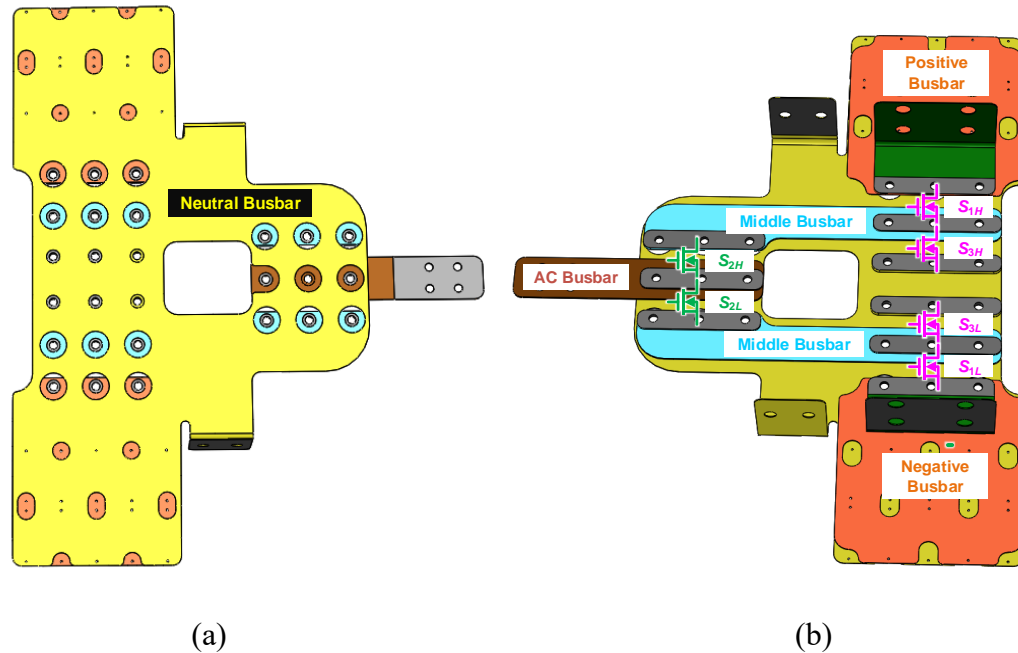


Fig. 7-14. Designed laminated busbar for single phase. (a) Top view. (b) Bottom view.

7.5.1 Cutting

Two methods are commonly used for metal cutting: laser and water jet. Laser cutters use a focused laser, such as a CO₂ gas laser, to generate the energy to burn and cut the material. On the other hand, as the name suggests, water jet cutters rely on pressurized water to hit the material with very high speed. The beam of the two methods are illustrated in Fig. 7-15, and the performance comparison is given in Table 7-2. It can be concluded that laser is more precise than water jet. The reason is that abrasives like garnets and aluminum oxide are usually added to increase the cutting ability. In addition, water jet cutter takes more time and cost to cut the same length. Therefore, laser is more suitable for busbars with thin metals. However, water jet can also be used for most applications if laser is not applicable.



(a)

(b)

Fig. 7-15. Metal cutting methods. (a) Water jet. (b) Laser [167].

Table 7-2. Performance comparison between typical laser and water jet.

| | Thickness (inch) | Min. size (inch) | Tolerance (inch) | Speed (inch/min) | Smoothness | Cleaning | Cost (\$/h) |
|-----------|------------------|------------------|------------------|------------------|------------|----------|-------------|
| Laser | 0.12-0.4 | 0.006 | 0.002 | 20-70 | High | Easy | 13-20 |
| Water jet | 0.4-2 | 0.02 | 0.008 | 1-15 | Low | Hard | 15-30 |

After the cutting, edges are preferred to be smoothed with sand papers or filing machines to avoid the high electric field around sharp corners.

7.5.2 Insulation

For medium voltage high power converters, insulation is extremely important in terms of reliability and safety. Layers in laminated busbar are close to each other for loop inductance reduction. As a result, partial discharge and arcing can occur when the busbar insulation is not well implemented. Thus, creepage and clearance need to be calculated, and insulation should be

designed and applied to the surface area between two layers, the edges and corners of the busbar, and the inner edge of the screw holes.

Fig. 7-16 draws the side view of the laminated busbar with insulation. The insulation paper is used on the surface of the metal bars and for edge sealing. In addition, epoxy is applied to fill the inner edge of the screw hole and the outside edge of the busbar. It is also feasible not to seal the edge as long as the clearance and creepage distance can meet the requirement of the standard.

7.5.2.1 Insulation Material Selection

With the basic insulation design, it is critical to select the proper insulation materials. For insulation papers, the key properties are the dielectric capability and the operating temperature range. Four types of commonly used insulation papers are compared in Table 7-3. It is noted that Kapton has highest dielectric strength as well as widest temperature range. So Kapton is adopted in this dissertation, but other papers are also applicable if the dielectric and temperature performance can be guaranteed.

Compared to insulation papers, the selection of epoxy materials is more complicated because it is not only related to the dielectric and temperature characteristics, but also dependent on the feasibility of implementation. The process of applying epoxy includes mixing, coating, vacuuming and curing, and the detailed procedure will be introduced in the next section. The key properties of three epoxy materials are listed in Table 7-4. The viscosity mainly influences the difficulty of vacuuming. If the epoxy compound is too viscous, it is more difficult to remove the air from the epoxy. Pot life is defined as the amount of time it takes for an initial mixed viscosity to double or quadruple. The processing should be completed, and the curing should start before the pot life ends.

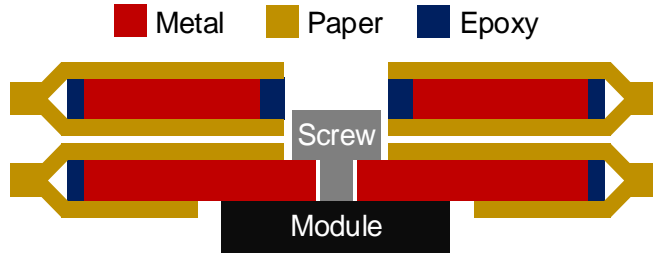


Fig. 7-16. Cross section of laminated busbar layers with insulation.

Table 7-3. Properties of commonly used insulation papers.

| Name | Material | Dielectric strength (kV/mil) | Operating Temp. (°C) |
|--------|----------------------------|------------------------------|----------------------|
| Tedlar | Polyvinyl fluoride | 3.5 | -72~107 |
| Mylar | Polyethylene terephthalate | 7 | -250~150 |
| Kapton | Polyimide | 7.7 | -269~400 |
| Nomex | Polyamide polymer | 0.4 | -196~250 |

Table 7-4. Properties of epoxy materials.

| Name | Dielectric strength (V/mil) | Viscosity (cPs) | Pot life (h) | Curing time (h) | Curing Temp. (°C) | Max operating Temp. (°C) |
|---------------|-----------------------------|-----------------|--------------|-----------------|-------------------|--------------------------|
| Stycast 2662 | 420 | 40000 | 24 | 3 | 150 | 230 |
| EPO-TEK 301-1 | 370 | 80-100 | 1-2 | 2 | 65 | 300 |
| EPO-TEK 301-2 | 410 | 225-425 | 8 | 3 | 80 | 300 |

Considering the required time for coating and vacuuming, it is not recommended to use the epoxy with very short pot life. Here the EPO-TEK 301-2 with moderate viscosity and pot life is selected.

7.5.2.2 Insulation Implementation

The key of implementing insulation papers and epoxy is to remove the voids. Voids, namely dusts or air bubbles, can significantly deteriorate the dielectric capability and are the main source of causing partial discharge or even voltage breakdown.

The implementation of insulation papers is straightforward and is like applying screen protectors to the screen of mobile phones. First, use a piece of soft cloth to clean the surface of the busbar with a mild solvent like eyeglass cleaner or alcohol. Second, gradually apply the sticky side of the insulation paper to the busbar surface. At the same time, use a card with hard edges to wipe the air out from under the paper.

The implementation of epoxy requires four steps: mixing, coating, vacuuming and curing. First, fully mix the compounds of the epoxy in a container like a petri dish. Note that during this process, air is also mixed with the compounds even though it is difficult to directly observe it.

Second, apply an adhesive sheet to one side of the busbar, and carefully fill the screw holes with the mixed epoxy compound from the other side.

Third, put the busbar into a vacuum chamber and start deair. Fig. 7-17 shows the busbar inside the vacuum chamber. A large number of air bubbles occur and break. This whole process can last from several minutes to more than one hour depending on the epoxy characteristic and the ability of the vacuum chamber. The comparison of completed busbar sample with and without vacuuming is illustrated in Fig. 7-18. Apparently, many voids remain inside the epoxy if the vacuuming is not applied.

Fourth, move the busbar to an oven and cure it under required temperature.



Fig. 7-17. Busbar under vacuuming inside vacuum chamber.

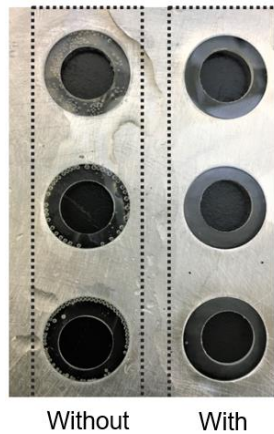


Fig. 7-18. Comparison between epoxy with and without vacuum.

7.5.3 Soldering

Generally, it is difficult to solder on aluminum because the tough oxides on the metal surface prevent wetting [168]. Meanwhile, different aluminum alloys also show different solderability as listed in Table 7-5. When selecting the aluminum alloy for applications requiring soldering, alloys with high solderability like 1000 and 3000 series are preferred. Special solder and flux are also mandatory for soldering on aluminum. It has been proved that Zn based lead free solder such as

Table 7-5. Solderability of aluminum alloys.

| Series | Alloy | Solderability |
|--------|---------|---------------|
| 1000 | Pure Al | High |
| 2000 | Al, Cu | Fair |
| 3000 | Al, Mn | High |
| 4000 | Al, Si | Low |
| 5000 | Al, Mg | Low |
| 7000 | Al, Zn | High |

Sn91Zn9 cooperating with Superior No. 1260 flux can be used for aluminum [169]. Moreover, it is worth highlighting that the melting temperature of the solder should be lower than the operating temperature of the insulation paper and epoxy if soldering is done after the insulation implementation. Fig. 7-19 presents the solder joints for the DC-link capacitors on the busbar based on 3003 aluminum alloy.

A laminated busbar following the process mentioned above is developed for a 500 kVA 3L-ANPC converter. Fig. 7-20 shows the fabricated busbar of one phase leg, which follows the design in Fig. 7-14.

7.6 Simulation and Experimental Results

The designed busbar is simulated in Ansys Q3D to extract the parasitics. Fig. 7-21 illustrates the surface current density of the neutral bar at 20 MHz. Remarkably, the current does not flow along the shortest path A. Instead, it follows path B, which overlaps with the middle bars in Fig. 7-14(b).



Fig. 7-19. Soldering joints of capacitors on aluminum busbar.



Fig. 7-20. Bottom view of fabricated busbar for a 500 kVA 3L-ANPC converter phase leg.

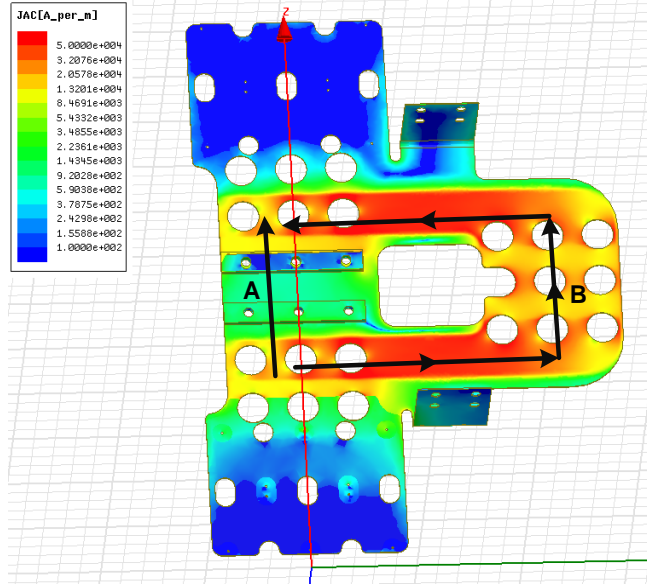


Fig. 7-21. Surface current density on neutral busbar.

The equivalent circuit of the busbar with parasitics was extracted and simulated in Saber along with the SiC MOSFET module model. Fig. 7-22 shows the turn-on switching transient of the MOSFET drain-source voltage. The ringing frequency of the short loop is 34.5 MHz while that of the long loop is 18.9 MHz. Based on the output capacitance value from the SiC MOSFET datasheet, the parasitic inductances of the short and long loop can be calculated as 6.5 nH and 17.5 nH, respectively.

Current sharing can be a potential issue for multiple paralleled DC-link capacitors. Fig. 7-23 plots the simulated current waveforms of ten paralleled DC-link capacitors in one switching cycle. The current RMS value of each capacitor is about 9 A and the largest RMS difference among the capacitors is 0.6 A, which indicates good current balancing in capacitors.

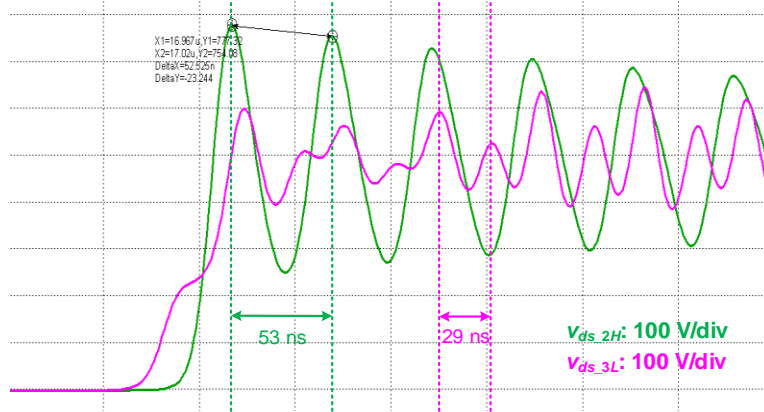


Fig. 7-22. Simulated switching transient waveform with module model and extracted busbar equivalent circuit.

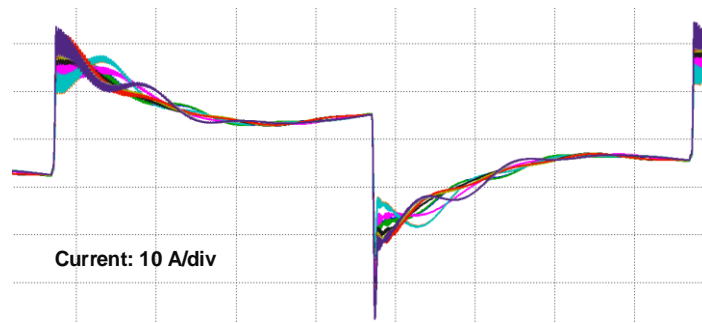


Fig. 7-23. Simulated current waveforms of ten paralleled DC-link capacitors during one switching cycle.

With the fabricated busbar, the impedance analyzer E4990A from Keysight is used to measure the impedance of the busbar loops. From Fig. 7-24, the measured short and long loop inductances are 2.5 nH and 10 nH, respectively. Considering the inductance of one power switch L_s is around 4 nH, the result can match with the simulation in Fig. 7-22.

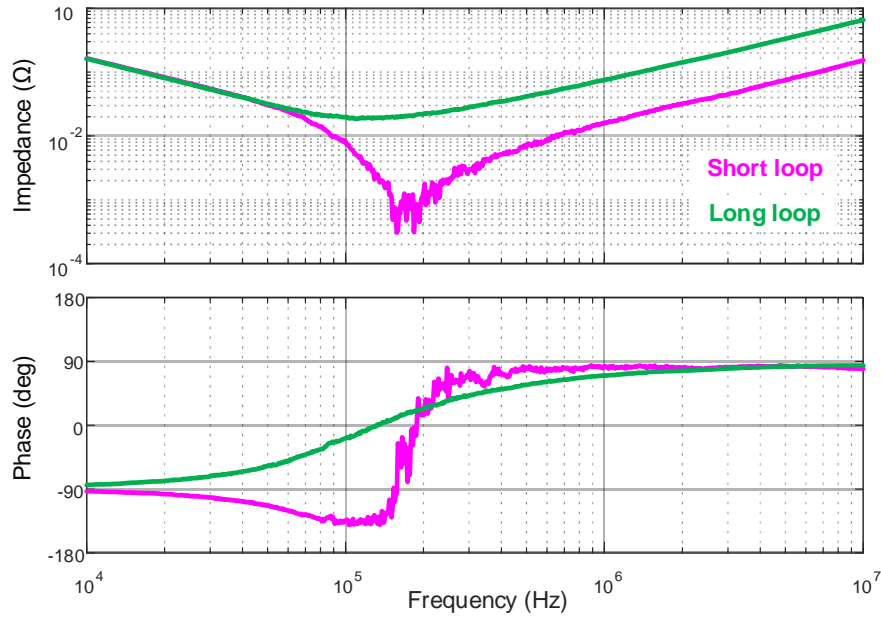


Fig. 7-24. Measured impedance spectra of busbar.

The fabricated busbar is tested with the 500 kVA 3L-ANPC converter shown in Section 6.4. Five line cycles are generated and the tested output line-to-line voltage and phase current waveforms at full voltage and load condition are plotted in Fig. 7-25.

The tested switching transient waveforms are shown in Fig. 7-26. The ringing frequencies of the short and long loops are 35.7 MHz and 17.2 MHz, which are very close to the simulation result in Fig. 7-22. The peak drain-source voltage of S_{2H} and S_{3L} are 736 V and 754 V, respectively, which is lower than the voltage rating of the SiC MOSFET (900 V). No extra snubber circuit is required in the converter.

Table 7-6 compares the loop inductances of the busbar in this dissertation and those in other NPC type converters. The proposed busbar achieves significantly lower parasitic inductances for both short loop and long loop.

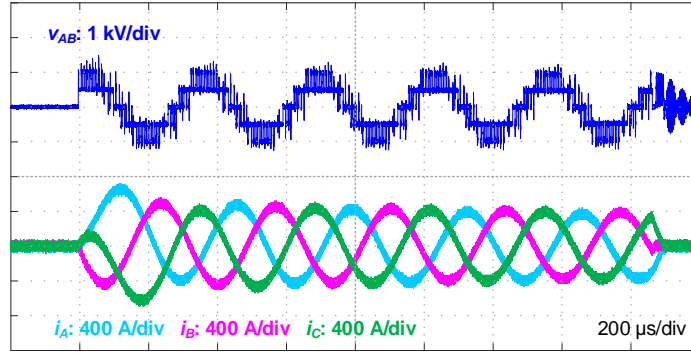


Fig. 7-25. Tested output waveforms of 3L-ANPC converter.

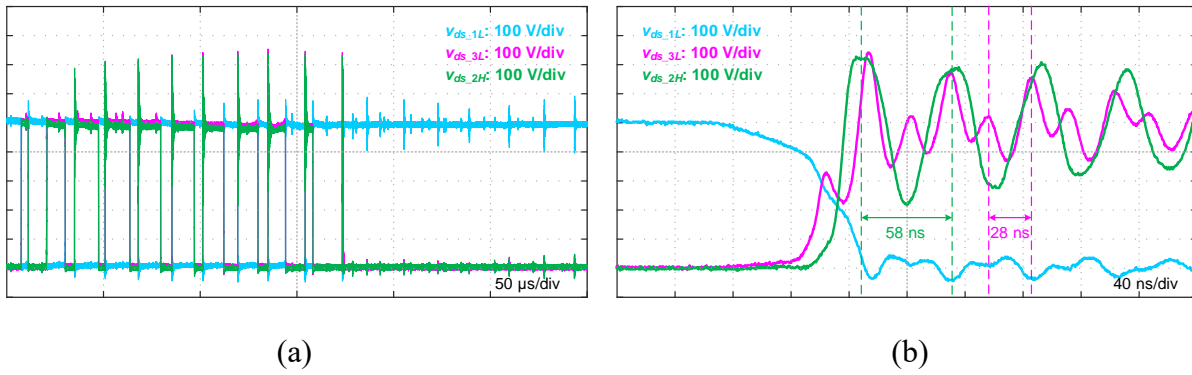


Fig. 7-26. Tested switching waveforms with fabricated busbar.

(a) One line cycle. (b) Switching transient.

Table 7-6. Loop inductance comparison.

| | Proposed | [74] | [159] | [98] | [99] | [100] | [101] |
|-----------------|----------|------|-------|------|------|-------|-------|
| Power (kVA) | 500 | 200 | 1000 | 750 | N/A | N/A | 475 |
| DC voltage (kV) | 1 | 1.2 | 2.4 | 2 | N/A | N/A | 1.1 |
| Short loop (nH) | 6.5 | 55 | N/A | 78 | 96 | 48 | 95 |
| Long loop (nH) | 17.5 | 135 | 115 | 208 | 150 | 76 | 118 |

N/A: Not available

7.7 Conclusion

To shrink the parasitic inductance and reduce the device drain-source overvoltage, design criteria is introduced for three-level converter layout. Multiple commutation loops are taken into consideration, and the magnetic cancellation effect is utilized to minimize the loop inductance. Vertical and lateral layout are compared in a PCB based 3L-ANPC converter, which shows the superiority of the vertical loop design.

Following the design criteria, a design example of a laminated busbar is given in detail for a 500 kVA 3L-ANPC converter based on SiC MOSFET power modules. Two commutation loops in the converter are optimized with the placement of busbar parts. Moreover, distributed film capacitors with special placement are adopted to serve as the DC-link capacitors. Due to the low inductance, no extra decoupling capacitor is needed.

In addition, the fabrication process of the laminated busbar based on aluminum is investigated. The insulation material selection and implementation is introduced in detail. In the meantime, soldering on aluminum is also discussed.

Together with the SiC MOSFET power modules with low stray inductance, the overall parasitic inductances of the short and long loop in the converter are 6.5 nH and 17.5 nH, respectively. Compared to the high power NPC type converters in other references, the proposed busbar achieves at least 84% and 77% reduction in small and large loop inductances. The experimental results verified the performance of the busbar.

8 Cryogenically Cooled High Power Inverter with SiC MOSFETs

Based on the analysis and methodology developed in previous chapters, the example of a high switching speed high power inverter based on SiC MOSFETs is presented in this chapter. According to the specifications given by NASA, the design of a MW-class cryogenically cooled inverter for aircraft application is developed. The characterization of SiC MOSFETs at cryogenic temperatures is introduced first as the basis for power converter design and optimization. The switching loss of the inverter is analyzed in detail with the technologies in previous chapters embedded. Then, the detailed inverter system design including converter layout, thermal management, filters, gate drive, busbar, and system integration are presented. The testing result of a single 500 kVA inverter is presented with experimental results.

This part of work is published or accepted in the journal and conference papers [170-173].

8.1 Background and Specifications

High power inverters will be a key enabler for future aircraft based on hybrid electric or turbo-electric propulsion as envisioned by NASA and Boeing. A technological hurdle exists however, in that the components for power generation, distribution, and transformation are not currently available in the high-power ranges with the necessary efficiency and power density required for transport-class aircraft.

At the system level in aircraft applications, superconducting technologies such as motors/generators along with their supportive power systems will grow in importance. Integrating the associated power electronics into the superconductive motor/generator systems can avoid extra thermal insulation and temperature regulation system and reduce system complexity and improve the power density. However, many of the necessary power electronics to control and protect a

cryogenic system are not yet available. There are not many reports about power converter designs at cryogenic temperatures. According to recent literature [174-186], the maximum reported power level of a cryogenically cooled converter prototype was 2.5 kW. Moreover, there is no specific detailed cooling system design provided that would be suitable for high power electronics applications.

Based on the above analysis, NASA released the “Research Opportunities in Aeronautics – 2015 (ROA-2015)”, in which one of the objectives is to design, build, and test a technology demonstrator high efficiency/high specific power cryogenic MW-class inverter to meet the anticipated needs of aircraft electric propulsion drives. It is targeting specific vehicle concepts which exploit cryogenic cooling to gain system benefits. The key performance goals of the inverter are shown in Table 8-1, where efficiency is measured as the ratio of the output to input power at half-rated power at nominal bus voltage. The key specifications are continuous power rating ≥ 1 MW; nominal bus voltage: 1 kV DC; peak output line to line RMS voltage: 600 V; peak line frequency: 3 kHz.

8.2 Device Characterization at Cryogenic Temperatures

In high power applications, Si IGBTs and SiC MOSFETs are two main candidates for power semiconductor devices. Due to the high power density and high efficiency requirement, SiC MOSFET power modules are preferred to achieve lower switching loss. To optimize the performance of the converter, it is desired to understand the device characteristics at cryogenic temperatures, which is normally not provided in device datasheets from the manufacturers. In addition, packaging is worth investigating to make sure the device can operate properly in cold environment.

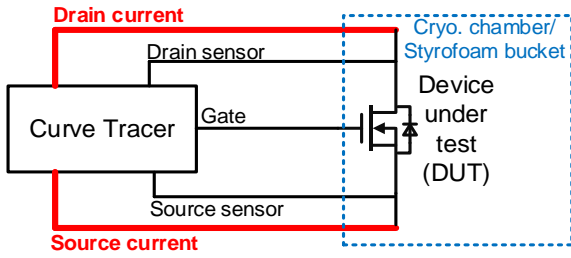
Table 8-1. Key performance goals.

| Goals | Specific Power (kW/kg) | Specific Power (HP/lb) | Efficiency (%) |
|---------|------------------------|------------------------|----------------|
| Min | 17 | 10.4 | 99.1 |
| Target | 26 | 15.8 | 99.3 |
| Stretch | 35 | 21.3 | 99.4 |

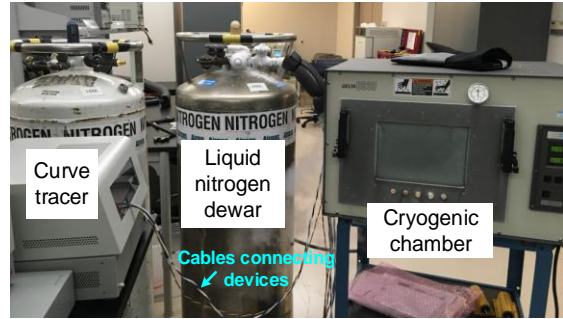
A cryogenic chamber is used to serve as the container for the device under test (DUT) and provide the required cryogenic temperature. For the static characterization, the curve tracer B1505A from Keysight is connected with the DUT, and the Kelvin connection is used to guarantee the accuracy of the measurement as shown in Fig. 8-1(a). The picture of the testing platform is shown in Fig. 8-1(b). The temperature inside the chamber can be regulated, and the liquid nitrogen is injected from a dewar. A high accuracy diode based temperature sensor from Lakeshore is attached to the device to provide the temperature information.

For the dynamic characterization, double pulse test (DPT) is adopted to get the switching performance. Fig. 8-2 illustrates the configuration and testing platform of the DPT. Not only the DUT, but also the gate drive, DC link capacitors, signal isolator and other auxiliary circuits are located inside the chamber at cryogenic temperature. This is due to the concern for high ringing and noise during fast switching transients caused by parasitics. Thus, putting the gate drive circuits close to the DUT can minimize the parasitics in the loop. Moreover, it can help mimic the real operating condition in a converter.

SiC MOSFETs from three different manufacturers are tested in the range of room temperature to $-200\text{ }^{\circ}\text{C}$ (77 K), whose parameters at room temperature are listed in Table 8-2.

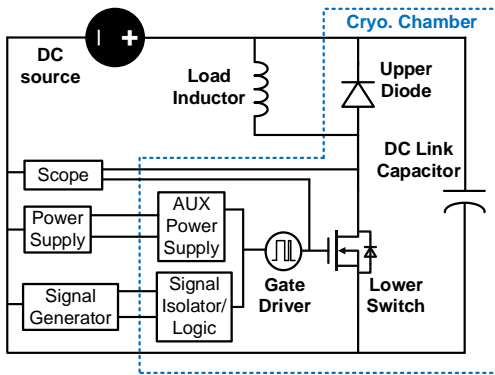


(a)

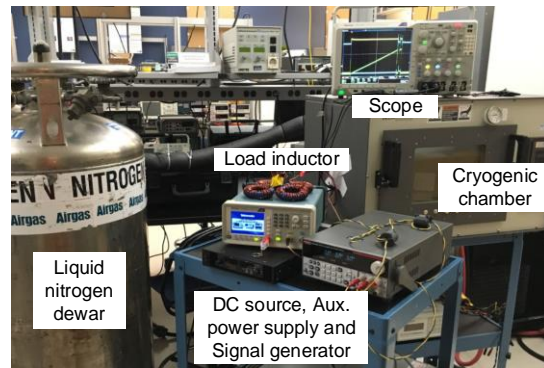


(b)

Fig. 8-1. Static characterization. (a) Configuration. (b) Setup.



(a)



(b)

Fig. 8-2. Dynamic characterization. (a) Configuration. (b) Setup.

Table 8-2. Parameters of tested SiC MOSFETs.

| Part | C3M0075120K | SCT3030KL | SCT50N120 |
|------------------------|-------------|-----------|-----------|
| Manufacturer | Wolfspeed | Rohm | ST |
| V_{br} (V) | 1200 | 1200 | 1200 |
| I_d (A) | 30 | 72 | 65 |
| R_{ds} (m Ω) | 75 | 30 | 52 |
| R_g (Ω) | 10 | 5 | 1.9 |

Fig. 8-3 plots the tested on-resistance. Generally, the on-resistance increases as the temperature drops. There are two possible reasons that contribute to the trend. First, the carrier freeze-out phenomenon makes fewer carriers ionized at lower temperatures [187]. Second, the interface states density between SiC and SiO₂ increases rapidly at lower temperatures, which results in more trapped electrons [188]. Note that the Wolfspeed device shows larger increase in on-resistance than the other two devices at cryogenic temperatures. This is possibly due to the different device structure they use. The Wolfspeed device is planar based while the other devices are trench based.

Fig. 8-4 illustrates the relationship between breakdown voltage and temperature. It is observed that the Wolfspeed and Rohm devices have almost constant breakdown voltage throughout the whole temperature range while that of ST decreases a little but is still higher than 1.1 kV. Therefore, the SiC MOSFETs have relatively good breakdown performance compared with Si MOSFETs, whose breakdown voltage can drop by 25%- 35% from room temperature to 77 K [189]. This trend can also be explained by the carrier freeze-out, which mitigates the impact ionization and allows higher voltage across the drift region.

The switching waveform of the Wolfspeed device at 500 V and 30 A with 1 Ω gate resistance is shown in Fig. 8-5. It is observed that the overlap time of current and voltage during the transient at cryogenic temperature is longer than that at room temperature, which means that the device switching speed is slower at cryogenic temperature. However, it should be noted that the voltage drops faster at the beginning of turn-on at 93 K then becomes flatter. This shape shrinks the overlap area of voltage and current and reduces the switching loss.

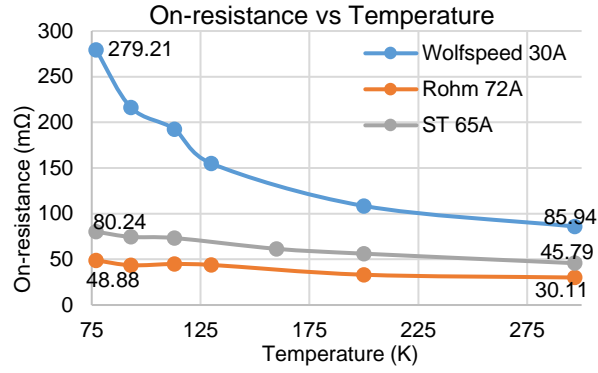


Fig. 8-3. Tested on-resistance at different temperatures.

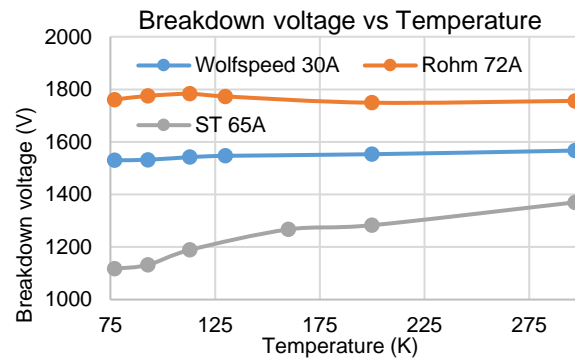


Fig. 8-4. Tested breakdown voltage at different temperatures.

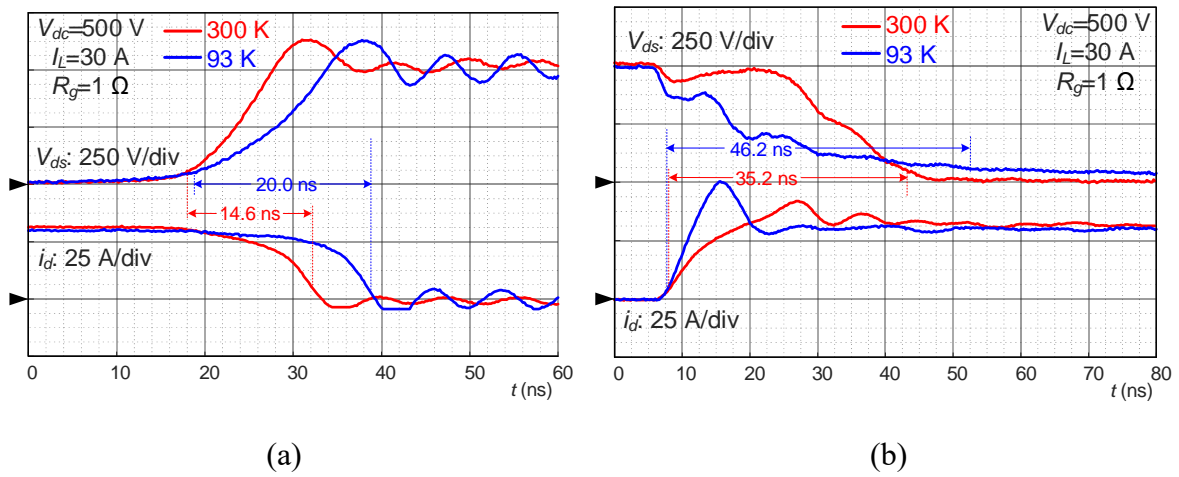


Fig. 8-5. Tested switching waveforms of Wolfspeed device at 500 V and 30 A with 1 Ω gate resistance. (a) Turn-on. (b) Turn-off.

Fig. 8-6 plots the tested switching loss of the Wolfspeed and Rohm devices at different temperatures. For the Wolfspeed device, the switching loss first increases then decreases when the temperature drops. Meanwhile, the switching loss of the Rohm device keeps increasing as temperature decreases.

Generally speaking, the SiC MOSFET is not suitable for cryogenic operation due to the loss increase. Moreover, silicone gel is used as the encapsulant in most power modules, which cannot survive at low temperatures. As a result, the operating temperature of the SiC MOSFET should be kept higher than $-50\text{ }^{\circ}\text{C}$ [190].

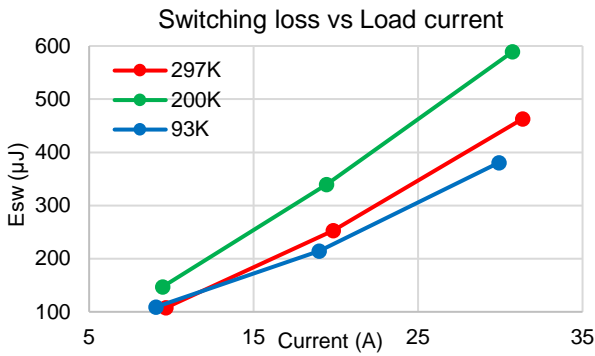
The SiC MOSFET module shown in Fig. 3-8 is adopted as the power devices in the converter due to its high current rating ($>800\text{ A}$), light weight (179 g), and the state-of-the-art die and packaging technology. The static characteristics of the module from -40 to $125\text{ }^{\circ}\text{C}$ (235 to 400 K) are shown in Fig. 8-7. The trend of on-resistance follows the previous test with discrete devices, and the lowest point occurs at around $0\text{ }^{\circ}\text{C}$. The breakdown voltage keeps increasing as temperature drops. Although the device is rated at 900 V by the manufacturer, the tested breakdown voltage is always higher than 1.05 kV, which provides more room to increase the switching speed.

With the DPT setup in Fig. 3-13, the switching loss with $1.3\ \Omega$ gate resistance at room temperature is obtained and illustrated in Fig. 8-8.

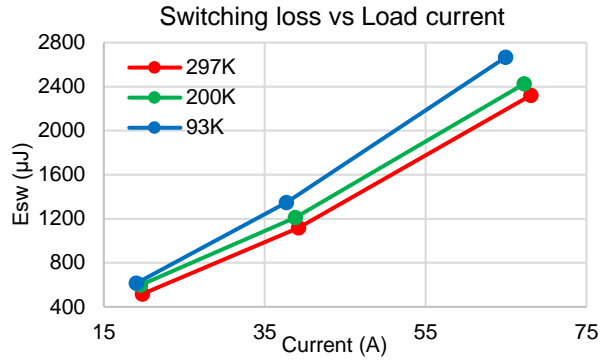
8.3 Switching Loss Evaluation

8.3.1 Switching Frequency Selection

The selection of the switching frequency needs to consider both the power module operation and the EMI standard. From the SiC module point of view, higher switching frequency leads to higher loss and heat. In terms of EMI, the size and weight of the filter is also strongly related to

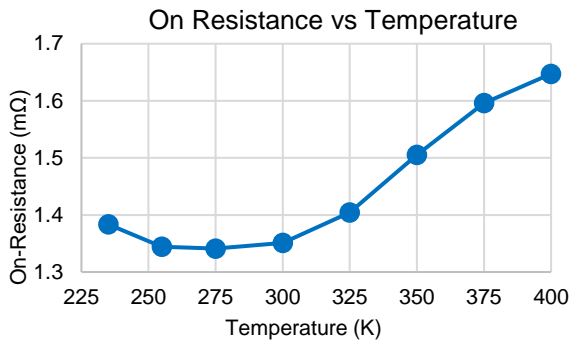


(a)

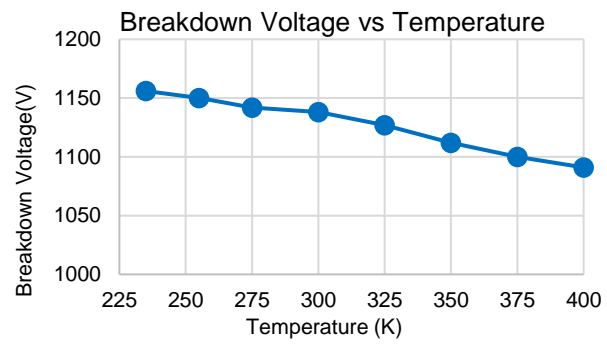


(b)

Fig. 8-6. Tested switching loss at 500 V and different load current. (a) Wolfspeed. (b) Rohm.



(a)



(b)

Fig. 8-7. Tested characteristics of SiC power module. (a) On-resistance. (b) Breakdown voltage.

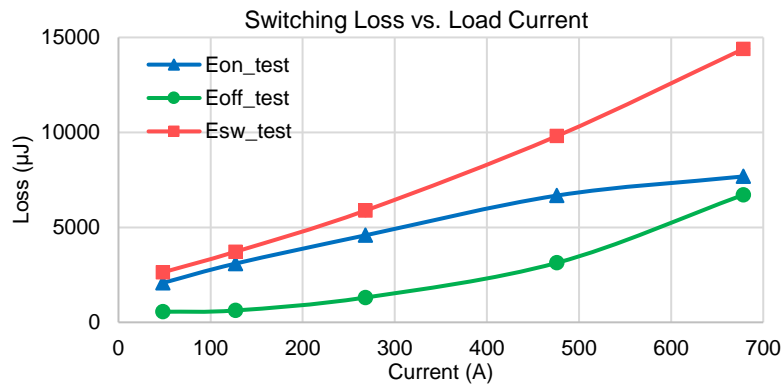


Fig. 8-8. Tested switching loss of the SiC module at room temperature.

switching frequency. Fig. 8-9 shows the calculated relationship between the corner frequency of the filter and switching frequency. Generally, higher corner frequency means smaller size and weight of the filter. It is observed that the optimized point is 140 kHz. However, based on the DPT data, the switching loss is too high to meet the efficiency target. The second frequency candidate is 70 kHz, and the switching loss is acceptable. Nevertheless, the 2nd order harmonic sideband enters the EMI measurement range (starting at 150 kHz). To avoid the increased noise, the switching frequency is selected as 60 kHz. In the 3L-ANPC converter, the equivalent switching frequency is 30 kHz as the device only operates during half line cycle.

8.3.2 Switching Loss Correction in 3L-ANPC Converter

As has been analyzed in Section 6.2.1, there are multiple switching loops in 3L converters. It not only impacts the drain-source overvoltage, but also shows influence on switching loss. The simplified equivalent circuit of a 3L phase leg with major parasitics highlighted is drawn in Fig. 8-10. The non-active switch M_p is paralleled with the active switch M_L operating at high switching frequency.

During the turn-on transient of M_L , the current flowing through its channel i_{ch} consists of the following parts: the load current I_L , the charging current of the drain-source capacitance from the upper device i_{cdsH} , the discharging current of the drain-source capacitance from the lower device i_{cdsL} , the discharging current of the transfer capacitance from the lower device i_{cgdL} , and the discharging current of the drain-source capacitance from the paralleled non-active device i_{cdsP} . Note that in a DPT current measurement, i_{cdsL} and i_{cgdL} are not included as they are inside the device. Compared with a 2L phase leg, there is additional i_{cdsP} , introducing higher turn-on switching loss as shown by the blue shaded area in Fig. 8-11. It is worth noting that the switching

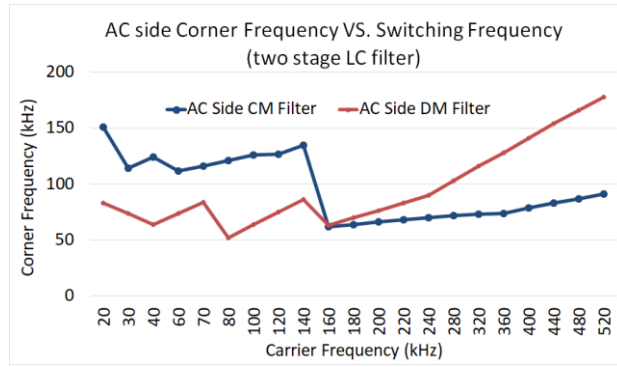


Fig. 8-9. Relationship between filter corner frequency and switching frequency.

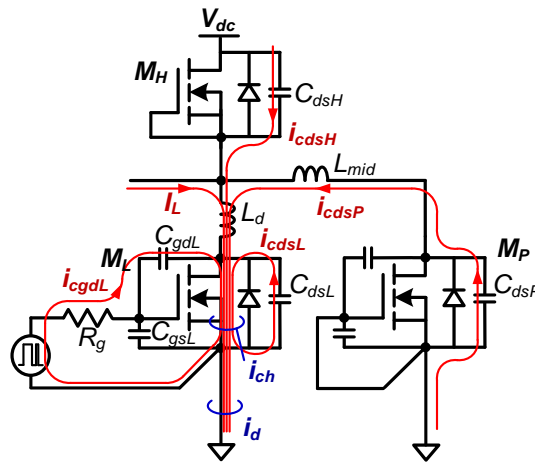


Fig. 8-10. Typical equivalent circuit of 3L phase leg.

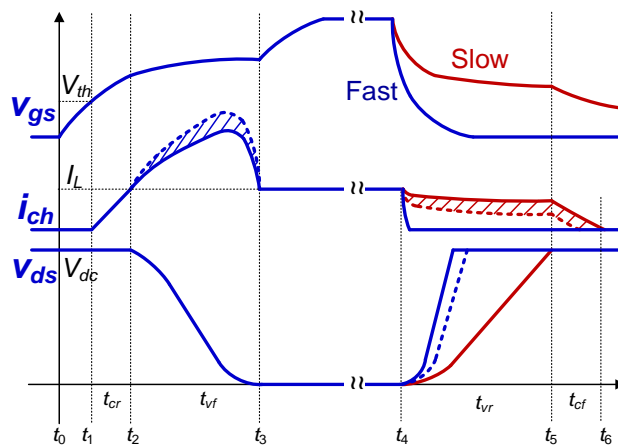


Fig. 8-11. Waveform of active switch considering paralleled non-active switch.

time is not increased according to the analysis in Section 6.3.4. The increased turn-on loss is purely caused by the extra capacitance energy from the paralleled non-active device.

During the turn-off transient, all the currents change to opposite direction except the load current I_L . In other words, the capacitance current should be deducted from the load current when calculating the device channel current. As a result, there are two possibilities when calculating the turn-off loss.

In case 1 shown by the blue line in Fig. 8-11 from t_4 to t_6 , when the switching speed is very fast or the load current is low, all the load current is used to charge/discharge the capacitances. As a result, no current flows through the device channel, leading to zero turn-off loss. The trajectory of the turn-off in such cases are plotted with blue lines in Fig. 8-12.

In case 2, when the switching speed is not high enough, and under heavy load conditions, the load current is sufficient to charge/discharge the capacitances. The remaining current flows through the device channel, causing turn-off loss. From the red lines in Fig. 8-11, the extra capacitance from the paralleled non-active switch shares more current, leading to larger channel current drop, which is also plotted in Fig. 8-12. Therefore, the turn-off loss of the device in a 3L phase leg is lower than that in a 2L phase leg. Since the reduced loss is caused by charging the extra capacitance of the paralleled non-active switch, it compensates the increased loss during the turn-on transient. Thus, the total switching loss is the same for 2L and 3L phase leg under case 2. However, since there is no such compensation during the turn-off under case 1, the total switching loss in a 3L phase leg is higher than that in 2L.

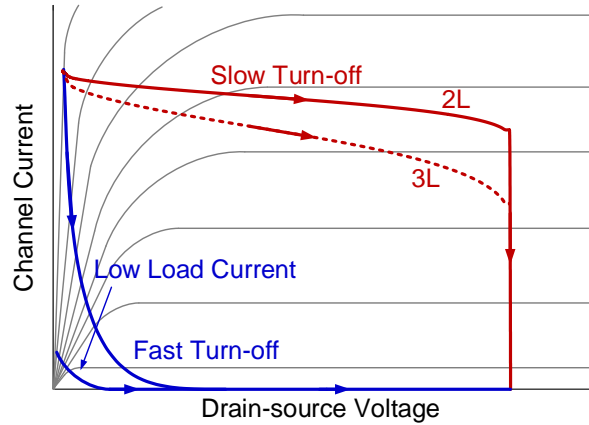


Fig. 8-12. Trajectory during turn-off transient.

With a fixed gate resistance, the switching speed is determined, and the difference of the loss between 3L and 2L phase leg is mainly caused by the load condition. During one AC line cycle, case 1 occurs near the zero crossing point, while case 2 occurs near the peak current. To better estimate the switching loss in an actual converter, the correction should be made based on the DPT result with a typical 2L phase leg.

A simulation model based on the SiC module is established in Saber. The simulated switching loss with 2L and 3L phase leg under different load conditions are plotted in Fig. 8-13. The loss in 2L phase leg can match well with the DPT result in Fig. 8-8, which suggests the accuracy of the simulation model. Comparing the 3L with 2L, case 1 changes to case 2 in 200-300 A load current. With the corrected loss curve, the switching loss of the inverter can be estimated.

8.3.3 Switching Loss Estimation

Fig. 8-14 shows the estimated switching loss of the inverter at full and half load conditions with different gate resistances. After the correction considering the effect of the 3L structure, the

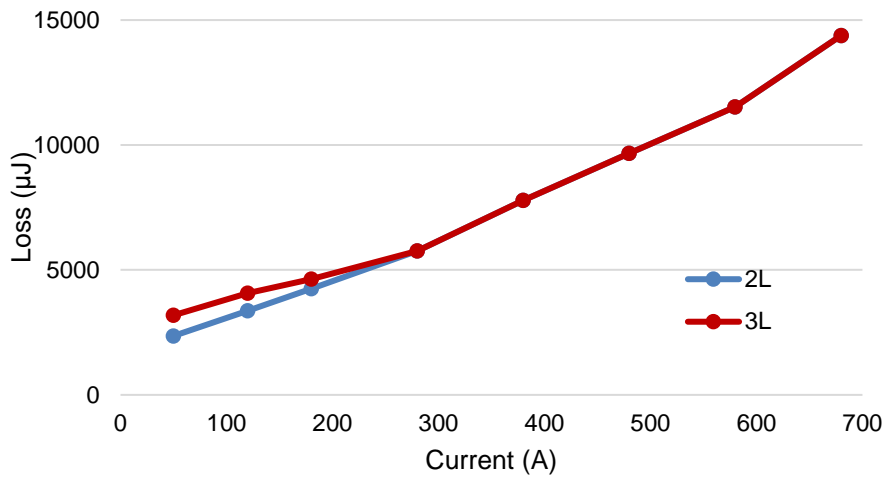


Fig. 8-13. Simulated switching loss in 2L and 3L phase legs.

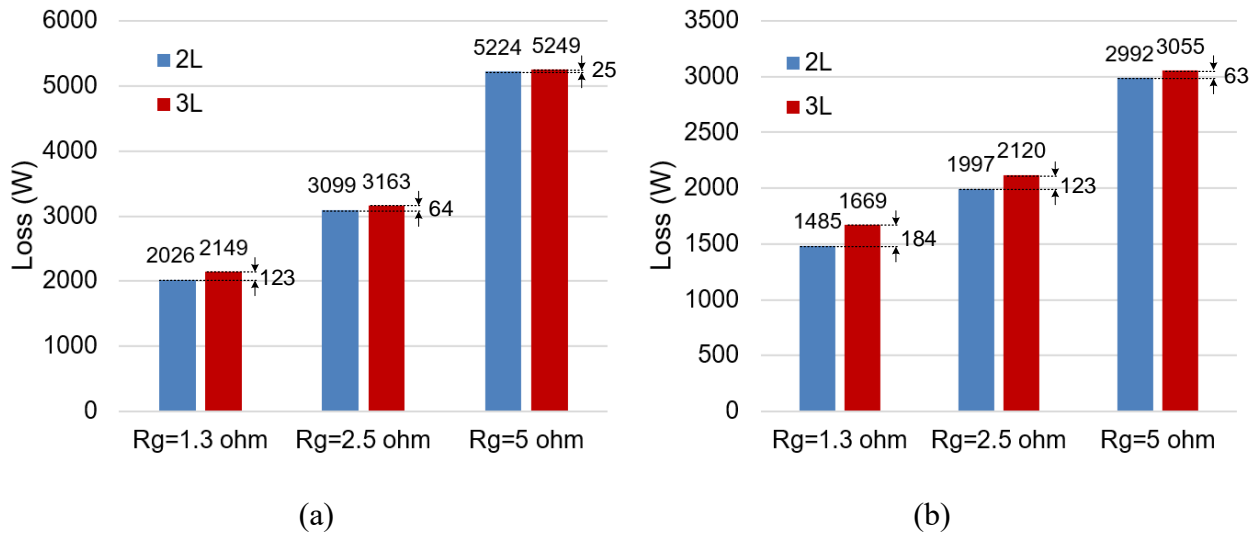


Fig. 8-14. Estimated switching loss with different gate resistances. (a) Full load. (b) Half load.

switching loss increases compared with the result based on 2L DPT. From Fig. 8-14(a), the loss difference between 2L and 3L inverters is 123 W with 1.3 Ω gate resistance, which is higher than the 25 W with 5 Ω resistance. This result matches with the analysis above that higher switching speed results in higher loss caused by the non-active switch. Comparing Fig. 8-14(a) and (b), with

the same gate resistance, the loss difference between 2L and 3L inverters is larger at half load, which also matches with Fig. 8-13 where two loss curves have larger gap at lighter load conditions.

With the proposed methods in Chapters 6 and 7, the switching loss can be significantly reduced. If the conventional modulation scheme is used, the gate resistance requires 2.5Ω due to the higher overvoltage according to Section 6.4. As a result, the switching loss at full load is 3163 W, which is 47.2% higher than using 1.3Ω gate resistance. If the busbars from other references in Table 7-6 are adopted, the gate resistance has to be increased to at least 5Ω based on the simulation results, and the switching loss is increased by 144.3%. With higher switching loss, the device temperature rises, leading to higher conduction loss. To keep the stable temperature, cooling system with larger size and weight has to be used, which decreases the power density of the system.

8.4 System Development

8.4.1 Overall Architecture

According to the load requirement, two SiC power modules have to be paralleled to deliver the current, which can introduce dynamic current sharing issues. In practice, two 500 kW inverters are paralleled and interleaved with coupled inductors to achieve 1 MW power with reduced current ripple. Taking the device voltage rating (900 V) into consideration, the 3L-ANPC converter is utilized as the topology. The paralleled inverter system is drawn in Fig. 8-15, where both DC and AC side EMI filters are inserted to suppress EMI noise and meet DO-160 EMI standards.

8.4.2 Filters

Fabricated EMI filters and the coupled inductors are shown in Fig. 8-16. Liquid nitrogen can directly flow into the 3D-printing housing to cool the magnetic components and wires. The filters are characterized at cryogenic temperatures, which is not covered here as it is not the focus of this

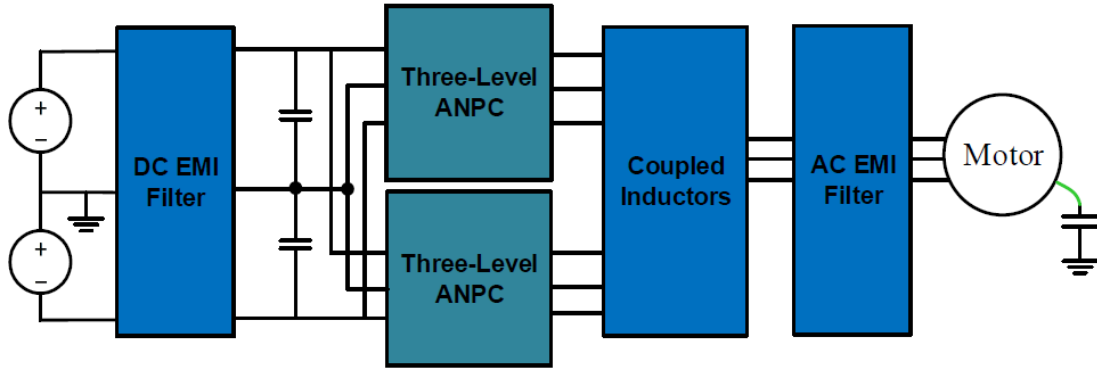


Fig. 8-15. 1 MW converter system.

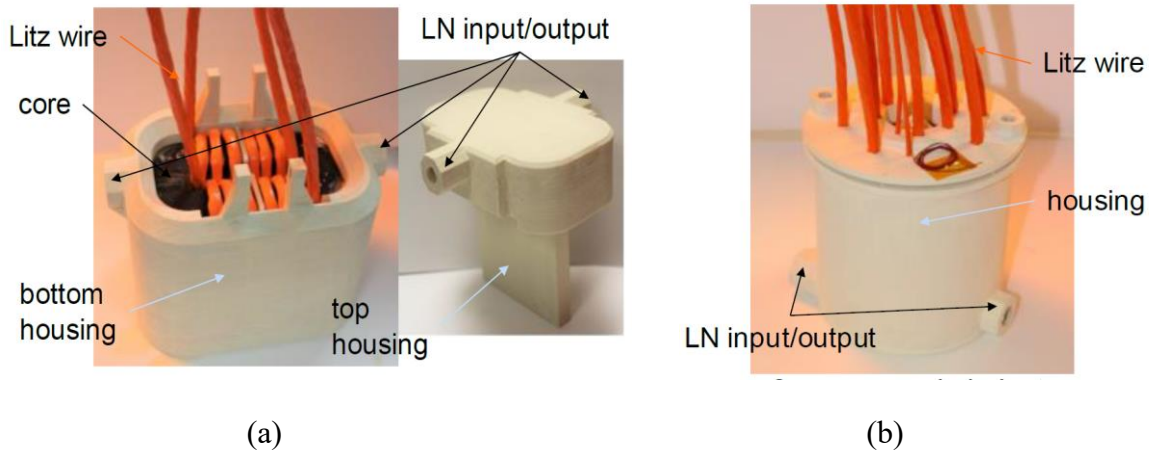


Fig. 8-16. Fabricated filters. (a) Coupled inductors. (b) CM choke.

dissertation. The equivalent switching frequency of the converter is selected as 30 kHz considering the noise spectrum and filter weight optimization.

8.4.3 Gate Drives and Busbars

The gate drive follows the design in Section 3.1.3.2. For power devices operating at high current, it is important to provide sufficient protection to avoid device damage. The main protection that needs to be implemented is short circuit protection. Because of the high current

requirement in the 1 MW inverter, high DC-link capacitance is required to supply enough transient energy. Once the short circuit occurs, the energy stored in the capacitors is dissipated in the device, which can easily cause damage. Among the short-circuit protection circuits and control schemes, the de-saturation (de-sat) protection is a commonly used method for power semiconductor devices [191-193]. Basically, the drain-source or collector-emitter voltage of the device under test is detected when the device is on. Once the voltage exceeds a certain threshold, which indicates that the drain current is too high, the device is turned-off.

The detailed de-sat protection circuit for a MOSFET is drawn in Fig. 8-17. The diode D_{sat} blocks the high drain-source voltage when the device is off and conducts when device is on. The de-sat voltage v_{sat} is sensed with a RC network and compared with the threshold voltage V_{th} . The output of the comparator triggers the logic circuits and turns off the gate drive when the device saturation occurs. Notably, a soft turn-off circuit should be adopted to slow down the turn-off process so that the device is not damaged due to the overvoltage caused by the high di/dt during the switching transient. The soft turn-off resistance R_s is larger than the normal gate resistance R_g , and the detailed value should be selected based on the short-circuit testing results.

The false triggering issue during normal switching transients requires special attention. The reverse recovery current of D_{sat} and the displacement current through the junction capacitance C_j of D_{sat} can result in voltage increase of v_{sat} . To mitigate this effect, a SiC diode with small footprint is preferred for D_{sat} , while several diodes can be series connected to reduce the junction capacitance. In addition, the blanking capacitance C_b should be carefully designed to balance the false triggering immunity and the reaction speed.

The waveform of short circuit current with de-sat protection test is shown in Fig. 8-18. It is observed that the peak total drain current of the SiC module is around 3 kA. From the start of the

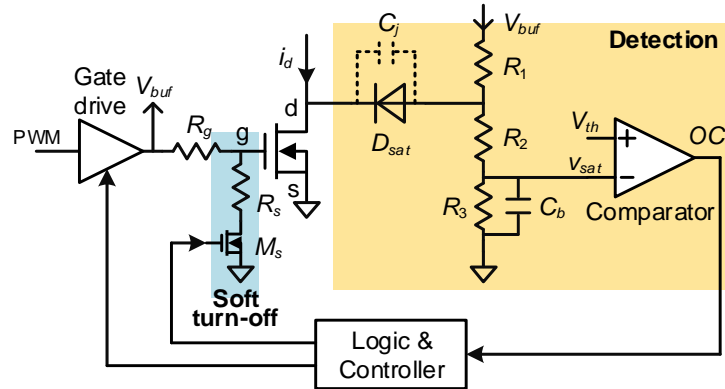


Fig. 8-17. De-sat protection circuit.

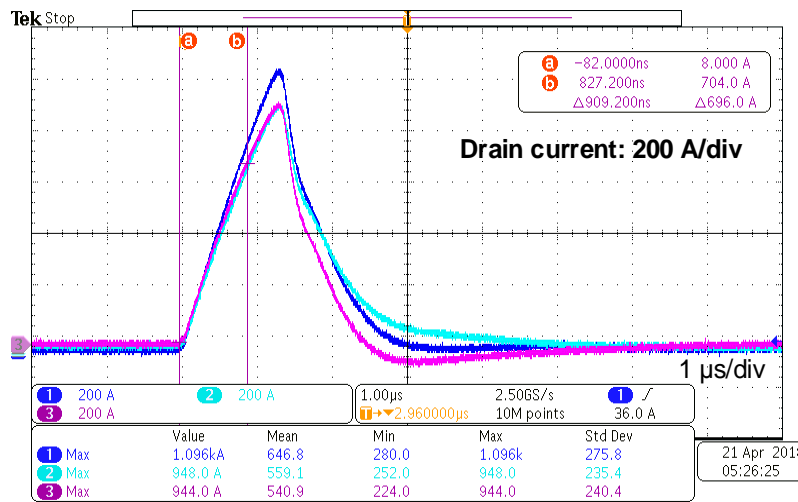


Fig. 8-18. Short-circuit current with de-sat protection.

short circuit to the moment when the drain current decreases to zero, the total time is less than 3 μ s, which is quick enough to protect the device.

Another issue worth highlighting is cross-talk. As reviewed in Section 2.1.2, the displacement current on the transfer capacitance of the device caused by dv/dt during switching transients flows through the gate loop, which leads to a spurious gate voltage. If this voltage is high enough, it can

falsely turn-on the device, which significantly deteriorates the switching performance and the switching loss.

One of the commonly used methods for cross-talk suppression is the gate impedance regulation. Fig. 8-19 presents the example of a cross-talk suppression circuit as well as its control schemes [37]. An impedance regulation branch is added which consists of a small MOSFET and a capacitor whose value is higher than 50-100 times of the main switch input capacitance. When the gate signal v_{g_L} is applied to the lower main switch, the control signal of the upper small MOSFET v_{a_H} is also applied with a delay. It should be noted that the small MOSFET M_{a_H} should be turned-off after the lower main switch is off and before the upper main switch is on. Hence, the cross-talk of the upper main switch is mitigated, and its normal turn-on is not affected. Fig. 8-20 shows the tested gate voltage waveform under full bus voltage and load current condition. The spurious voltage during the switching transient is less than 1 V, which is lower than the threshold voltage of the SiC MOSFET.

With the busbar prototype in Chapter 7 verified in the lab, the busbar shown in Fig. 8-21 is fabricated by a manufacturer and used in the converter.

8.4.4 Thermal Management

Cryogenic thermal interface is essential and requires special design of the converter test in the lab. As mentioned in Section 8.2, SiC power modules cannot operate under $-50\text{ }^{\circ}\text{C}$. On the other hand, over-heating should also be avoided. Therefore, a cooling system with the ability to dynamically adjust the operating temperature is needed, and the conventional liquid nitrogen cannot be directly used to cool the devices as the liquid temperature is too low and fixed.

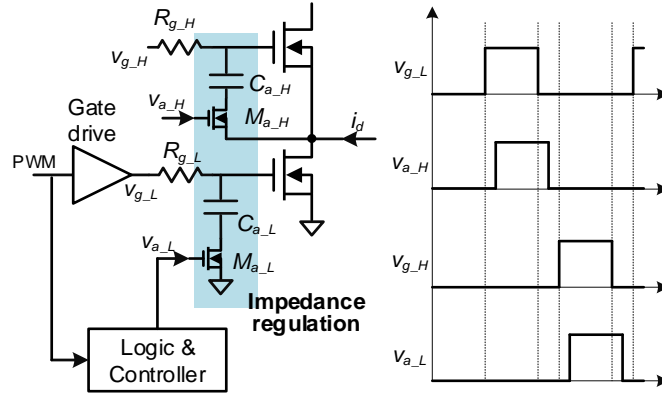


Fig. 8-19. Circuit and control signals of cross-talk suppression.

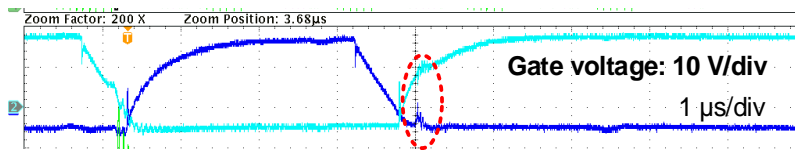


Fig. 8-20. Gate voltage under full bus voltage and load current condition.

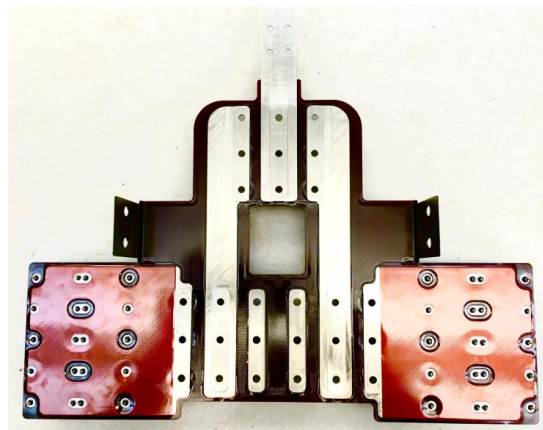


Fig. 8-21. Fabricated busbar by manufacturer used in converter.

The concept of the cooling system is illustrated in Fig. 8-22. The nitrogen gas flows through tube coils that are submerged into a liquid nitrogen bucket. By adjusting the height of the jack, the number of turns of the coils that are submerged into liquid nitrogen can be adjusted. As a result,

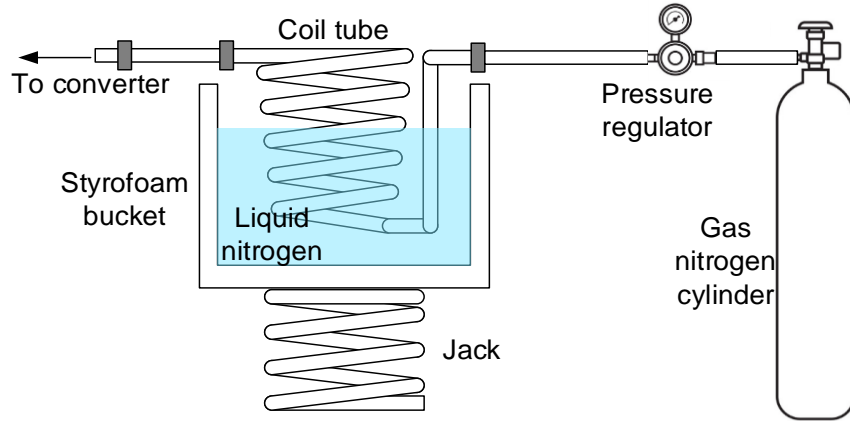


Fig. 8-22. Concept of converter cooling system.

the cooling performance of gaseous nitrogen system can be controlled by adjusting the flow rate of the gas through a pressure regulator combined with adjusting the number of coil turns submerged in the liquid nitrogen.

The cooled nitrogen gas flows into the coldplates, on top of which are the SiC power modules. The coldplate is designed by Boeing, with three independent channels and embedded fins for three modules on each phase leg of the 3L-ANPC converter. Therefore, each three-phase converter has three coldplates. To test the performance of the fabricated coldplates, resistor heaters are mounted on the coldplates as shown in Fig. 8-23. Power loss based on the estimated converter loss are generated from the heaters to mimic the operation of the converter. Due to the similar junction to case thermal resistance of the resistor heater and the power module, the temperature of the power modules can be estimated by sensing the case temperature of the heaters under the same load condition. Fig. 8-24 plots the measured temperature with the loss at full load condition. The maximum heater case temperature is slightly higher than 60 °C, which indicates that the cooling performance is good enough for full load operation.

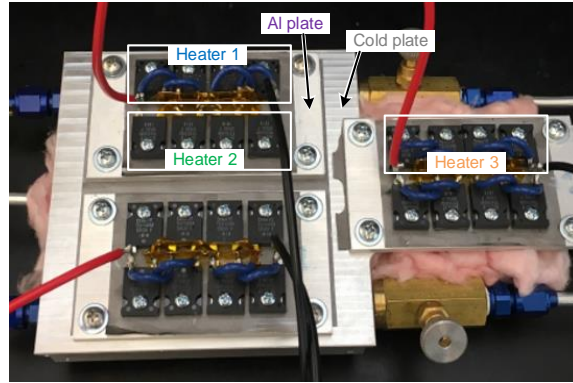


Fig. 8-23. Cold plate testing setup with resistor heaters.

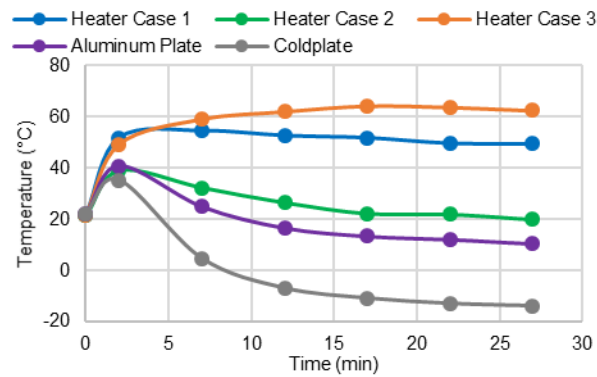


Fig. 8-24. Cold plate testing result under full load condition.

8.4.5 System Integration

Due to the EHS (Environment, health and safety) requirement, the whole converter system is located inside an enclosure to avoid the potential icing and shock issues. With all the designed subsystems, the system integration is designed as Fig. 8-25. Note that all the liquid and gas nitrogen tubes, coldplates and filters are covered with Styrofoam (yellow parts) to reduce the thermal exchange between the coolant and the environment.

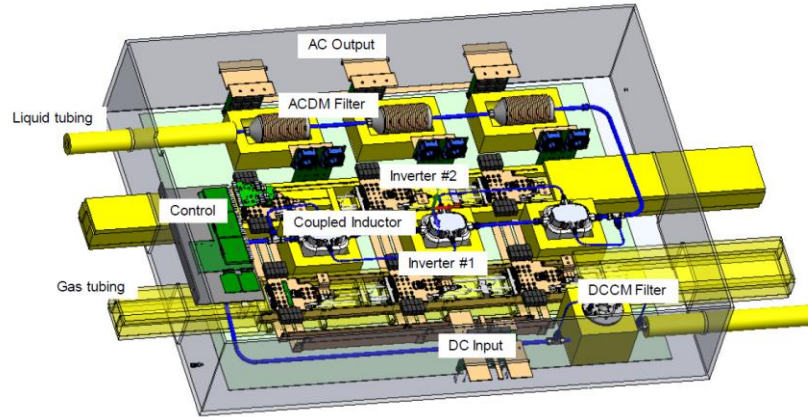


Fig. 8-25. Designed cryogenic system integration for two paralleled inverters.

8.5 Experimental Results

The established converter is first tested at room temperature. The testing setup is shown in Fig. 8-26. Water cooled coldplates are utilized to provide the cooling. Pure inductive load is used to achieve the required load current. Fig. 8-27 illustrates the tested continuous output current waveforms of the single converter at 1 kV input voltage. The peak value of the output current is 292 A, which corresponds to 210 kVA power. There is a slight current unbalance among the three phases due to the load inductor unbalance and the open loop operation. The maximum measured temperature on the busbar is 41 °C.

The testing setup at cryogenic temperatures is shown in Fig. 8-28. Six nitrogen cylinders are used to provide the gas for the coldplates. By changing the pressure at the outlet of the cylinder with the regulators, the gas velocity can be tuned to manage the temperature on the SiC MOSFET modules.

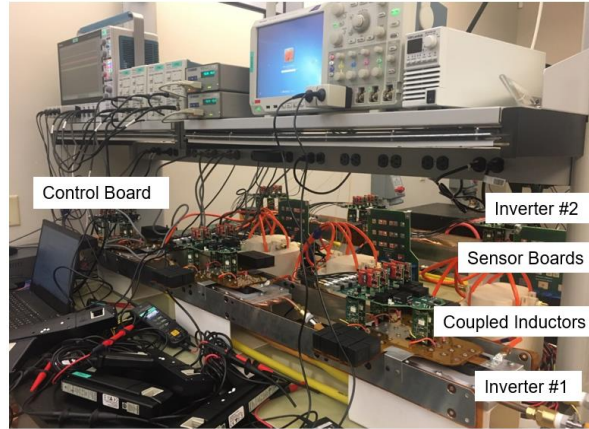


Fig. 8-26. Room temperature testing setup.

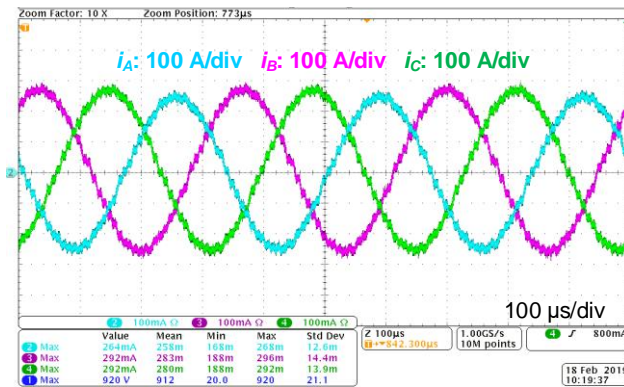


Fig. 8-27. Tested output current of single inverter at room temperature.

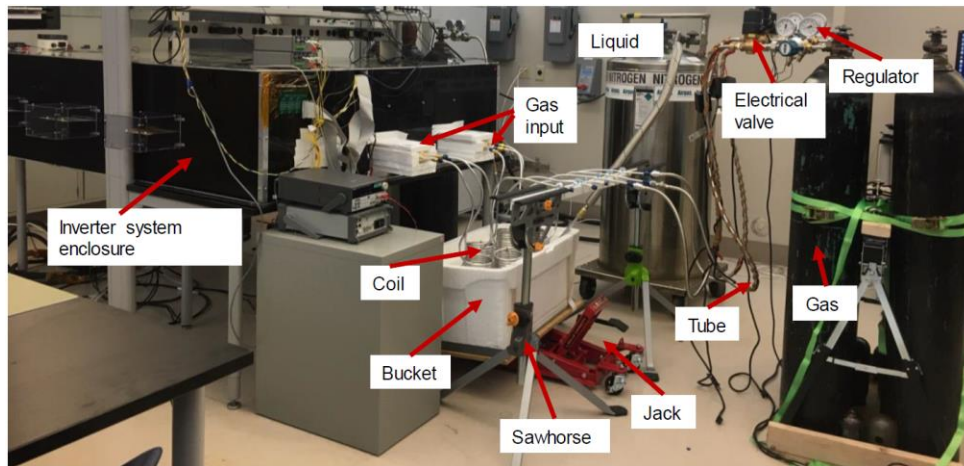


Fig. 8-28. Cryogenic temperature testing setup.

The tested output current of a single inverter at full load condition is plotted in Fig. 8-29. The peak phase current reaches 680 A, which corresponds to 500 kVA power level.

It is necessary to estimate the loss breakdown of the inverter, which is shown in Fig. 8-30 for the full load condition. It is observed that the dominant loss is from the power module as shown in the yellow area. The conduction and switching loss are almost 50% each of the total device loss. The total estimated loss corresponds to 99.0% efficiency.

In the experiment, the conventional space vector modulation (SVM) is adopted. To reduce the switching loss, discontinuous modulation strategies can be used. Based on the simulation, the switching loss can be reduced from 2149 W to 1547 W with the discontinuous modulation, resulting in 0.12% increase in efficiency.

Weight is the other main target of the inverter system. The weight breakdown of the 1 MW system as well as the sub-systems is shown in Fig. 8-31. Clearly, the filters dominate the total weight, and the heaviest part is the coupled inductor balancing the current between two paralleled inverters. The measured power density is 11.3 kW/kg. If the AC side has no EMI requirement, and only dv/dt filter is needed, the filter weight can be significantly reduced.

8.6 Conclusion

In this chapter, a 1 MW inverter based on SiC MOSFET power module is developed to operate at cryogenic temperature. SiC MOSFETs are first characterized at low temperatures with liquid nitrogen and a cryogenic chamber. The result indicates that the optimal operating temperature is around 0 °C.

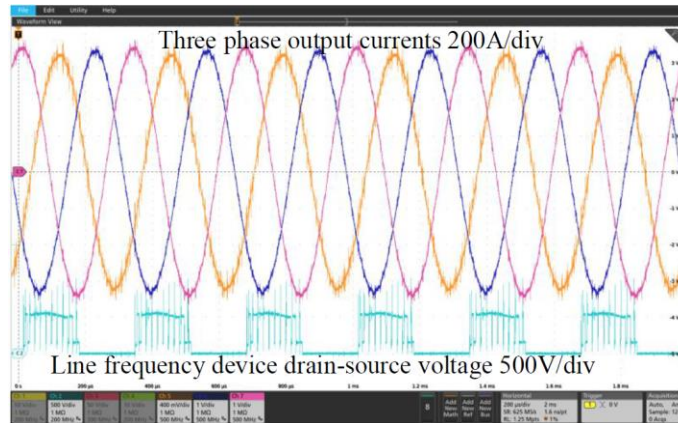


Fig. 8-29. Tested output current of single inverter at full load condition.

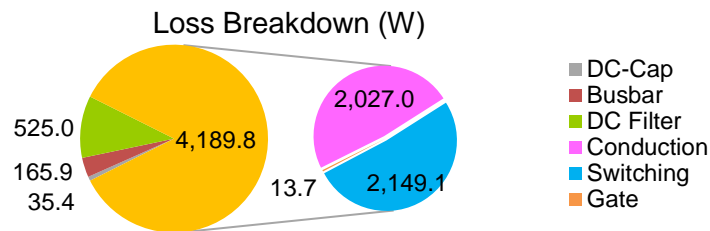
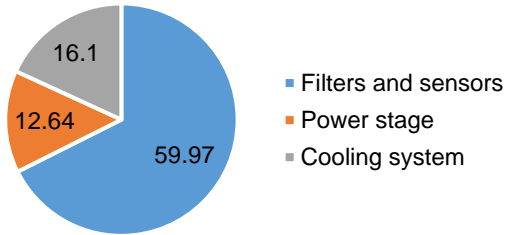


Fig. 8-30. Estimated loss breakdown under full load.

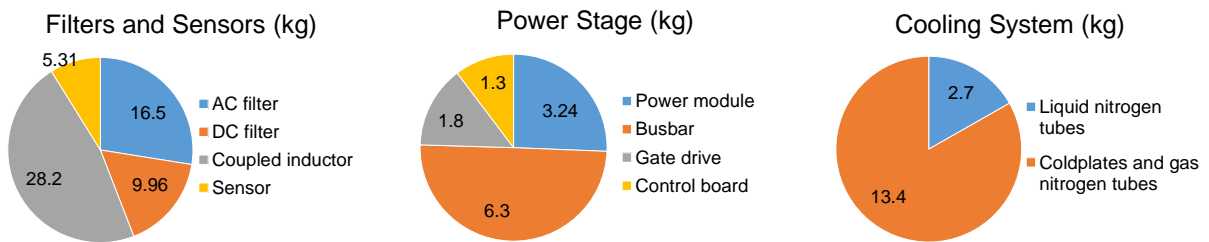
The switching loss considering the effect of the paralleled non-active switch in the 3L phase leg is analyzed. With low load current, the switching loss increases compared with the typical 2L phase leg. The correction of the switching loss with the simulation model is made based on the DPT result of a 2L phase leg. By utilizing the technologies in previous chapters, the switching speed of the power module increases, and lower switching loss is achieved.

Based on the characterized data, the inverter system is designed. Two 500 kVA inverters are connected in parallel with the coupled inductors. EMI filters are manufactured with 3D printing for low temperature operation. Gate drives are developed with de-sat protection and miller clamp function integrated. The busbar following the design in previous chapter is also utilized. Two

Weight Breakdown of 1 MW Inverter System (kg)



(a)



(b)

Fig. 8-31. Weight breakdown inverter system. (a) 1 MW system. (b) Sub-systems.

independent cooling systems are introduced with gas and liquid nitrogen for power modules and filters. An enclosure is used for EHS purpose.

The developed inverter is first tested at room temperature with water cooling at half power condition. With the basic function verified, the inverter is tested with cryogenic cooling. The estimated efficiency of single inverter at full load condition is 99.0%, and the specific power of the 1 MW system is 11.3 kW/kg. The detailed loss and weight breakdown are provided, and the advantage in reducing switching loss with the methods in previous chapters is discussed.

9 Conclusions and Future Work

Based on the work presented in chapters 1-8, the conclusions of this dissertation are summarized. The potential future research is also discussed in this chapter.

9.1 Conclusions

This dissertation investigates the methodology and solutions to improve the switching speed of SiC MOSFETs in hard switching applications. The main contributions of this dissertation are summarized as follows.

The major impact factors that limit the switching speed of SiC MOSFETs are analyzed comprehensively with double pulse tests. By comparing a low current SiC discrete device with a high current SiC power module, it is concluded that the switching speed of the low current discrete device is mainly limited by the gate drives, which cannot provide sufficient gate current to improve the switching speed. On the other hand, the switching speed of the high current power module is difficult to increase because of the high overvoltage induced by the higher di/dt during the switching transient and the parasitic inductance in the power loop. Therefore, different solutions are required for SiC MOSFETs with different current ratings.

1. For SiC MOSFETs with low current ratings, existing gate drive technologies are not enough to fully utilize the device switching speed capability. So the key point is to enhance the gate current during the switching transient.

- 1.1. A current source gate drive is proposed that can mitigate the influence of the large internal gate resistance and maintain constant gate current during the switching transient. After the switching transient, it can be controlled back to a voltage source gate drive to avoid gate overcharging and energy waste. In comparison with the conventional voltage source gate drive,

the turn-on and turn-off time is shortened by 67% and 50% respectively, while the switching loss is shrunk by 68% with the proposed gate drive at full load condition.

1.2. To overcome the drawback of the current source gate drive such as the required extra inductor and accurate timing control, a charge pump gate drive is proposed with simple structure. It can dynamically increase the gate drive output voltage during the turn-on switching transient to increase the switching speed of the SiC MOSFET. The gate drive voltage can automatically drop back to the normal value without additional control. The proposed gate drive can achieve 67.4% and 71.7% reduction for the turn-on switching time and loss.

2. For SiC MOSFET power modules with high current ratings, the key to increase the switching speed is attenuating the overvoltage resulting from the parasitics. Different control modulations can change the overvoltage, while optimizing the layout design is a straightforward way to reduce the parasitics.

2.1. The device drain-source overvoltage in 3L-ANPC converters is modeled for two modulation schemes with state space analysis. The coupling effect of the two commutation loops as well as the non-linear capacitance is considered. By turning off the non-active clamping switch, a modified modulation that builds an initial voltage across the line switching frequency device is developed, which helps the device output capacitance avoid the non-linear region and reduce the overvoltage. The overvoltage models for the conventional and the modified modulations are verified with a 500 kVA 3L-ANPC converter. With the modified modulation, 162 V and 176 V overvoltage reduction is achieved for the high and line switching frequency devices, which enables higher switching speed operation.

2.2. To minimize the parasitic loop inductance in three-level converters, the layout design criteria are introduced. Multiple commutation loops are taken into consideration, and the magnetic

cancellation effect is utilized. Following the design criteria, a design example of a laminated busbar with distributed DC-link capacitors is given for a 500 kVA 3L-ANPC converter based on SiC MOSFET power modules. In addition, the fabrication process of the laminated busbar based on aluminum is investigated. The overall parasitic inductances of the short and long loop in the fabricated busbar are 6.5 nH and 17.5 nH, respectively. Compared to the high power NPC type converters in other references, the proposed busbar achieves at least 84% and 77% reduction in small and large loop inductances.

3. A high power inverter based on SiC power module is developed for cryogenic applications. The detailed design for the sub-components in the inverter system is introduced. Taking into account the influence from the paralleled non-active switch in the 3L phase leg, a correction of the switching loss is made based on the DPT result of a 2L phase leg. By utilizing the proposed control and busbar, the switching speed of the power module increases, and lower switching loss is achieved. The inverter system is tested under room and low temperatures, achieving 99.0% estimated efficiency and 11.3 kW/kg power density.

9.2 Main Contributions

1. A novel current source gate drive is proposed that can provide constant gate current during the switching transient of the SiC MOSFET. The voltage fall time of the MOSFET is significantly decreased, and the switching loss is reduced.

2. A novel charge pump gate drive is proposed with simple structure and without additional control. The supply voltage can be dynamically increased to enhance the gate charging process. The turn-on switching loss of the SiC MOSFET is reduced, and the switching speed can be regulated with high flexibility by changing the external gate resistance.

3. An analytical model to predict the device overvoltage in 3L-ANPC converters is proposed. Taking into account the multiple switching loops, the relationship between the overvoltage and loop inductances is established to help the converter design.

4. A control scheme that can reduce the device overvoltage in 3L-ANPC converters is proposed. By avoiding the non-linear region of the device output capacitance, the drain-source overvoltage of the SiC MOSFET is reduced, which is beneficial for increasing switching speed.

5. A layout design methodology is proposed to reduce the loop inductances in 3L converters. A laminated busbar is designed and fabricated following the methodology, achieving significantly lower loop inductances compared with the existing references.

6. A high power inverter utilizing SiC power modules is established and tested for cryogenic applications. Special concerns are provided for low temperature operation.

9.3 Future Work

On the basis of the work presented in this dissertation, some recommended future work is discussed here:

1. Active gate drive technology to balance switching loss and EMI noise

The proposed current source gate drive and charge pump gate drive in this dissertation mainly focus on increasing the switching speed and reducing the switching loss. Although the overvoltage can be regulated, the EMI noise issue caused by the high dv/dt and oscillation on the drain-source voltage of the SiC MOSFET should be taken into consideration when implementing the gate drive. Hence, there should be a balance between the switching speed and EMI immunity according to the requirement of the applications.

One potential solution is to develop active gate drives with tunable dv/dt and di/dt during the device switching transient. This concept has already been proposed and developed for IGBTs such as by integrating a feedback unit to actively monitor the dv/dt or di/dt and adjust the switching speed. However, SiC MOSFETs switch much faster than IGBTs, making the bandwidth and execution time of such control a problem. In all, a gate drive with the ability to regulate the shaping of the device current and voltage during the switching transient should be beneficial for the operation of SiC MOSFETs.

2. Intelligent gate drive for high voltage SiC MOSFET

In this dissertation, the devices under test and analysis are mainly rated in the range of 900-1200 V. Actually, there is a trend to develop SiC MOSFETs with higher breakdown voltage (e.g. 10 kV) because of the superior voltage blocking ability of the SiC material, which raises higher requirement for gate drives.

First, the gate drive should meet the requirement of voltage isolation and common mode transient immunity (CMTI). Smaller coupling capacitance between the primary and secondary side of the isolation is preferred, which needs special design of the layout and structure of the auxiliary power supply and signal isolator.

Second, the gate drive should have the functions to monitor and control the SiC MOSFET completely. For example, the regulation of switching speed mentioned above needs to be included. Moreover, the online junction temperature monitoring, the lifetime estimation, and fast protection should all be realized.

3. Packaging development with multi-level topology integrated

The existing power modules available are mainly based on 2L structure, either a simple half-bridge or a three-phase six-pack inverter. With the wider adoption of 3L converters such as T-type or NPC type, several 2L power modules have to be combined to build the converter. As analyzed in the dissertation, large amount of effort is paid to design and optimize the layout for the 3L-ANPC converter. If all the devices needed for a 3L converter phase-leg are integrated in one module, the switching loops are easier to be optimized, and the size of the converter can be reduced. In addition, the integrated module can make it more friendly for end users because the layout design in a PCB or busbar can be significantly simplified.

4. Integration of traction inverter and motor

In hard switching applications, there is always a trade-off between high switching speed and noise caused by high dv/dt . For traction inverters driving motors, the increased dv/dt not only influence the performance of the converter, but also impacts the electric machine. In most cases, motors are connected with converters through power cables. These cables increase the weight and size of the system. Moreover, they introduce higher voltage stress at the motor terminal due to voltage reflection phenomenon, resulting in insulation issues. In consequence, either the switching speed of SiC MOSFETs needs decreasing, or dv/dt filters are required before the motors. Therefore, even though the concept of integrating inverters with motors is not new, eliminating the power cable can help fully utilize the high switching speed capability of SiC MOSFETs [194].

The main challenge of such integration is the reliability. With integration, the overall room of the system is limited, which makes the thermal design more difficult. Also, the vibration caused by motors calls for more robust power electronics systems.

5. Current source inverter

Current source inverters (CSIs) are far less popular than voltage source inverters (VSIs) mainly because they require power devices with reverse voltage blocking ability. With IGBTs or MOSFETs, two devices have to be connected in series, which significantly increases the conduction loss. Nevertheless, CSIs have some intrinsic superiorities over VSIs. For example, CSIs can operate at higher temperature by eliminating the large DC-link capacitors. Because of lower source voltage amplitude at high frequency domain as well as lower dv/dt , CSIs generate less conducted EMI and overvoltage. In addition, CSIs are much less vulnerable to short-circuit fault that is fatal for power semiconductors, especially WBG devices with less overcurrent withstand capability.

With emerging WBG devices, the conduction loss can be significantly reduced compared to the conventional Si devices with the same chip size. As a result, same or less loss can be achieved even though more device numbers are required. Considering the advantages mentioned above, CSIs become more attractive when combining with WBG devices.

6. Design interface for performance optimization

In this dissertation, SiC discrete devices and power modules are analyzed separately as the representatives of devices with different current ratings. In reality, whether the switching speed of a device is limited by gate drive or by parasitics is highly dependent case by case. The question is how to select the right device in a specific application and design the layout so that the overall performance of the converter can meet the requirement of the application.

To answer this question, a design interface should be developed. This is a systematic optimization tool that can generate the components and layout of the converter, and achieve good balance between efficiency, power density, EMI, cost and other aspects based on the specific requirement of the application.

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