Low Resource FPGA Based Time-to-Digital Converter

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Abstract: For the precise measurement of the time difference between the arrival of different signals coming from the different channels, the time-to-digital converter (TDC) implemented in Field Programmable Gate Array (FPGA) is a very useful device. The TDC implemented so far are basically tapped delay lines which provides a resolution of about 10 ps however such high resolution is necessary for some specific applications. So a low resource TDC implemented in FPGA is preferred which helps to measure the time difference between the signals.

Keywords: analog-to-digital converter (ADC), resolution, DPLL, clock generation, jitter

1. Introduction

Time-to-digital converter (TDC) is a device which can be used for the precise measurements of the time intervals between two or more physical events which are needed for many applications in science and industry [1] and provides the digital representation of the time they occurred. In the field of electronics time to digital converters are commonly used to measure a time interval and convert it into binary output and in some cases interpolating TDCs are also called time converters. The time-to-digital converters are widely used to measure the time interval for each incoming pulse in space science [2][3], high energy physics [2][4], laser range finders [2][5] and test instrumentation [2][6]. The TDC can be applied to frequency synthesis in delay-locked loops for faster acquisition and to avoid false-locking [7]. The working of TDC is similar to ADC except that instead of quantizing the amplitude of the signal, the TDC quantizes the time interval between two rising edges [8]. The TDC is implemented to measure the phase in All Digital Phase Locked Loops (ADPLL) [8] by replacing the loop amplifier which is only the analog component of PLL allowing the output word to drive a digital loop filter. The advantages of using DPLL over traditional PLL is that the need for large capacitors is eliminated within the loop filter by utilizing digital circuits in order to achieve the desired filtering function [9]. A narrow range time to digital converter (TDC) can be used to measure the input to output delay of a synchronizer which typically varies for each input transition over a range of 1 clock period. The delay can be as low as 1 to 2 clock periods or 2-3 clock periods or more dependent on the synchronizer design. The resolution of such time to digital converters is equivalent to that possible when using a counter and synchronizer clocked at very high frequency. Typically the resolution is equivalent to that obtained with a clock frequency of 10GHz or higher. State of the art TDCs have a resolution equivalent to that obtained with a clock frequency of 1 THz or more [10].

The proposed time-to-digital converter provides a resolution of 4 ns which is sufficient for the precise measurement of the difference of time between the arrivals of different signals coming from the different channels. Looking at the resource available the proposed TDC is implemented in SPARTAN 3E based FPGA which would provide a resolution of 4 ns.

The background of TDC is discussed in the second section. The proposed model for TDC is discussed in the third section. In the next section the methodology to implement the TDC is reported. The design of the various components to implement the TDC is discussed in the next section. The results of the components designed are discussed in the subsequent section. The advantages and limitations of the proposed model of TDC is discussed in the next section followed by a conclusion and future work. We finally conclude this piece with acknowledgement and references.

2. Model for Time-to-Digital Converter

The TDC is widely applicable in every branch of science and engineering. It is applicable in the field of physics where it can measure the time difference between the arrivals of showers of cosmic rays coming from the different channels [11]. In the field of communication, TDC is used for the reduction of jitter which will result in increase in bit rates.

A time-to-digital converter consists of the following essential components:

2.1. Digital Clock Manager (DCM): Digital Clock Manager (DCM) provides flexible and complete control of

the clock frequency [12]. DCM is a clock management system that enables the input clock frequency duplication, multiplication and division in addition to generating four different phase shifting clock versions 0^o, 90^o, 180^o and 270^o, maintaining the sane 50/50 ON-time/OFF-time relationship [13] as shown in Figure 1 [12].

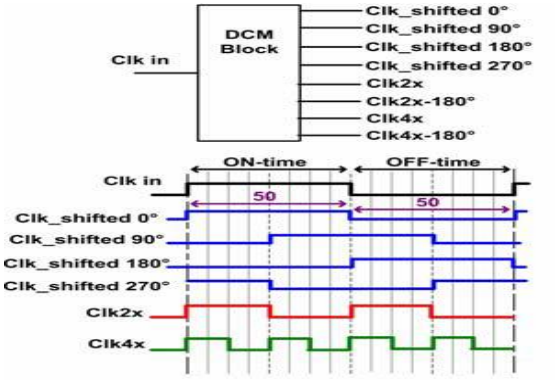


Figure 1: Block diagram of Digital Clock Manager [12]

The digital clock manager (DCM) primitive in Xilinx FPGA parts is used to implement delay locked loop, digital frequency synthesizer, digital phase shifter, or a digital spread spectrum. DCM feature available on some FPGAs (notably ones produced by Xilinx), for manipulating clock signals by:

- multiplying or dividing an incoming clock (DFS)
- reconditioning a clock for a steady duty cycle
- adding a phase shift using delay-locked loop (DLL)
- eliminating clock skew within an FPGA design.

2.2. Shift Registers: A shift register is a very important functional unit in modern digital systems, as it is used for helping to move data from one system to another. More importantly it is able to swap data transfer from serial to parallel, or parallel to serial. In our application inputs to the system are sampled and updated shift resister bank with same sampling frequency. Each channel having independent shift resister bank to store sampled data using shifting.

2.3. Random Access Memory (RAM): Data from the shift register are shifted to RAM to store the data temporarily.

2.4. Universal Asynchronous Receiver Transmitter: A universal asynchronous receiver/transmitter (UART) is a hardware device that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as TIA (formerly EIA) RS-232, RS-422 or RS-485. The universal designation indicates that the data format and transmission speeds are configurable. The electric signaling levels and methods (such as differential signaling etc.) are handled by a driver circuit external to the UART. We require developing a UART module in order to transfer the data stored in RAM to the computer using RS-232 protocol.

2.5. Multichannel Analyzer Software: Function of this software is to receive the data from UART through serial port (RS232) of the computer. These data will contain these two arrays of bit and the sampling interval information to a computing unit, then we can develop logic to evaluate the time difference between two pulses in same channel or the time difference between two pulses in two different channel.

3. Proposed Model for Time-to-Digital Converter

With a brief introduction of the various components of time to-digital converter, we have proposed a model for the implementaion of the proposed device which is shown in Figure 2.

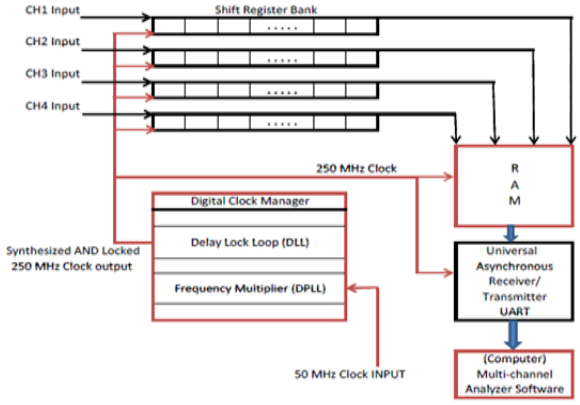


Figure 2: Proposed Model for Time-to-Digital Converter

The digital clock manager (DCM) will generate a clock of 250 MHz from an input of 50 MHz by using some sophisticated techniques like digital phase locked loop (DPLL) or the generation of high frequency clock using the delay of adder circuit. The clock generated from the delay of adder circuit is called carry-chain implementation of TDC. The four shift registers is used where the input data arriving from different channels are then fed to the corresponding shift register. All the four shift register are driven by the same clock. The input data from the four shift registers are then parallely transferred to the random access memory (RAM) module for temporary storage of the data from different channels. After that the data from the RAM module is then transferred to the multichannel analyzer software using RS-232 protocol and then we have to develop logic to measure the time-difference between the arrivals of four different input signals coming from the four different channels.

4. Methodology

To find the time difference between two different pulses can be explained using Figure 3.

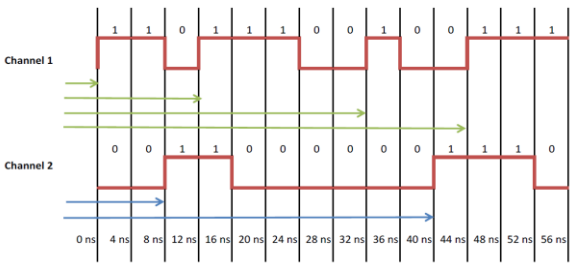


Figure 3: Working Methodology

Suppose we have two input channel of TTL input and we are sampling both the input with same sampling clock. In the example given in Figure 3, we have chosen a clock of 4 ns (250 MHz). After sampling the input for a certain interval of time, we can see that the input pulses have been encoded to a two arrays of digital bits for Channel 1 and Channel 2. If we pass these two arrays of bit and the sampling interval information to a computing unit, then we can develop logic to evaluate the time difference between two pulses in same channel or the time difference between two pulses two different channel. In the example shown in the Figure 3, for the Channel 1 there are four pluses in given sampling interval these are at 0^{th} ns, 12^{th} ns, 32^{th} ns and 44^{th} ns and that for Channel 2 there are two pluses in given sampling interval these are at 8^{th} ns and 40^{th} ns. If we have the timing information to pulse occurring in the same channel and different channel the gathering time difference information for any schemes of pulses is possible.

5. Design of the Components of the Proposed Time-to-Digital Converter

The design of various components used for the implementation time-to-digital converter is discussed in this section.

5.1 Design of Digital Clock Manager (DCM)

The digital clock manager can be implemented by using any of the following process:

5.1.1 High frequency generated by digital phase locked loop (DPLL)

The high clock frequency can be generated by using digital phase locked loop (DPLL) with a divider in the feedback loop. The basic block diagram of the DPLL with a divider block is shown in Figure 4 [14].

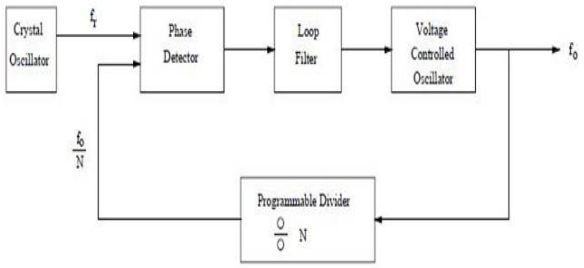


Figure 4: Block diagram of High Frequency Digital Phase Locked Loop [14]

Digital phase locked loop (DPLL) is most commonly used as frequency synthesizer [14]. In addition to the DPLL, it includes a very stable crystal oscillator with a programmable divider N in the feedback loop. The programmable divider divides the output of the voltage controlled oscillator (VCO) by N and locks to the reference frequency generated by a crystal oscillator [14][15]. The output frequency of the VCO is a function of the control voltage generated by the phase detector (PD). The phase detector output is proportional to the phase difference between the signals applied at its two inputs which control the frequency of the VCO. So the phase comparator input from the VCO through the programmable divider remains in phase with the reference input of the crystal oscillator. The VCO frequency is thus maintained at Nf_r where f_r is the reference frequency generated by the crystal oscillator [14].

The generation of high clock frequency can be obtained by using equations (1) and (2).

When the phase of the input reference signal is matched with the phase of the voltage control oscillator (VCO) through the programmable divider then

$$f_r = \frac{f_0}{N} \quad (1)$$

So the output frequency f_0 is given by

$$f_0 = N f_r \quad (2)$$

where, N is any integer, f_r is the input reference frequency and f_0 is the output frequency.

It is seen from equation (2) that the output frequency f_0 is a function of N and f_r. So if we have an input reference frequency as 50 MHz and we set N=5 then an output frequency of 250 MHz can be obtained. In our proposed TDC, a clock frequency of 250 MHz can be obtained using the digital phase locked loop with a divider in the feedback loop thereby providing a resolution of 4 ns which will help to precisely measure the time difference between the arrivals of different signals. The higher clock frequency and hence the resolution of the proposed TDC can also be increased with higher capacity RAM and higher frequency FPGA. However the cost will also increases as RAM increases.

5.1.2 High frequency clock generation using the delay of adder circuit

The delay that occurs in the adder circuit can be used as a high frequency clock which can be used to drive the shift registers of the proposed TDC device and also to sample the signals arriving from different channels. This technique of generation of clock using the delay of adder circuit which is in pico-second range [15] is called carry-chain implementation of TDC. The delay occurred in 4-bit ripple carry adder and look-ahead carry adder for the generation of high frequency clock is discussed in this piece.

(a) Clock generation using the delay of 4-bit ripple carry adder

The basic block diagram of 4-bit ripple carry adder is shown in Figure 5.

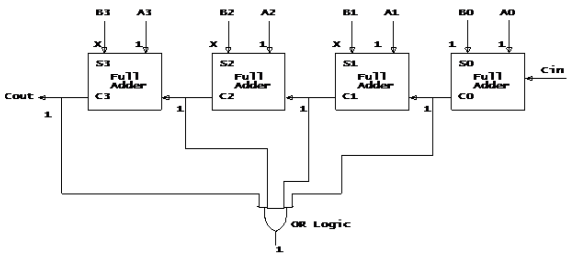


Figure 5: Block diagram of 4-bit Ripple Carry Adder

The 4-bit ripple carry adder is constructed by cascading four full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. For an n-bit parallel adder, it requires n computational elements (FA). The main objective of designing the parallel adder is to evaluate the delay occurred in the parallel adder and use this delay to generate the high frequency clock as the delay in the parallel adder is in pico-second range. In order to achieve this delay we have to take the inputs of the full adder in such a way that when we add the sum bit is always '0' and the carry bit is always '1'. The 4-bit carry generated after the addition operation is fed to the OR logic to provide the output. However the generation of the high frequency clock from the delay of 4-bit ripple carry adder is under study process.

(b) Generation of clock frequency using the delay of look-ahead carry adder

The basic circuit diagram of look ahead carry adder is shown in Figure 6.

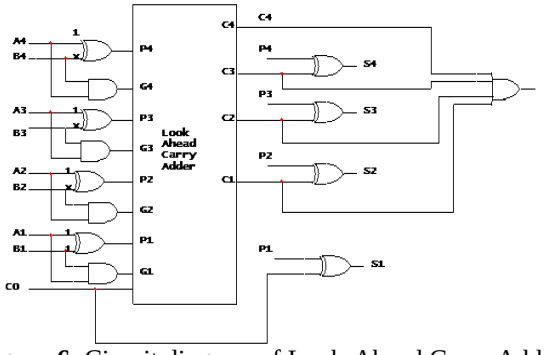


Figure 6: Circuit diagram of Look-Ahead Carry Adder

The look ahead carry adder calculates the carry signal in advanced based on the input signals. It is based on the fact that a carry signal will be generated in two possible cases:

- When both the input bits A_i and B_i are high i.e. '1'.
- When at least one of the input bits are high and the previous carry bit is high.

The internal signals P_i and G_i are given by equations (3) and (4) respectively.

$$P_i = A_i \oplus B_i \qquad (3)$$

$$G_i = A_i B_i \qquad (4)$$

where, G_i is called the carry generate signal and P_i is called carry propagate signal.

It is clear from equations (3) and (4) that computing the values of P_i and G_i only depend on the input operand bits (A_i and B_i). Thus these signals settle to their steady state value after the propagation through their respective gates.

The Boolean expression of the carry outputs of various stages can be written as follows:

$$C_1 = G_1 + P_1 C_0$$

$$C_2 = G_2 + P_2 C_1 = G_2 + P_2 G_1 + P_2 P_1 C_0$$

$$C_3 = G_3 + P_3 C_2 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_0$$

$$C_4 = G_4 + P_4 C_3 = G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 C_0$$

From the circuit diagram shown in Figure 6, first we generate all P and G signals (each consists of an XOR gate and an AND gate). The output of P's and G's are valid after 1τ. The carry signals are generated as defined by the expressions given above. The output signals are valid after 3τ. The four XOR gates will generate the sum signals and the output signals are valid after 4τ. The output of the generated carry signals is fed to the OR logic to generate high frequency clock. The generation of high frequency clock from the delay of look ahead carry adder is under study process.

5.2 Design of Shift Register

For the implementation of time-to-digital converter, we have considered four different channels where the input signals from each channel are fed to the four different shift registers. The four different shift registers are driven by the same clock pulse generated by the digital clock manager. The objective of shift register in our applications is to take the data from the four channels serially and finally after the shifting operations are over the data from all the channels are transferred from the four different shift registers.

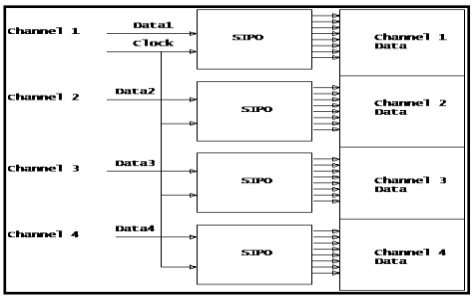


Figure 7: Block diagram of SIPO Shift Register

To fulfill this objective we have used four different serial-in-parallel-out (SIPO) registers all are driven by the same clock

pulse which takes input coming from the corresponding channels serially and finally after some time the data will be transferred in parallel. So the block diagram of the SIPO register is shown in Figure 7.

From the block diagram shown in Figure 7, the four different arbitrary 8-bit input data namely, data1, data2, data3 and data4 coming from four different channels namely channel1, channel2, channel3 and channel4 respectively are fed to four different SIPO registers. The four SIPO registers are driven by the same clock. At this time I am arbitrary taking the clock frequency, however this clock frequency is provided by the digital clock manager (DCM). The 8-bit input data from different channels will be fed serially to the SIPO registers and after the eighth clock the 8-bit data from all the SIPO registers is fed to the RAM module.

6. Experimental Details

The time-to-digital converter can be implemented by using all its essential components. First of all we have to generate a clock frequency which can be generated by digital clock manager. For the design of clock manager we can have two approaches. The first approach is the generation of high frequency clock by using digital phase locked loop (DPLL) with a divider as a feedback loop. The second approach is to generate a high frequency clock using the delay of adder circuit. For this we have used two types of adder circuits namely 4-bit parallel adder and look-ahead carry adder from which the delay occurred can be used as a high frequency clock. To implement both 4-bit ripple carry adder and look-ahead carry adder, our objective is to choose the condition such that we have to take those input bits for which the carry bit is high in every case. In that case, if we have the inputs as A,B and C_{in} we have chosen the input such as A is "1111" and B is "0001" and the previous carry C_{in} is chosen to be '0'. So after the addition operation of LSB's of A, B and C_{in} the first carry bit obtain is '1' which is added with the next higher input bit. The next high bit of A is '1' and B is '0' so after the addition again the second carry bit is '1' which is added with the next higher bit. In this way we can obtain four high carry bits which are then fed to the OR logic and its output is one. In adder circuit, delay occurs because after the operation of the first full adder circuit, the second full-adder circuit is active only when the first carry bit is fed to it and similarly this delay increases for the subsequent full adder circuits. So we can use these different delays as a high frequency clock. The generation of high frequency clock using the delay of the adder circuit is under study process.

The signals coming from four different channels are fed to four different serial-in-parallel-out (SIPO) shift registers. All the shift registers are driven by the same clock generated by digital clock manager (DCM). For the design of SIPO shift registers we have taken eight bit of input data coming from four different channels and all the four shift registers are driven by the same clock pulse. At this stage we are taking an arbitrary clock pulse to test the working of the proposed model for SIPO shift register. The eight bit data from four different channels are then fed to the corresponding SIPO shift register and at the eight clock pulse all the data from the four SIPO registers are transferred to the RAM module in parallel. The RAM module will store the data from the four different channels and finally transferred to a computing unit by using RS-232 protocols and then we have to develop logic for the precise measurement of the time difference between the arrival of the input signals arriving from the four different channels.

7. Results and Discussion

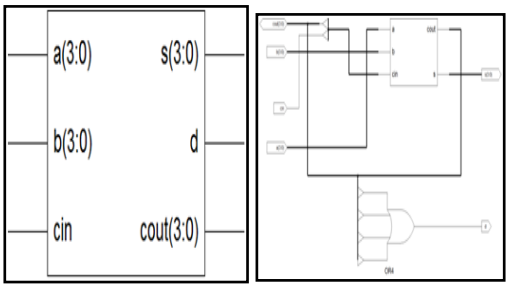
In this section we will discuss the results obtained till now after the design of some of the components of TDC.

7.1 Results of Adder Circuit

The results of 4-bit ripple carry adder and look-ahead carry adder are discussed.

7.1.1 Results of 4-bit Ripple Carry Adder

The RTL schematic of 4-bit ripple carry adder is shown in Figure 8.



(a) (b)

Figure 8: RTL Schematic of 4-bit Ripple Carry Adder

From the RTL schematic of 4-bit ripple carry adder shown in Figure 8, we have taken four bits inputs 'A' and 'B' and a previous carry 'C_{in}.' The output obtained is the four bit sum and four bit carry. The four bit carry is then fed to the OR logic to produce output as 'D'.

The test bench waveform of 4-bit ripple carry adder is shown in Figure 9.

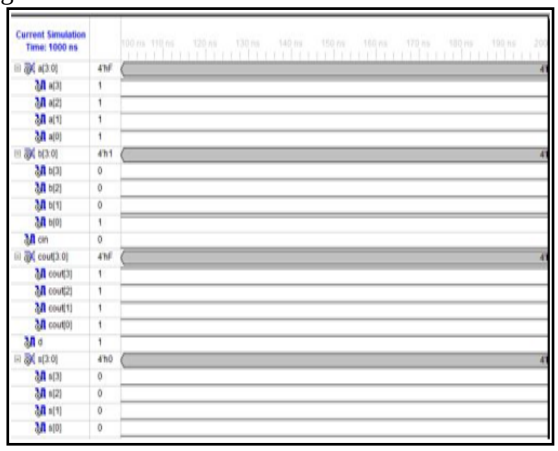


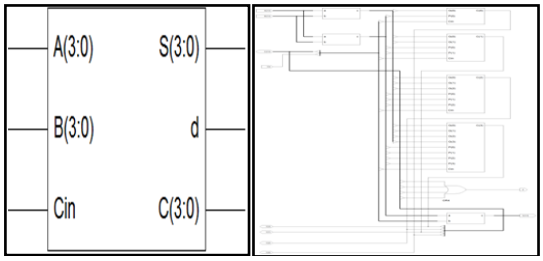
Figure 9: Test Bench Waveform of 4-bit Ripple Carry Adder

From the test bench waveform shown in Figure 9, we have taken 4-bit augend A as "1111", and the 4-bit addend B as "1000". The previous carry Cin is taken as zero. After the addition operation the 4-bit sum obtained is "0000" and the

4-bit carry obtained is "1111". The 4-bit carry is fed to the OR logic and the output of the OR logic is '1'.

7.1.2 Result of Look Ahead Carry Adder

The RTL schematic of look-ahead carry adder is shown in Figure 10.



(a) (b)

Figure 10: RTL Schematic of Look-Ahead Carry Adder

From the RTL schematic of look-ahead carry adder shown in Figure 10, we have taken four bits input s A and B and a previous carry C_{in}. The output obtained is the four bit sum and four bit carry. The four bit carry is then fed to the OR logic to produce output as D. The test bench waveform of look-ahead carry adder is shown in Figure 11.

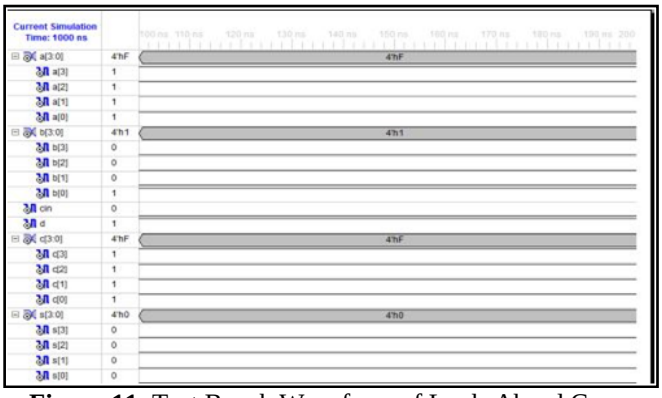
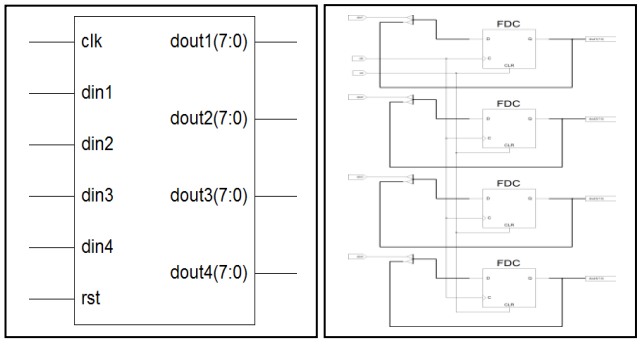


Figure 11: Test Bench Waveform of Look-Ahead Carry Adder

From the test bench waveform shown in Figure 11, we have taken 4-bit augend A as "1111", and the 4-bit addend B as "1000". The previous carry Cin is taken as zero. After the addition operation the 4-bit sum obtained is "0000" and the 4-bit carry obtained is "1111". The 4-bit carry is fed to the OR logic and the output of the OR logic is '1'.

7.2 Results of Serial-in-Parallel-out (SIPO) Shift Register

The RTL schematic of serial-in-parallel-out shift register is shown in Figure 12.



(a) (b)

Figure 12: RTL Schematic of Serial-in-Parallel-out (SIPO) Shift Register

From the RTL Schematic shown in Figure 12, we have four 8-bit input data say din1, din2, din3 and din4 coming from four different channels are fed serially to the four different SIPO registers. The four different SIPO registers are driven by the same clock pulse and each SIPO registers produces 8-bit output parallelly as dout1, dout2, dout3 and dout4. The reset pin is used to reset all the data coming from the different channels and it is active high pin i.e. if reset is '1' then the data will be reset.

The test bench waveform of serial-in-parallel-out shift register is shown in Figure 13.

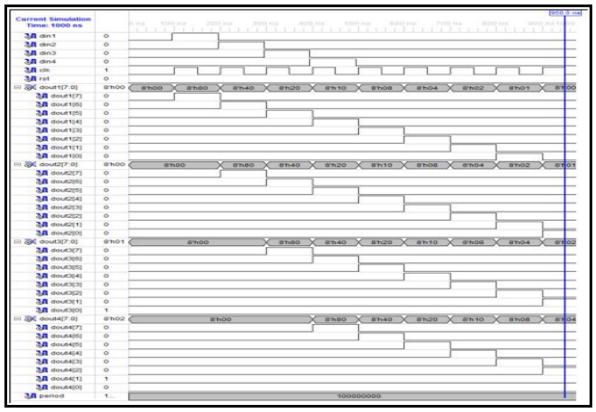


Figure 13: Test Bench Waveform of Serial-in-Parallel-out (SIPO) Shift Register

From the test bench waveform shown in Figure 13, the four input din1, din2, din3 and din4 coming from four different channels are fed to four different SIPO registers and each SIPO registers are driven by the same clock. At the end of the eighth clock we obtained the complete 8-bit data as can be seen from the test bench waveform.

8. Advantages and Limitations

Advantages

- Very simplistic design of TDC.
- Low cost as low resource components are used.

Limitation

- Low resolution due to low resource used.

9. Conclusion

Time-to-digital converter is widely used in high energy physics and other branches of science and engineering. In the field of communication, the TDC helps to provide low jitter and as a result it increases the bit rate. We have a detailed discussion on the different methods to implement the time-to-digital converter. Firstly we have a detailed study on the implementation of digital clock manager (DCM) and then we have discussed two approaches two implement DCM based on that study. After that we have discussed the design of serial-in-parallel-out (SIPO) shift register which is required

since the input signals coming from different channels has to be stored and then shifts the data from the shift registers after some time for further processing.

10. Future Work

After completion of the SIPO shift register, we would try to implement the RAM module for the storage of data from the different SIPO registers and then transferred to the computer by using RS-232 protocols. After transferring the data from the RAM to the computing unit, we have to develop logic to evaluate the time difference between the two pulses in between different channels. Also we would try to increase the resolution of the time-to-digital converter by implementing some sophisticated techniques such as carry chain design of TDC and tapped delay-line TDC. One feature is to implement the design using a Smart Phone compatible Android Apps.

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