Design Consideration and Impact of Gate Length Variation on Junctionless Strained Double Gate MOSFET

K. E. Kaharudin, Ameer F. Roslan, F. Salehuddin, Z. A. F. M. Napiah, A. S. M. Zain

Abstract*: Aggressive scaling of Metal-oxide-semiconductor Field Effect Transistors (MOSFET) have been conducted over the past several decades and now is becoming more intricate due to its scaling limit and short channel effects (SCE). To overcome this adversity, a lot of new transistor structures have been proposed, including multi gate structure, high-k/metal gate stack, strained channel, fully-depleted body and junctionless configuration. This paper describes a comprehensive 2-D simulation design of a proposed transistor that employs all the aforementioned structures, named as Junctionless Strained Double Gate MOSFETs (JLSDGM). Variation in critical design parameter such as gate length (L_g) is considered and its impact on the output properties is comprehensively investigated. The results shows that the variation in gate length (L_g) does contributes a significant impact on the drain current (I_D), on-current (I_{ON}), off-current (I_{OFF}), I_{ON}/I_{OFF} ratio, subthreshold swing (SS) and transconductance (g_m). The JLSDGM device with the least investigated gate length (4nm) still provides remarkable device properties in which both I_{ON} and g_m(max) are measured at 1680 µA/µm and 2.79 mS/µm respectively.

Keywords* : Gate length, on-current, off-current, subthreshold swing, transconductance.

I. INTRODUCTION

Over the past decades, the dimension of a transistor has been miniaturized from micrometer into nanometer regime, following the Moore's law prediction. Scaling attempt in a transistor's size has been proven to increase the drive current and also the device's speed. However, transistor's scaling is becoming even more intricate with each successive transistor generation reaches the theoretical and technological restriction. For instance, the aggressive scaling of a transistor reaches a critical situation where an extremely thin gate oxide are no longer capable of suppressing the short channel effects (SCE) effectively [1]. As a result, the SCE is becoming more severe, thus degrading both gate controllability and electron mobility of a transistor [2].

High leakage current is regarded as one of the main obstacles in transistor's scaling. The traditional Poly/SiO_2 stack structure is no longer practical for sub-nanometer transistor technology mainly due to SCE and poly depletion effects. An ultra-small transistor requires an increased capacitance of gate dielectric to suppress SCE problems, which can be achieved by reducing the insulator's thickness [3]. However, a massive attempt on reducing the gate oxide would results in larger gate leakage, which consequently affects the transistor's performances. Theoretically, the leakage current is found unacceptably high when the gate oxide is scaled below 2 nm of thickness [4]. As a solution, an increased dielectric material (high-*k*) is employed to substitute silicon dioxide (SiO_2) in which a thicker dielectric layer can be growth on the top of silicon body without having electrical thickness penalties [5]. The high-*k* dielectric is normally incorporated with metal-gate for solving the compatibility issue between poly-gate and high-*k* dielectric that might result in lower on-current (I_{ON}) [6].

Multi-gate transistor is one of the solutions to prolong the continuity of transistor scaling. This type of structure takes advantage of an enhance channel to reduce the SCE. The term "multi-gate" refer to the transistor's structure that comprises more than a single gate in which these gate electrodes is wrapped around the channel region [7]. One of the common configurations of multi-gate transistor is called double-gate MOSFET. Double-gate MOSFET's structure has been proven to be less sensitive to SCE mainly because of its excellent electrostatic control over the channel region [8-11]. The mobility of the electrons/holes within the conductive channel are improved due to its excellent gate control that allows a significant amount of volume inversion [12]. The current drivability in the double-gate structure can be improved without having any increment in the area by simply etching the silicon body a lot more thinner[13, 14].

Fully depleted configuration is an important feature used in most of double-gate and silicon-on-insulator (SOI) transistors [15-20]. The fully depleted channel is found to be very effective in mitigating the SCE [21-23]. The SCE become more prominent when the subthreshold swing (SS) is increased in which the degrading drain current (I_D) stands up against a gate voltage (V_G) and threshold roll-off to negative direction in the case of the n-channel transistor. These effects should be well mitigated by lessening the thickness of silicon body to less than 20 nm [24]. In ultrathin channel, the majority carriers (electrons/holes) concentration will be fully depleted when a certain amount of voltage is supplied to the gate terminal.

Revised Manuscript Received on July 22, 2019.

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As a certain threshold reached, the channel begins to deplete and a surface inversion layer is formed. The fully depleted channel could avoid high electric field that might cause an increased SS at high drain bias, thanks to a fully or partly elimination of floating body effect [25-27].

Strained silicon is also one of the alternative methods to improve the carrier mobility of a transistor [28-30]. The strained silicon method offers significant enhancements in transistor's performance via tuning the material properties rather than geometrical structure and carrier's density [31]. The physical attributes of strained silicon is basically due to the presence of incorporated germanium in the silicon substrate [32]. As the different layers stacking on each other, the strained channel would experience a change in band gap energies [33]. The primary advantage of strained silicon method is to form high mobility area within the conductive channel region. However, the mobility within strained channel is often diminished by phonon scattering as the electrons/holes are not totally restrained due high electric field [34]. As a solution, high doping concentrations and shorter channel are employed so that the carrier mobility can be effectively enhanced.

Junctionless configuration is another alternative solution to allow the continuity of transistor's shrinkage without degrading the device performance [35-38]. This configuration has been aggressively studied and applied by many researchers due to its simplified fabrication process [39]. Junctionless transistor totally neglects the need of complicated channel and source/drain S/D engineering in forming an ultra-shallow S/D junctions with high doping concentration gradient [40]. The working principle of junctionless transistor is totally relies on the heavily doped channel and S/D regions that utilizes similar type of dopants [41]. Junctionless transistor is normally fabricated using thin/narrow semi conductive layer which enables the majority carriers to be fully depleted during off-state condition [42]. Highly doped of an extremely thin channel would allow a decent flow of current from the source to the drain as the transistor is switched on [43].

This paper focuses on describing a comprehensive 2-D simulation design of a new transistor's structure with consideration of all the aforementioned methods, called as Junctionless Strained Double Gate MOSFETs (JLSDGM). Furthermore, the impact of critical parameter variations on the output properties is also investigated. The organization of this work is structured as follows: Section 2 describe the device structure of JLSDGM device and its process flow using Silvaco Athena TCAD tools. Section 3 briefly explains the transistor's simulation employing Silvaco Atlas device simulator. Section 4 provides a comprehensive insight on the impact of gate length (L_g) on drain current (I_D), on-current (I_{ON}), off-current (I_{OFF}), I_{ON}/I_{OFF} ratio, subthreshold swing (SS) and transconductance (g_m). Section 5 suggests the possible recommendations for the future work. The conclusion summarizing this simulation study is presented later in section 6.

II. PROCEDURE FOR PAPER SUBMISSION

2-D process simulation for the JLSDGMs was conducted in which the process flow of the device is shown in Fig.1. The process simulation (via Athena module) comprises the initial SiGe substrate (Ge<20%), ultrathin silicon layer formation (1nm), channel doping, high-*k*/metal-gate (HKMG) deposition, source/drain doping, metallization and structure reflection.

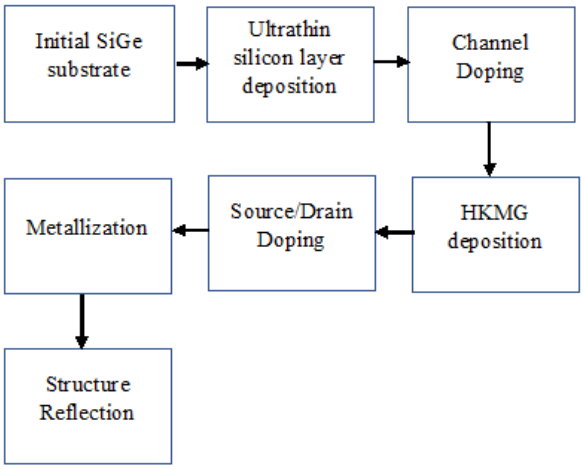

Fig. 1. Simulated process flow for ultra-thin JLSDGM

The structure of JLSDGM device employs silicon germanium (SiGe) with thickness of 8nm as the main substrate due to its larger interatomic distances compared to a pure crystal of silicon. Then, an ultrathin silicon film is formed on the top of SiGe layer in order to create a strained silicon layer. The strained silicon layer is formed due to a phenomenon in which the silicon atoms are strongly stretched from each other as the majority atoms inside the conductive channel attempting to align with the SiGe atoms. As a result, the ultrathin silicon layer becomes tensile stretched substantially due to its relatively smaller lattice constant than the main substrate (SiGe). The strained channel is then heavily doped with $1x10^{17}$ cm^{-3} of Arsenic dose (n-type). Double-gate configuration is applied in order to extend enhanced gate controllability over the channel. Tungsten silicide (WSi_x) layer is used as the metal-gate due to its tunable work function capability [44]. This WSi_x-gate is then deposited on a high-*k* dielectric layer which provides better compatibility than a poly-gate.

Titanium dioxide (TiO_2) is used as a gate dielectric attributable to its remarkable high permittivity (~85 eV) which allows the employment of thicker insulator. For instance, a TiO_2 layer with a dielectric constant of 85 eV (compared to 3.9 eV for silicon dioxide) can be deposited 21 times thicker than silicon dioxide (SiO_2) which subsequently assists in reducing the leakage of electrons across the dielectric layer, while retaining the similar capacitance [45]. Therefore, equivalent oxide thickness (EOT) is used to indicate how thick SiO_2 layer would need to be to produce the same effect as the TiO_2 material being used. Since the thickness of TiO_2 used in this structure is 3 nm, the EOT can be calculated as:

$$EOT = \left[\frac{\varepsilon_{SiO2}}{\varepsilon_{TiO2}}\right] T_{TiO2} \quad (1)$$

where ε_{SiO2} is the permittivity of SiO_2 which is 3.9, ε_{TiO2} is the permittivity of TiO_2 which is 85 and T_{TiO2} is the physical thickness of TiO_2 layer. Hence, the *EOT* of the insulator for this structure would be 0.138 nm.

The source/drain (S/D) regions for n-type device are doped with the same type of dopant used in previous channel doping process in order to form N N^+ N configuration (junctionless). The metallization process is then conducted by sputtering the aluminum layer on the top part of the device. Any excessive aluminum layer is removed accordingly to pattern the contacts and the electrodes. The investigated geometrical and process parameters of the JLSDGMs are listed in Table I. Finally, the structure is reflected in both *x* and *y* directions as depicted in Fig. 2.

Table- I: Parameters used in the simulated JLSDGMs

Variables	Units	Fixed value	Manipulated range
Gate Length, L_g	nm	6	4-12
Channel doping, N_{ch}	Atom/cm^3	1.0E17	N/A
S/D doping, N_{sd}	Atom/cm^3	1.0E13	N/A
Metal work-function, *WF*	eV	4.6	N/A

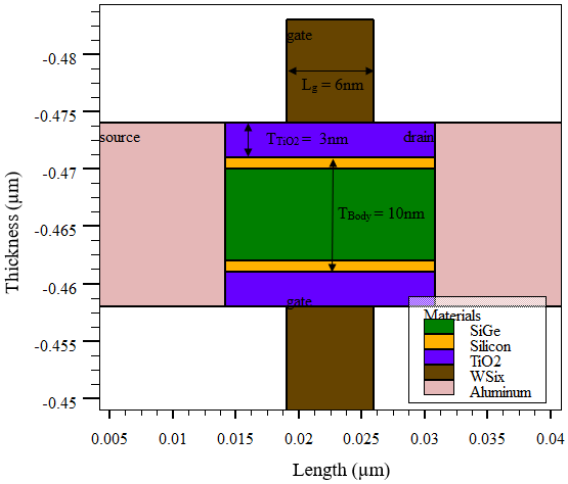

Fig. 2. 2-D cross section of the JLSDGM device

III. DEVICE SIMULATION

Device simulation for n-type JLSDGM device is carried out through Silvaco TCAD Atlas module. The output structure from the previous Athena module is fed into Atlas module as mesh infile. Fig. 3 depicts the contour mode of the JLSDGM device, showing the net doping for SiGe, silicon, titanium dioxide, tungsten silicide and aluminum. Based on the contour mode, the effective channel length (L_{eff}) is approximately measured at 8nm.

The n-type JLSDGM device is characterized via device simulation (Atlas module) in linear and saturation mode. The device simulation employs a built-in physical model that takes the drift diffusion (DD) model, simplified Boltzmann carrier statistics, inversion mobility model combined with Shockley-Read-Hall (SRH) recombination into account. Since the proposed device is non-planar, the Lombardi CVT model is selected to provide an accurate simulation [46]. The Lombardi CVT model is employed for considering the scattering processes such as lattice vibration (phonons), impurity ions, surfaces, and other material imperfections during the simulation. Critical device characteristics such as on-state current (I_{ON}), off-state current (I_{OFF}), I_{ON}/I_{OFF} ratio, subthreshold swing (*SS*) and transconductance (g_m) can be extracted from the generated I_D-V_G curve. The device simulation conditions for the investigated characteristics are set up as shown in Table II [46].

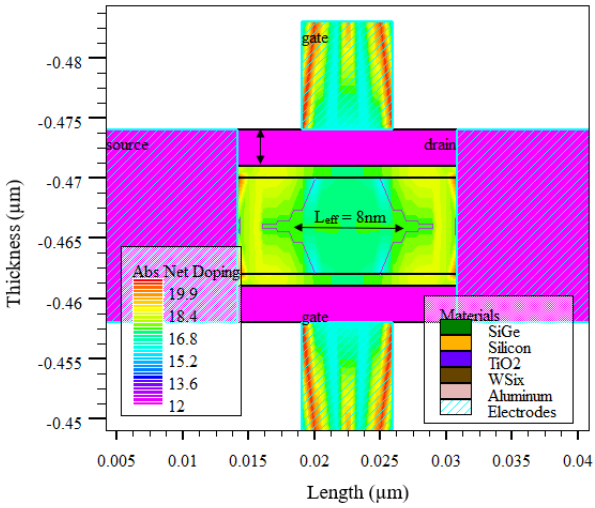

Fig. 3. Contour mode of the JLSDGM device

Table- II: Device Simulation Conditions

Electrical Characteristics	Drain Voltage, V_D (V)	Gate Voltage, V_G (V)		
		$V_{Initial}$	V_{Step}	V_{Final}
Threshold Voltage, V_{TH} (V)	0.5	0	0.1	1.0
On-state Current, I_{ON} (µA/µm)	0.5	0	0.1	1.0
Off-state Current, I_{OFF} (A/µm)	0.5	0	0.1	1.0
Subthreshold Slope, SS (mV/decade)	0.5	0	0.1	1.0
Transconductance, g_m (mS/µm)	0.5	0	0.1	1.0

IV. IMPACT OF GATE LENGTH VARIATIONS ON JLSDGM'S PERFORMANCES

For the purpose of comprehensive invesigation on the behaviors of JLSDGM device, the impact of the gate length variations on I_D-V_G transfer characteristics is presented in this section. Section A, B, C, and D describe the impact of variations in gate length (L_g) upon the I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, *SS* and g_m respectively.

A. Impact of Gate Length Variations on On-current

In transistor's fabrication, physical gate length (L_g) is the most crucial parameter which is grown using the minimum feature size of mask in a particular technology node.

The impact of L_g variations on the device's characteristics is important to be investigated because it could contribute significant changes in L_{eff} as well as the saturation current. Fig. 4 shows the combined plot of I_D-V_G transfer characteristics at V_D = 0.5V in linear and log scales for multiple L_g variations.

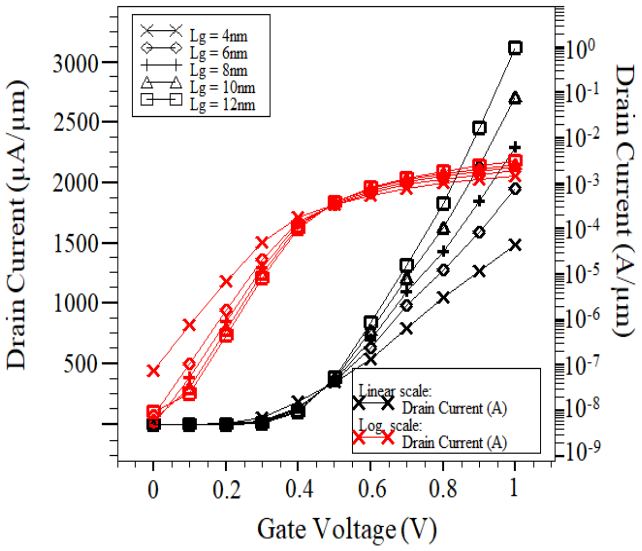

Fig. 4. Combined plot of the I_D-V_G transfer characteristics at V_D = 0.5 V

It is observed that the drain current (I_D) of the JLSDGM device is gradually decreased as the L_g is scaled down from 12nm to 4nm, shifting the I_D-V_G curves towards the maximum positive *x*-axis (1V). Shrinking the L_g would reduce the area of the inverted channel, predominantly due to the shorter distance between the source and the drain regions. As a result, the V_{TH} decreases, causing the I_D to gradually decrease as the L_g is further scaled down. However, the maximum I_D at V_G = 1V, also known as on-current (I_{ON})_ is still considerably high for the device with 4nm of gate length, thanks to the positive impact of double-gate structure, ultrathin body, strained channel and junctionless configuration. Fig. 5 depicts the impact of L_g variations on the I_{ON} characteristic of the JLSDGM device.

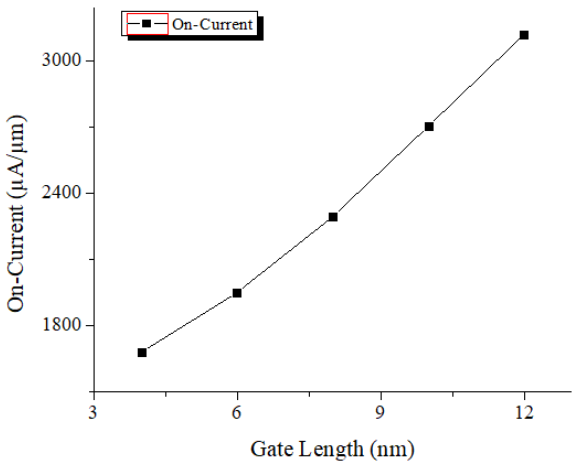

Fig. 5. Plot of on-current versus gate length

Based on the plot, it is observed that the I_{ON} increases almost linearly with the increase of the L_g. The I_{ON} of the JLSDGM device is decreased by approximately 46% as the L_g is scaled down from 12nm to 4nm. The device with 4nm of gate length still exhibits a remarkable on-current characteristic which is measured at 1680 μA/μm. This is mainly contributed from the implementation of double-gate structure and HKMG that boost the amount of electron inversion into the channel region, even with a shorter effective channel length. The double-gate mode enhances the ability to regulate the distribution of the field and flow of the current in the channel. With an extra gate, the gate to channel coupling is doubled, resulting in a better SCE's suppression and higher current density [47].

The utilization of HKMG also contributes to high I_{ON} value due to a total elimination of poly depletion effects. The JLSDGM device with HKMG emulates like it has a thinner oxide in inversion with associated improved capacitance that subsequently results in significant I_{ON} improvements. Furthermore, the reduction in L_g cause high average stress across the channel due to much smaller channel region [48]. The application of strained channel is aimed to boost the electron mobility with high doping concentration, thus leading to higher on-current [49].

B. Impact of Gate Length Variation on Off-current

According to Fig. 4, the off-current (I_{OFF}) is measured when the gate voltage (V_G) is zero and the drain voltage (V_D) is set equal to the drain supply (V_{DD}) which is 0.5V. In other words, I_{OFF} is the drain current (I_D) when there is no input voltage supplied to the gate. As the gate length shrinks, I_{OFF} becomes one of the crucial characteristics that need to be considerably monitored. Fig. 6 depicts the impact of L_g variation on I_{OFF} characteristic.

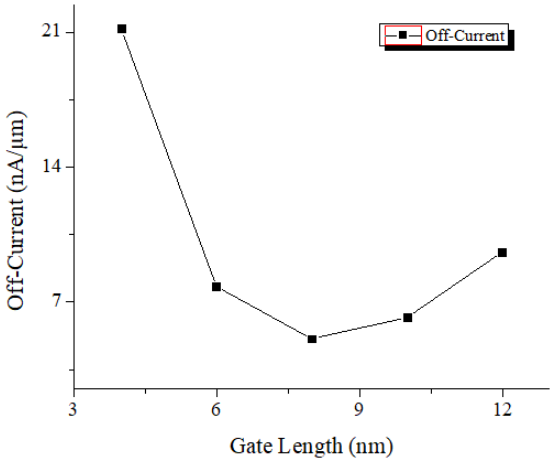

Fig. 6. Plot of off-current versus gate length

Based on the plot, it can be concluded that the L_g variation cause unpredictable behavior of drain current in off-state condition. Such occurrence is mainly due to the variation of physical gate length upon the band-to-band-tunneling (BTBT) current. During off-state condition, the electrons in the channel is randomly distributed that result in uncertain amount of positive trapped charges in the insulator. This would lead to random variations within the electric field eventually causing erratic leakage behaviors.

The JLSDGM device with 4nm of L_g demonstrates the highest I_{OFF} value, implying that the channel begin to suffer from the SCE at this point.

C. Impact of Gate Length Variations on I_{ON}/I_{OFF} ratio

I_{ON}/I_{OFF} ratio is the numerical expression to indicate increased performance (higher I_{ON}) and reduced leakage power (lower I_{OFF}) for the CMOS transistors. Normally, when a transistor has more gate control over the channel, the I_{ON}/I_{OFF} ratio would be larger. The I_{ON}/I_{OFF} ratio in JLSDGM device is largely determined by the position of the V_{TH} in which its value would significantly affect the amount of current in on-state and off-state condition. The I_{ON}/I_{OFF} ratio of JLSDGM device is measured at V_G = 0V and V_G = 1V while V_D = 0.5V (constant) and equals to maximum allowed V_{DD}, which can be calculated as:

$$I_{ON} / I_{OFF} ratio = \frac{I_{ON}(I_D when V_G = 1V)}{I_{OFF}(I_D when V_G = 0V)} \quad (2)$$

Fig. 7 depicts the impact of L_g variation on I_{ON}/I_{OFF} ratio for JLSDGM device.

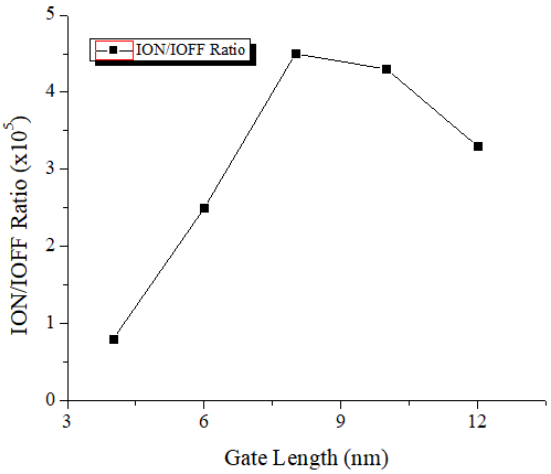

Fig. 7. Plot of I_{ON}/I_{OFF} ratio versus gate length

Based on the plot, it can be seen that the I_{ON}/I_{OFF} ratio improves linearly as the L_g increases from 4nm to 8nm. However, the I_{ON}/I_{OFF} ratio begins to decline when the L_g is scaled beyond 8nm. This is because the variation in L_g has caused slight increases in drain leakage, which makes the device requires a larger gate voltage to turn on. The JLSDGM device with 8nm of L_g exhibits the largest I_{ON}/I_{OFF} ratio which is measured at 4.5 x 10^5. The largest I_{ON}/I_{OFF} ratio of a transistor should be attained as large as possible because it decides the speed requirement in logic stage and current carrying capability. The larger I_{ON}/I_{OFF} ratio would contribute to much lower static power dissipation due to off-state leakage. From the perspective of inverter's design consideration which an inverter comprises a series of of two resistors, the larger I_{ON}/I_{OFF} ratio between these two equivalent resistors yields better output level.

D. Impact of Gate Length Variations on SS

Subthreshold swing (*SS*) is a crucial characteristic that decides the scalability limits of a transistor. When the I_D is plotted on a logarithmic scale as shown in Fig. 4, the I_D is observed varies exponentially with the V_G below the threshold value. The increasing rate of I_D below the V_{TH} is characterized by the *SS*, which is relationally calculated as:

$$SS = \left[\frac{dV_G}{d(\log_{10} I_D)} \right] \quad (3)$$

Fig. 8 depicts the impact of L_g variation on *SS* for JLSDGM device.

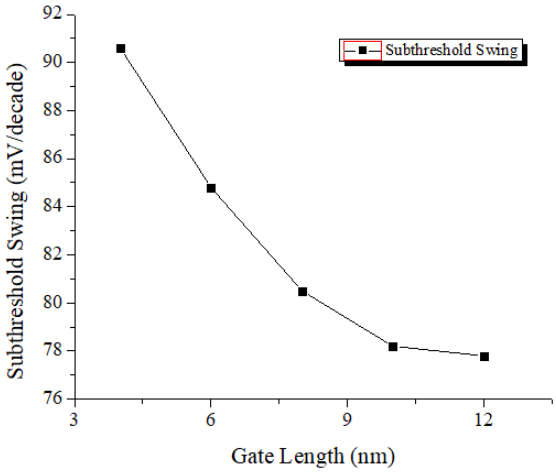

Fig. 8. Plot of subthreshold swing versus gate length

Based on the plot, it can be concluded that the variations in L_g is inversely proportional with the *SS*, which means that as the L_g is further scaled down from 12nm to 4nm, the SS value is constantly increasing. The *SS* should be minimized when it is allowed by certain applications. Smaller *SS* implies that the JLSDGM has better controllability of the gate governing the channel that leads to much improved I_{ON}/I_{OFF} ratio, low leakage and low power consumption. In practice, the gate control is not always perfect due the electrostatic coupling between the channel and the ultrathin body via the depletion layer [7]. The SCE becomes noticeable when there is an increase in *SS* in which the degrading I_D withstands the increasing V_G with threshold roll-off to negative direction. These effects can be effectively suppressed by etching the silicon body much thinner, thus subsequently decreasing the *SS*. The JLSDGM device with 12nm of L_g demonstrates the lowest *SS* which is measured at 77.8 mV/decade. A lower *SS* value indicates that the device has a very high-speed switching capability, meaning that less changes in V_G is required to increase one decade of I_D.

E. Impact of Gate Length (L_g) Variation on g_m

Transconductance (g_m) is a numerical expression that represents the output performance of a transistor, expressing the relation between the current through the output and the voltage across the input.

The transconductance (g_m) in JLSDGM device is particularly defined as the change in the I_D divided by the minor change in the V_G with a constant V_D = 0.5V which is mathematically described as:

$$g_m = \frac{\partial I_D}{\partial V_G} \quad (4)$$

Fig. 9 depicts a plot of transconductance (g_m) as a function of gate voltage (V_G) for multiple L_g variation.

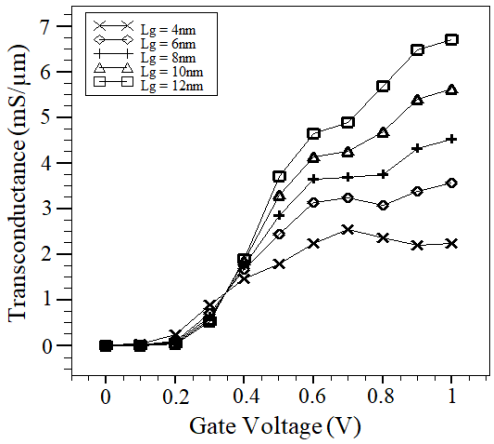

Fig. 9. Plot transconductance (g_m) as a function of V_G

Based on the plot, it is observed that the g_m of the JLSDGM device is decreased by approximately 58% as the L_g is scaled down from 12nm to 4nm. The smaller L_g lessens the current flow due to much higher electric field in the channel. Since the I_D is directly proportional with the L_g (Fig. 5), any decrease in V_{TH} would definitely lessen the I_D as well as the g_m. Fig. 10 depicts the impact of L_g variation on g_m for JLSDGM device. Based on the plot, it can be concluded that the variation in L_g is directly proportional with the g_m, indicating that as the L_g is further scaled down from 12nm to 4nm, the g_m is constantly decreasing.

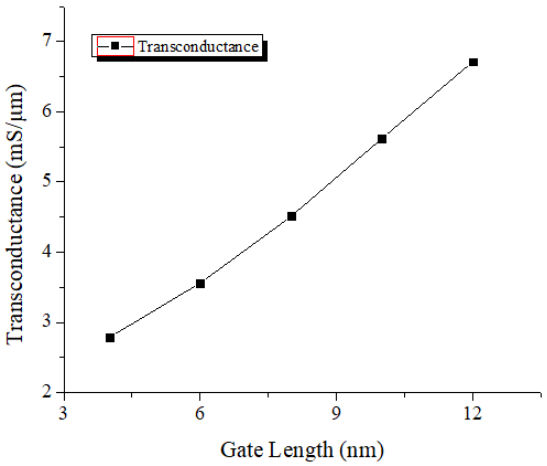

Fig. 10. Plot of transconductance versus gate length

It shows that the variation in L_g do contribute a significant impact on the g_m as the maximum transconductance, $g_m(max)$ is decreased over the reduction of L_g. The highest $g_m(max)$ of the JLSDGM device is measured at 6.71 mS/μm as the L_g is scaled at 12nm. However, the device with 4nm of L_g still exhibits an acceptable $g_m(max)$ value which is measured at 2.79 mS/μm. Even with much smaller L_g, the JLSDGM device is still able to produce a quite high the $g_m(max)$. This is mainly due to the bulk phenomenon effects where the carrier's absorption happens inside the entire part of the ultrathin body. An excellent transport efficiency of this JLSDGM device is portrayed by its high $g_m(max)$ which is suitably applicable for analog based applications. The I_{ON} and g_m (max) magnitude of the JLSDGM device with 8 nm gate length have been compared to different structures of double-gate transistor from previous studies [50, 51] as shown in Figure 11.

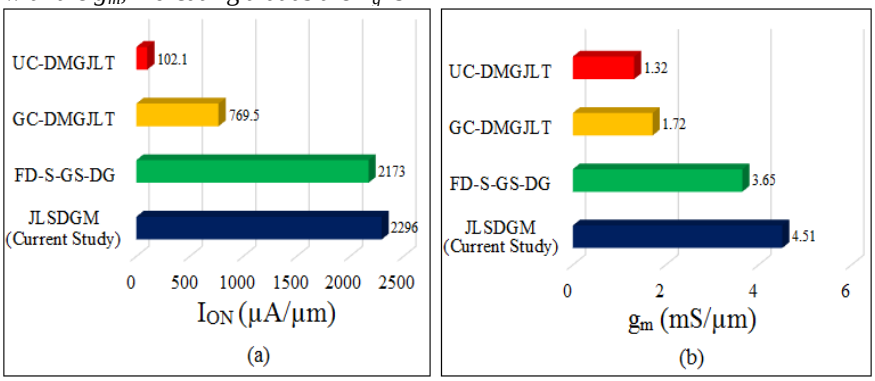

Fig. 11. Benchmark of Junctionless Strained Double Gate MOSFET (JLSDGM) with Uniform channel dual material gate junctionless transistor (UC-DMGJLT), Graded Channel Dual Material Gate Junctionless Transistor (GC-DMGJLT) and Fully Depleted Strained Gate Stack Double gate (FD-S-GS-DG) for a) On-current (I_{ON}); b) Max Transconductance ($g_m(max)$)

Based on the comparison, it is shown that the current study (JLSDGM) has demonstrated the highest I_{ON} and g_m magnitudes compared to other double-gate structure technology. Both JLSDGM (current study) and FD-S-GS-DG devices have employed the strained channel to significantly boost the I_{ON} and g_m magnitudes. Large differences in I_{ON} and $g_m(max)$ magnitudes of JLSDGM (current study) and FD-S-GS-DG devices compared to UC-DMGJLT and GC-DMGJLT clearly imply that the presence of strained channel do form a high mobility field in the channel region of the double-gate device. Despite of being operated at low power supply (V_{DD} = 0.5V), the JLSDGM device are still capable of producing a large I_{ON} and $g_m(max)$ magnitudes which makes it as one of the potential transistor's structure for low power and analog based applications.

V. RECOMMENDATIONS FOR FUTURE WORK

From the observation of the results, it could be stated that the variation in gate length (L_g) does contributes a significant impact on the JLSDGM's performance. Hence, the L_g can be regarded as one of the critical design parameters that have to be controlled for tuning the JLSDGM's performance. Remarkable device properties like high I_{ON}, low I_{OFF}, high I_{ON}/I_{OFF} ratio, low *SS* and high g_m at small scale of gate length implies that the JLSDGM device might be a potential transistor's configuration for future low power nano-scaled device. For future work, a comprehensive investigation on the impact of other design parameters besides L_g (e.g. channel doping, S/D doping, work function and etc.) towards the JLSDGM's performance can be carried out. Besides, the investigation can be further extended by considering the analog and RF performance of the JLSDGM device. Furthermore, the DC and AC characteristics of the JLSDGM should be further enhanced by optimizing multiple design parameters simultaneously through various application of optimization approaches [52-58].

VI. CONCLUSION

In summary, the design consideration and impact of gate length variation towards the drain current (I_D), on-current (I_{ON}), off-current (I_{OFF}), I_{ON}/I_{OFF} ratio, subthreshold swing (*SS*) and transconductance (g_m) have been comprehensively discussed. The investigation has been conducted via 2-D process and device simulation that includes the drift diffusion (DD) model with simplified Boltzmann carrier statistics and the Lombardi CVT model which is combined with Shockley-Read-Hall (SRH). The results show that the variation in gate length (L_g) does contribute a significant impact on the investigated JLSDGM's performance. The I_{ON} of the JLSDGM device is decreased by approximately 46% as the L_g is scaled down from 12nm to 4nm. It is also shown that the g_m of the JLSDGM device is decreased by approximately 58% as the L_g is scaled down from 12nm to 4nm. However, the JLSDGM device with 4nm of L_g still provides a remarkable I_{ON} *and* g_m*(max)* in which both of them are measured at 1680 µA/µm and 2.79 mS/µm respectively. Such remarkable device characteristics indicate that the JLSDGM device could be a potential transistor's structure for low power based applications.

ACKNOWLEDGMENT

The authors would like to thank to the Ministry of Higher Education (MOHE) of Malaysia, Mybrain15 and Centre for Telecommunication Research and Innovation (CeTRI), Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for sponsoring this research works under research grants FRGS/1/2017/TK04/FKEKK-CeTRI/F00335.

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