Doctoral Thesis

Shibaura Institute of Technology

Power Line Noise Suppression using N-path Notch
Filter in ECG Signal Acquisition

2020/September

Khilda Afifah

POWER LINE NOISE SUPPRESSION USING N-PATH NOTCH FILTER IN ECG SIGNAL ACQUISITION

Author:

Khilda AFIFAH

Supervisor:

Prof. Nicodimus RETDIAN

A thesis submitted in fulfillment of the requirements

for the award of the degree of

Doctor of Engineering

Shibaura Institute of Technology

2020/September

Declaration of Authorship

I, Khilda AFIFAH, declare that this thesis titled, "POWER LINE NOISE SUPPRESSION USING N-PATH NOTCH FILTER IN ECG SIGNAL ACQUISITION" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.

- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.

- Where I have consulted the published work of others, this is always clearly attributed.

- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.

- I have acknowledged all main sources of help.

- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed:

_____

Date:

_____

Abstract

POWER LINE NOISE SUPPRESSION USING N-PATH NOTCH FILTER IN ECG SIGNAL ACQUISITION

by Khilda AFIFAH

Bio-sensing activities such as electrocardiogram (ECG) and electroencephalography (EEG) are challenging to obtain high-quality electrical signals because biomedical signals have small amplitude and low frequency. When performing a biomedical signal acquisition, common-mode noise such as power line interference appears near the desired biomedical signal. It has made a problem when the power line interference has amplitude higher than the primary signal.

Common-mode noise reduction has been recognized as important research. The driven right leg (DRL) circuit was significant and effective to suppress common-mode noise. However, in the actual ECG measurements using DRL circuit, sometimes noise still appears at the output and mismatching in the electrode impedance makes an impact to convert common-mode noise into a differential input voltage. The body in DRL circuit is expressed as a single node and cannot be used to simulate the effect of the electrode impedance mismatch. Therefore, a new body model is needed to be able to analyze the effect of electrode impedance mismatch and other problem with common body model.

The proposed DRL circuit is an improved circuit from common DRL circuit. The first improved DRL circuit, biomedical signal is expressed by current source in parallel with electrode impedance. The simulation results of improved circuit show mismatch between right and left electrode impedance makes noise appears at the output signal. The common human body from DRL circuit represented skin-electrode impedance as a single node. The second improved circuit, the skin-electrode impedance is expressed by resistance and stray capacitance are on each electrode. The simulation results of this improved circuit show the proposed circuit achieved smaller noise when stray capacitance in the arm and right leg are the same. Combination between proposed human body model and DRL circuit achieved output of the circuit is noise

appear in the output signal. Therefore, human body model with DRL circuit still need another filter to get high quality biomedical signal (noise free signal).

The other techniques to suppress common-mode noise have been proposed by using digital and analog notch filters. The technique to suppress common-mode noise used a digital notch filter, but it requires an analog front-end with a wide dynamic range since the noise contaminated input signal need to be converted to digital signal. The techniques with analog notch filter such as conventional N-path notch filters have disadvantage because these techniques require 3GΩ switches off-resistance and 18 paths to reach notch depth target. The problem to implement previous N-path notch filter is the difficulty in implementing switch with off-resistance. On-chip implementation of the system is also a challenge in the realization of portable ECG devices because the notch filter has a large time constant in which requires large capacitance and high resistance.

Two topologies of N-path notch filter with leak buffer circuit have been proposed. The proposed N-path notch filters are Topology 1 and Topology 2. Topology 1 and Topology 2 achieved notch depth of 62.4dB and 63dB in measurement results with sampling frequency 50Hz, even if the proposed circuits use less number of path and small of switches off-resistance. Topology 1 and Topology 2 are verified using artificial ECG signal with 2Hz which is contaminated by power line interference with frequency 50Hz or 60Hz. Experiment results show that the proposed circuit significantly reduces the power line noise.

Topology 1 and Topology 2 N-path notch filters achieved notch depth higher than notch depth target, but have a problem in the size of capacitor. The total capacitance for Topology 1 and Topology 2 are 2.3 µF and 930nF, respectively. Therefore, the next proposed circuit aims to propose a new technique of N-path notch filter with switched capacitance scaling to decrease the total capacitance for a fully on-chip implementation. The proposed N-path notch filter replace the resistor in N-path core into resistor equivalent of switched-capacitor to reduce the total capacitance. Topology 1 and Topology 2 with capacitor scaling and also Topology 3 using CMOS switch with total capacitance for all topologies equal to 1nF achieved notch depth higher than 40dB.

Topology 1 and Topology 2 using CMOS switch with scaling factor 1000 achieved

notch depth of 64dB and 68dB, respectively. The total capacitance of Topology 1 and Topology 2 using CMOS switch with scaling factor 1000 are 2.34nF and 930pF, respectively. Below are advantage and disadvantage of Topology 1, Topology 2, and Topology 3 with/without capacitance scaling. Topology 1 with capacitor scaling is more effective in the total capacitance for on-chip implementation because of to achieve notch depth around 44dB. It used the smallest total capacitance than the other topologies.

Acknowledgements

Contents

List of Figures

List of Tables

List of Abbreviations

AFE   Analog Front End

BOTA   Balanced Operational Transconductance Amplifier

CM   Common-mode

CMOS   Complementary Metal Oxide Semiconductor

CMRR   Common Mode Rejection Ratio

CSI   Current Steering Integrator

CVDs   Cardiovascular Diseases

DRL   Driven Right Leg

ECG   Electrocardiogram

EEG   Electroencephalogram

FIR   Finite Impulse Response

FPGA   Field Programmable Gate Array

Gm-C   Operational Transconductance Amplifier Capacitor

IC   Integrated Circuit

IIR   Infinite Impulse Response

LC   Inductor Capacitor

LPF   Low Pass Filter

LPN   Low Pass Notch

OTA   Operational Transconductance Amplifier

OTA-C Operational Transconductance Amplifier Capacitor

S/H   Sample and Hold

SNR   Signal to Noise Ratio

WHO   World Health Organization

Physical Constants

The unit capacitance of MIM capacitor   = 1fF/μm^2

List of Symbols

Ω	Unit of resistance	ohm
F	Unit of capacitance	farad
f	Clock frequency	hertz (Hz)
f_s	Sampling frequency	hertz (Hz)
C	Capacitor	farad (F)
C_h	Capacitor in S/H circuit	farad (F)
C_L	Capacitor in leak buffer circuit	farad (F)
C_N	Capacitor in N-path core circuit	farad (F)
C_R	Capacitor in resistor equivalent switched-capacitor	farad (F)
R	Resistor	ohm (Ω)
R_{off}	Switch off-Resistance	ohm (Ω)
R_{on}	Switch on-Resistance	ohm (Ω)
v_{cm}	Common-mode voltage	volt (V)
v_p	Power line voltage	volt (V)
k	Relative permittivity	Fm^{-1}
A	Area of plate	m^2
d	Separation between the plates (distance)	meter (m)
q	Charge of capacitor	coulomb (C)

Chapter 1

INTRODUCTION

1.1   Research Background

As data from the world health organization (WHO) in 2017 as shown in Fig. 1.1, cardiovascular diseases (CVDs) are the number one cause of death globally. An estimated in 2016, 9 million people in the world died cause of CVDs. Therefore, the prevention and diagnosis of cardiovascular disease become one of the primary issues for medician today. Furthermore, measuring body information continuously is very important to monitor the condition or abnormal function in the organ. With the introduction of prevention-oriented healthcare technologies, the realization of a portable device as shown in Fig. 1.2 for electroencephalography (EEG)/ electrocardiogram (ECG) recording is essential for monitoring body physiological signals from humans without restricting their mobility. Figure 1.2 shows ECG portable device. It can use wherever patients need to monitor their heart rate and can be seen on the computer.

However, bio-sensing activities such as ECG and EEG are challenging to obtain high-quality electrical signals because biomedical signals have small amplitude and low frequency. In the primary organ such as heart signal, the wrong diagnostic can make fatal to the patient. Accordingly, the reliability of biomedical signal acquisition is needed to minimize the wrong diagnosis. Table 1.1 shown a detail of frequency and amplitude from biomedical signals.

As shown in Table 1.1, a typical ECG potential on the body is about 0.1 - 5mV and frequency 0.05 - 150Hz. The common-mode noise such as power line noise contaminates ECG signal which has an amplitude in a common environment as large as
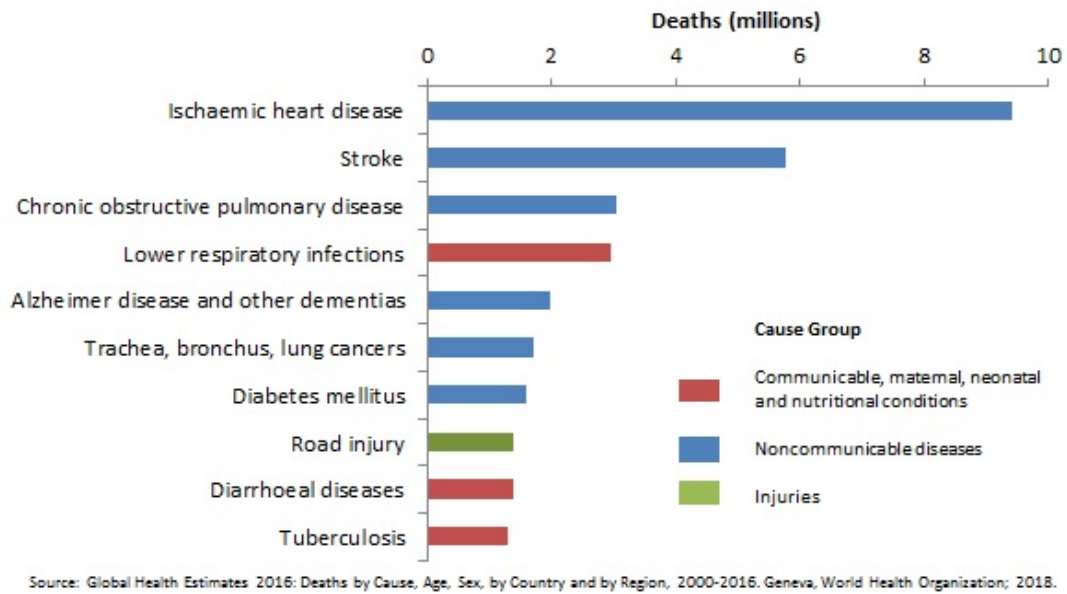
Figure 1.1: Top 10 global cause of deaths, 2016.
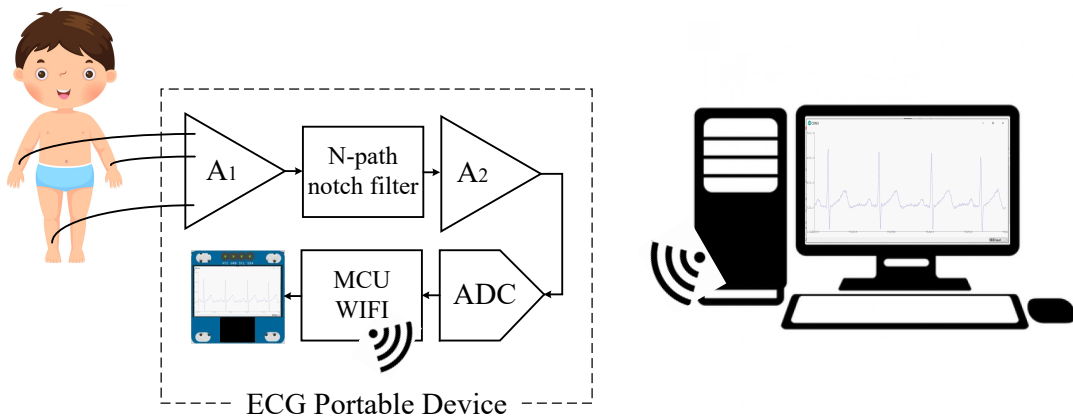
Figure 1.2: ECG portable design.

Table 1.1: Biomedical signals frequency and amplitude

	ECG [1]	**EEG** [2]
Frequency	0.05 - 150Hz	0.5 - 30Hz
Amplitude	0.1 - 5mV	20-70 μV

a few millivolts up to tens of millivolts at a frequency 50Hz or 60Hz. It is envisaged that the power line interference is a significant noise source during physiological signal recording and is ubiquitous in most clinical situations. Power line noise could be easily picked up through electrode cables, electrical devices and the patient being monitored.

Common-mode noise reduction has been recognized as important research. The

techniques to reduce common-mode noise use differential amplifiers with CMRR higher than 80dB, but it has a problem if there is different values of impedance between two electrodes. The other proposed are shielding, isolation, and driven right leg (DRL) configuration. The DRL techniques effective to reduce the influence of stray currents through the body. However, noise still appears even measurement used the DRL circuit.

As shown in Table 1.1, the other techniques to suppress common-mode noise have been proposed by using analog and digital notch filters. The signal-to-noise ratio (SNR) calculation between power line noise's amplitude and biosignal's amplitude as shown in Table 1.1, shows that the minimum notch depth for ECG and EEG are 30dB [3] and 40dB [4] respectively.

The solution using digital signal processing [5] and IIR digital notch filters [6] have been proposed. However, these techniques require an AFE with a wide dynamic range because it processes the input signal, including noise in the digital domain. The other techniques using analog notch filters such as low-pass notch filter (LPN) [2] and Gm-C notch filter [7] have been proposed to suppress power line interference. The techniques with LPN filter performed 66dB attenuation in the simulation and experiment; however, this circuit only uses in EEG signal acquisition. The solution with 6th-order Gm-C notch filter achieved a 68dB notch depth in the experiment, but the circuit needs sixth-order OTAs which consumes power. The previous techniques to suppress power line interference use N-path notch filter as described in [4] and [8]. However, the technique from [4] requires around 3GΩ switches off-resistance to reach a 40dB notch depth. Then, the technique from [8] requires 18 paths to achieved a 40dB notch depth.

1.2 Research Questions

In the biomedical signal acquisition, common-mode noise has become an interference to obtain a high-quality signal. One technique to suppress common-mode noise uses the DRL circuit. It was significant and effective to suppress common-mode noise. However, in the actual ECG measurements using DRL circuit, sometimes noise still appears at the output.

The other techniques to suppress common-mode noise have been proposed as described in section 1.1. The previous works [4] to suppress power line interference used N-path notch filter. However, the circuits assume impractical switch off-resistance (1TΩ) or need a higher number of path to obtain a sufficient notch depth.

Several research questions that would arise when designing biomedical signal acquisition system are listed below:

- Why does noise still appear even though the measurement is done using DRL circuit?

- What is the appropriate design for practical implementation of N-path notch filter to suppress common-mode noise?

1.3   Problem Statement

Driven right leg circuit has been proposed to reduce common-mode noise in the [9]. It described mismatching in the electrode impedance makes an impact to convert common-mode noise into a differential input voltage. However, the body is expressed as a single node and cannot be used to simulate the effect of the electrode impedance mismatch. As a result, the reason why power line, electrode impedance, patient skin, etc. can interference biomedical signal acquisition can be express with a new body model. Therefore, a new body model is needed to be able to analyze the effect of electrode impedance mismatch and other problem with common body model.

Another technique to suppress common-mode noise used a digital notch filter, but it requires an analog front-end with a wide dynamic range since the noise contaminated input signal need to be converted to digital signal. The methods with LPN filter performed 66dB attenuation of power line interference in the simulation and experiment; however, this circuit only can be used in EEG signal acquisition. The solution with Gm-C notch filter achieved a 68dB attenuation of power line interference in the experiment with sixth-order OTAs. Therefore, this technique requires more components and power consumption. The previous N-path notch filters [4] and [8] require 3GΩ switches off-resistance and 18 paths to reach 40dB notch depth.

The problem to implement previous N-path notch filter is the difficulty in implementing switch with off-resistance. On-chip implementation of the system is also a challenge in the realization of portable ECG devices because the notch filter has a large time constant in which requires large capacitance and high resistance.

1.4 Research Objectives

The objectives of this research are as follows:

- To propose a body model with the DRL circuit that can express the effect of skin-electrode impedance to the output signal

- To propose N-path notch filter topologies which are suitable for practical realization either using discrete components or fully on-chip implementations.

1.5 Scope of Work

The scopes of the research are listed below:

- The verification of a new body model to be used in the analysis of the impact of electrode impedance mismatching and patient skin impedance.

- The design and verification of N-path notch filter to suppress common-mode noise in ECG signal acquisition with a suppression level of at least 40dB.

- The design of a fully on-chip N-path notch filter for common-mode noise suppression in ECG signal acquisition.

1.6 Significance of the Research

As described in the previous section, cardiovascular diseases are the number one cause of death globally. Therefore, the prevention and diagnosis of cardiovascular disease become one of the primary issues for medician today. Furthermore, measuring body information continuously is very important to monitor the condition or abnormal function in the organ. Common-mode noise makes interference causes noise appear in the output signal and reduce the signal quality. Furthermore, the

complexity of biological tissue, which makes modeling of skin-electrode impedance very hard increases the difficulties in the analysis of problems in the biomedical measurement systems. Therefore, this research aims to the realization of a portable device with N-path Notch filter to suppress power line interference for electroencephalography (EEG)/ electrocardiogram (ECG) recording. It is essential for monitoring body physiological signals from humans without restricting their mobility. For the researcher, the new ECG body model can be used to find and analyze why is biomedical signal acquisition achieved poor signals and how to fix it.

1.7   Thesis Organization

This thesis is organized into six chapters. Chapter two presents a collection of literature from previous research works to suppress power line interference in biomedical signal acquisition.

Chapter three discusses the proposed body model of biomedical signal acquisition to improve conventional body model of DRL circuit and also describes measurement skin-electrode impedance on the patient. Chapter four describes the proposed N-path notch filter with leak buffer circuit to reach notch depth at least 40dB. Chapter five focuses on the scaling capacitor in N-path notch filter circuit because the proposed N-path notch filter with leak buffer circuit has a problem with the capacitor size when on-chip implementation. Chapter six concludes this research. Additionally, several ideas for future works are also proposed.

Chapter 2

LITERATURE REVIEW

In the biomedical signal acquisition, common-mode (CM) noise is one of critical problems to obtain a high-quality biomedical signal. This chapter focuses on a review of previous techniques to reduce common-mode noise with driven right leg circuit, digital notch filter, and analog notch filter. The method to suppress common-mode noise, especially power line interference in digital notch filters used IIR and FIR notch filter. In the analog filters, a low-pass notch filter [2] and Gm-C notch filter [7] are use to suppress power line interference. The other notch filter that can be used to suppress power line interference is N-path notch filter, which is build base on the switched high-pass filter. The signal to noise ratio (SNR) calculation between power line noise's amplitude and biosignal's amplitude as shown in Table 1.1, the minimum notch depth for ECG and EEG are 30dB [3] and 40dB [4] respectively. A power line interference suppression level of at least 40dB is required to guarantee the biosignal's quality.

2.1 Driven Right Leg Circuit

The common-mode noise, such as power line noise, could be easily picked up through electrode cables and the patient being monitored. Here are some interferences that can contaminate the ECG signal as described in [10]-[11]:

1. A magnetic field can pass to the loops formed by electrode leads and induce interference electric and magnetic fields (EMFs).

2. An electric field induces into the electrode leads to a displacement current that flows to earth through the skin-electrode impedance. This condition creates

a skin-electrode imbalance, therefore, result of common-mode to differential-mode conversion.

3. The current induced (i_d) into the patient creates a voltage between the two recording electrodes and is referred as common-mode voltage (v_{cm}). When the common-mode rejection ratio (CMRR) of the amplifier is not high enough, it makes common-mode noise appear in the output.
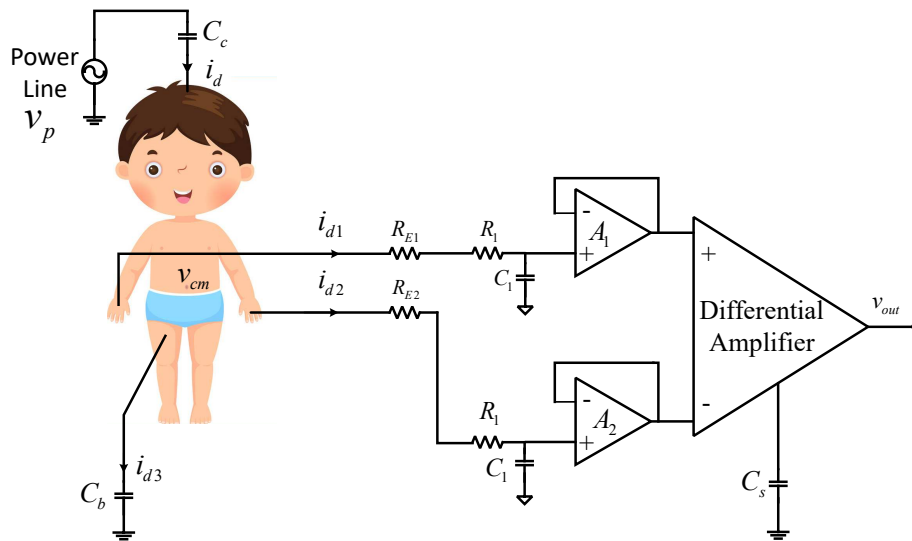
(a) ECG signal acquisition circuit with parasitic capacitors and electrode resistances.
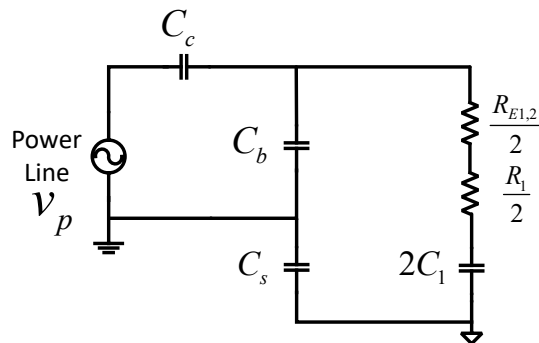
(b) Common-mode equivalent circuit of ECG signal acquisition circuit.

Figure 2.1: ECG signal acquisition circuit with parasitic capacitors and electrode resistances and its equivalent circuit of common-mode voltage.

As a point of interference in the above, Driven Right Leg circuit with parasitic capacitors and electrode resistances can be illustrated as Fig. 2.1. There is small interference current to flow through the body because of stray capacitance between the patient, power line, and earth. The stray capacitance between the power line and the patient's body C_c is taken to be 2pF, and the stray capacitance between the

body and earth C_b is taken to be 200pF [9]. If the body connects with the electrode and ECG instrumentation, there is electrode impedance between the body and ECG instrumentation $R_{E1,2}$ usually has value of 100kΩ. And also, there is the capacitance between the instrument amplifier (differential amplifier) and ground C_s is taken to be 200pF. R_1 and C_1 are low-pass filter that has a value of 1KΩ and 200pF respectively. The cut-off frequency of low-pass filter is 800KHz. A_1 and A_2 are amplifiers that are used as voltage buffers.

As shown in Fig. 2.1 (b), the common-mode voltage v_{cm} is given by

$$v_{cm} = \frac{(s^2\tau_0 + sC_3)sC_c}{((s^2\tau_0 + sC_3)sC_b) + ((s^2\tau_0 + sC_3) + s^2C_4)}v_p \tag{2.1}$$

where v_p is power line voltage, $\tau_0 = C_2R_0$, $C_2 = C_0C_S$, $R_0 = (R_1 + R_{E1,2})/2$, $C_0 = 2C_1$, $C_3 = C_s + C_0$, and $C_4 = C_1C_s$. Using the value of stray capacitance and resistance that described above, then the value of v_{cm} is 331mV with the amplitude and frequency of v_p is 141V and 50Hz, respectively. The simulation result of Fig. 2.1 shown in Fig. 2.2.
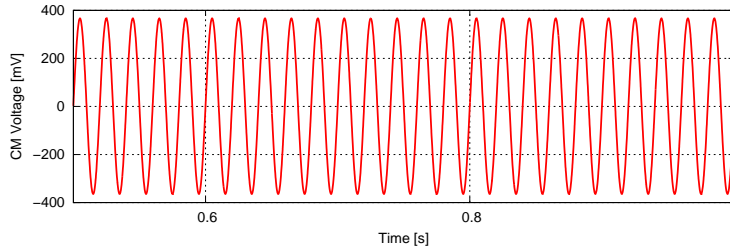
Figure 2.2: Simulation resul of common-mode voltage from Fig. 2.1.

As described in [12], there are two causes why common-mode voltage can appear at the output of ECG instrumentation. The first cause is the limited common-mode rejection ratio (CMRR) of the differential amplifier. The minimum requirement of differential amplifier CMRR in ECG signal acquisition is 80dB, hence this limit is not often problematic because in most cases the CMRR of differential amplifier is higher than 80dB. The second cause is mistmatch in electrode impedance ($R_{E1,2}$) which converts common-mode voltage into a differential input voltage. This is also known as "the potential divider effect" [9].

The techniques to reduce common-mode voltage are shielding, isolation, and

driven right leg (DRL) configuration. Shielding combined with guarding techniques is a proper technique to prevent interference currents, but most of the commercially available electrode systems do not provide standard shielded. The good isolation can be improved with isolation between the device ground and the earth. However, low capacitances are usually not easy to achieve, and isolation must be improved patient safety [12]. More effective to reduce common-mode voltage is by placing a third electrode on the patient, to provide a low-impedance path to ground for displacement current. However, the third electrode cannot be connected directly to the ground because the patient must be protected from any currents higher than $20\,\mu A$.
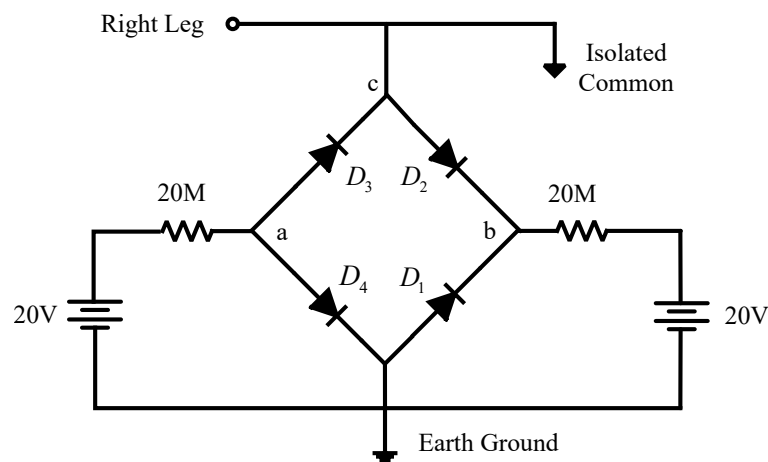
Figure 2.3: Grounding circuit to reduce common-mode voltage

The other way to reduce common-mode voltage by placing the third electrode with the circuit shown in Fig. 2.3, which makes node **c** as a virtual ground. To keep the currents under $1\,\mu A$, diodes D_1 and D_4 conduct and clamp node **a** and **b** potentials close to the ground. The impedance from node c to the ground is the forward bias resistance of diodes D_2 and D_3 plus the forward bias resistance of D_1 and D_4. The impedance to ground is typically around 150 kΩ. However, to reach currents above $1\,\mu A$, diodes D_1 and D_3 are reverse biased, and the impedance to ground increases to 20MΩ.

The most effective way to connect the third electrode to the ECG instrumentation system is to use a driven right leg (DRL) circuit where it can reduce common-mode voltage to a few tenths of a millivolt. Figure 2.4 shows ECG signal acquisition with
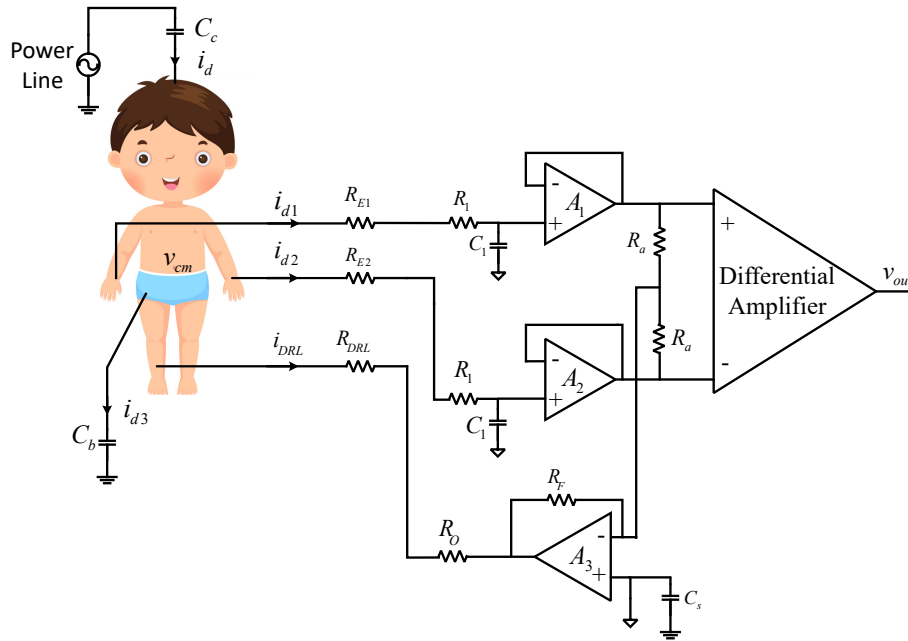
(a) Driven Right Leg circuit with parasitic capacitors and electrode resistances.
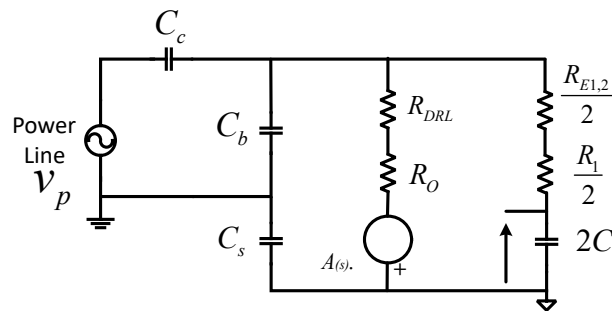
(b) Common-mode equivalent circuit of the Driven Right Leg circuit.

Figure 2.4: Driven Right Leg circuit with parasitic capacitors and electrode resistances and its equivalent circuit of common-mode voltage.

the DRL circuit. As shown in Fig. 2.4, two resistors R_a are used to extract common-mode voltage from the differential input signals. The third amplifier A_3, which is connected to the right leg, amplifies common-mode voltage and inverts it. After that, it feeds common-mode voltage back to the body via the right leg electrode. R_o and R_{DRL} are current limiting and electrode-skin impedance in the DRL circuit, respectively. As described in [13], the transfer function from power line voltage v_p

is given by

$$\frac{v_{cm}}{v_p} = K_c s \frac{\dfrac{(1 + s\tau_0)R_S}{(1 + s\tau_0)(1 + s\tau_1) + s\tau_2}}{1 + \dfrac{A(s)}{(1 + s\tau_0)(1 + s\tau_1) + s\tau_2}} \tag{2.2}$$

where $R_0 = (R_1 + R_{E1,2})/2$; $R_S = R_o + R_{DRL}$; $C_0 = 2C_1$; $\tau_0 = R_0 C_0$; $\tau_1 = R_S C_N$; $\tau_2 = R_S C_0$; and also

$$K_c = \frac{C_c C_s}{C_s + C_c + C_b}; \tag{2.3}$$

$$C_N = \frac{C_s(C_c + C_b)}{C_s + C_c + C_b}. \tag{2.4}$$
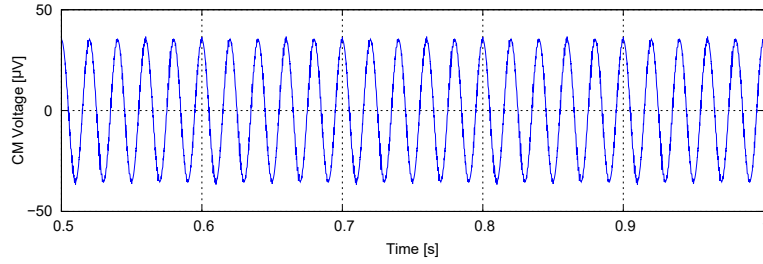
Figure 2.5: Simulation resul of common-mode voltage from Fig. 2.4.

As described before, A_3 works as an inverting amplifier such that $A(s) = -2(R_F/R_a)$. Figure 2.5 shows simulation result of common-mode voltage and the value of v_{cm} is $35\,\mu V$. Comparing Figs. 2.5 and 2.2, the DRL circuit has a significant effect on reducing common-mode voltage. This result shows that the DRL circuit can effectively reduce common-mode voltage as far as the ECG amplifier is concerned and effectively ground the patient [14]. However, the DRL circuit has the stability problem of the right leg amplifier when using high gain. Circuit stability is dependent on a number of variables such as isolation capacitance and electrode resistances.

2.2   Digital Notch Filter

The application of digital filters has been growing since the advent of computing technology achieves cost-effective. The function of filters is to suppress the unwanted frequency signal. Based on their frequency response, filters are divided into low pass, high pass, bandpass, and bandstop filters. Out of these, the bandstop filter having a very narrow bandwidth is defined as the notch filter. This notch filter can be used to reduce common-mode noise, especially power line interference. The notch response from the notch filter removes interference from 50Hz/60Hz as power line frequency even in presences of the potential divider effect. It is more effective than the DRL circuit that has the stability problem of the right leg configuration, leading to much higher power line interference attenuation while maintaining low power consumption [15].

A digital notch filter can be implemented as Infinite Impulse Response (IIR) or Finite Impulse Response (FIR) filter. IIR filters are recursive filters that can give very narrow bandwidths but might be unstable under some conditions. On the other hand, FIR filters are non-recursive filters and cannot achieve bandwidth as narrow as IIR filters, but its a better stability and linear phase. IIR filters require lower orders to obtain narrower bandwidth at the notch frequency [16].

As described in [17], a second-order efficient digital IIR notch filter is designed to suppress powerline interference. The performance of the designed filter has been investigated with a ECG signal contaminated by a 50Hz pure sinusoid signal of 1mV on field-programmable gate array (FPGA) in the LabVIEW environment. In the implemented design on FPGA, a PSD of -26dB was obtained for ECG at 50Hz and -26dB for sinusoidal signals, respectively.

FIR filters with a linear phase property are used to obtain power line noise reduction without introducing the phase distortion [18]. In this design, the notch filter is implemented with a pole/zero canceling method, the comb notch filter with a pole/zero canceling method, and the equiripple notch filter with the usage of the Parks-McClellan algorithm. The equiripple notch filter effectively to reduce power line interference but require a higher-order filter. It achieved notch depth 93.5dB

with 52th order FIR notch filter. A higher order filter uses more CPU time and consumes more power.

2.3   Analog Notch Filter

The techniques with digital notch filters such as IIR and FIR notch filters, which are described in the section 2.2, are useful when the powerline interference is smaller than the actual signal. However, the techniques with digital notch filters require an AFE with a wide dynamic range because it processes the input signal, including noise in the digital domain.
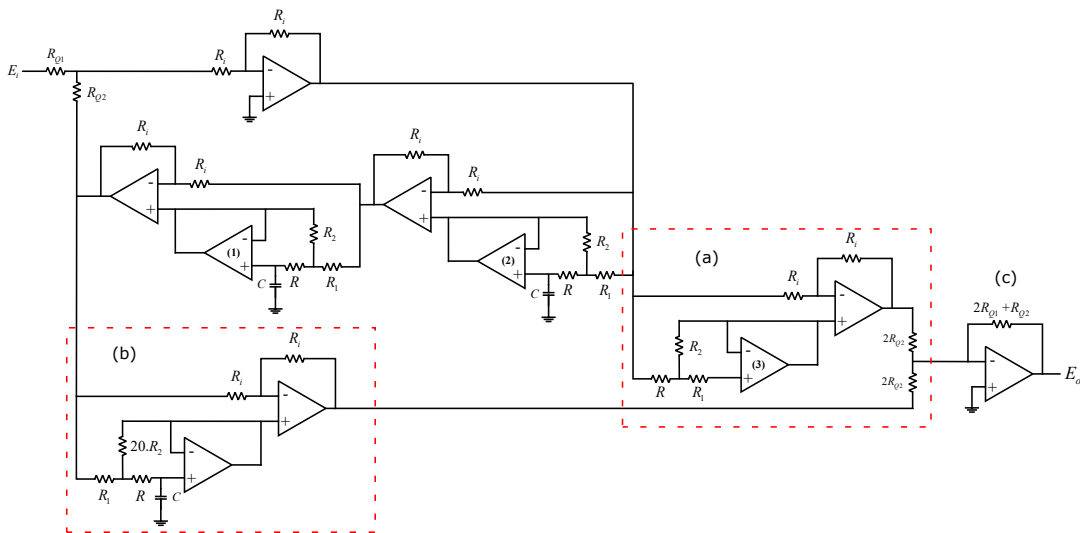
Figure 2.6: A 60Hz time contant multiplier notch filter with compensation circuit [19]

As described in [19], it design notch filter based on first-order all-pass networks uses time constant multiplication circuitry to achieve large time constants using resistors and capacitors that can be integrated into the IC. This design used a time constant multiplier (TCM) with ten opamps, as shown in Fig. 2.6. The additional TCM compensator circuit is shown in Fig. 2.6 as (a) sign, gives a second-order transfer function that has two imaginary zero. The most noticeable of these second-order effects is due to the unity gain buffer's corner frequency. Not only does the TCM circuit reduce the 3-dB point of the low-pass, but it also decreases the buffer's corner frequency by the same factor. This effect causes the attenuation compensation stage to create an extra phase shift above the notch frequency. As a result, the high-frequency gain will fall off dramatically. A phase compensator must be added to

fix gain degradation, as in Fig. 2.6 as (b) sign. By using chopper stabilized opamps with low noise and offsets, these filters can be designed to have a notch depth and dynamic range exceeding 60dB at 60Hz.
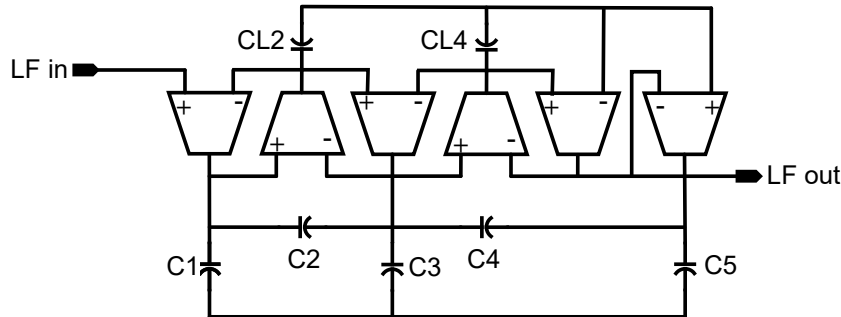
Figure 2.7: 5th-order single-ended low-pass notch filter circuit [2]
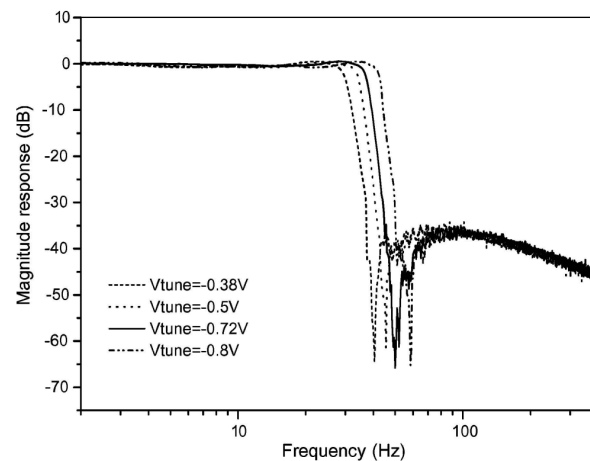
Figure 2.8: Measured frequency responses of 5th-order single-ended lowpass notch filter [2]

A CMOS continuous-time OTA-C low-pass notch filter for EEG application is described [2]. The single-ended low-pass notch filter design is based on a standard 5th-order elliptic LC-ladder prototype as shown in Fig. 2.7. All OTAs have the same transconductance and the value of capacitor range from 1 to 15pF. The elliptic filter has equal ripples in the pass-band and stop-band. The 5th-order elliptic filter has two finite zeros in the stop-band. The narrow notches appear in the frequency response of the filter at the null frequencies. To make the design less sensitive to paracitic capacitance and other parameters, the elliptic filter has been modified. The two notches of filter are design to be close enough so that the filter shows only one notch at 50Hz. The circuit achieved 66dB attenuation at frequency 50Hz as shown in Fig. 2.8. This circuit performed high notch depth in the simulation and experiment;

however, this circuit only can be used in EEG application.

A novel continuous-time notch filter based on the current steering integrator (CSI) technique was described in [20]. The second-order notch filter consisted of two integrators, one unity-gain inverter and two alpha blocks that were fully integrated onto a silicon chip. This proposed with 2nd order circuit achieved notch depth of 55.4dB at 50Hz in the simulation.
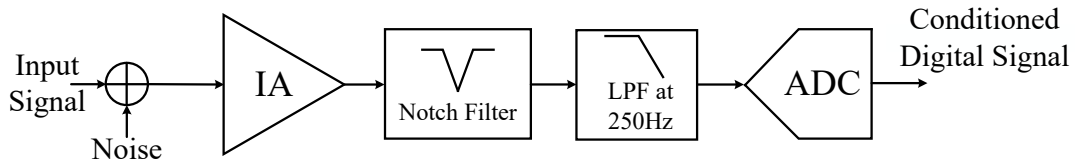
(a) A typical system of ECG signal acquisition.
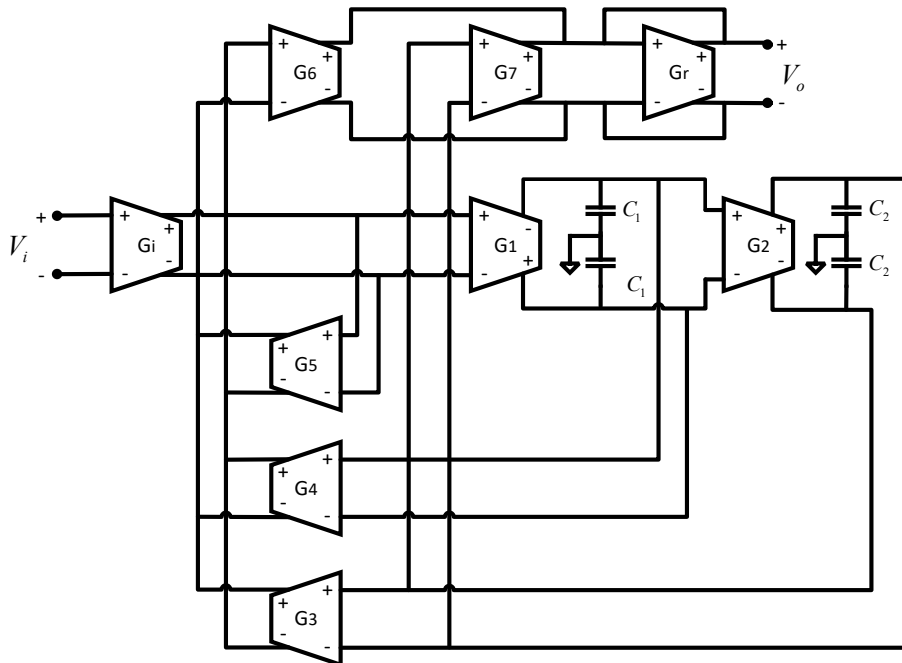
(b) Design of The fully differential notch filter with the added output circuitry of one balanced OTA (BOTA)

Figure 2.9: The fully differential notch filter with the added output circuitry of one balanced OTA (BOTA) [7].

The other work [21] uses a chopper notch filter, which is modified from a simple LC notch filter with the inductor *L* being implemented by active circuitry: transistor, resistor, and capacitor for silicon-area reduction. This circuit achieved notch depth of 41dB at 50Hz in the simulation. Another work [15] proposed a fully integrated notch filter based on Tow-Thomas Biquad with an active-RC. This design was replacing passive resistors by R-2R ladders for area-saving of approximately 120 times. It achieved a notch depth of 43dB (78dB for 4th-order).

An operational transconductance amplifier-C (OTA-C) notch filter with 6th-order cascaded filter for a portable Electrocardiogram (ECG) detection system proposed in [7]. This circuit used a design system and 6th-order notch filter circuit, as shown in Fig. 2.9. The 6th-order notch filter provides a notch depth of 65dB (43dB for 4th-order) as shown in Fig. 2.10. The adopted LPF filter must be capable of attenuating the out of band interference and suitable for ECG signal characteristics. Therefore, a 5th-order OTAC Butterworth LPF that was designed precisely to meet the ECG detection system criteria with a cut-off frequency of 250Hz is selected. However, this design requires more components and consumes more power. Table 2.1 shows a comparison of the analog notch filters.
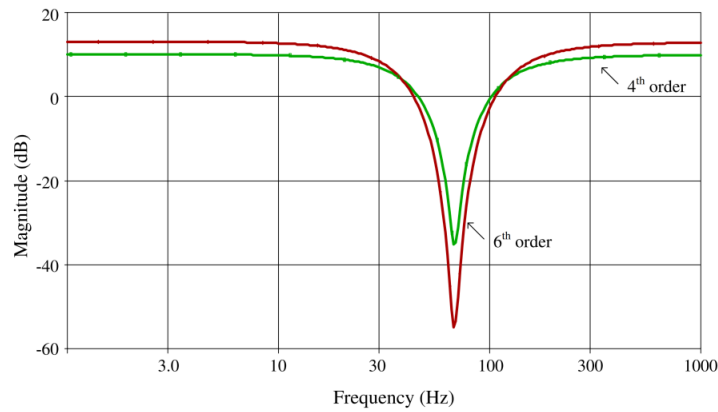
Figure 2.10: Measured result of fully differential notch filter with the added output circuitry of one balanced OTA (BOTA) [7].

Table 2.1: Comparison of analog notch filter

Ref.	[19]	[2]	[20]	[21]	[15]	[7]
Technology	2 µm	0.35 µm	0.18 µm	90nm	0.18 µm	0.25 µm
Frequency	60Hz	50Hz	50Hz	50Hz	60Hz	50-60Hz
Stucture	Chopper	OTA-C	CSI	Chopper	R-2R	OTA-C
Notch depth	60dB	66dB	55.4dB (2nd)	41dB	78dB (4th)	68dB (6th)
Result	Sim.	Exp.	Sim.	Sim.	Exp.	Sim.

2.4   N-path Notch Filter

Another technique to suppress power line interference is N-path notch filter. The conventional N-path notch filter is implemented by a switched high-pass filter (HPF) [8] as shown in Fig. 2.11 (c) which is base on HPF circuit as shown in Fig. 2.11 (a). By

switching the capacitors, each of capacitors only connects to the input in a limited
period (T/N) where T is the clock period and N is the number of path. As a result,
each of capacitors will only have a constant part of the input signal as its input when
the input signal frequency is equal to the clock frequency or its harmonics. Thus, the
signal transfer from the input to the output is reduced to create notch characteristics
on the transfer function.

(a) HPF circuit

(b) Switched HPF circuit

(c) Implementation of conventional N-path
notch filter
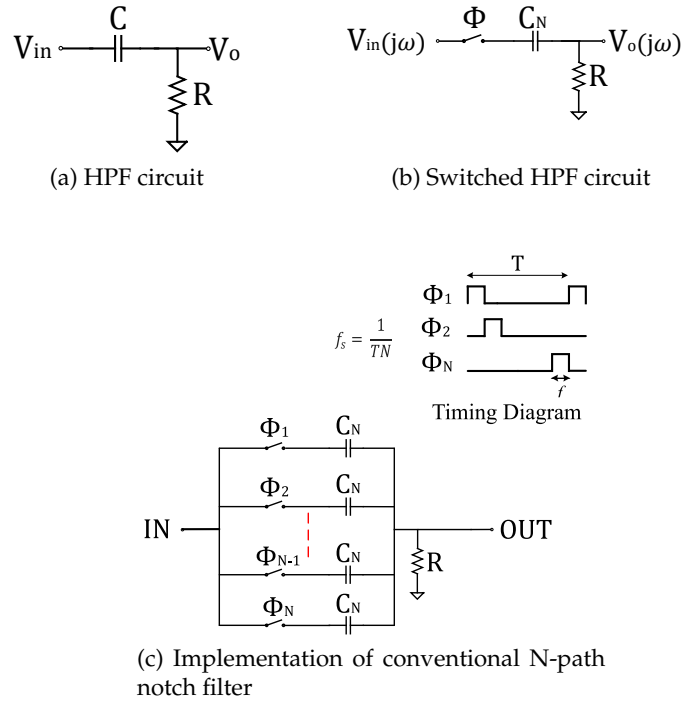
Figure 2.11: Conventional N-path notch filter.

As described in [4] the output voltage of $V_o(j\omega)$ as shown in Fig. 2.11 is given by

$$V_o(j\omega) = V_i(j\omega) - V_{Cs}(j\omega)$$

$$= V_i(j\omega) - \sum_{k=-\infty}^{\infty} H_k(j\omega)V_i(j(\omega - k\omega_s))$$

$$= (1 - H_0(j\omega))V_i(j\omega) - \sum_{k=-\infty, k\neq 0}^{\infty} H_k(j\omega)V_i(j(\omega - k\omega_s))$$

where $V_{Cs}(j\omega)$ is the voltage across capacitor C_s. For an N-path, the transfer function
for each harmonics $H_k(j\omega)$ is

$$H_k(j\omega) = \sum_{l=1}^{N} e^{(jk\omega_s \delta_l)} H_{k,l}(j\omega) \tag{2.5}$$

where $H_{k,l}(j\omega)$ is the k-th order harmonic transfer function of l-th path. In other words, $H_{k,l}(j\omega)$ is the transfer characteristic around $k \times f_s$ harmonic where $f_s = 1/T_s$ is the clock frequency of switches. In case of a single-end topology,

$$H_{k,l}(j\omega) = \frac{1 - e^{-jk\omega_s\tau_l}}{j2\pi k(1 + j\omega/\omega_{rc,l})} + \frac{1 - e^{-j(\omega-k\omega_s)(T_s-\tau_l)-jn\omega_s\tau_l}}{2\pi\omega_{rc,l}/\omega_s(1 + j\omega/\omega_{rc,l})}G(j\omega)$$

$$G(j\omega) = \frac{e^{j(\omega-k\omega_s)} - e^{-\omega_{rc,l}\tau_l}}{e^{j2\pi(\omega-k\omega_s)/\omega_{rc}} - e^{-\omega_{rc,l}\tau_l}} x \frac{1}{1 + j(\omega - k\omega_s)/\omega rc, l}$$

(2.6)

$\omega_{rc,l} = 1/(RC_l)$ and τ_l is the aperture (the period where the switch is truned on) of switch Φ_l. Finally, $H_0(j\omega)$ is given by

$$H_0(j\omega) = (1 - ND) + \frac{N}{1 + j\omega/\omega_{rc}}\left(D + \frac{1 - e^{j\omega(T_s-\tau)}}{2\pi\omega_{rc}/\omega_s}x\left(\frac{e^{j\omega\tau} - e^{\omega_{rc}\tau}}{e^{j2\pi\omega/\omega_s} - e^{-\omega_{rc}\tau}}\frac{1}{1 + j\omega/\omega_{rc}}\right)\right)$$

(2.7)

where $C_1 = ... = C_N = C/N$, $\omega_{rc} = N/(RC)$, $\tau_1 = ... = \tau_N = DT_s$ and D is the clock duty ratio. Assuming $\omega_s \gg \omega_{rc}$ and $D = 1/N$, the notch depth H_N of the N-path notch filter appoximately

$$H_N \approx 1 + \frac{N\sin^2(\pi D) + D\pi^2(1 - ND)}{N((D\pi)^2 - \sin^2(\pi D)).}$$

(2.8)

If $D = 1/N$ then

$$H_N \approx 1 + \frac{N^2\sin^2(\frac{\pi}{N})}{\pi^2 - N^2\sin^2(\frac{\pi}{N})} = \frac{1}{1 - \text{sinc}^2\left(\frac{1}{N}\right)}$$

(2.9)

where $\text{sinc}(x) = \sin(\pi x)/\pi x$. For larger N, $\text{sinc}(1/N)$ approaches 1 and H_N increases rapidly. From Eq. (2.9), the relation between the number of path N and notch depth H_N is illustrated in Fig. 2.12. As described at introduction, a minimum power line interference attenuation of 40dB is necessary. Therefore, the convention N-path notch filter requires at least $N = 18$ to achieve notch depth of 40dB.
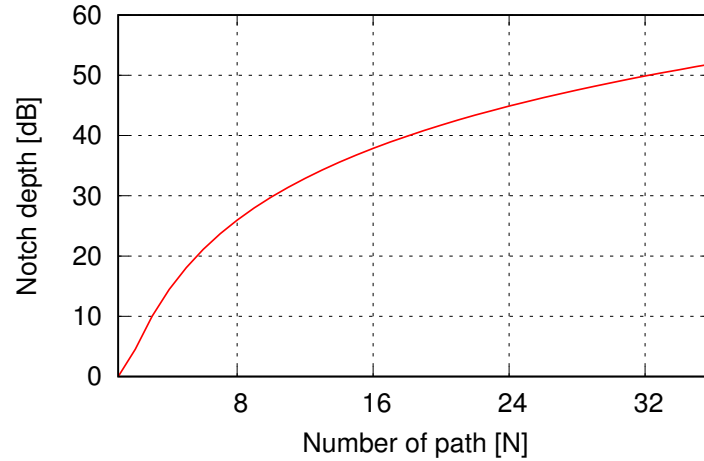
Figure 2.12: The relation between the number of path N and notch depth H_N in the conventional N-path notch filter.

2.5   Previous Work on N-path Notch filter

Figure 2.13 (a) shows a typical AFE for signal acquisition, which is less efficient in filtering power line interference because power line interference exists in the output of the filter [22]. While this approach is suitable for filtering high-frequency noise, the signal that goes to ADC still has power line interference component. It is amplified by the high gain amplifier, decreasing the number of effective bits of ADC which are consumed by the noise. Figure 2.13 (b) shows the system method, using N-path notch filter, which ensures the hum noise reduction from the signal before A/D conversion. The pre-amplifier (A_1) is introduced to make sure the signal reaches an appropriate voltage level, while also amplified the hum noise which will be removed in the next stage. The post-amplifier (A_2) amplifies the signal which has the hum noise suppressed by notch filter.

The notch filter is implemented using an N-path notch filter circuit, which is shown in Fig. 2.14 (a). The previous N-path notch filter circuit is implemented by adding a sample-and-hold (S/H) circuit before conventional N-path notch filter, as described in the section 2.4. Two S/H circuits are added at the front of the N-path notch filter to hold the input signal at the even and odd phase of the N-path core circuit sequentially. The even phase of the S/H circuit is connected to the odd paths of the N-path filter core and vice versa. As a result input signal will be held by S/H circuit before passed it into N-path core circuit. Therefore, the input signal in this circuit is a discrete-time signal.

(a) Conventional method

(b) Proposed method
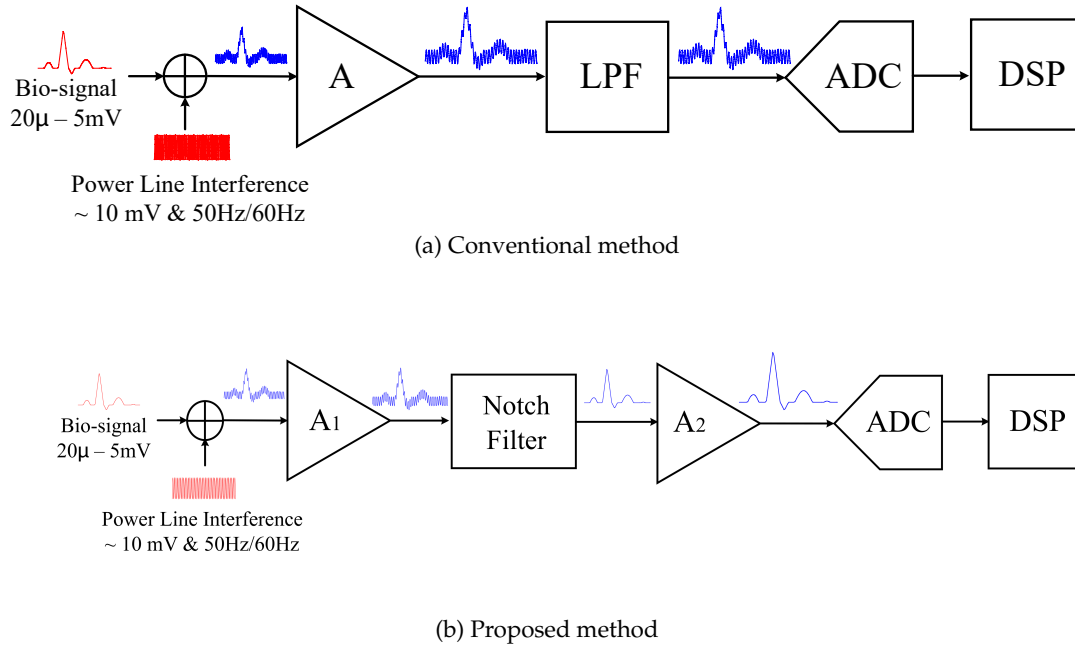
Figure 2.13: Analog front-end for biomedical signals acquisition

The even paths is defined by switching frequency ϕ_N where $N = [1, 3, ..., N-1]$ while the odd paths is defined where $N = [2, 4, ..., N]$. Figure 2.14 (b) shows an example of timing diagram with a number of paths are 10. As shown in timing diagram, frequency of the clock f_c is half of sampling frequency of each path f_s or $f_c = 1/2TN$.

Figure 2.14a shows when ϕ_o and ϕ_1 of the switch are close. The opened switches are represented by their off-resistance. The transfer function of this mechanism is given by

$$\frac{V_o}{V_{in}} = \frac{s\tau_1}{s^2\tau_1\tau_3 + s\tau_3 + s\tau_2 + 1} \tag{2.10}$$

where

$$\tau_1 = C_N R$$
$$\tau_2 = C_N R_{off} \tag{2.11}$$
$$\tau_3 = C_h R_{off}.$$

R_{off} is switches off-resistance when switch is opened.

Simulation and measurement conditions of previous N-path notch filter shows
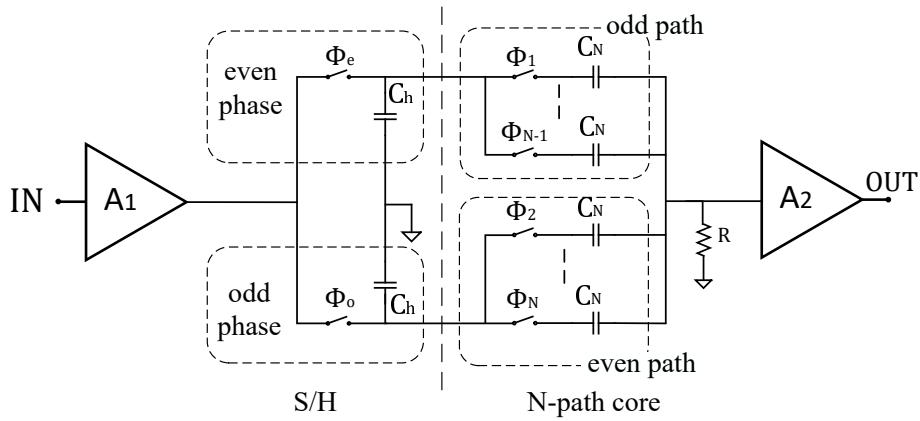
(a) Previous N-path notch filter circuit
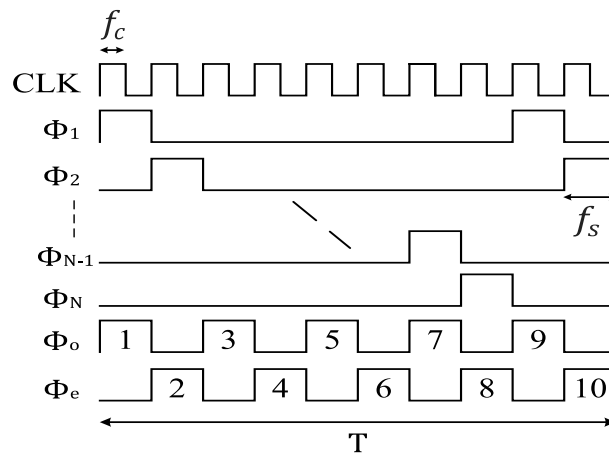
(b) Timing diagram of previous N-path Notch Filter

Figure 2.14: The conventional of 10-phase N-path notch filter [4]

Table 2.2: Simulation and measurement condition of previous N-path notch filter

Parameter	Value
N	10
BW	2Hz
C_h	1 μF
C_N	15nF
R	1MΩ
A_1	20dB
A_2	20dB
Switches	
R_{on}	35Ω
R_{off}	80MΩ

in Table 2.2. Figure 2.16 shows simulation and measurement result of previous N-path notch filter. It shows a notch depth of 21dB in the simulation and 25dB in measurement at 50Hz.

Figure 2.17 shows measurement investigation of previous N-path notch filter. In
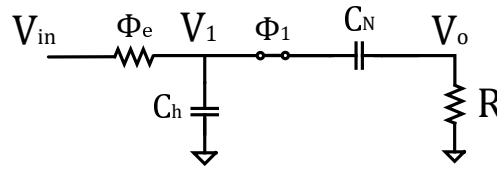
Figure 2.15: Mechanism in the first path when ϕ_o and ϕ_1 are closed
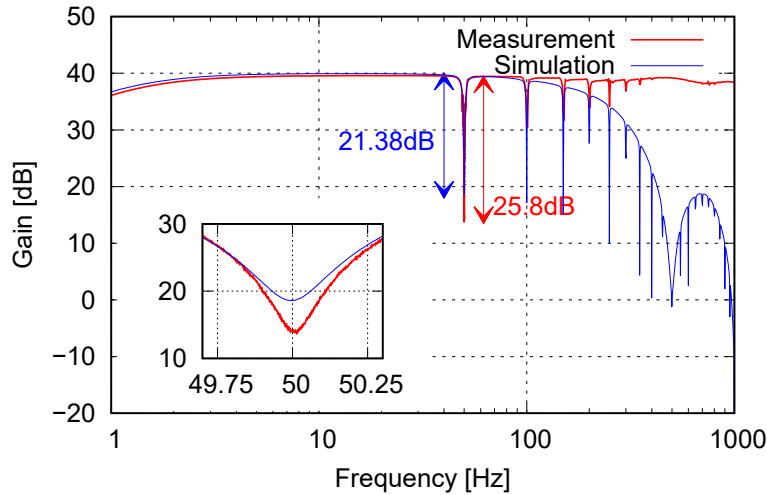
Figure 2.16: Simulation and Measurement result of previous N-path notch filter at frequency 50Hz

the measurement result, when the input signal is contaminated by power line noise with an amplitude ratio between the input signal and noise are the same as shown in Fig. 2.17 (a). The noise still appears in the output, as shown in Fig. 2.17 (b). It happened because of the value of switches off-resistance less than under 1GΩ. The filter achieved a notch depth around 20dB, as shown in Fig. 2.18. As shown in Fig. 2.18, the previous N-path notch filter needs to increase switch off-resistance at least to 3GΩ to reach notch depth of 40dB. It makes a problem if the previous N-path notch filter implemented with a discrete component because of the value of switch off-resistance is around a hundred ohms. Likewise, the conventional N-path notch filter as described in section 2.4 needs at least 18 paths to meet the target. Therefore, both circuits are less efficient in suppressing power line noise.

2.6 Conclusion

Common-mode noise is one of the critical problems in biomedical signal acquisition. The DLR circuit has a significant effect of lowering common-mode noise. However,

(a) Input signal with power line noise

(b) Output signal of previous N-path notch filter
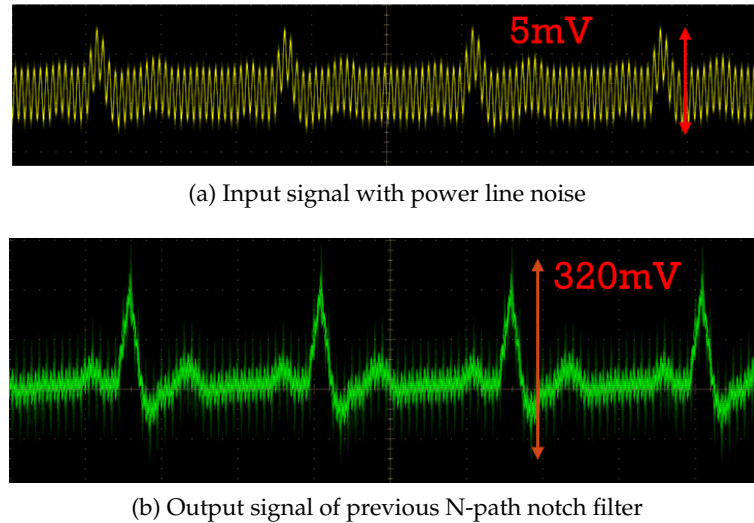
Figure 2.17: Measurement investigation of previous N-path notch filter circuit
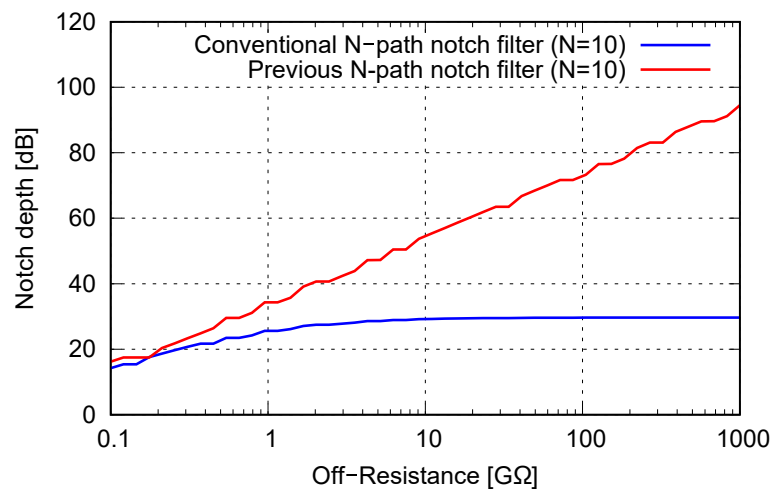
Figure 2.18: The simulation result of relation between switch off-resistance and notch depth in conventional circuit.

the DRL circuit has a stability problem when the gain in the third amplifier is too high. Notch response from the notch filter removes interference from 50Hz/60Hz even in presences of the potential divider effect caused by the mismatch between two electrodes impedance. The notch filter can be implemented either using digital or analog filters.

The techniques with digital notch filters such as IIR and FIR notch filters are useful when the powerline interference is smaller than the actual signal. The techniques with digital notch filters require an AFE with a wide dynamic range because it processes the input signal, including noise in the digital domain. The analog notch filter, such as with Gm-C and Chopper opamp, achieved higher notch depth compared

to IIR notch filter. However, it requires more components. The conventional and previous N-path notch filters depend on a high number of paths or high switches off-resistance to 40dB.

Chapter 3

INVESTIGATION ON BIOMEDICAL BODY MODEL

Most of the medicians have experience when biomedical instrumentation cannot read body signals. When it happened, they try to fix the problem by adjusting the biomedical signal monitor to replacing all the electrodes, lead wires or cables and even call biomedical engineering to fix it. All of that takes time, increases costs, adds more staff, and sometimes makes patient frustration or may place the patient at risk.

As described in chapter 1, the DRL circuit effectively reduces common-mode voltage. However, sometimes noise still appears even ECG instrumentation such as AD8232 used DRL circuit, as shown in Fig. 3.1. And also, as described in [23], a new survey shows lowering patient skin impedance can significantly reduce biomedical signal artifacts because the skin contributes to noise or artifact associated with electrode impedance. However, the common biomedical body model assumed the body as express a single node. Another problem with the common biomedical body model is when there is a difference between the two electrodes impedance in the left and right arm, the output of the body model still noise-free signal. However, the difference between the two electrodes impedance will convert the common-mode noise into the differential input voltage makes noise appear at the output.

This chapter will describe a proposed body model to find the detail of how power lines, electrode impedance, patient skin, etc. can cause interference with biomedical signals and how it affects the output of the signal. In this chapter, the biomedical signal acquisition that will be used is the ECG signal acquisition. However, the methods and calculations outlined here are not restricted to ECG signal acquisition
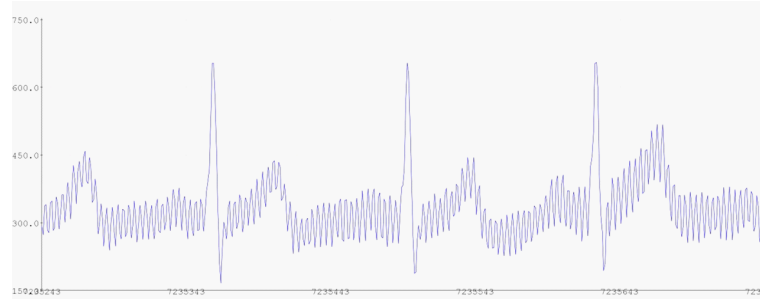
Figure 3.1: Measurement result of ECG instrumentation using DRL circuit

and could be applied to any biomedical signal acquisition system.

3.1   Improved ECG Body Model with DRL Circuit
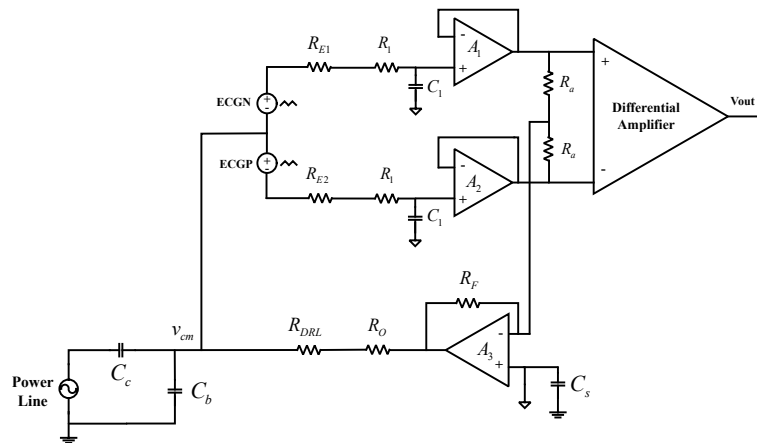
Figure 3.2: Simulation circuit of Driven Right Leg circuit with parasitic capacitors and electrode resistances as shown in Fig.2.4 (a)

Figure 3.2 shows a circuit for the simulation of ECG acquisition with the DRL circuit. As described in section 2.1, stray capacitance, electrode impedance, DRL circuit, etc. have an impact on the output signal. There are two types of ground in this biomedical signal acquisition with or without the DRL circuit. The first is the earth as the global ground of the measurement system and the second is the device ground. The device ground is connected to the earth with a capacitor of a few pF. The two voltage sources (ECGP and ECGN) are put before the left and right electrode impedance as a biomedical signal. However, this circuit cannot express why body model components have an impact on the output signal. It is because of the value of lowpass filter between R_{E1}/R_{E2}, R_1, and C_1. If the value of $R_{E1} = R_{E2} =$ 100kΩ so it achieve cut-off frequency 7.2kHz and it is higher than 50Hz. Therefore,

it makes the output of the DRL circuit is a noise-free signal. If R_{E1} = 10kΩ so that the cut-off frequency is 40kHz and it still higher than 50Hz, that makes the output of the DRL circuit is a noise-free signal. The cut-off frequency will smaller than 50Hz that makes noise appear in the output if R_{E1} = 10MΩ. However, the maximum value R_{E1}/R_{E2} = 2MΩ.

Therefore, this section introduces an improved body model to investigate from the biomedical body model how the mismatch between electrode impedance would convert common-mode noise into differential input voltage and how much gain needed in differential and feedback amplifiers. Since the output of a biomedical signal is in millivolts or microvolts range, the voltage gain value of the differential amplifier should be high. The feedback amplifier is used to keep common-mode voltage as small as possible.

Figure 3.3 (a) shows an improved circuit model including skin impedances for driven right leg circuit with parasitic capacitors and electrode resistances. In the improved DRL circuit, biomedical signal is expressed by current source in parallel with electrode impedance $R_{E1,2}$. Meanwhile, Fig. 3.3 (b) shows simulation circuit using the improved DRL circuit. Figure 3.4 shows the output of ECG signal acquisition with simulation condition that is shown in Table 3.1. There is noise in the output, but it is not visible because it is too small (around 2.4mV when output signal is 4.5V) if compared with output voltage.

Table 3.1: Simulation conditions of ECG Body Model

Parameter	Value
v_p	141V
Frequency	50Hz
C_c	2pF
R_{E1}, R_{E2}, R_{DRL}	100kΩ
R_1, R_a, R_o	10kΩ
C_1, C_b, C_s	200pF
R_F	1MΩ
Diff. Amp.	60dB
A_3	60dB
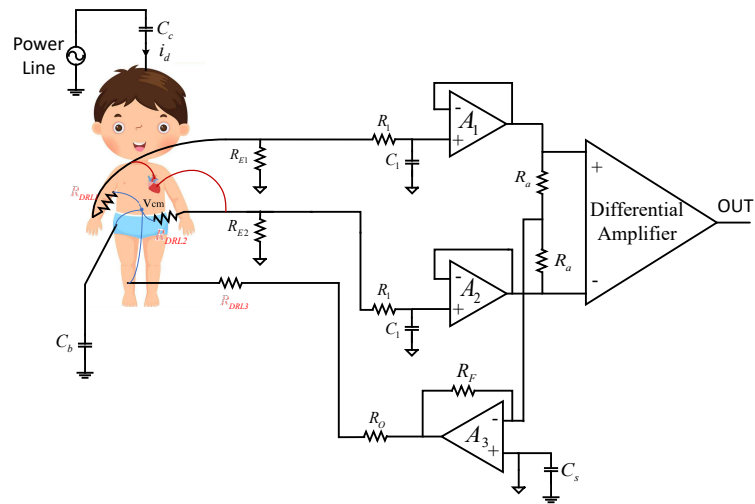
(a) Improved DRL circuit with parasitic capacitors and electrode resistances.
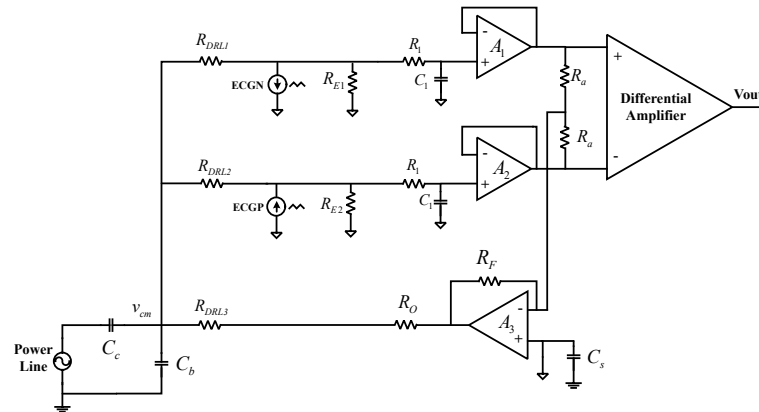
(b) Simulation circuit of improved DRL circuit with parasitic capacitors and electrode resistances.

Figure 3.3: Proposed DRL circuit with parasitic capacitors and electrode resistances and its simulation circuit.

3.1.1   Electrode Impedance

As described in Chapter 2, mismatch between electrode impedance converts common-mode voltage into differential voltage. However, simulation result with common ECG signal acquisition with DRL circuit as shown in Fig. 3.4, shows that the output is noise-free signal. A severe mismatch in the electrode impedances causes the potential to be higher at one input than the other [12]. That problem makes common-mode noise appears at the output. Figure 3.5 shows simulation result, when the value of R_{E1} = 30kΩ, R_{E2} = 100kΩ, and R_{DRL} = 100kΩ (R_{E2} match with R_{DRL}). As shown in Fig. 3.5, there is noise at the output. The amplitude of common-mode voltage at the output is 40mV. It appears because the value of impedance from two
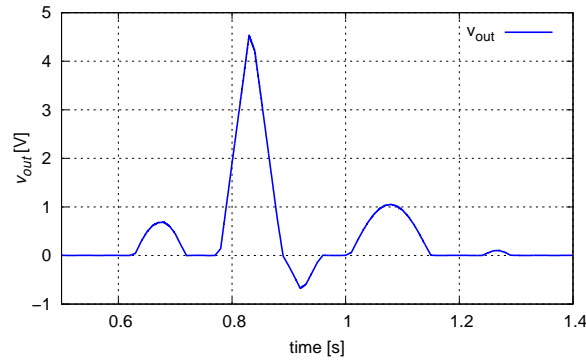
Figure 3.4: Output of ECG body model of ECG measurement using DRL circuit.

electrodes are mismatched. Even if this circuit use DRL circuit to reduce common-mode noise, the noise still appears at the output signal.

Figure 3.6 shows why the common body model cannot express the effect of electrode impedance mismatch that makes noise appear at the output, but the proposed circuit can express it. Figure 3.6 (a) shows circuit comparation with voltage and current sources are not added to each other. Figure 3.6 (b) show simulation result of voltage between nodes $A1$ and $B1$ are the same even R_{E1} and R_{E2} mismatch each other. While the voltage between the nodes $A2$ and $B2$ is not the same, it proves why the noise appears in the output signal.
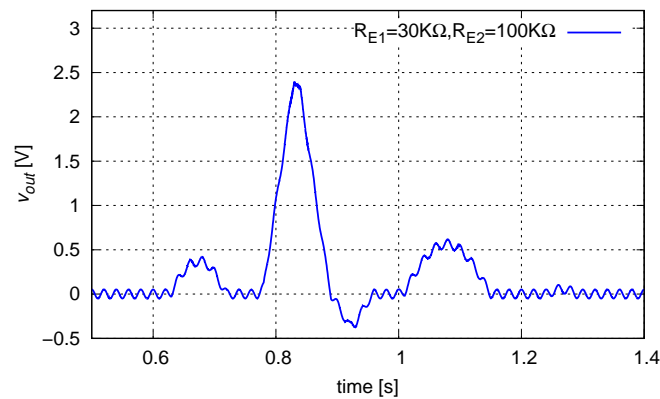
Figure 3.5: v_{out} when $R_{E1} = 30K\Omega$ and $R_{E2} = 100K\Omega$

Figure 3.7 (a) shows relation between one of electrode impedance in the arm (R_{E1} or R_{E2}) with v_{out} and noise in the output. The condition of that figure is the same as the previous simulation. The difference is this simulation sweep the value of impedance R_{E1} to see the result if mismatch between two electrodes increases. As shown in Fig. 3.7, increasing the value of mismatch (a gap between R_{E1} and R_{E2}), will increase the common-mode noise in the output. Increasing the value of R_{E1} or
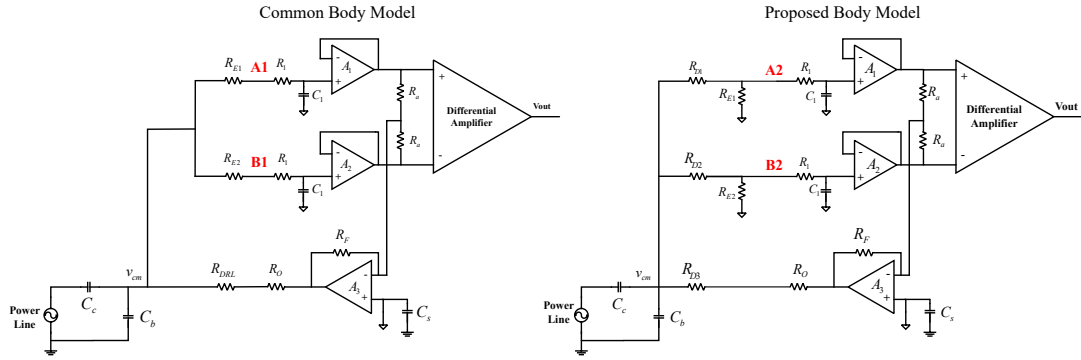
(a) Circuit design for comparation the effect of electrode impedance mismatch between common and proposed ECG signal acquisition with DRL circuit.

(b) Simulation result of comparison the effect of electrode impedance mismatch between common and proposed ECG signal acquisition with DRL circuit.

Figure 3.6: Comparation the effect of electrode impedance mismatch between common and proposed ECG signal acquisition with DRL circuit.

R_{E2} increase the output voltage magnitude. Fig. 3.7 (b) shows the percentage of noise in the output. If the maximum tolerance noise in the output is 1 percent of the desired signal, hence the maximum mismatch between two electrodes is 20KΩ (R_{E1} = 80KΩ and R_{E2} = 100KΩ).

Figure 3.8 shows relation between $R_{E1,2}$ and $v_{cm} - v_{out}$. The condition of this simulation is when $R_{E1} = R_{E2}$ and $R_{DRL} = 100$kΩ. As shown in Fig. 3.8, noise in the output still small when the value of R_{E1} and R_{E2} are the same. If the value of R_{E1} and R_{E2} increase and match each other, then output voltage would increase.

Figure 3.9 shows the effect of electrode impedance in the right leg with the value of R_{E1} and R_{E2} are the same. R_{DRL} affects common-mode noise and output voltage. Increasing the value of R_{DRL} makes increase common-mode noise and output voltage while noise in the output still small. This result can make noise appear in the output because that makes noise appear in the output is mismatch between
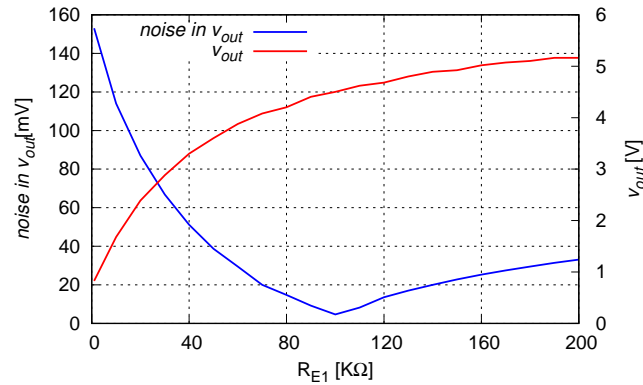
(a) Relation between R_{E1} with noise in the output and output voltage when $R_{E2} = R_{DRL} = 100\text{k}\Omega$.
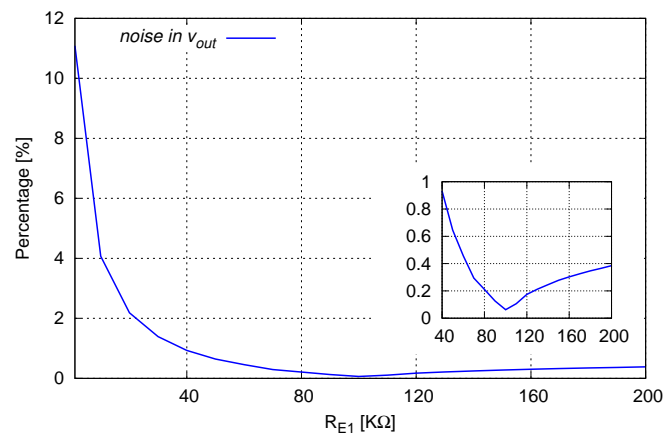
(b) Percentage noise in the output.

Figure 3.7: Effect of R_{E1} in the output when $R_{E2} = R_{DRL} = 100\text{k}\Omega$.

impedance in the left and right arm (R_{E1} and R_{E2}). However, if common-mode noise to high, it makes the system hard to suppress noise. For example, it will require a higher CMRR or number of orders in the filter design.

3.1.2 Gain of differential amplifier and feedback amplifier A_3

In the ECG signal acquisition, a differential amplifier can reduce common-mode voltage with a minimum of CMRR is 80dB [1]. And currently, the common differential amplifier has CMRR higher than 80dB. The ideal differential amplifier was used in this simulation; hence the value of CMRR is infinite. Therefore, the simulation result of noise in the output is very small (under ten millivolts) with condition $R_{E1} = R_{E2}$ and gain in differential amplifier is 60dB.

Figure 3.10 shows the effect of amplifier in the third electrode. To get small
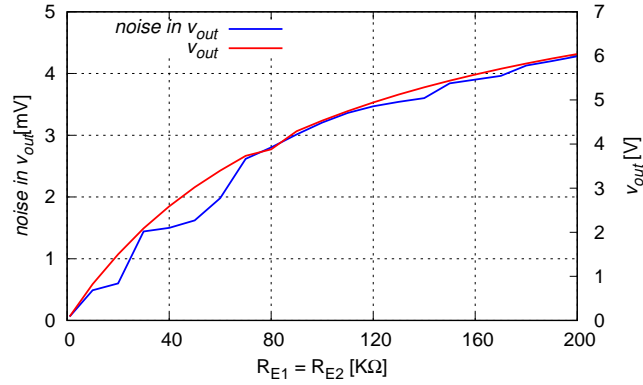
Figure 3.8: Relation between $R_{E1,2}$ and $v_{cm} - v_{out}$ when $R_{E1} = R_{E2}$ and $R_{DRL} = 100\text{k}\Omega$.
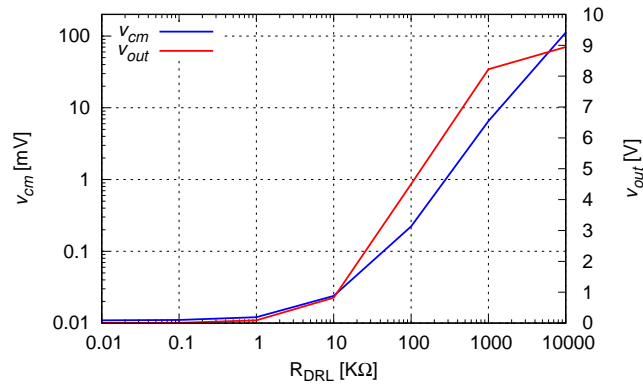
Figure 3.9: Relation between R_{DRL} and $v_{cm} - v_{out}$ when $R_{E1}=R_{E2}=100\text{K}\Omega$.

common-mode noise, minimum gain in the third amplifier is 60dB to get common-mode noise under $200\,\mu\text{V}$. As described in the previous chapter, higher value of common-mode noise makes a problem to obtain high-quality biomedical signal.

3.2 Proposed Human Body Model

One of biomedical signal artifact interference is the skin-electrode impedance that contributed by skin or electrode placement. However, the studies or practices shows the skin-electrode impedance is frequently overlooked as a significant source of artifact affecting many ECG signal acquisition [23]. The common ECG body model assumed the body as a single node as shown in Fig.3.11 (a). However, in actual, when the electrode is placed on the skin surface, the skin becomes an integral part of the circuitry. An electrode basically consists of a sensing element in contact with an electrolyte (gel). When a patient has a high skin impedance, biomedical signals can be adversely affected, causing baseline wander, artifact interference and even
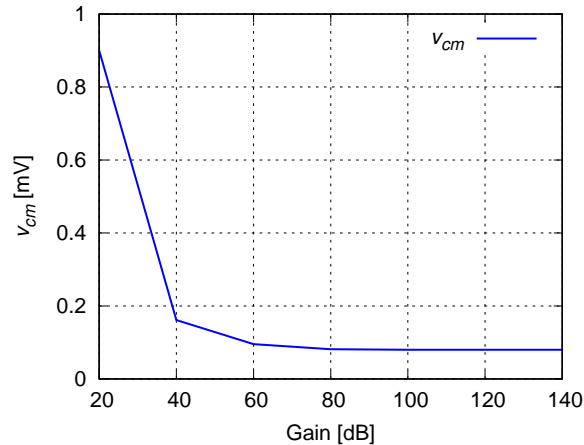
Figure 3.10: Relation between A_3 and v_{cm}

loss of the ECG trace. Other causes that make high patient skin impedance that can contribute to high patient skin impedance artifact include the environment i.e. power line interference, humidity, temperature, static electricity or the patient's skin condition such as diaphoresis.

As described in [23], the skin has two distinct layers; the epidermis (the outermost layer), and the dermis (the inner layer). Most of the epidermis is stratified squamous epithelium and lacks blood vessels. The cells deeper and closer to the dermis, however, are nourished by dermal blood vessels and can reproduce. As this happens, they push old cells toward the skin's surface. By the time they reach the surface, those cells are dead and flattened. The remaining dead cells contain keratin fibers packed with plasma membranes. This outermost layer is named the stratum corneum. It is tough, shedding millions of skin cells daily. This layer is the source of most problems with ECG trace quality.

When the ECG was measured using a simple ECG measurement board, the ECG could not be accurately measured depending on the position of the electrodes. One of the reasons is common-mode noise transmitted to both wrists are not the same. As described in subsection 3.1.1, increasing mismatch gap between right and left electrode impedance that makes increasing common-mode noise in the output. However, the common human body represented skin-electrode impedance as a single node. This section proposes a human body model to be used in ECG measurement using DRL circuit. When doing ECG measurement using the DRL circuit, common-mode noise would be transmitted to both wrist and right leg as shown in Fig. 3.11

(b). R_{ra} and R_{la} are resistances that represent transmission from the heart to the right and left hands, respectively. R_{rl} is resistances that represent transmission from the heart to the right leg. C_{c1}, C_{c2}, and C_{c3} are parasitic capacitance between the electric wire and each part of body that is connected by electrode. C_{b1}, C_{b2}, and C_{b3} are parasitic capacitance between each part of body and ground.

(a) Common human body model

(b) Proposed human body model

(c) Equivalent circuit of human body model
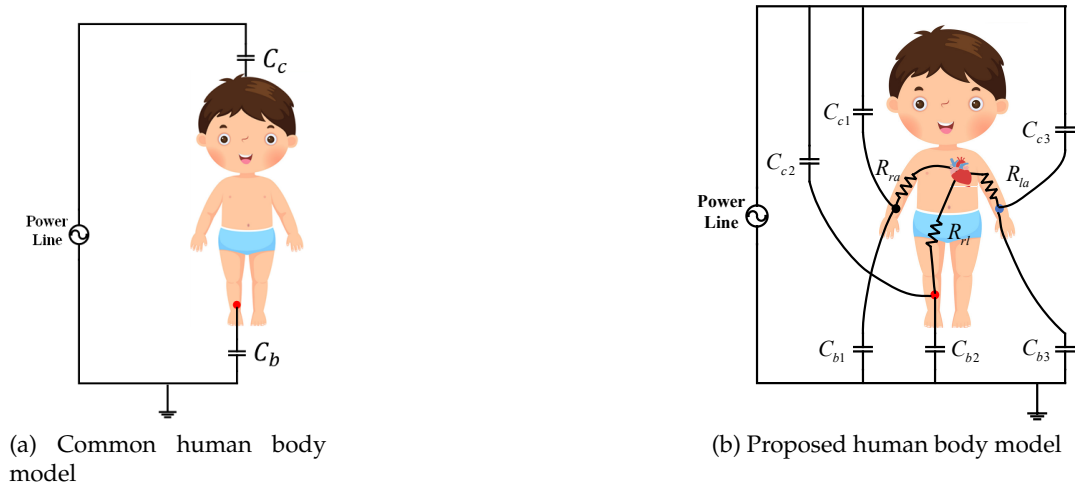
Figure 3.11: Human body model.

The value of these parasitic capacitance are inversely proportional to the distance, and vary depending on the measurement system. It may be assumed that the values of C_{c1} to C_{c3} are equal at a certain distance from the wire. Parasitic capacitance between body and ground depends on the posture; it is divided into standing/sitting and sleeping. When standing or sitting, the distance from both wrists to the ground is long, so it can be assumed that C_{b1}, $C_{b3} \ll C_{b2}$ and only consider C_{b2}. When lying down like sleeping, the distance from each part to the ground is almost the same, so $C_{b1} = C_{b2} = C_{b3} = C_{b0}$. Fig. 3.11 (b). When $C_{a1} = C_{a3}$; $C_{b1} = C_{b3}$, it is

assumed that

$$C_{arm} = C_{c1} + C_{b1} = C_{c3} + C_{b3}$$

$$C_{lg} = C_{c2} + C_{b2}$$

(3.1)

(a) Proposed circuit of human body model   (b) Equivalent circuit of human body model
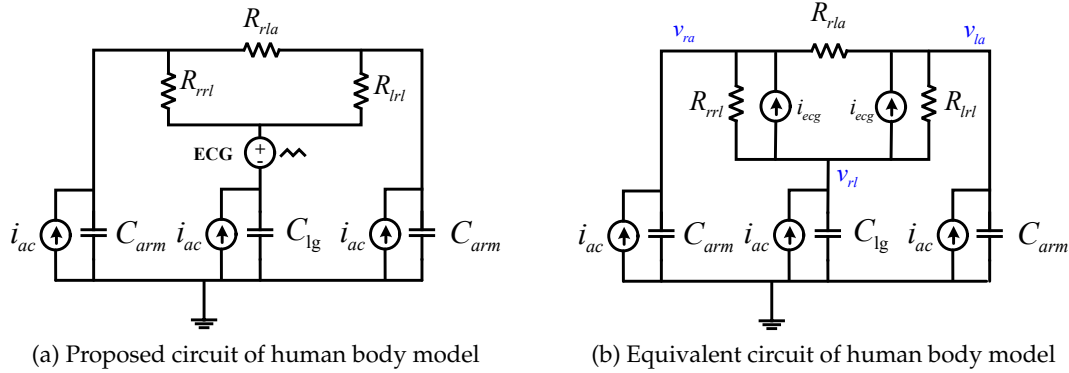
Figure 3.12: Proposed human body model.

Figure 3.12 (a) obtained when the positions of R_{la} and ECG voltage are switched, and Y-Δ conversion is applied to R_{ra}, R_{la}, and R_{la}. Finally, the circuit shown in Fig. 3.12 (b) is obtained by converting ECG voltage into current source using the equivalent conversion of power supply. As shown in Fig. 3.12 (b), R_{rla} is the resistance between two wrists, and R_{rrl} is the resistance between right wrist and right ankle. R_{lrl} is the resistance between the left wrist and right leg. The next section would describe about survey to find the value of R_{rla}, R_{rrl}, and R_{lrl} and how to get high-quality biomedical signal.

3.3 Skin-Electrode Impedance

This section will describe the result of skin-impedance survey to find the value of R_{rla}, R_{rrl}, and R_{lrl} for the proposed body model in Fig. 3.12. This survey uses AD8232 board. The AD8232 is an integrated signal conditioning block for ECG and other biopotential measurement applications. It is designed to extract, amplify, and filter small biopotential signals in the presence of noisy conditions, such as those created by motion or remote electrode placement. AD8232 use three input electrodes in right arm, left arm, and right leg. The output of AD8232 would be processed with Arduino device, and the result of biomedical signal is monitored using Arduino IDE.

The skin-electrode impedance is measured by a multimeter while monitoring the ECG waveform. The measurement setup of skin-electrode impedance measurement is show in Fig. 3.13.
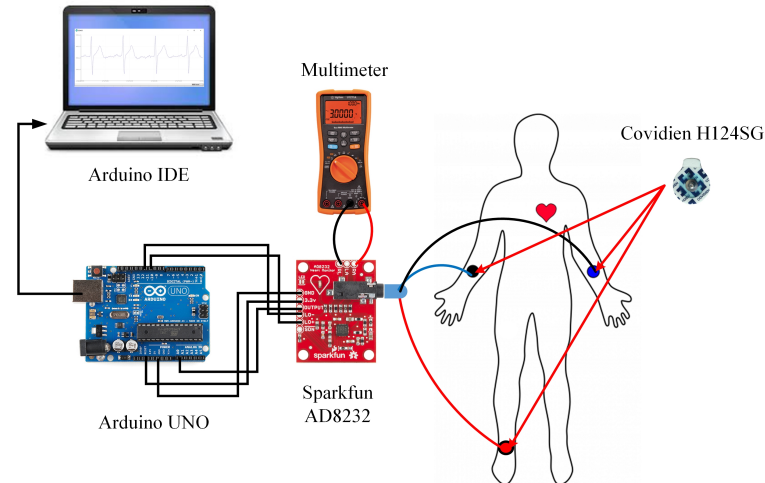
Figure 3.13: Implementation of skin-electrode measurement

Figure 3.14 and Fig. 3.15 shows classifications of the output signal from AD8232 board that has six categories. The first category is very good. In a very good category, there is no noise in the output or small noise in the output signal, as shown in Fig. 3.14 (a). The second category is good; there is higher noise in the output signal, as shown in Fig. 3.14 (b). The third is a fair category that has fair noise in the output signal, as shown in Fig. 3.14 (c). The fourth and fifth category is bad and very bad. In that category, there is very high noise in the output signal, as shown in Fig. 3.14 (d) and Fig. 3.15 (a). The last category is an unstable category that shows an unstable output signal, as shown in Fig. 3.15 (b). Even the output signals have small noise; this signal still includes unstable category when this signal unstable. In the biomedical signal acquisition, the tolerance between the output signal and noise is one percent. So that just very good, good criteria and fair can accept as a biomedical signal because it can represent ECG signal without there is not domination from noise in the output signal.

When doing ECG signal acquisition with the AD8232 device, the electrode must put on the wrists (position of radial artery) in the left and right arm to get a good ECG signal. In the input of the AD8232 device, there is three input for the left arm, right arm, and right leg. Three inputs are distinguished by the color of the cable,

(a) Very good category

(b) Good category

(c) Fair category

(d) Bad category
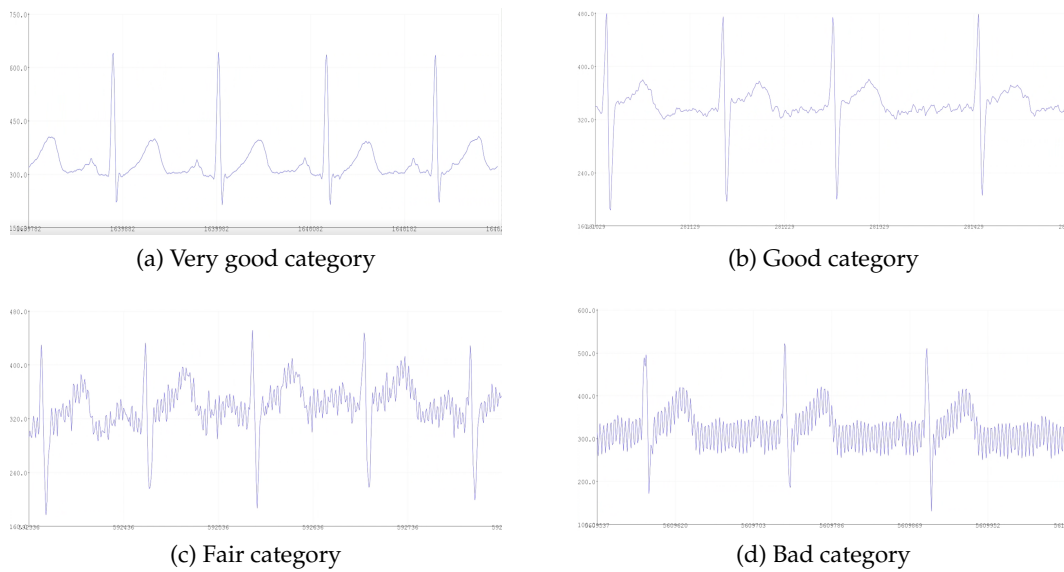
Figure 3.14: Category of output ECG signal acquisition with AD8232.

such as a black cable for the left arm, blue cable for the right arm, and red cable for the right leg. If the position of cable changes like put the blue cable in the left arm and red cable in the right arm, the output of the signal would inverse from the right signal. The inverse of the output signal can be seen in Fig. 3.15 (c).

(a) Very bad category

(b) Unstable category

(c) Inverse output
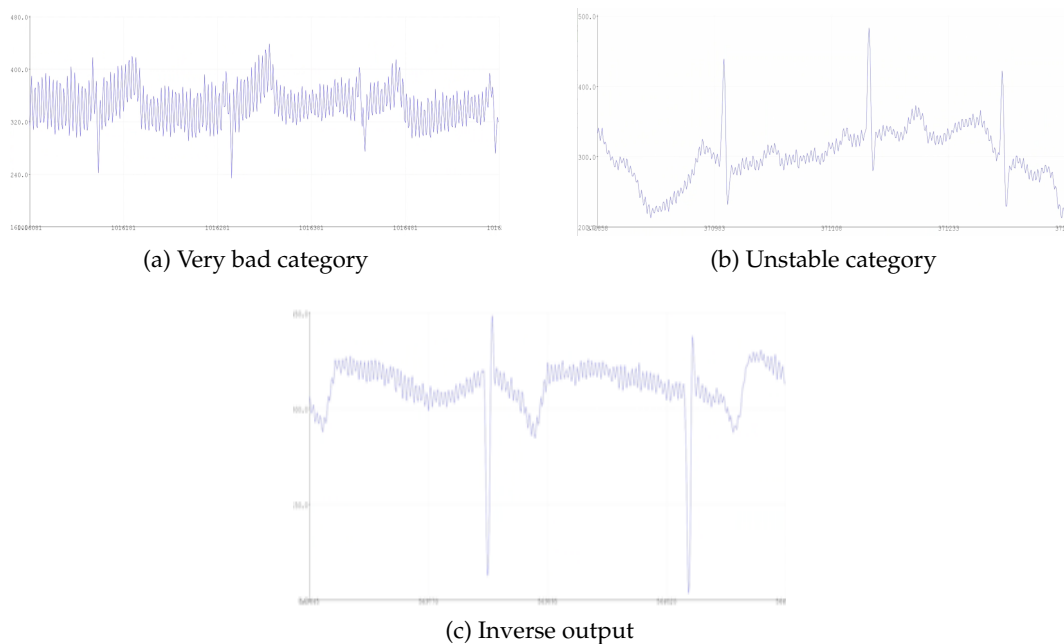
Figure 3.15: Category and output of ECG signal acquisition with AD8232.

The survey conducted to find the value of skin-electrode impedance and how to get quality biomedical signal in the real condition. This survey approved by

Shibaura Institute of Technology with 受付番号 19-007. The number of subjects of this survey is 115 people as shown in Table 3.2. The condition of the participant must health, never or have abnormal in the heart, and not pregnant.

Table 3.2: Survey Participants

Age	Target of samples	Actual of samples
12 up to 17	30	31
18 up to 25	20	24
26 up to 35	20	20
36 up to 45	10	16
46 up to 55	10	11
56 up to 80	10	13

The survey is done under the following considerations:

1. Minimize power line interference

   Minimize electronic devices when doing measurement because power line interference has a significant effect on the biomedical signals. An example to minimize power line interference does not plug-in power supply to a Laptop because the noise from power line would interference biomedical signal. The other consideration is the location of measurement. Almost of participants that measure in the laboratory gives bad criteria signal. Using a wood table is very good to get high-quality signal because it can minimize interference in the measurement device or isolation of measurement devices can do to reduce power line interference.

2. Skin preparation

   As described in the [23] and [11], skin preparation can reduce noise and make a high-quality biomedical signal. As a result of observation, rubbing with alcohol swabs can increase skin-electrode impedance. The average of impedance increase around 300kΩ. In somebody that uses body lotion, rubbing with alcohol can decrease skin-electrode impedance and decrease noise in the output. As described in another study [23] and [11], to reduce skin-electrode impedance use alcohol and abrasive paper. Observation result when the skin-electrode impedance of the participant too high (higher then 75MΩ), AD8232 device cannot detect ECG signal and the display shows a straight line.
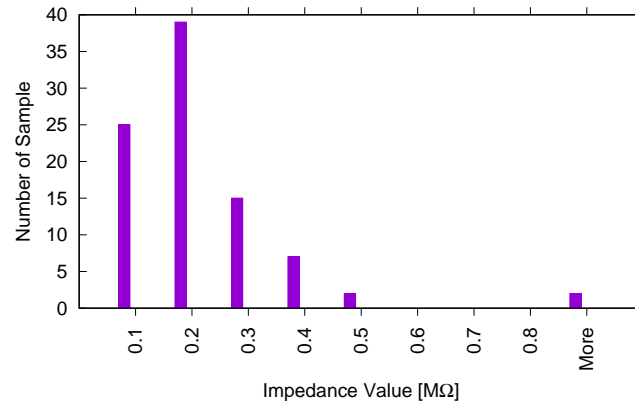
Figure 3.16: Result of skin-electrode impedance in right arm and left arm R_{rla} from ECG signal acquisition with AD8232.

The result of the skin-electrode impedance measurement can be seen in Fig. 3.16, Fig.3.17, and Fig. 3.18. In that figure, only use data that has a very good, good, and fair category to process in the calculation of average skin-electrode impedance. Figure 3.16 shows the result of skin-electrode impedance in the right arm and left arm R_{rla}. As a result, in the skin-electrode impedance in R_{rla} achieved average of impedance 189kΩ. Figure 3.17 shows the result of skin-electrode impedance in the right arm and right leg R_{rrl}. As a result, in the skin-electrode impedance in R_{rrl} achieved average of impedance 1.152MΩ.
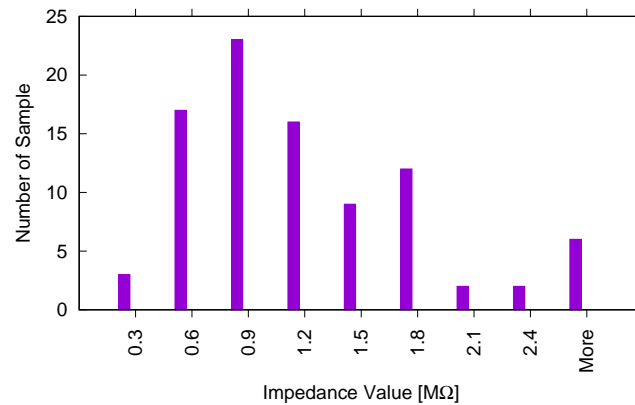
Figure 3.17: Result of skin-elecrode impedance in right arm and right leg R_{rrl} from ECG signal acquisition with AD8232.

The result of the value skin-electrode impedance in the left arm and right leg R_{lrl} can be seen in Fig. 3.18. The average calculation of R_{lrl} is 1.659MΩ. The results of skin-electrode impedance in this survey will be used to simulation in the next section.
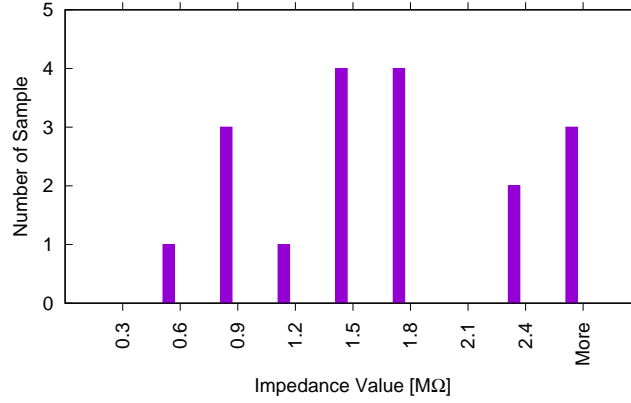
Figure 3.18: Result of skin-elecrode impedance in left arm and right leg R_{lrl} from ECG signal acquisition with AD8232.

3.4   Investigation on Human Body Model

Proposed human body model circuit as shown in Fig. 3.12 (b) is simulated using Spectre. The simulation conditions are given in Table 3.3. ECG current source in this simulation is represented by an artificial ECG signal that has frequency 2Hz.

Table 3.3: Simulation conditions of human body model

Parameter	Value
v_p	141V
Frequency	50Hz
R_{rrl}	1.152MΩ
R_{lrl}	1.659MΩ
R_{rla}	189kΩ
C_{arm}	2pF/200pF
C_{lg}	200pF

The result of skin-electrode impedance in the survey is used in this simulation, as shown in Table 3.3. The value of ECG current source is determined to achieve current in ECG signal is about 1mV, as described in Chapter 1. The value of common-mode noise is 2mV or $4mV_{pp}$ because of the value of common-mode noise a few millivolts up to ten millivolts. Converting the value of R_{rrl}, R_{lrl}, and R_{rla} into R_{ra}, R_{la}, and R_{rl} with Y-Δ conversion then R_{ra}=72kΩ, R_{la}=637kΩ, and R_{rl}=104kΩ. Figure 3.19 shows simulation result of v_{in} (v_{in} = v_{ra} - v_{la}) in proposed human body model when i_{ac} and ECG current source are added separately. It can be confirmed the desired voltage of the ECG signal and common-mode noise is appropriate.
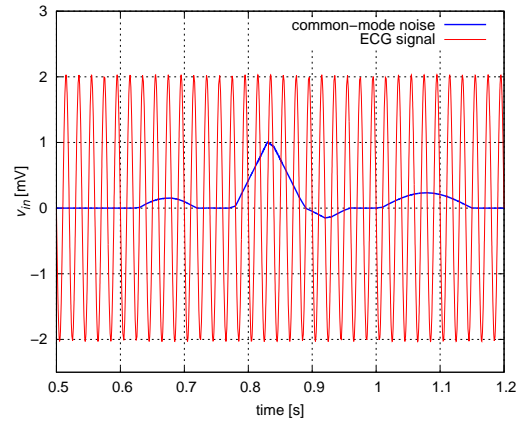
Figure 3.19: Simulation result of v_{in} when ECG current source and i_{ac} are added separately

Figure 3.19 (a) shows simulation result when ECG current source and i_{ac} are added at the same time and $C_{arm} \neq C_{lg}$. It can be confirmed that the ECG signal and common-mode noise are mixed, and the ECG signal cannot be measured correctly unless the components are caused by the common-mode noise are removed. It can be expressed when patient stand-up because the value of stray capacitance depends on the distance of wire. The solution to reducing noise, the value of C_{arm} and C_{lg} must be equal. It can be true when the patient is lying down, as shown in Fig.3.21 (b). Figure 3.19 (b) shows simulation result of v_{in} when $C_{arm} = C_{lg}$. It is considered that the value of C_{arm} and C_{lg} can be made closer by placing the patient's body parallel with the ground.
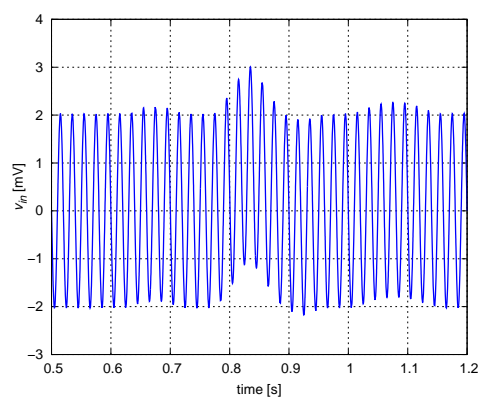
(a) Simulation result of v_{in} when ECG current source and i_{ac} are added at the same time and $C_{arm} \neq C_{lg}$
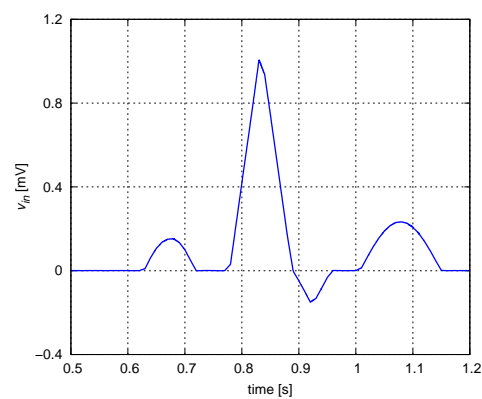
(b) Simulation result of v_{in} when ECG current source and i_{ac} are added at the same time and $C_{arm} = C_{lg}$

Figure 3.20: Simulation result of v_{in} when ECG current source and i_{ac} are added at the same time.

(a) Human body model illustration when a patient stands up as shown in Fig. 3.12 (a)

(b) Human body model illustration when a patient is lying down
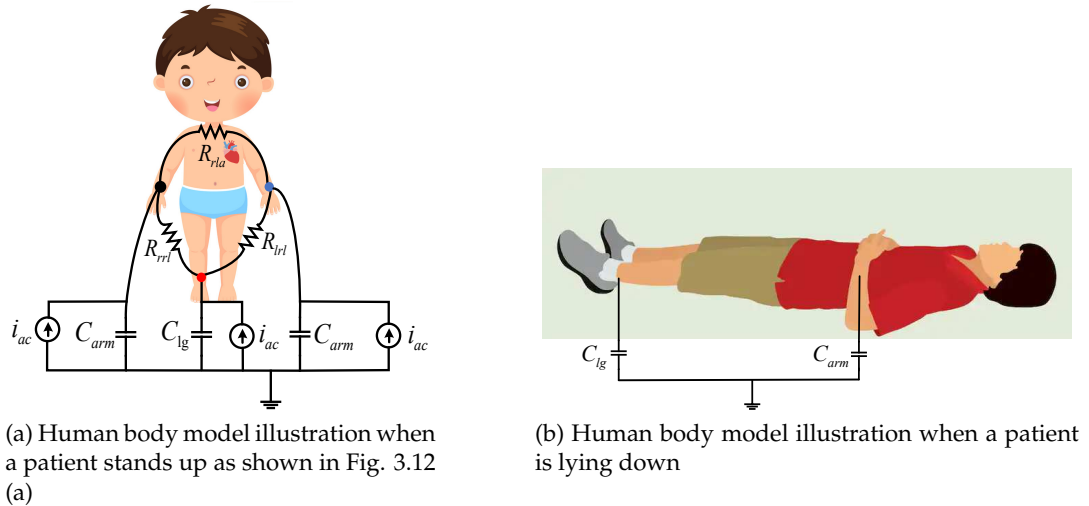
Figure 3.21: Proposed human body model.

3.5   Discussion
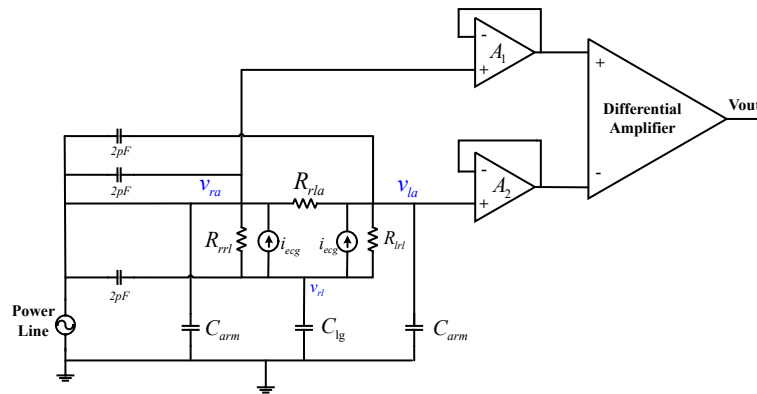
Figure 3.22: Human body model with DRL circuit

The combination circuit between human body model and DRL circuit can be seen in Fig. 3.22. The simulation conditions of this circuit can be seen in Table 3.1 and 3.3. The simulation result of Human body model with DRL circuit shows in Fig. 3.23. The simulation result of v_{in} where v_{in} equal to v_{ra} - v_{la} shows the ECG signal and common-mode noise are mixed. So that the output of ECG signal acquisition is an ECG signal mix with noise. Therefore, ECG signal acquisition with DRL circuit still requires notch filter as shown in Fig. 2.9 (a) to get a high-quality biomedical signal (noise-free signal). Moreover, this output signal looks like in the actual measurement with AD8232, as shown in Fig. 3.1. In the biomedical signal acquisition condition, the third electrode cannot be removed. It happens because of DRL circuit reduces the common-mode voltage by using a negative feedback loop, where A_3 amplifies

and reinjects common-mode voltage to the patient through the third electrode, so the skin-electrode impedance is reduced by the open-loop gain factor.
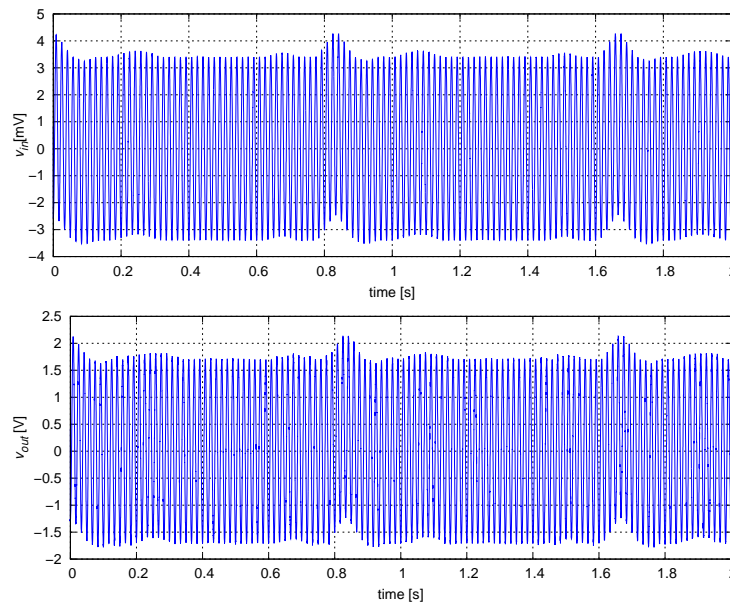
Figure 3.23: Simulation result of human body model with DRL circuit

3.6 Conclusion

This chapter proposed new ECG signal acquisition with DRL circuit and human body model. The simulation results show with improved ECG signal acquisition with DRL circuit, there is significant noise in output when the value of electrode impedance between left and right arm mismatch each other. Increasing mismatch gap between right and left electrode impedance that makes increasing common-mode noise in the output.

The effect of third electrode (right leg electrode) has impact to common-mode voltage. Increasing third electrode impedance can make increasing common-mode and output voltage. It is not good in biomedical signal acquisition if the value of common-mode noise is too high, because it makes system hard to remove noise interference. In order to get small common-mode noise, minimum gain in the third amplifier is 60dB. It can reduce the value of common-mode voltage under $200\,\mu V$.

In the common ECG body model, the resistance in the body is considered by $0\,\Omega$ and expresses as a single node. Therefore, section 3.2 improved the human body model to represent body impedance when doing ECG measurement. The survey

conducted to find the value of skin-electrode impedance and how to get quality biomedical signal in the real condition. Simulation result of combination circuit between human body model and DRL circuit shows the output of ECG signal acquisition is an ECG signal mix with noise. So that ECG signal acquisition with DRL circuit still requires another filter to get noise-free signal.

Chapter 4

PROPOSED N-PATH NOTCH FILTER

Common-mode noise, especially power line noise reduction techniques have been proposed. The techniques to reduce noise use differential amplifier, shielding, isolation, and driven right leg (DRL) circuit. The conventional techniques with differential amplifier require CMRR at least 80dB and DRL circuit to effectively reduce common-mode noise. However, the common-mode noise appears at the output of the circuit when there are different values between the right and left arm electrode impedance. As described in Chapter 3, the simulation result of combination circuit between human body model and DRL circuit shows the output of ECG signal acquisition is an ECG signal mix with noise. So that ECG signal acquisition with DRL circuit still requires notch filter to get a noise-free signal.

The other techniques to suppress common-mode noise have been proposed by using analog and digital notch filters. In this case, as described in Chapter 2, the biomedical signal acquisition must have notch depth at least 40dB to suppress power line interference. The technique with a digital notch filter requires an AFE with a wide dynamic range because it processes the input signal, including noise in the digital domain. The other techniques using analog notch filters such as Low-pass notch filter (LPN) [2] and Gm-C notch filter [7] have been proposed to suppress power line interference. The techniques with LPN filter performed notch depth more then 40dB in the simulation and experiment; however, this circuit can only be used in EEG signal acquisition. The solution with Gm-C notch filter achieved notch depth more then 40dB in the experiment, but this technique requires high order filters that

increase power consumption. The previous work of noise suppression with N-path notch filter, i.e., conventional and previous N-path notch filter require more number of paths and high switch off-resistances, respectively. This chapter will describe a new topology of N-path notch filter circuit that aims to improve notch depth to suppress power line noise interference.

4.1   N-path Notch Filter with Leak Buffer Circuit

4.1.1   Topology 1

Topology 1 N-path notch filter adds leak buffer circuit to improve notch depth. The function of leak buffer circuit is to reduce the charge leakage in the circuit. In this circuit, the leak buffer is placed between S/H circuits and N-path core circuit, as shown in Fig. 4.1. The odd path in leak buffer and even path in the N-path core are activated at the same time while even path in leak buffer and odd path in N-path core are activated at the same time. This circuit uses the same timing diagram as the previous N-path notch filter circuit as shown in Fig. 2.14 (b).
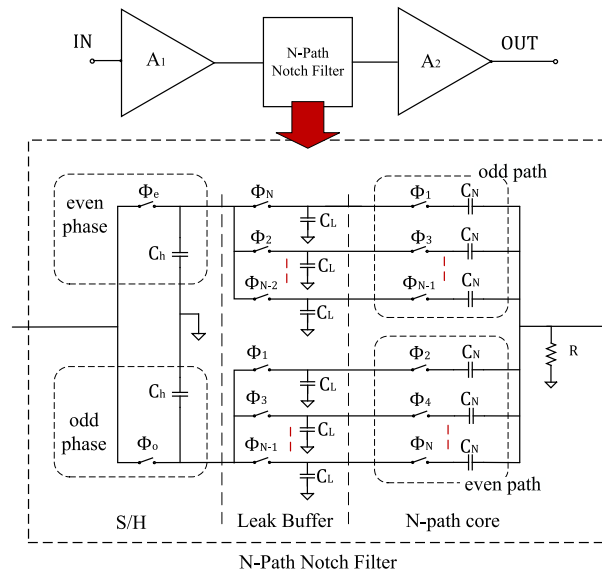
Figure 4.1: Design of Topology 1

Figure 4.2 (a) shows the mechanism of leak path in previous N-path notch filter circuit and Topology 1 when ϕ_o and ϕ_1 are closed. The open switches are represented by their off-resistance. The black arrow expresses the signal leak in the circuit and its size represents the magnitude of the leak signal. The grey arrow expresses the
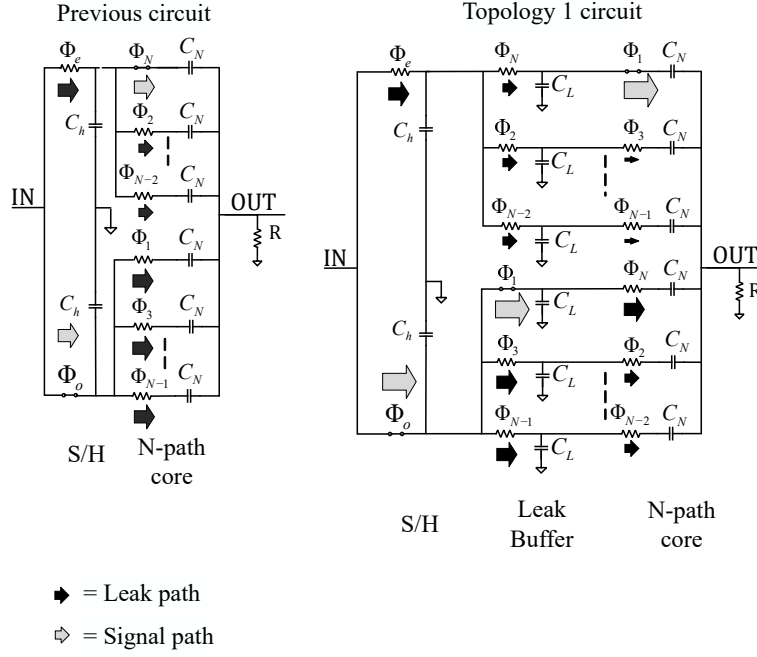
(a) Mechanism of leak path in previous N-path notch filter circuit and Topology 1 when ϕ_o and ϕ_1 are closed
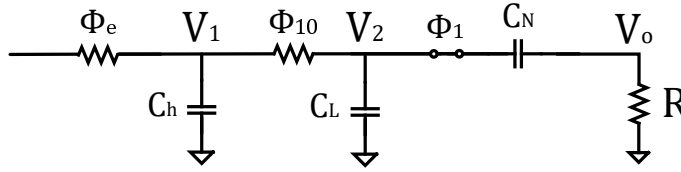
(b) Equivalent circuit of the first path of Topology 1 when ϕ_o and ϕ_1 are closed

Figure 4.2: Mechanism of leak path in previous N-path notch filter circuit and Topology 1 when ϕ_o and ϕ_1 are closed and its equivalent circuit of the first path of Topology 1

signal path. As shown in Fig. 4.2 (a), charge leakage decreases when it goes through the switch off-resistance and is expressed by a smaller black arrow. The total charge leakage in the proposed circuit is smaller when it is compared with the previous circuit. It happened because the proposed circuit adds leak buffer to decrease charge leak in the circuit design. However, this circuit has limited notch depth, even the number of path is increased. It is because of this circuit use a shared node in even and odd path of S/H circuits. As shown in Fig. 4.2 (b), the transfer function is given by

$$\frac{V_o}{V_{in}} = \frac{s\tau_1}{s^3 t1t3t4 + s^2(t1t4 + t1t3 + t2t4) + s(\tau_1 + 2\tau_2 + 2\tau_3 + \tau_4) + 1} \tag{4.1}$$

where,

$$\tau_1 = C_N R$$

$$\tau_2 = C_N R_{off}$$

$$\tau_3 = C_L R_{off}$$

$$\tau_4 = C_H R_{off}.$$

(4.2)

If Eq. (2.10) compared to Eq. (4.1), this circuit improves notch depth. The notch bandwidth *BW* of N-path notch filter is given by

$$BW = \frac{1}{\pi C_N R N}$$

(4.3)

where C_N and R are the value of capacitor and resistor in N-path core and N is the number of path.

4.1.2 Topology 2

As described in the subsection 4.1.1, Topology 1 has limited notch depth, even the number of path is increased. Topology 2 improves notch depth by adding S/H circuit in each path of N-path notch filter as shown in Fig. 4.3. This S/H circuits sample the signal at different clock phases.
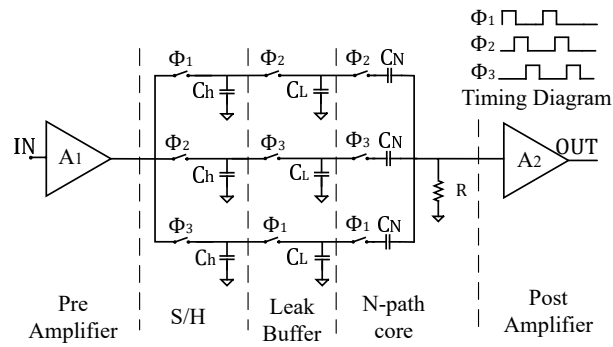
Figure 4.3: Design of Topology 2

Figure 4.4 shows Topology 2 when ϕ_1 is closed. Compared with Topology 1, Topology 2 has a smaller charge leakage because it has more off-resistance in each path that effectively decrease charge leak. Decreasing charge leakage will increase notch depth in the circuit. The number of switches and capacitors in the Topology
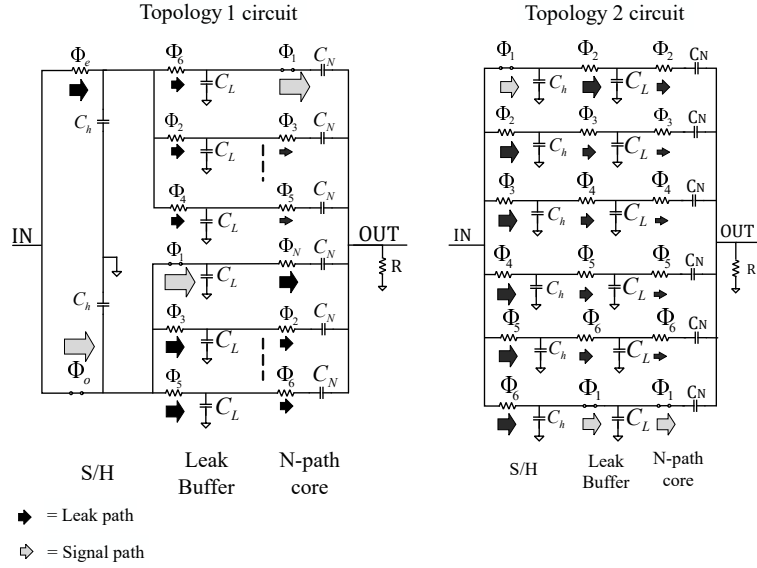
Figure 4.4: Mechanism of leak path in Topology 1 and Topology 2 when ϕ_o and ϕ_1 are closed

1 is given by $(2xN) + 2$. If the number of paths is 10, the number of switches and capacitors are both 22. On the other hand, the number of switches and capacitors in the Topology 2 is $3xN$. Thus, if the number of paths is 10, the number of switches and capacitors are both 30. Therefore, Topology 2 has a disadvantage if it is used to implement a high number of path because S/H circuit in each of its path. Topology 2 is best if used to implement an N-path notch filter with small number of path. An increasing number of paths in Topology 1 does not make increasing notch depth because of a shared node in the even and odd of S/H circuit.

4.2 Simulation and Measurement Result

Topology 1 and Topology 2 N-path notch filter are simulated using Spectre, off-resistance and on-resistance of 80MΩ and 35Ω, respectively. The measurement investigation is implemented using discrete components on a printed circuit board (PCB). The ICs used in the measurement are TI HC4066 for switches and OPA 2535UA for the amplifiers. The simulation and measurement conditions are given in Table 4.1.

As shown in Table 4.1, if a number of paths in the circuit are ten and the sampling frequency of each path f_s is set to the power line frequency (50Hz). It gives clock frequency of 500Hz for Topology 1 since the clock frequency $f = f_s N$. The Nyquist frequency f_N is half of the clock frequency, hence the value of f_N = 250Hz. The

Table 4.1: Simulation and measurement condition of N-path notch filter with leak buffer circuit

Parameter	Topology 1	Topology 2
N	10	3
BW	2Hz	1Hz
C_h	1 μF	100nF
C_N	15nF	100nF
R	1MΩ	1MΩ
C_L	15nF	10nF
A_1	20dB	20dB
A_2	20dB	20dB
Clock frequency		
50Hz	500Hz	150Hz
60Hz	600Hz	180Hz
Switches		
R_{on}	35Ω	
R_{off}	80MΩ	

clock frequency 500Hz are used to generate 10-phase clock (ϕ_1, ϕ_2, ϕ_3, ... , and ϕ_{10}) respectively to drive the switches. This scheme also applies to Topology 2 circuit. The gains A_1 and A_2 are set to 20dB in in the simulation and measurement.
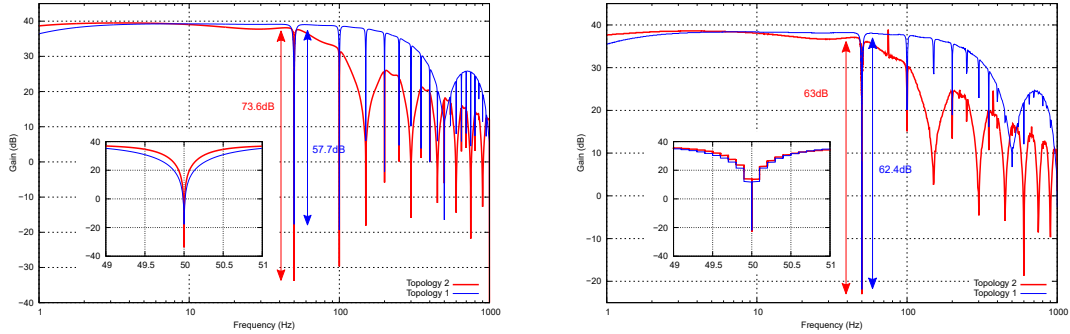
(a) Simulation result of N-path notch filter with leak buffer circuit for power line frequency of 50Hz

(b) Measurement result of N-path notch filter with leak buffer circuit for power line frequency of 50Hz

Figure 4.5: Simulation and measurement results of N-path notch filter with leak buffer circuit for power line frequency of 50Hz

As shown in Table 4.1 and Eq. (4.3), bandwidth for each of circuits is 1Hz for Topology 2 and 2Hz for Topology 1. As described in [24], the range of power line frequency in Western Japan is 59.9Hz to 60.1Hz. It makes the problem for noise suppression if notch filter design has small bandwidth. The solution to fix it is increasing bandwidth with change the value of C_N and R and keeps notch depth at 59.9Hz~60.1Hz at least 40dB. Furthermore, notch-frequency of the proposed circuit

can be easily controlled by changing the clock frequency. There is also a technique to create the clock frequency according to the power line frequency using Automatic Synchronous PLL [25].
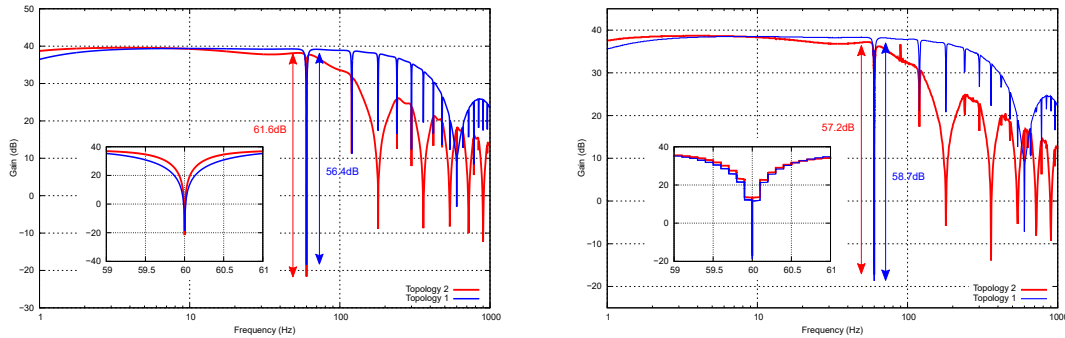
(a) Simulation result of N-path notch filter with leak buffer circuit at frequency 60Hz

(b) Measurement result of N-path notch filter with leak buffer circuit at frequency 60Hz

Figure 4.6: Simulation and measurement results of N-path notch filter with leak buffer circuit at frequency 60Hz
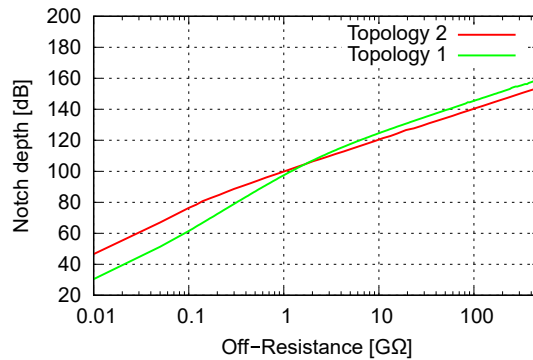
Figure 4.7: Relation between of switch off-resistance and notch depth with frequency 50Hz

The simulation and measurement result of the frequency response at 50Hz and 60Hz from the circuits are shown in Figs. 4.5 and 4.6. A deeper notch, can be done by increasing the value of switches off-resistance or the value of capacitor. The simulation result of the relation between switches off-resistance and notch depth at 50Hz is shown in Fig. 4.7. If Fig. 4.7 is compared with Fig. 4.5, measurement and simulation result in Fig. 4.5 achieved notch depth almost same with notch depth in Fig. 4.7 with off-resistance around 80M - 100MΩ.

Figure 4.8 shows simulation results from Topology 1 and Topology 2 when the circuits have same a number of paths ($N = 10$). It shows increasing N will increase notch depth. Topology 2 with $N = 10$ achieved notch depth almost twice deeper than Topology 1's notch depth, but in this case, an increasing the number of path
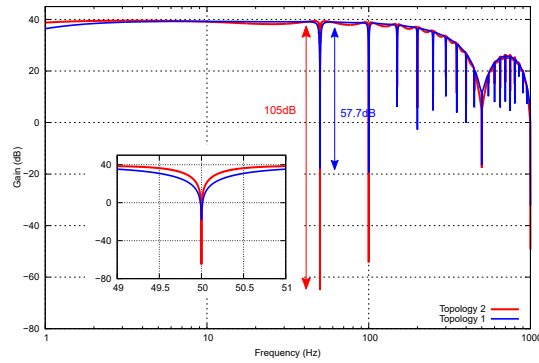
Figure 4.8: Comparison between Topology 1 and Topology 2 with N=10

in Topology 2 also increases the number of components. Therefore, considering the number of components, if the requirement of notch depth is not severe, Topology 2 is more suitable to implement an N-path notch filter with a low number of path. The notch depth can be improved by increasing the number of path.

4.3   Experiment Investigation
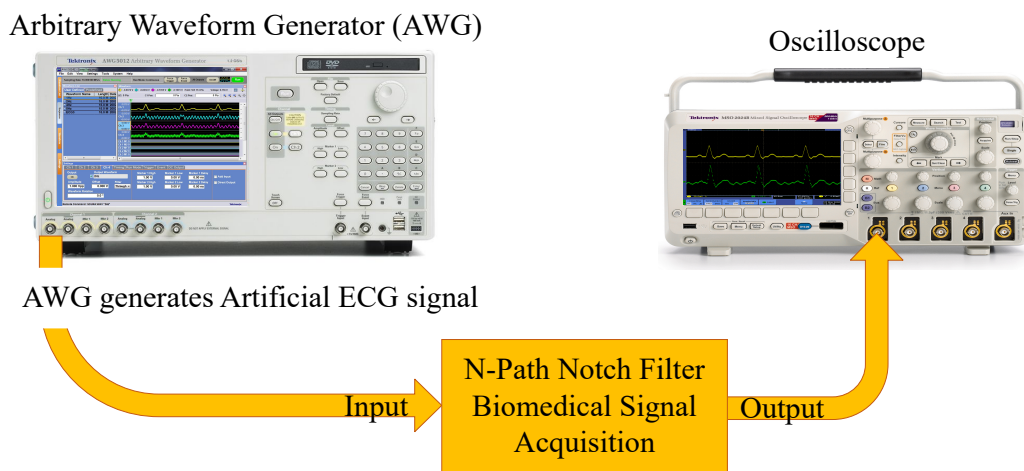
Figure 4.9: Method of experiment investigation

The performance of the proposed circuits are verified using an artificial ECG signal generated using MATLAB. The measurement setting is shown in Fig. 4.9 where the output of the filter is observed using an oscilloscope. All of the input signals are generated by an arbitrary waveform generator and has an amplitude 5mV. The frequency of the ECG signal is 2Hz; it is equivalent to a heart beat rate of 120bpm. The average heart beat rate per minute of human is ranged from 60bpm
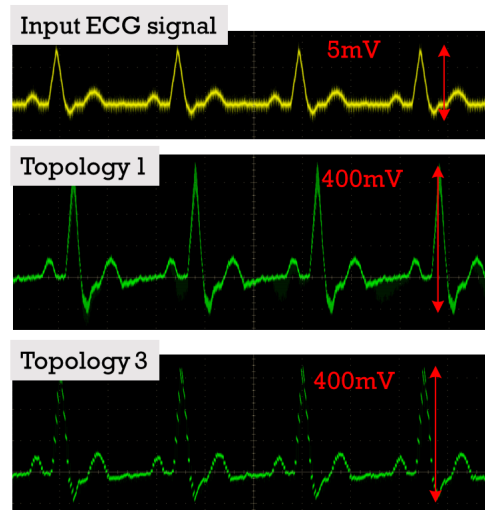
Figure 4.10: Measurement result investigation in the ECG signal acquisition without noise interference
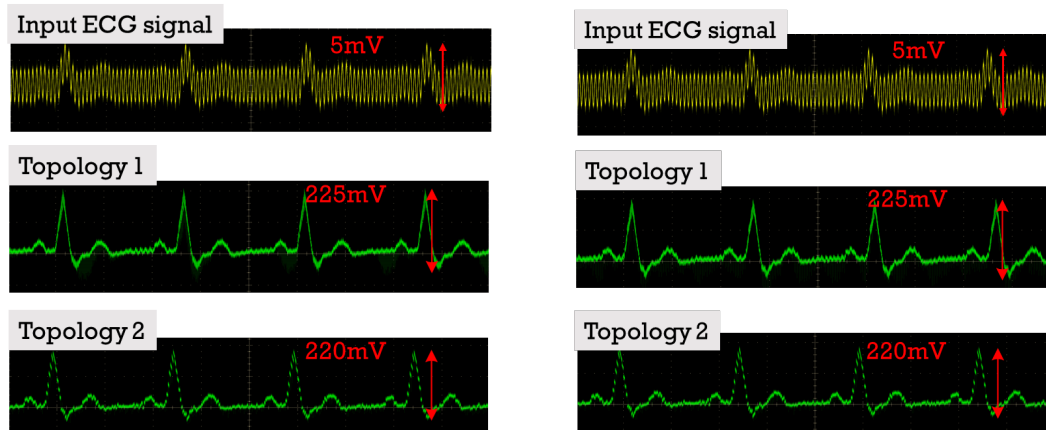
(a) Input ECG signal with 50Hz power line interference and output ECG signal acquisition with N-path notch filter

(b) Input ECG signal with 60Hz power line interference and output ECG signal acquisition with N-path notch filter

Figure 4.11: Measurement result investigation in the ECG signal acquisition with noise interference

(1Hz) up to 200bpm (3.33Hz). The power line frequency is 50Hz or 60Hz. The first investigation is when there is no noise interference in the input signal, as shown in Fig. 4.10. The second and third investigations are if there is noise interference in the input signal, as shown in Fig. 4.11a and Fig. 4.11b. The noise interference, in this case, is power line interference that has a frequency of 50Hz or 60Hz. In this case, the ratio of ECG signal amplitude and power line interference amplitude are the same. In Figs. 4.11a and 4.11b, the output of two filters are noise-free ECG signals.

4.4   Discussion

As shown at 4.10, there is an gradient between T-P interval in the output filter when the input ECG signal is a noise-free signal. Consultation with medician is used to verify whether this problem is causing mislead of the ECG signal or not. Here is a comment from Hirohito Shima, M.D., Ph.D. from Departement of Pediatrics Sendai City Hospital. *"Between the T and P waves, a U wave could be found in some patients with hypokalemia, hypercalcemia, myocardial ischemia, left ventricular volume overload and so on. The exact source of U waves remains unclear. Though the amplitude of a typical U-wave is 0.1-0.33mV, the U wave could merge with the T wave or the R wave of the next cardiac cycle. Therefore, it cannot be ruled out that the gradient increase of the baseline could potentially mislead the clinician into misidentifying the U wave."*
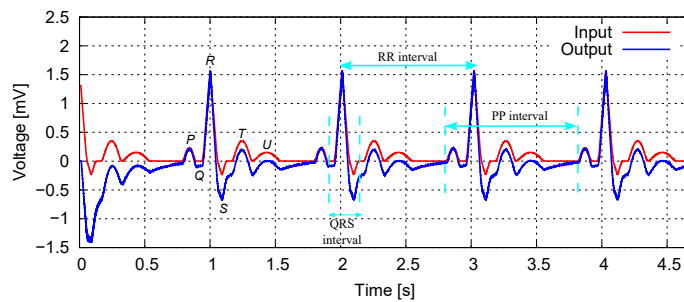
(a) Transient analysis results when there is no noise interference in input ECG signal
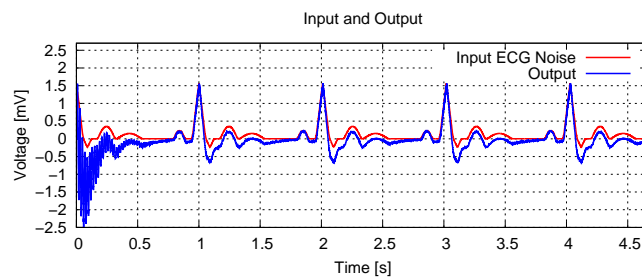
(b) Transient analysis results when there is noise interference in input ECG signal

Figure 4.12: Simulation investigation of N-path notch filter with leak buffer circuit by adding U wave

Therefore, another investigation to see the output filter is used by adding U wave in the ECG signal. Fig. 4.12 (a) shows the simulation result of input and output of N-path notch filter with leak buffer circuit when there is no noise interference in the input ECG signal. Fig. 4.12 (b) shows the simulation results of input and output of N-path notch filter with leak buffer circuit when there is noise interference in input

ECG signal. The gradient in the output of the filter is still found. This happened probably because of each capacitor stores the voltage of one cycle before. If the output of the filter looks like gradient, it happens because of charge and discharges due to the RC time constant so that the output of the filter is not a straight line like as input signal, but it becomes a curve of $1 - e^{-t/CR}$.

As shown in Fig. 4.12, there is almost no delay between input and output of filter, so that it is considered possible to make a diagnosis (e.g. arrhythmia) using time information such as P-P interval, R-R interval, and QRS interval. This filter cannot be used for amplitude diagnosis because there is a difference in the amplitude and baseline between input and output signals.

4.5 Conclusion

Two topologies of N-path notch filter with leak buffer circuit have been proposed. The proposed N-path notch filter achieves notch depth in measurement results higher than 40dB with sampling frequency 50Hz, even if the proposed circuits use less number of path and small of switches off-resistance. Topology 1 and Topology 2 are verified using artificial ECG signal with 2Hz which is contaminated by power line interference with frequency 50Hz or 60Hz. Experiment results show that the proposed circuit significantly reduces the power line noise.

Table 4.2: Comparison of other reports
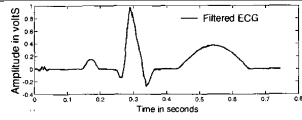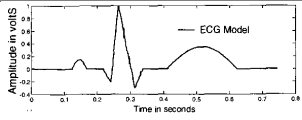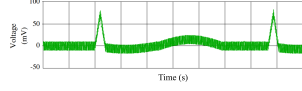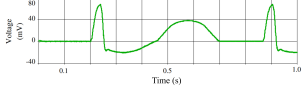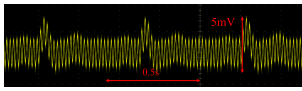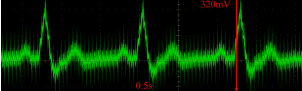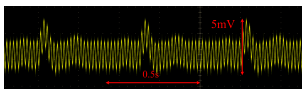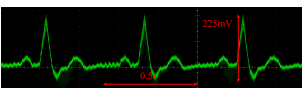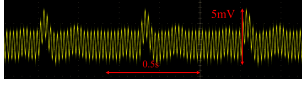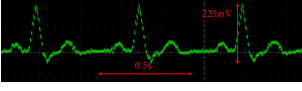
	[18]	[7]		[4]	This work			
					Topology 1		Topology 2	
Frequency	50Hz	50/60Hz		50Hz	50/60Hz			
Filter order/N	52nd	4th	6th		10		3	
Result	Sim.	Sim.		Exp.	Sim.	Exp.	Sim.	Exp.
Notch depth	93.5dB	43dB	65dB	25.8dB	57.7dB	62.4dB	73dB	63dB

N is number of path
Sim. is simulation result
Exp. is experiment result

Table 4.2 summarizes the result of this work and compare it with the other works. The work from [18] used FIR Notch filter to suppress the power line interference

which achieved notch depth of 93.5dB with a filter order of 52. Moreover, [7] used Gm-C filter to suppress power line interference and achieved notch depth of 43dB with a filter order of 4, 65dB with a filter order of 6. The result from our previous work [4] achieved notch depth of 25.8dB. The notch depth of the previous work does not reach a target notch depth of 40dB. On the other hand, the notch depth of the proposed N-path notch filter can be improved by reducing switch leak.

Table 4.3: Comparison of input and output filter to other works

Works	Input	Output	Result
[18]			Sim.
[7]			Sim.
[4]			Exp.
Topology 1			Exp.
Topology 2			Exp.

Sim. is simulation result
Exp. is experiment result

Table 4.2 shows the comparison of input signal and output filter to other works. The work from [18] used FIR Notch filter has a delay between input and output filter. [7] used a Gm-C filter is useful to suppress noise, but it looks different between input and output filter. The previous [4] cannot suppress noise because noise still appears in the output signal. Topology 1 and Topology 2 can suppress power line interference, no delay between input and output, and also get a noise-free signal in the output of the filter.

Chapter 5

N-PATH NOTCH FILTER WITH CAPACITANCE SCALING

As described in the chapter 4, Topology 1 and Topology 2 N-path notch filters achieved notch depth higher than 40dB, but have a problem in the size of capacitor. The unit capacitance of MIM capacitor is 1fF/μm^2. The size of capacitor in Topology 1 and Topology 2 are around 10nm up to 1 μm farad. Because of the size of capacitor proportional to the area, so it implies a large size of capacitor requires more space and cost. If the value of capacitor is 100pF, so it needs 100 mm^2 is not a practical area for an on-chip implementation. Thus, discrete capacitors were used to implement Topology 1 and Topology 2.

The technique to reduce total capacitance in Topology 1 and Topology 2 is increasing the value of resistance R. For example, if the value of R increase from 1MΩ to 1GΩ, so the total capacitance of the circuit will decrease 1000 times. However, it makes a problem for on-chip implementation. It happens because if resistor builds with a diffused resistor, it makes the length of the resistor too long and width of resistor too thick as shown in the equation 5.1 below.

$$R = R_s \frac{L}{W} \tag{5.1}$$

where R is the value of resistor, R_s is sheet resistor Ω/sqr, L is the length of resistor and W is width of resistor.

Furthermore, the use of external components requires more input-output (I/O) pins. For example, Topology 1 with ten paths requires 22 I/O pin. Therefore, this

chapter aims to propose a new technique of N-path notch filter with switched capacitance scaling to decrease the total capacitance for a fully on-chip implementation. A fully on-chip implementation of N-path notch filter makes it efficient to design portable ECG signal acquisition.

5.1   N-path Notch Filter with Capacitor Scaling

5.1.1   Basic Design
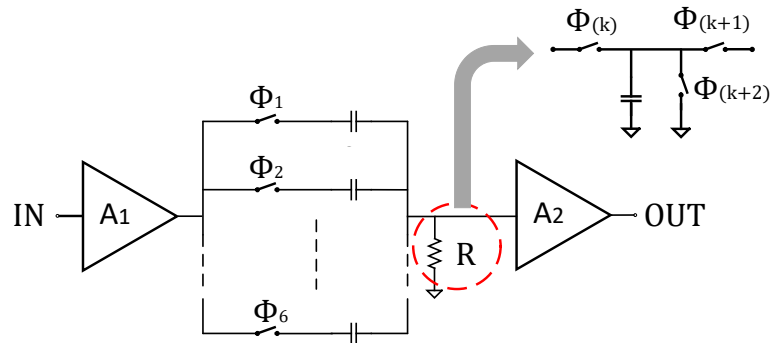
(a) Resistor equivalent of switched capacitor
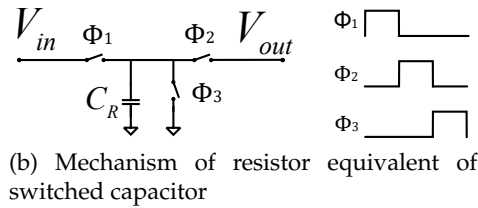
(b) Mechanism of resistor equivalent of switched capacitor

Figure 5.1: Resistor equivalent of switched capacitor

The proposed circuit or Topology 3 is actually based on conventional N-path notch filter but the resistor is replaced by a resistor equivalent of switched capacitor. The resistor equivalent of switched-capacitor as shown in Fig. 5.1 (a) is made from one capacitor C and three switches ϕ_k, ϕ_{k+1}, and ϕ_{k+2} which connect the capacitor with a given frequency alternately to the input and output of the switched-capacitor. Each switching cycle transfers a charge q from the input to the output at the switching frequency f. The charge q on a capacitor C with a voltage V between the plates is given by:

$$q = CV \tag{5.2}$$

Therefore, when ϕ_1 is closed while ϕ_2 and ϕ_3 are open, the charge stored in the capacitor C is

$$q_1 = C_R V_{in}. \tag{5.3}$$

When ϕ_2 is closed while ϕ_1 and ϕ_3 are open, some of that charge is transferred out of the capacitor, after which the charge that remains in capacitor C is

$$q_2 = C_R V_{out}. \tag{5.4}$$

Thus, the charge moved out of the capacitor to the output is

$$q_T = q_1 - q_2 = C_R(V_{in} - V_{out}) \tag{5.5}$$

Because this charge q_T is transferred at a rate f, the rate of transfer of charge per unit time is

$$I = q_T f. \tag{5.6}$$

Substituting Eq. (5.5) and Eq. (5.6)for q_T in the above, then

$$I = C_R(V_{in} - V_{out})f \tag{5.7}$$

Let V be the voltage across the SC from input to output. So,

$$V = V_{in} - V_{out}. \tag{5.8}$$

The equivalent resistance R_{eq} is

$$R_{eq} = \frac{V}{I} = \frac{1}{C_R f} \tag{5.9}$$

since the resistor R in the conventional N-path notch filter is replaced by the resistor equivalent of switched-capacitor, then $R_{eq} = R$ such that C_R is the value of resistor equivalent of switched-capacitor. The proposed circuit with capacitance scaling is shown in Fig. 5.2. Resistor equivalent of switched-capacitor is added each path in the circuit because of capacitors are memory elements. However, a resistor in the previous is not a memory element, and only one path is active at any time, so one shared resistor can be used.
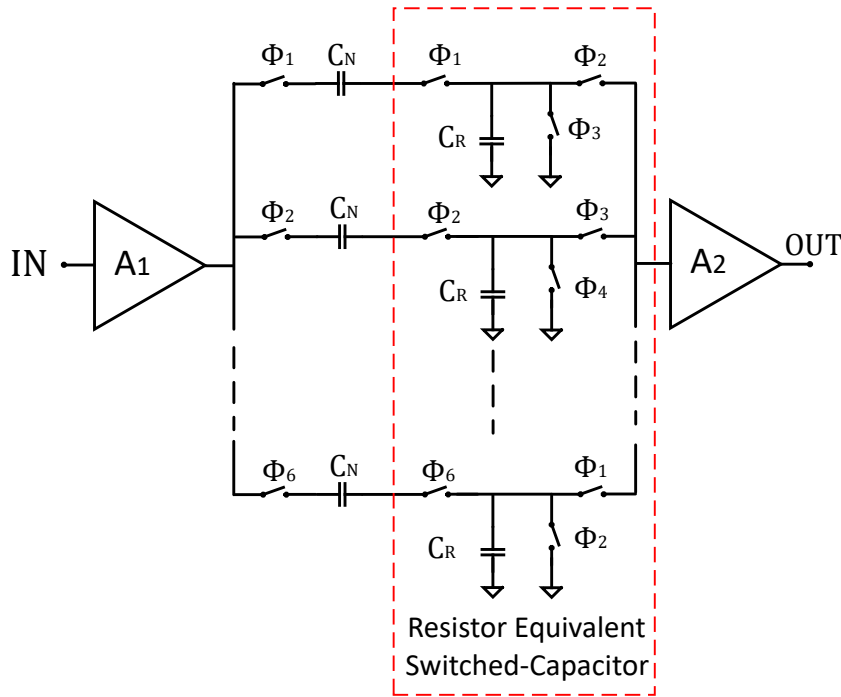
Figure 5.2: Topology 3 circuit

Figure 5.3 shows when ϕ_2 is closed. The opened switches are represented by their off-resistance. The transfer function from V_{in} to V_{out} is given by

$$H(s) = \frac{s\tau_1}{2s^2\tau_1\tau_2} \tag{5.10}$$

where $\tau_1 = C_N R_{off}$ and $\tau_2 = C_R R_{off}$. If Eq. (5.10) is compared with Eq. (2.10), this circuit improves notch depth. However, N-path notch filter with capacitance scaling has notch depth smaller than Topology 1 and Topology 2.
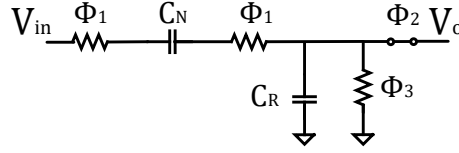
Figure 5.3: Circuit in the first path of 4-phase N-path notch filter circuit when ϕ_1 is closed

In this design, changing R into C_R can decrease value of capacitor in the circuit. The notch bandwidth BW of N-path notch filter with capacitance scaling is given by

$$BW = \frac{C_R f}{\pi C_N N} \tag{5.11}$$

where C_N and C_N are the value of capacitor in the N-path core and resistor equivalent of switched capacitor.

If the value of capacitor decreases ten times, then the value of R must increase ten times. For example, if the original capacitor values 1nF with scale down ten times, the value of capacitor will be 100pF and the value of R will change from 1MΩ to 10MΩ. As shown in Eq. 5.9, increasing the value of R can reduce the value of C_R. Therefore, this circuit is well implemented on the integrated circuit.

5.1.2 Implementation of Capacitor Scaling in Topology 1 and Topology 2

In the 5.1, the capacitance can be reduced with resistor equivalent of switched-capacitor (C_R). The capacitance scaling technique can also be applied to the Topology 1 and Topology 2. Figure 5.4 shows circuit design when resistor equivalent of switched-capacitor is implemented by Topology 1 and Topology 2. The N-path notch filter with capacitance scaling requires more components in each path, but it can achieve a higher notch depth compared to Topology 1 and Topology 2 without capacitance scaling. The application of this design can reduce the capacitance down to the order of pico-farads without degrading the notch depth as long as switches with off-resistance of 10GΩ or higher is implementable on the chip.

5.2 Simulation Results

Three of N-path notch filters with capacitor scaling as described in the section 5.1 are simulated using Spectre with CMOS technology 180nm. Three cases are used to
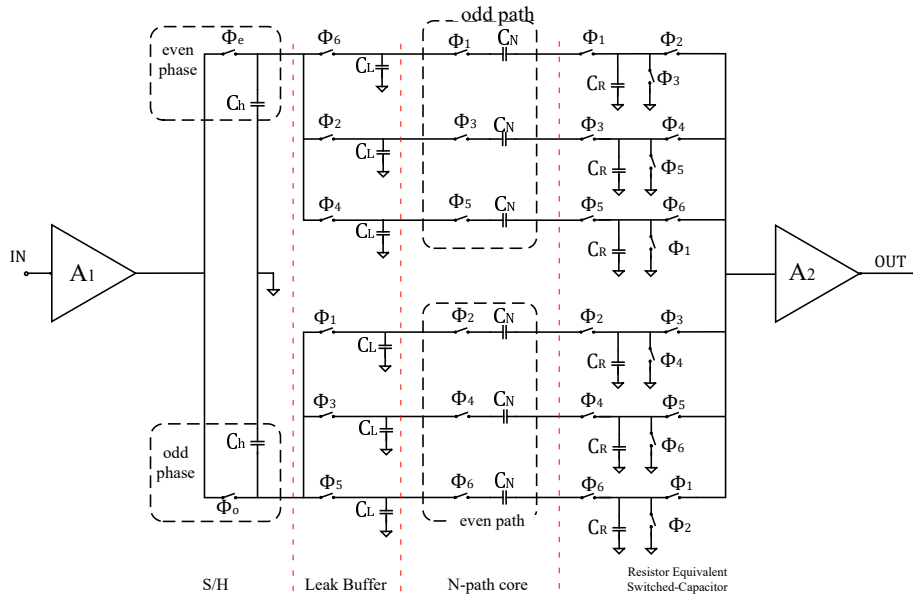
(a) Topology 1 with resistor equivalent switched-capacitor
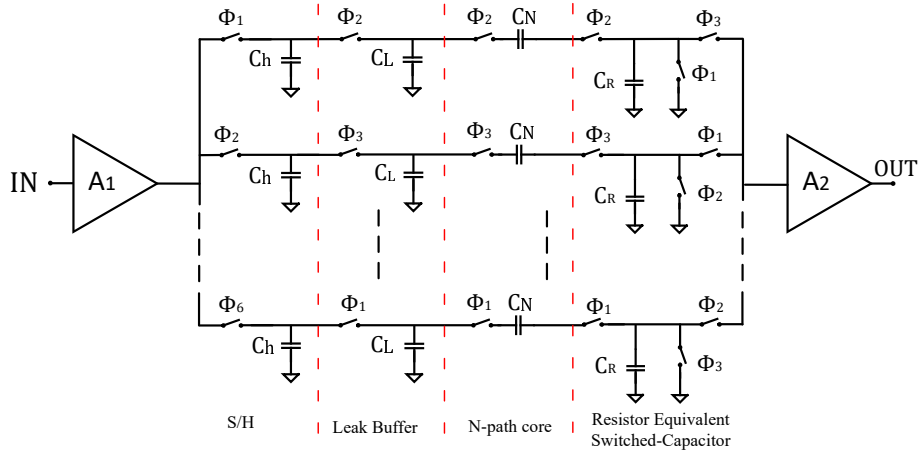
(b) Topology 2 with resistor equivalent switched-capacitor

Figure 5.4: Implementation of resistor equivalent switched-capacitor in N-path notch filter with leak buffer circuit.

find the best Topology for fully on-chip implementation.

5.2.1   Case 1

The simulation condition, in this case, is when total capacitance (C_T) each circuit equal to 1nF. The simulation conditions are given in Table 5.1.

As shown in Table 5.1, the number of paths is 6 and the sampling frequency of each path f_s is set to the power line frequency (50Hz). The Nyquist frequency f_N is half of the clock frequency, hence the value of f_N = 300Hz. The clock frequency 300Hz is used to generate six-phase clock (ϕ_1, ϕ_2, ϕ_3, and soon) respectively to drive

Table 5.1: Simulation condition of Case 1 in N-path notch filter with capacitance scaling

Parameter	Topology 1	Topology 2	Topology 3
N		6	
C_h	444pF	120pF	-
C_L	6.67pF	12pF	-
C_N	11.1pF	30.1pF	147pF
C_R	1.48pF	4.02pF	19.6pF
C_T		1nF	
f_s		50Hz	
A_1		20dB	
A_2		20dB	
Switches			
Ideal		R_{off}=1TΩ and R_{on}=1mΩ	
CMOS Switch	W=1 μm, L=1 μm, R_{off}=23.5GΩ and R_{on}=5.8kΩ		

the switches. All of the gains in simulation are set to 20dB. The CMOS switches in this research use CMOS complementary switch, if the value of W and L are 1 μm so that the value of R_{off} and R_{on} are 23.5GΩ and =5.8kΩ, respectively.

Figure 5.5 shows the simulation results of Case 1 with an ideal and CMOS switch. The simulation result uses an ideal switch, Topology 2 achieved a higher notch depth than the other Topologies. It is because Topology 2 has S/H circuit each path in the circuit so that leak path in the circuit smaller then Topology 1 with capacitor scaling and Topology 3. Using the CMOS switch, the proposed N-path notch filter with capacitance scaling achieved notch depth higher than 40dB and it can be used for on-chip implementation. Topology 1 with capacitor scaling achieved notch depth higher than Topology 2 with capacitor scaling in the simulation with CMOS switch. It is because of Topology 1 with capacitor scaling use higher capacitance at C_h, C_L, and C_N. The factor to make higher notch depth is increasing capacitance, off-resistance, and added more leak buffer circuit.

The relation between notch depth and off-resistance shown in Fig. 5.6. As shown in Fig. 5.6, Topology 3 is hard to implement on the chip because it needs a very high switch off-resistance because it need the minimum value of off-resistance is 20GΩ or more.

(a) Simulation result of Case 1 with ideal switches at frequency 50Hz
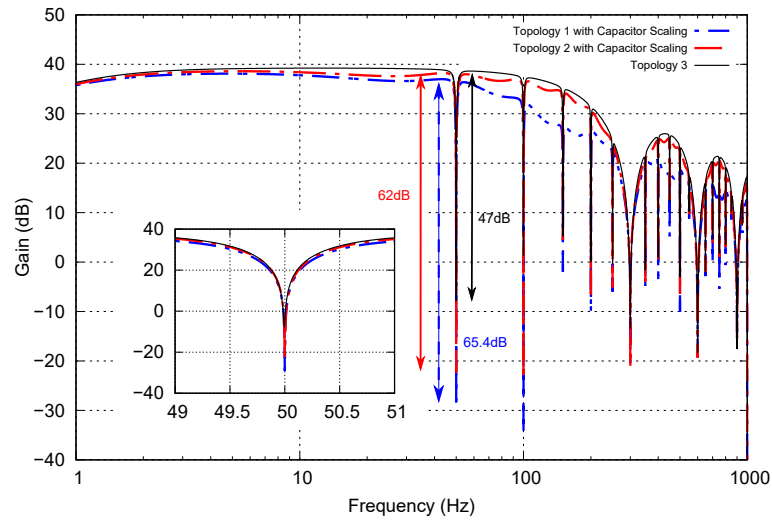
(b) Simulation result of Case 1 with CMOS switches at frequency 50Hz

Figure 5.5: Simulation result of Case 1 at frequency 50Hz
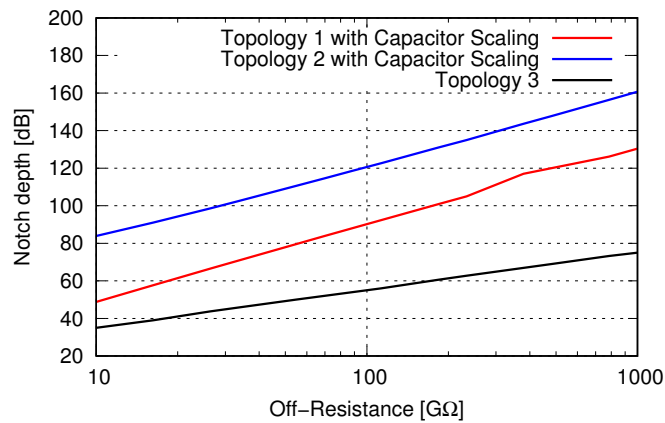
Figure 5.6: Relation between notch depth and off-resistance in Case 1

5.2.2 Case 2

The simulation condition, in this case, is when capacitor size scale down to 1000 times. The simulation conditions are given in Table 5.2.
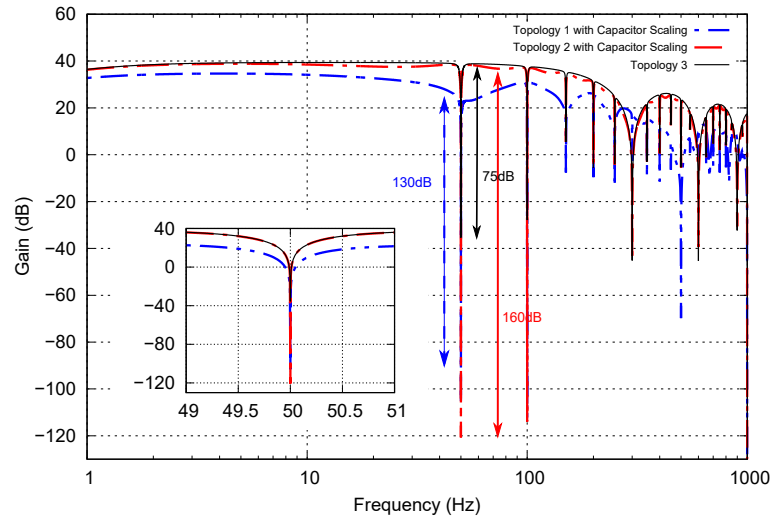
Table 5.2: Simulation condition of Case 2 in N-path notch filter with capacitance scaling

Parameter	Topology 1	Topology 2	Topology 3
N		6	
C_h		100pF	-
C_L		10pF	-
C_N		25pF	147pF
C_R		3.33pF	19.6pF
C_T	430pF	830pF	170pF
f_s		50Hz	
A_1		20dB	
A_2		20dB	
Switches			
Ideal		R_{off}=1TΩ and R_{on}=1mΩ	
CMOS Switch	W=1 μm, L=1 μm, R_{off}=23.5GΩ and R_{on}=5.8kΩ		

As shown in Table 5.2, the value of C_h, C_L, C_N, and C_R in the Topology 1 and Topology 2 are the same. The difference between Topology 1 with capacitor scaling and Topology 2 with capacitor scaling is the value of total capacitance because of Topology 1 with capacitor scaling use two S/H circuits and Topology 2 with capacitor scaling use six S/H circuits. All of conditions in this Case is the same with Case 1 as described at 5.2.1.

Figure 5.7 shows the simulation results of Case 2 with an ideal and CMOS switch. The simulation result uses an ideal switch, Topology 2 with capacitor scaling achieved a higher notch depth than the other Topologies. It is because Topology 2 has S/H circuit each path in the circuit and use high value of off-resistance so that leak path in the circuit smaller then Topology 1 with capacitor scaling and Topology 3. Using the CMOS switch, Topology 1 and Topology 2 with capacitor scaling achieved notch depth higher than 40dB and it can be used for on-chip implementation. However, Topology 3 cannot be used for on-chip implementation because it achieved notch depth small than 40dB.
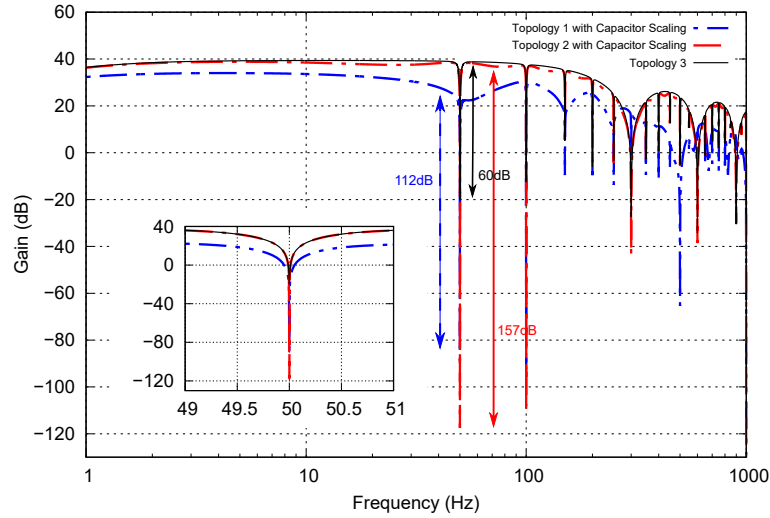
(a) Simulation result of Case 2 with ideal switches at frequency 50Hz

(b) Simulation result of Case 2 with CMOS switches at frequency 50Hz

Figure 5.7: Simulation result of Case 2 at frequency 50Hz

5.2.3   Case 3

The simulation condition, in this case, is when capacitor size scale down to 100 times. The simulation conditions are given in Table 5.3.

As shown in Table 5.3, the value of C_h, C_L, C_N, and C_R in the Topology 1 and Topology 2 with capacitor scaling are the same. The difference between Topology 1 and Topology 2 with capacitor scaling is the value of total capacitance because of Topology 1 with capacitor scaling use 2 S/H circuits and Topology 2 with capacitor scaling use 6 S/H circuits. All of conditions in this Case is the same with Case 1 as described at 5.2.1.

Figure 5.8 shows the simulation results of Case 2 with an ideal and CMOS switch.

Table 5.3: Simulation condition of Case 3 in N-path notch filter with capacitance scaling

Parameter	Topology 1	Topology 2	Topology 3
N		6	
C_h		1nF	-
C_L		100pF	-
C_N		250pF	147pF
C_R		33.3pF	19.6pF
C_T	4.3nF	8.3nF	1.7nF
f_s		50Hz	
A_1		20dB	
A_2		20dB	
Switches			
Ideal		R_{off}=1TΩ and R_{on}=1mΩ	
CMOS Switch	W=1 μm, L=1 μm, R_{off}=23.5GΩ and R_{on}=5.8kΩ		

The simulation result uses an ideal switch, Topology 1 with capacitor scaling achieved a higher notch depth than the other Topologies. Using the CMOS switch, all of topologies achieved notch depth higher than 40dB. However, it hard to use for on-chip implementation because it uses total capacitance more than 1nF. This implementation will require more chip size.

5.3 Discussion

The simulation condition, in this case, is when notch depth in the circuit around 44dB. The simulation conditions are given in Table 5.3.

Table 5.4: Simulation condition of Case 4 in N-path notch filter with capacitance scaling

Parameter	Topology 1	Topology 2	Topology 3
N		6	
C_h		16.6pF	-
C_L		1.6pF	-
C_N		4.1pF	83pF
C_R		555fF	11pF
C_T	76pF	138pF	566pF
f_s		50Hz	
A_1		20dB	
A_2		20dB	
Switches			
CMOS Switch	W=1 μm, L=1 μm, R_{off}=23.5GΩ and R_{on}=5.8kΩ		
H_N		around 44dB	
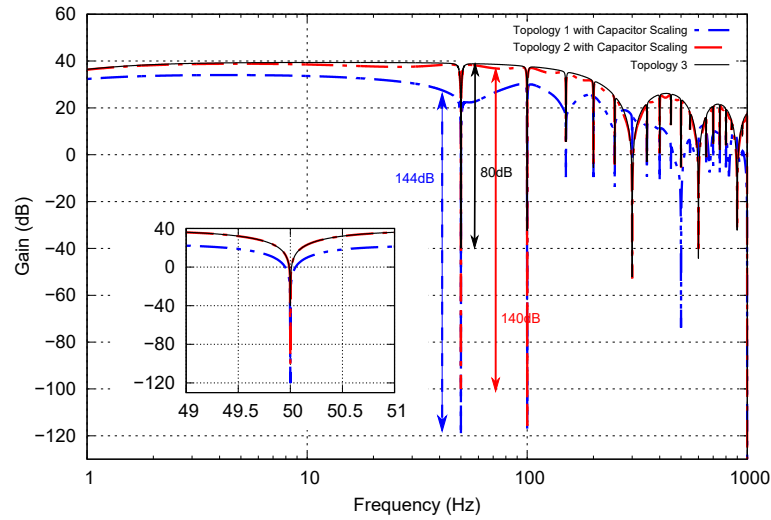
(a) Simulation result of Case 3 with ideal switches at frequency 50Hz
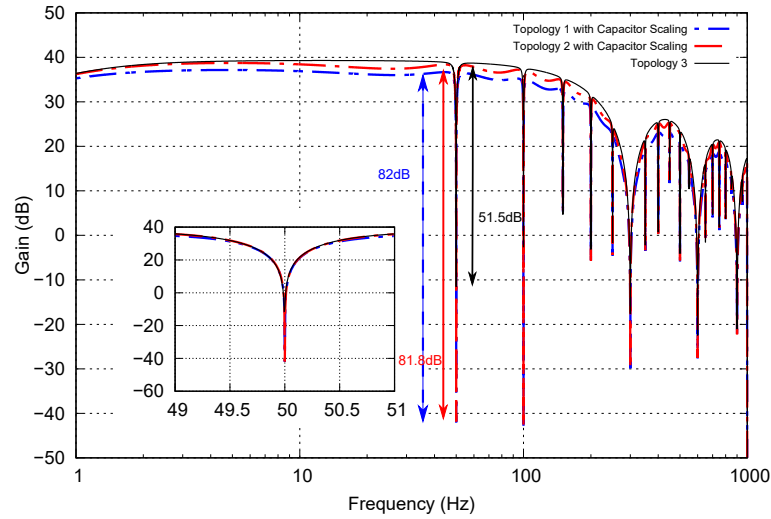
(b) Simulation result of Case 3 with CMOS switches at frequency 50Hz

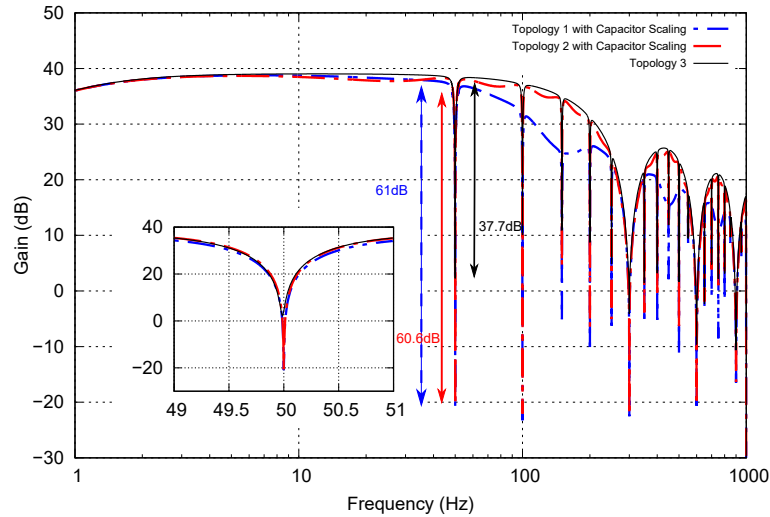Figure 5.8: Simulation result of Case 3 at frequency 50Hz

As shown in Table 5.4, Topology 1 with capacitor scaling is more effective in the total capacitance for on-chip implementation because of to achieve notch depth around 44dB. It used the smallest total capacitance than the other topologies.

5.4   Conclusion

This chapter works to reduce total capacitance in N-path notch filter circuit because of total capacitance for Topology 1 and Topology 2 are 2.3 µF and 930nF, respectively. The proposed N-path notch filter replace the resistor in N-path core into resistor equivalent of switched-capacitor to reduce the total capacitance. Topology 1 and Topology 2 with capacitor scaling and also Topology 3 using CMOS switch with total

capacitance for all topologies equal to 1nF achieved notch depth higher than 40dB. However, Topology 3 has notch depth very limited than Topology 1 and Topology 2 with capacitor scaling. Table 5.5 summarizes the result of N-path notch circuit implementation.

Table 5.5: Comparison of N-path notch filter implementation

Parameter	Topology 1		Topology 2		Topology 3
	WOCS	WCS	WOCS	WCS	
Discrete comp.	★★★★	★	★★★★	★	★★
On-chip	✕	★★★★★	✕	★★★★	★★
Smaller N	★★★		★★★★		★★★
Higher N	★★★★		★★★		★★★

WOCS is Topology without capacitor scaling
WCS is Topology with capacitor scaling

As shown in Tabel 5.5, Topology 1 and Topology 2 are suitable for implementation using a discrete component. However, Topology 3 achieved limited notch depth. Topology 1 with capacitor scaling is perfect for on-chip implementation because it uses smaller total capacitance as described at 5.3. Topology 2 with capacitor scaling also can be used for on-chip implementation but has higher total capacitance than Topology 1 with capacitor scaling. Topology 3 cannot be used for on-chip implementation if total capacitance smaller than 1nF because it will achieve notch depth lower than 40dB. Using a small number of path Topology 2 is very good because it reached a higher notch depth than the other topologies. Moreover, using a high number of paths, Topology 1 has less component than Topology 2 and achieve higher notch depth than Topology 3.

Chapter 6

CONCLUSIONS AND RECOMMENDATION

6.1 Overall Conclusion

Cardiovascular diseases (CVDs) are the number one cause of death globally. Therefore, the prevention and diagnosis of cardiovascular disease become one of the primary issues for medician today. However, electrocardiogram (ECG) signal is challenging to obtain high-quality electrical signals because ECG signal has small amplitude and low frequency. When performing ECG signal acquisition, common-mode noise such as power line interference appears near the desired ECG signal. It has made a problem when the power line interference has amplitude higher than the primary signal.

Common-mode noise reduction has been recognized as important research. The driven right leg (DRL) techniques effective to reduce the influence of stray currents through the body. However, noise still appears even measurement used the DRL circuit. Another problem with DRL circuit is mismatching in the electrode impedance makes an impact to convert common-mode noise into a differential input voltage. The body in DRL circuit is expressed as a single node and cannot be used to simulate the effect of the electrode impedance mismatch. Therefore, a new body model is needed to be able to analyze the effect of electrode impedance mismatch and other problem with common body model.

The proposed DRL circuit is an improved circuit from common DRL circuit. The

first improved DRL circuit, biomedical signal is expressed by current source in parallel with electrode impedance. The simulation results of improved circuit show mismatch between right and left electrode impedance makes noise appears at the output signal. The common human body from DRL circuit represented skin-electrode impedance as a single node. The second improved circuit, the skin-electrode impedance is expressed by resistance and stray capacitance are on each electrode. The simulation results of this improved circuit show the proposed circuit achieved smaller noise when stray capacitance in the arm and right leg are the same. Combination between proposed human body model and DRL circuit achieved output of the circuit is noise appear in the output signal. Therefore, human body model with DRL circuit still need another filter to get high quality biomedical signal (noise free signal).

The other techniques to suppress common-mode noise have been proposed by using digital and analog notch filters. The technique to suppress common-mode noise used a digital notch filter, but it requires an analog front-end with a wide dynamic range since the noise contaminated input signal need to be converted to digital signal. The techniques with analog notch filter such as conventional N-path notch filters have disadvantage because these techniques require more the number of path and higher switch off-resistance to reach notch depth target. The problem to implement previous N-path notch filter is the difficulty in implementing switch with off-resistance. On-chip implementation of the system is also a challenge in the realization of portable ECG devices because the notch filter has a large time constant in which requires large capacitance and high resistance.

Two topologies of N-path notch filter with leak buffer circuit have been proposed. The proposed N-path notch filters are Topology 1 and Topology 2. Topology 1 and Topology 2 achieved notch depth of 62.4dB and 63dB in measurement results with sampling frequency 50Hz, even if the proposed circuits use less number of path and small of switches off-resistance. Topology 1 and Topology 2 are verified using artificial ECG signal with 2Hz which is contaminated by power line interference with frequency 50Hz or 60Hz. Experiment results show that the proposed circuit significantly reduces the power line noise.

Topology 1 and Topology 2 N-path notch filters achieved notch depth higher

than notch depth target, but have a problem in the size of capacitor. The total capacitance for Topology 1 and Topology 2 are 2.3 µF and 930nF, respectively. Therefore, the next proposed circuit aims to propose a new technique of N-path notch filter with switched capacitance scaling to decrease the total capacitance for a fully on-chip implementation. The proposed N-path notch filter replace the resistor in N-path core into resistor equivalent of switched-capacitor to reduce the total capacitance. Topology 1 and Topology 2 with capacitor scaling and also Topology 3 using CMOS switch with total capacitance for all topologies equal to 1nF achieved notch depth higher than 40dB.

Topology 1 and Topology 2 using CMOS switch with scaling factor 1000 achieved notch depth of 64dB and 68dB, respectively. The total capacitance of Topology 1 and Topology 2 using CMOS switch with scaling factor 1000 are 2.34nF and 930pF, respectively. Below are advantage and disadvantage of Topology 1, Topology 2, and Topology 3 with/without capacitance scaling. Topology 1 with capacitor scaling is more effective in the total capacitance for on-chip implementation because of to achieve notch depth around 44dB. It used the smallest total capacitance than the other topologies.

6.2 Contributions

The main contributions of this research can be listed as below:

- Proposed ECG signal acquisition with DRL can express the effect of mismatch in the electrode impedance to the output signal. For the researcher, the new ECG body model can be used to find and analyze why is biomedical signal acquisition achieved poor signals and how to fix it.

- Proposed N-path notch filter with leak buffer has been proposed to improve notch depth and can suppress power line interference. The proposed circuit with Topology 1 and Topology 2 can be used in the discrete components. Meanwhile, Topology 3 design with resistor equivalent switched-capacitor can be implemented on an integrated circuit. To get higher notch depth and smaller

off-resistance than Topology 3, the resistor equivalent switched-capacitor circuit can be used in the Topology 1 and Topology 2. Therefore, the proposed N-path notch filter circuits suitable for practical realization either using discrete components or fully on-chip implementations. It is very useful to implement this design for portable biomedical devices.

6.3   Future Work

Some future works that can be done to improve this in the future are as follows:

- The proposed circuit should be implemented in the actual body. Safety for patients is very important. Therefore, every biomedical signal acquisition should consist of isolation and protection circuits, to prevent the patients from electrical shocks.

- The proposed N-path notch circuit would be implemented with two probe electrodes to make portable ECG acquisition devices more efficient for patients.

Appendix A

List of Publications

A.1 List of Journals

1. Afifah Khilda, Retdian Nicodimus. "Design of N-path Notch Filter Circuits for Hum Noise Suppression in Biomedical Signal Acquisition." Analog Circuits and Their Application Technologies, IEICE Transactions on Electronics. 2020. Volume and Number: Vol.E103-C,No.10,pp.-,Oct. 2020)

2. Afifah Khilda, Retdian Nicodimus. "Design of N-path Notch Filter Circuit with Switched-Capacitor Resistor." Analog Integrated Circuits and Signal Processing, Springer. (Under Review)

A.2 List of Published Conference Papers

A.2.1 International Conference Paper

1. Afifah, Khilda, Muhammad Arijal, Nicodimus Retdian, and Takeshi Shima. "Second-Order N-path Notch Filter for Hum Noise Suppression." In 2018 International Symposium on Electronics and Smart Devices (ISESD), pp. 1-4. IEEE, 2018.

2. Arijal, Muhammad, Khilda Afifah, and Nicodimus Retdian. "Direct Conversion Using N-Path Filter for ASK Demodulator." In 2018 International Symposium on Electronics and Smart Devices (ISESD), pp. 1-4. IEEE, 2018.

3. Afifah Khilda, Arijal Muhammad, Retdian Nicodimus, and Shima Takeshi. "Design of 10-phase and 3-Phase N-path Filter for Hum Noise Suppression." In 2018 International Conference on Analog VLSI Circuits (AVIC). IEEJ, 2018.

4. Afifah, Khilda, Muhammad Arijal, Nicodimus Retdian, and Takeshi Shima. "Experiment on Hum Noise Suppression using N-path Notch Filter." In 2018 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp. 519-522. IEEE, 2018.

5. Afifah, Khilda, Muhammad Arijal, Nicodimus Retdian, and Takeshi Shima. "Experiment of 3-Phase N-Path Filter for Hum Noise Suppression." In 2019 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-4. IEEE, 2019.

6. Afifah Khilda, Retdian Nicodimus. "Design of N-path Notch Filter with Resistor Equivalent Switched Capacitor for Hum Noise Suppression." In 2019 International Conference on Analog VLSI Circuits (AVIC). IEEJ, 2019.

A.2.2   Domestic Conference Paper

1. Afifah Khilda, Arijal Muhammad, Retdian Nicodimus, and Shima Takeshi. "Investigation on 10-phase N-path Filter for Hum Noise Suppression." The Institute of Electrical Engineers of Japan (IEEJ), (2018).

2. Arijal Muhammad, Afifah Khilda, Retdian Nicodimus, and Shima Takeshi. "50-dB Hum Noise Suppression using 3-phase N-path Filter." The Institute of Electrical Engineers of Japan (IEEJ), (2018).

3. Arijal Muhammad, Afifah Khilda, Retdian Nicodimus. "Direct conversion for NFC system using N-path filter." The Institute of Electrical Engineers of Japan (IEEJ), (2018).

4. Afifah Khilda, Arijal Muhammad, Retdian Nicodimus, and Shima Takeshi. "Investigation on 10-phase N-path Filter with Leak Buffer Circuit for Hum Noise Suppression." The Institute of Electrical Engineers of Japan (IEEJ), (2018).

5. Afifah Khilda, Retdian Nicodimus, Takeshi Shima. "Analysis on the Effect of Charge Leakage on N-path Notch Filter." The Institute of Electrical Engineers of Japan (IEEJ), (2018).

6. Afifah Khilda, Retdian Nicodimus. " Analysis the effect of Electrode-Skin Impedance and DRL Circuit to Common-Mode Voltage in ECG Signal Acquisition." The Institute of Electrical Engineers of Japan (IEEJ), (2019).

Bibliography

[1] A. S. Arnold, J. S. Wilson, M. G. Boshier, and J. Smith, "Recommendations for standardization of leads and of specifications for instruments in electrocardiography and vectorcardiography: Report of committee on electrocardiography, american heart association", *Circulation*, vol. 35, no. 3, pp. 583–602, Mar. 1967.

[2] X. Qian, Y. P. Xu, and X. Li, "A cmos continuous-time low-pass notch filter for eeg systems", *Analog Integrated Circuits and Signal Processing*, vol. 44, no. 3, pp. 231–238, Sep. 2005.

[3] M. M. Z. Zadeh, S. Niketeghad, and R. Amirfattahi, "A pll based adaptive power line interference filtering from ecg signals", *The 16th CSI International Symposium on Artificial Intelligence and Signal Processing (AISP 2012)*, pp. 490–496, May 2012.

[4] N. Retdian and T. Shima, "N-path notch filter with a 43-db notch depth improvement for power line noise suppression", *2016 International Symposium on Electronics and Smart Devices (ISESD)*, Nov. 2016.

[5] Z. dong Zhao and Y. quan Chen, "A new method for removal of baseline wander and power line interference in ecg signals", *2006 International Conference on Machine Learning and Cybernetics*, Aug. 2006.

[6] X. Qian, Y. P. Xu, and X. Li, "Suppression of baseline wander and power line interference in ecg using digital iir filter", *International journal of circuits, systems and signal processing*, vol. 3, no. 2, pp. 356–365, Aug. 2008.

[7] S. A. Mahmoud, A. Bamakhramah, and S. A. Al-Tunaiji, "Six order cascaded power line notch filter for ecg detection systems with noise shaping", *Circuits, Systems, and Signal Processing*, vol. 33, no. 8, pp. 2385–2400, Mar. 2014.

[8]   A. Ghiffari, E. A. M. Klumperink, and B. Nauta, "Tunable n-path notch filters for blocker suppression: Modeling and verification", *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, Apr. 2013.

[9]   B. B. Winter and J. G. Webster, "Driven-right-leg circuit design", *IEEE Transactions on Biomedical Engineering*, vol. BME30, no. 1, pp. 62–66, Jan. 1983.

[10]   Bruce B. Winter and John G. Webster, "Reduction of interference due to common mode voltage in biopotential amplifiers", *IEEE Tannsactions on Biomedical Engineering*, vol. BME30, no. 1, pp. 58–61, Mar. 1982.

[11]   S. W. Wan and H. T. Nguyen, "50hz interference and noise in ecg recordings - a review", *Australasian Physical and Engineering Sciences in Medicine*, vol. 17, no. 3, pp. 108–115, Jun. 1994.

[12]   A. C. M. van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events", *Medical and Biological Engineering and Computing*, vol. 28, no. 5, pp. 389–397, Sep. 1990.

[13]   E. M. Spinelli, N. H. Martinez, and M. A. Mayosky, "A transconductance driven-right-leg circuit", *IEEE Transactions on Biomedical Engineering*, vol. 46, no. 12, pp. 1466–1470, Dec. 1999.

[14]   A. Wong, K. P. Pun, Y. T. Zhang, and C. S. Choy, "An ecg measurement ic using driven-right-leg circuit", *2006 IEEE International Symposium on Circuits and Systems*, pp. 345–348, May 2006.

[15]   H. A. Alzaher, N. Tasadduq, and Y. Mahnashi, "A highly linear fully integrated powerline filter for biopotential acquisition systems", *IEEE transactions on biomedical circuits and system*, vol. 7, no. 5, pp. 703–712, Oct. 2013.

[16]   JacekPiskorowski, "Suppressing harmonic powerline interference using multiple-notch filtering methods with improved transient behavior", *Measurement*, vol. 45, no. 6, pp. 1350–1361, Jul. 2012.

[17]   H. K. Jayant, K. Rana, V. Kumar, S. S. Nair, and P. Mishra, "Efficient iir notch filter design using minimax optimization for 50hz noise suppression in ecg", *2015 International Conference on Signal Processing, Computing and Control (IS-PCC)*, Sep. 2015.

[18]   Y.-W. Bai, W.-Y. Chu, C.-Y. Chen, Y.-T. Lee, Y.-C. Tsai, and C.-H. Tsai, "Adjustable 60hz noise reduction by a notch filter for ecg signals", *Proceedings of the 21st IEEE Instrumentation and Measurement Technology Conference (IEEE Cat. No.04CH37510)*, May 2004.

[19]   B. K. Casper, D. J. Comer, and D. T. Comer, "An integrable 60-hz notch filters", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 1, pp. 74–77, Jan. 1999.

[20]   H. Li, J. Zhang, and L. Wang, "A fully integrated continuous-time 50-hz notch filter with center frequency tunability", *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 3558–3562, Sep. 2011.

[21]   P.-I. Mak, M.-I. Vai, P.-U. Mak, S.-H. Pun, W. Feng, and R. P. Martins, "A 90nm cmos bio-potential signal readout front-end with improved powerline interference rejection", *2009 IEEE International Symposium on Circuits and Systems*, pp. 1–4, May 2009.

[22]   J. L. Bohorquez, M. Yip, A. P. Chandrakasan, and J. L. Dawson, "A biomedical sensor interface with a sinc filter and interference cancellation", *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 746–756, Feb. 2011.

[23]   C. D. Oster, "Proper skin prep helps ensure ecg trace quality. 3m health care, 2005.", *Philips Healthcare*, Oct. 2014.

[24]   M. Hojo, T. Ohnishi, Y. Mitani, O. Saeki, and H. Ukai, "Observation of frequency oscillation in western japan 60 hz power system based on multiple synchronized phasor measurements", *2003 IEEE Bologna PowerTech Conference*, pp. 1–6, Jun. 2003.

[25]   R. Tanaka, T. Deguchi, and N. Nakano, "Prototype and measurement of automatic synchronous pll system for n-path filter for hum noise reduction", *2017 International Symposium on Electronics and Smart Devices*, pp. 295–299, Oct. 2017.