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Vertical Stacked Field Effect Transistor

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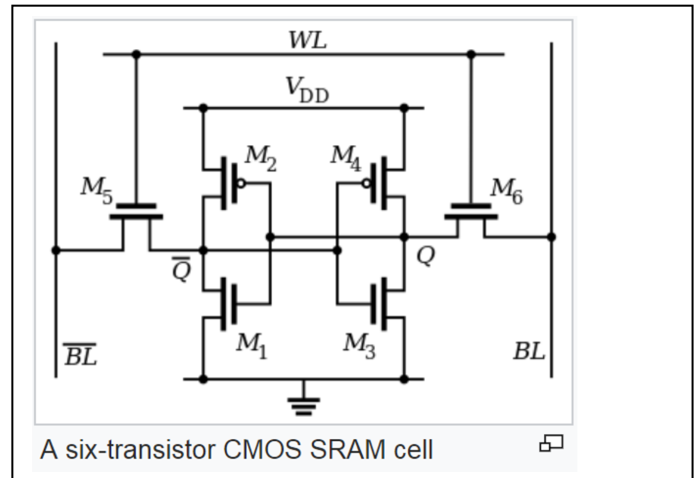
VERTICAL STACKED FIELD EFFECT TRANSISTOR

Authors: Benjamin VINCENT and Joseph ERVIN

Background

A 6 transistor (6T) complementary metal oxide semiconductor (CMOS) static random access memory (SRAM) cell includes 4 same type transistors (for example: n-type) and 2 additional transistors from the opposite type (for example: p-type). There are 2 inverters (including n- and p- transistor with drains and gate connected) designed back to back and 2 additional access transistors. In a traditional implementation (shown at right) using field effect transistors (FET), current flows horizontally and a vertical-FET may be used.

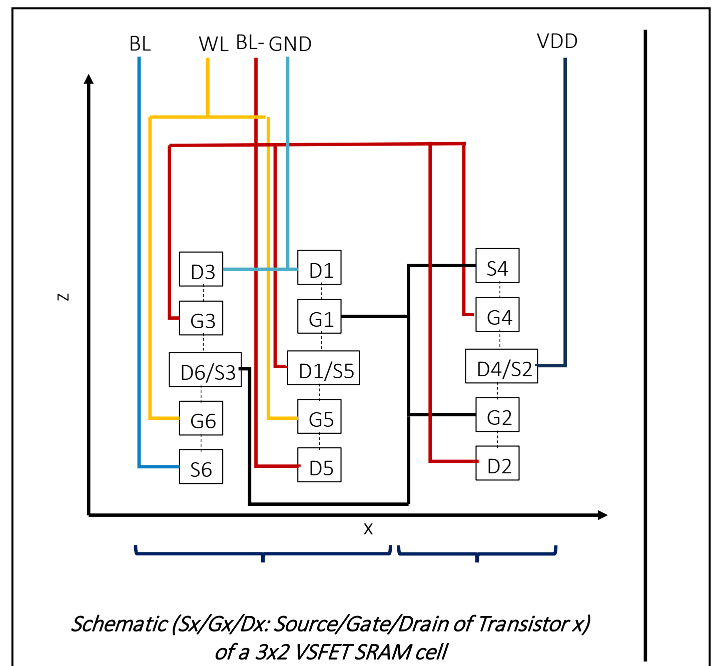


A six-transistor CMOS SRAM cell

Discussion

The move from planar to FinFET technology is expected to continue in the future. Current options include Nanosheet, Forksheet and Vertical FET architectures. While vertical FET is attractive, the footprint is currently too large. Improvement of the footprint of vertical FETs can be achieved if the vertical transistors can be stacked on top of each other with an easy integration path.

The present disclosure relates to an integration solution allowing two vertical FET transistors to be stacked on top of each other using a monolithic process integration flow. Stacking two transistors on top of each other (instead of having them conventionally side-by-side) offers a key benefit with respect to footprint reduction. A 6T SRAM design (shown at right) includes 2 Vertical-FETs that are stacked. A process flow (below) allows a 6T SRAM cell with an array of 3 pairs of transistors. Each pair of transistors includes 2 vertical transistors stacked on top of each other. The monolithic approach described below allows stacking of two vertical FET transistors using the Fin itself as a wall separation between the gate processing area and the source/drain processing area.

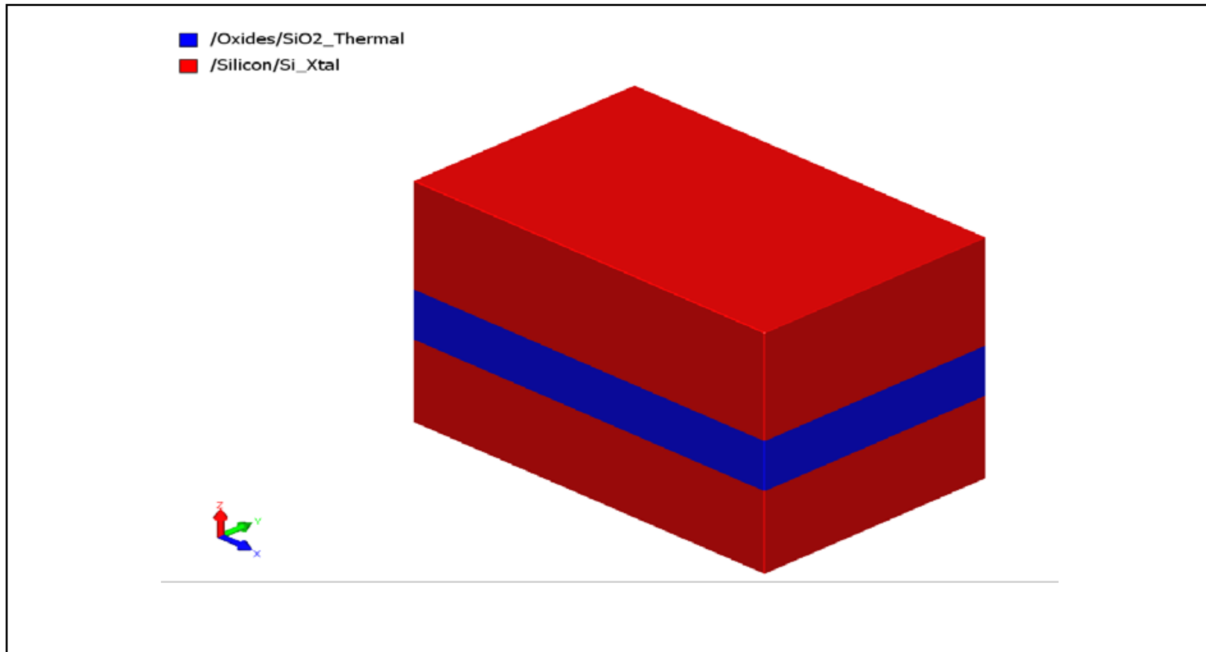


Schematic (Sx/Gx/Dx: Source/Gate/Drain of Transistor x) of a 3x2 VSFET SRAM cell

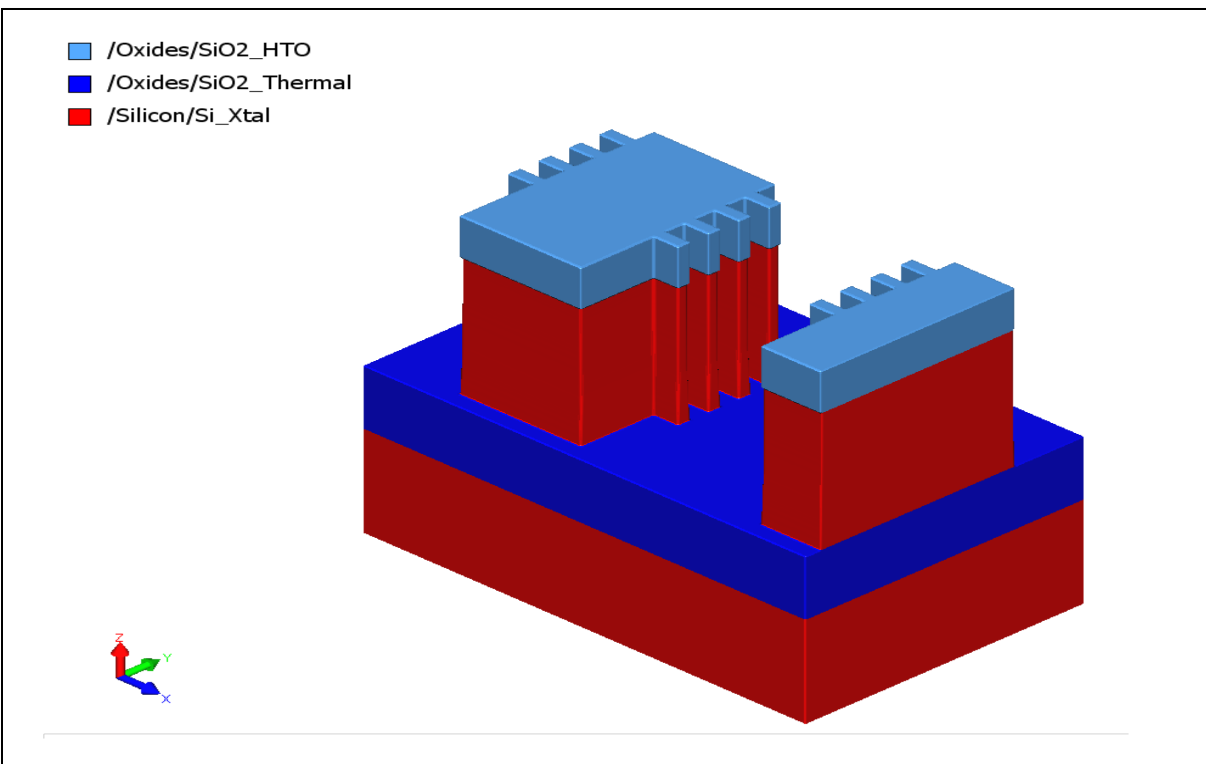
The following is an example of an integration solution for a 6T SRAM with 2 Vertical-FETs that are stacked.

SOI starting substrate and Fin formation

4.1.3. SOI starting material

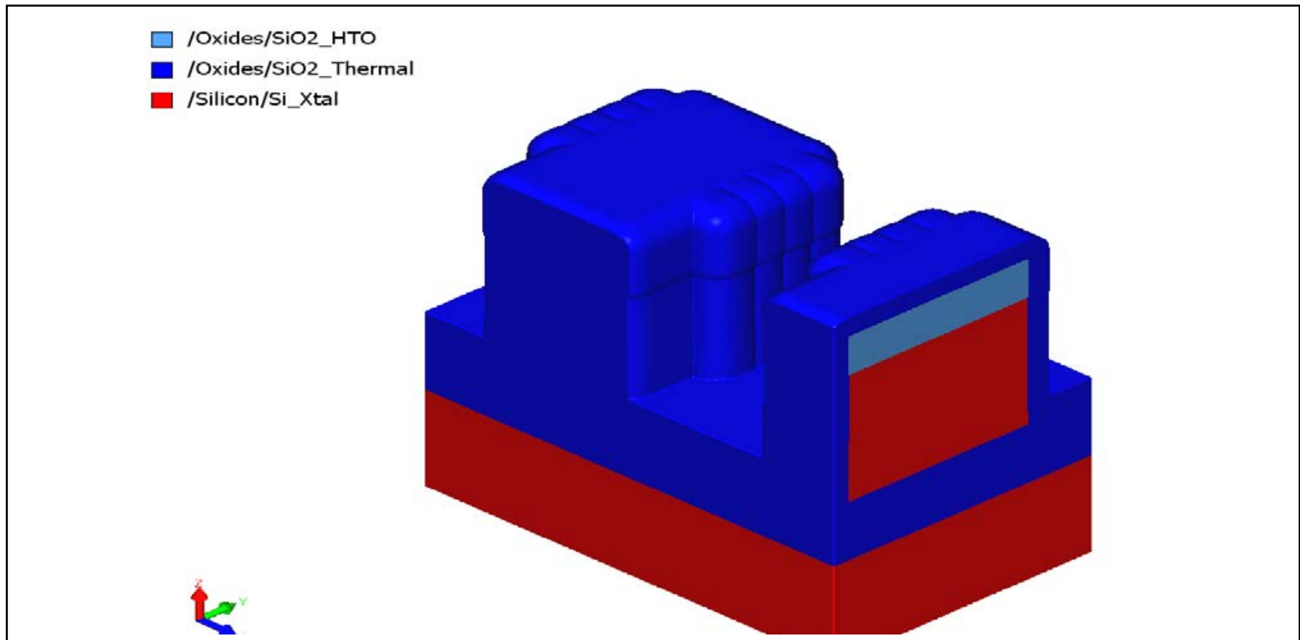


4.1.13.6. Remove Materials

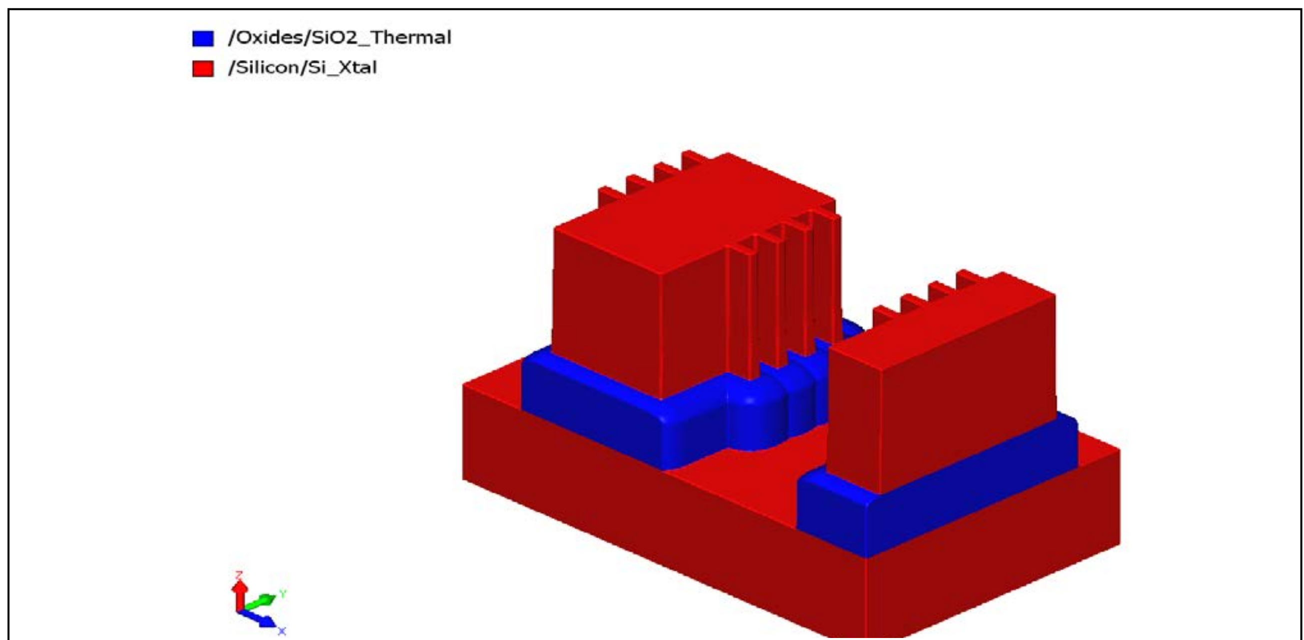


FinCUT module

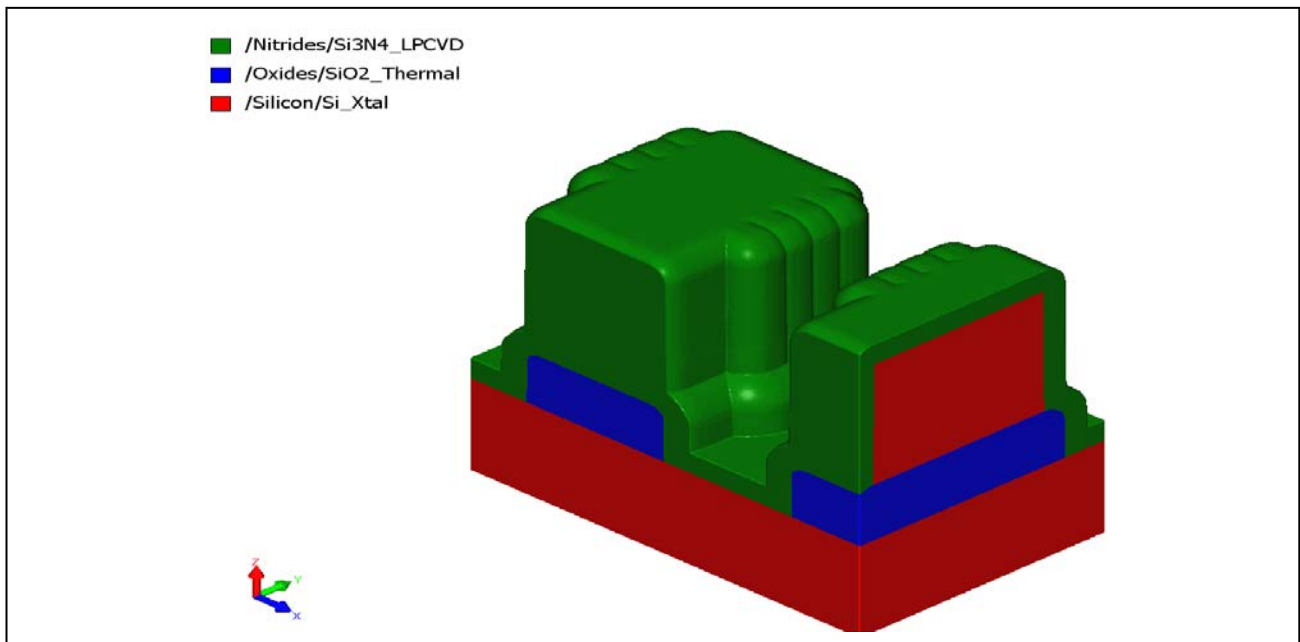
4.2.2.1. Conformal Deposit



4.2.2.2. Straight Etch



4.2.2.3. Conformal Deposit



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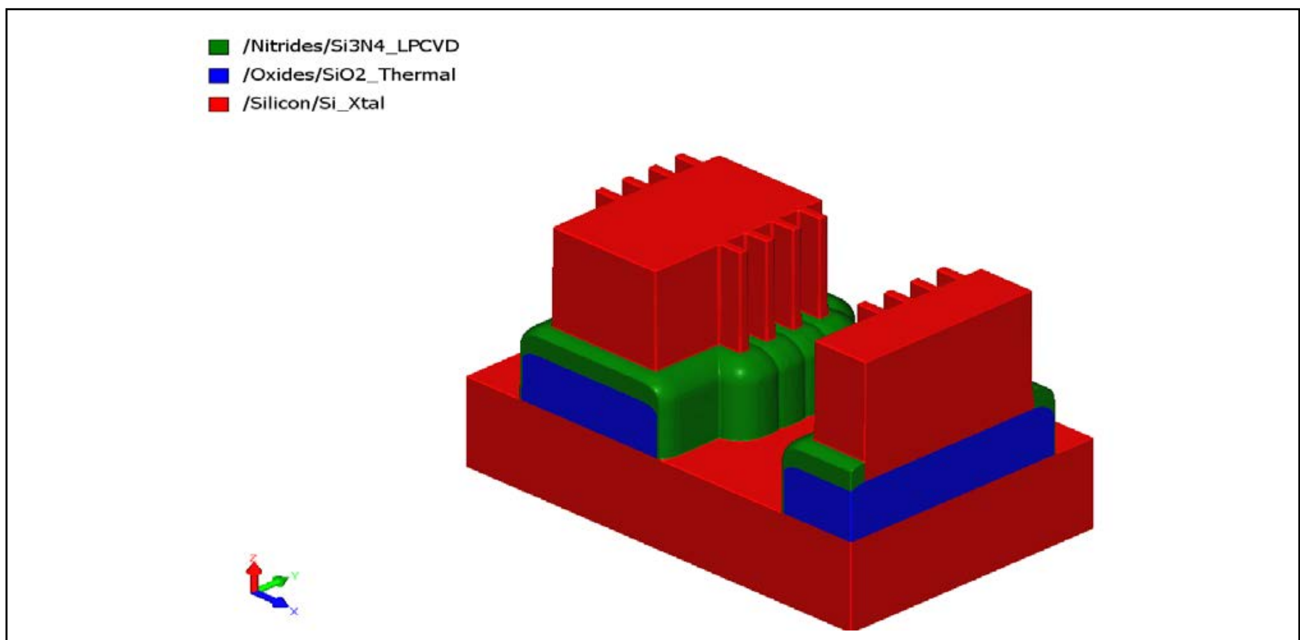

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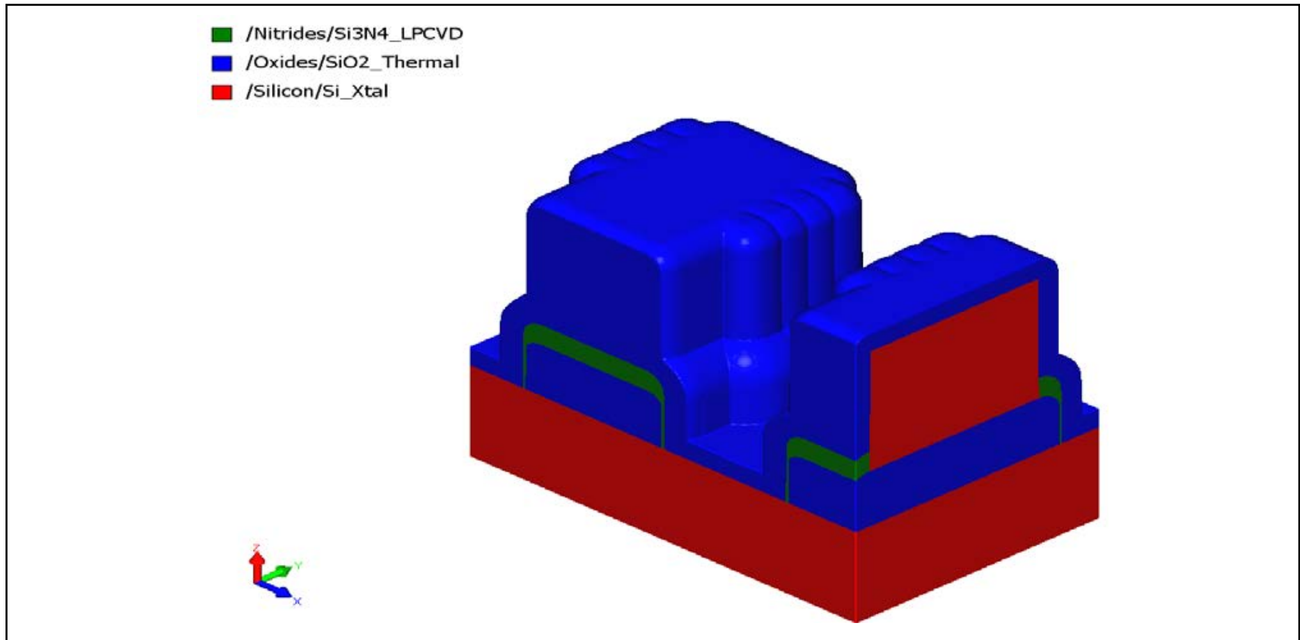
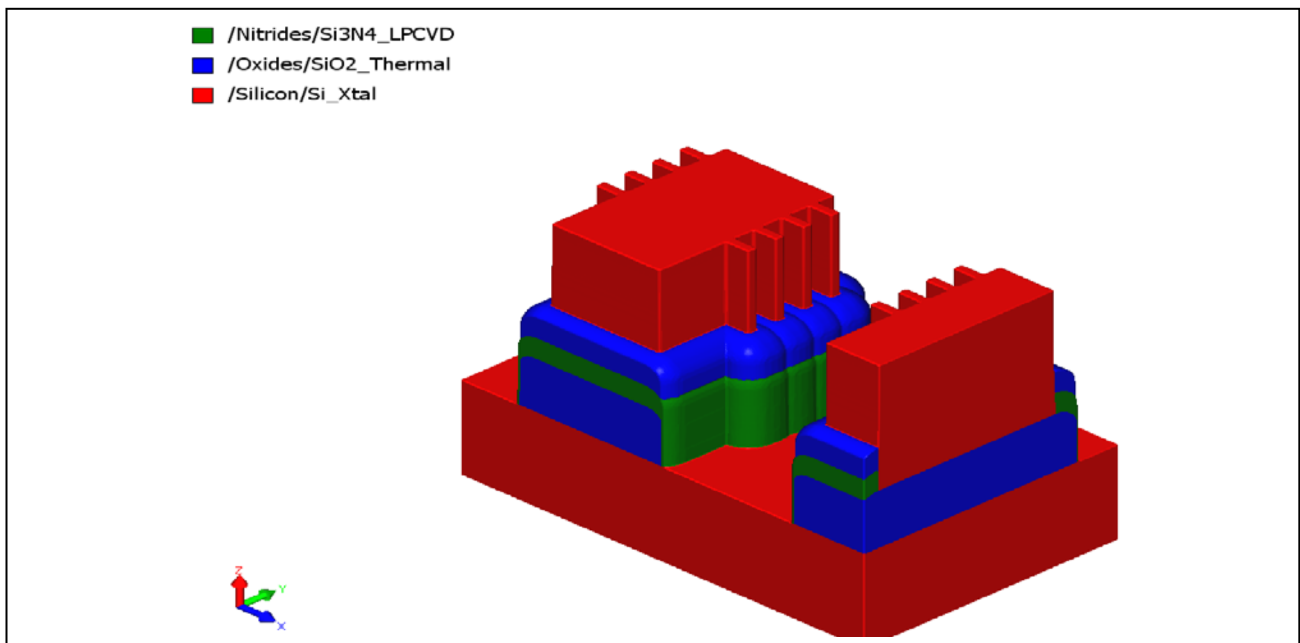
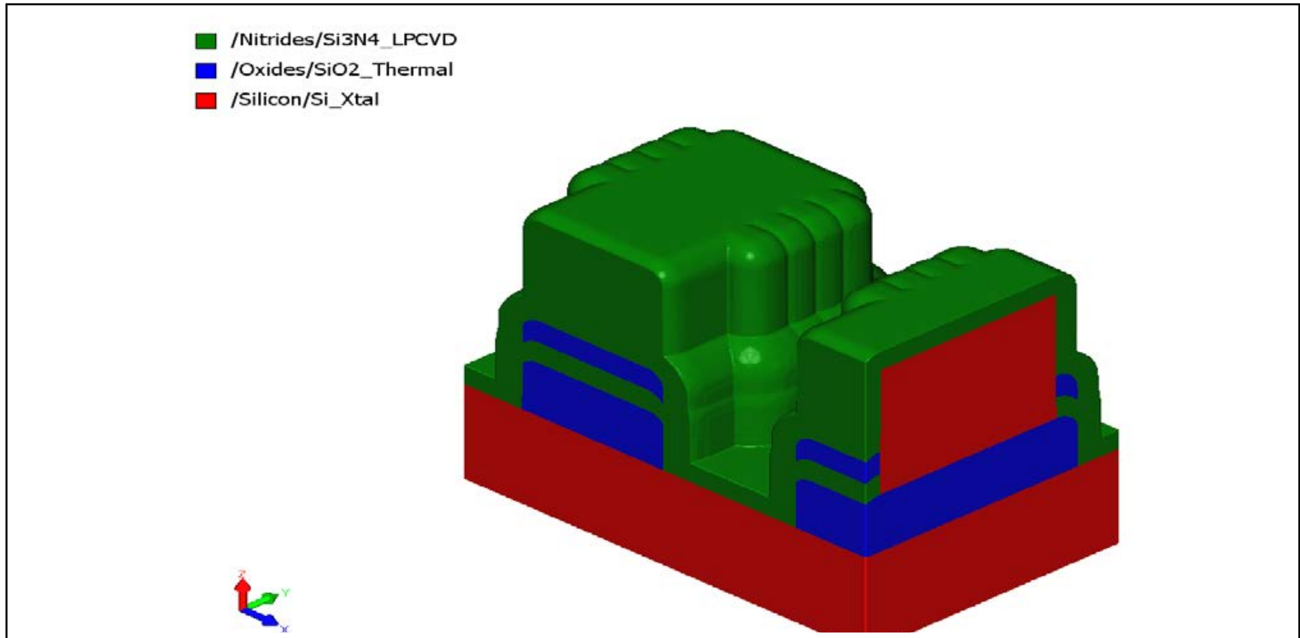


4.2.2.6. Straight Etch



4.2.2.7. Conformal Deposit



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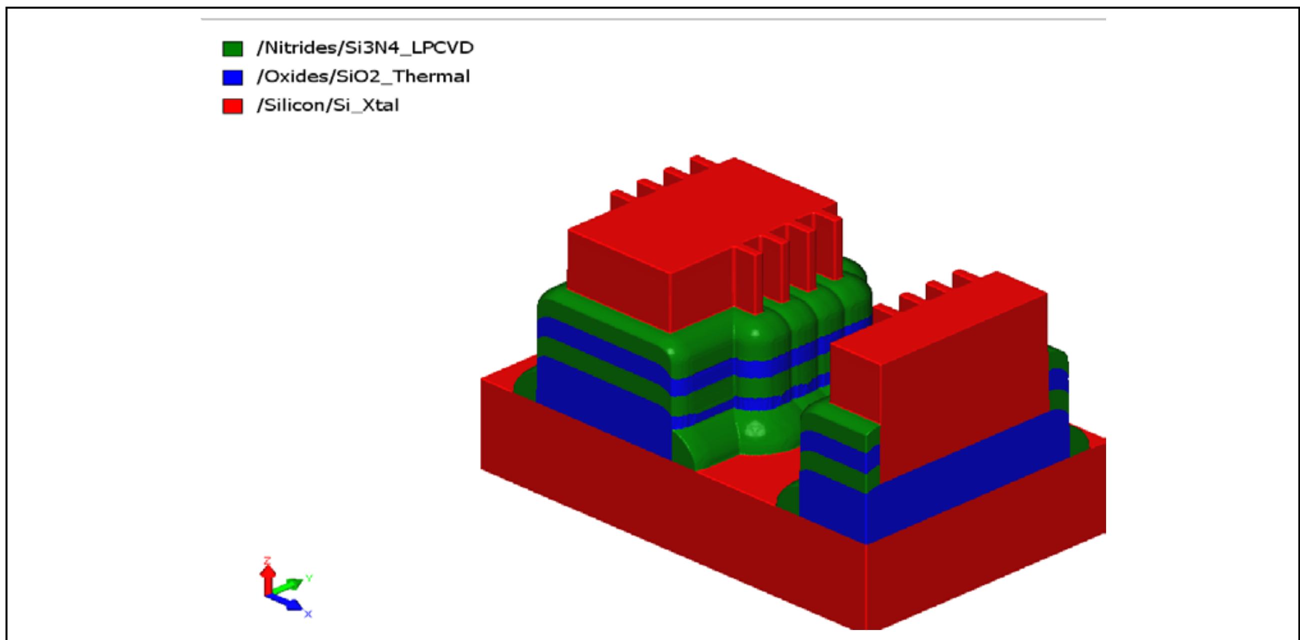

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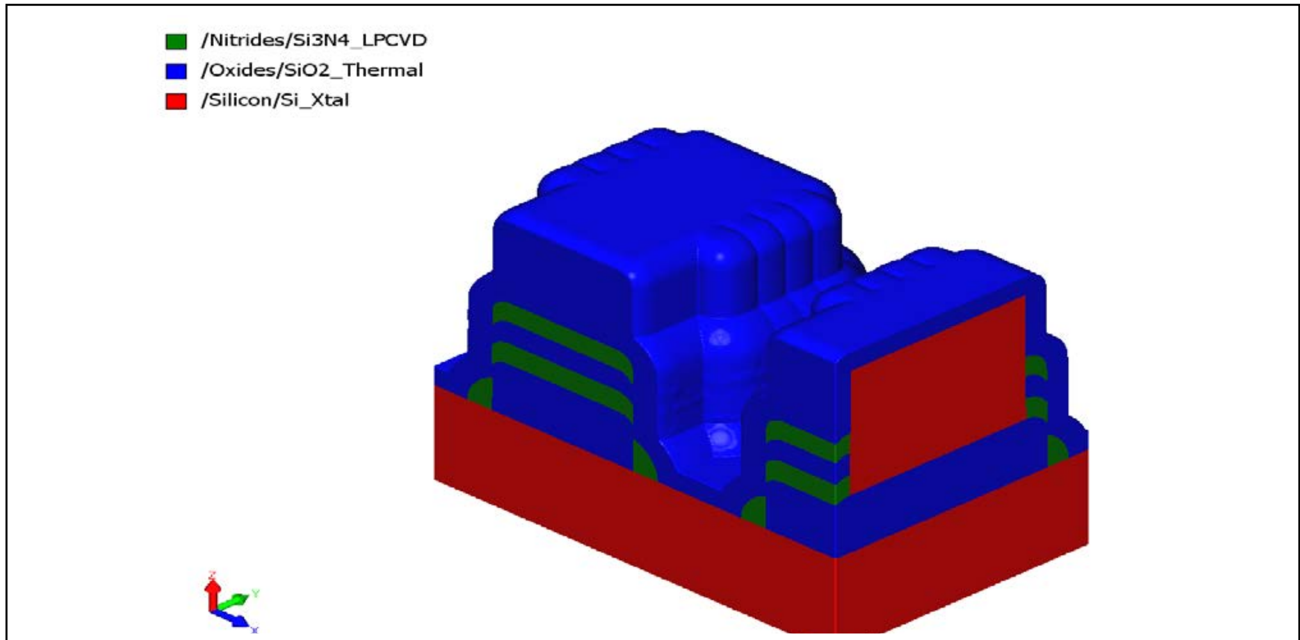

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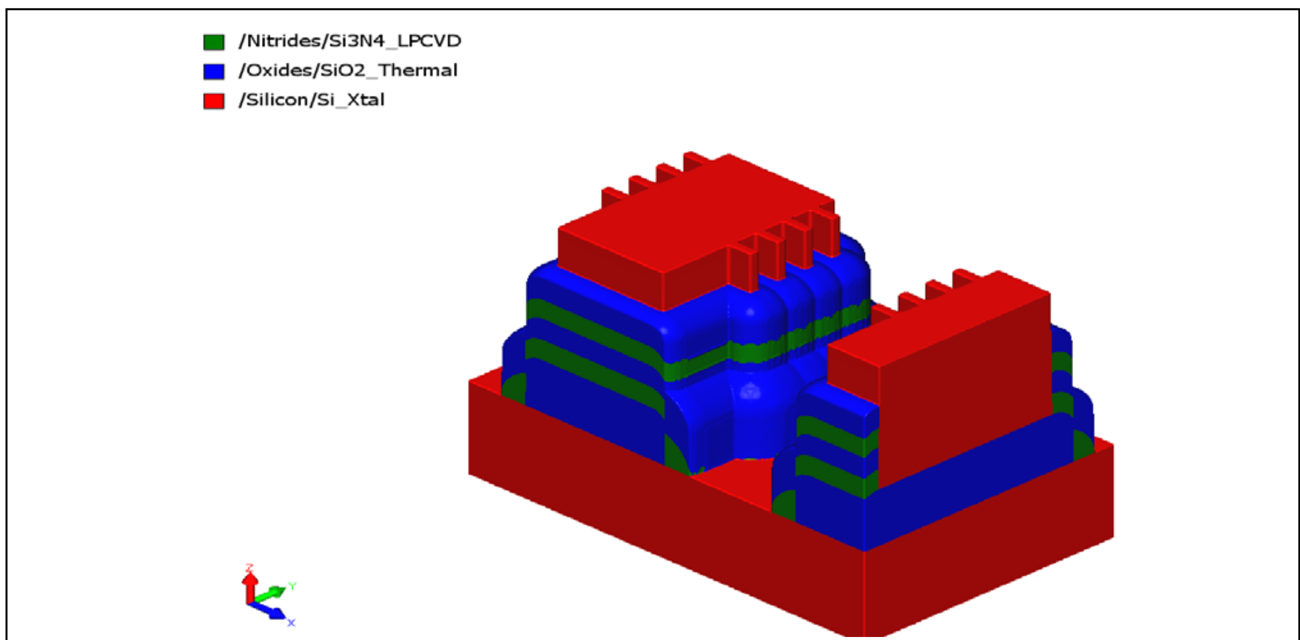
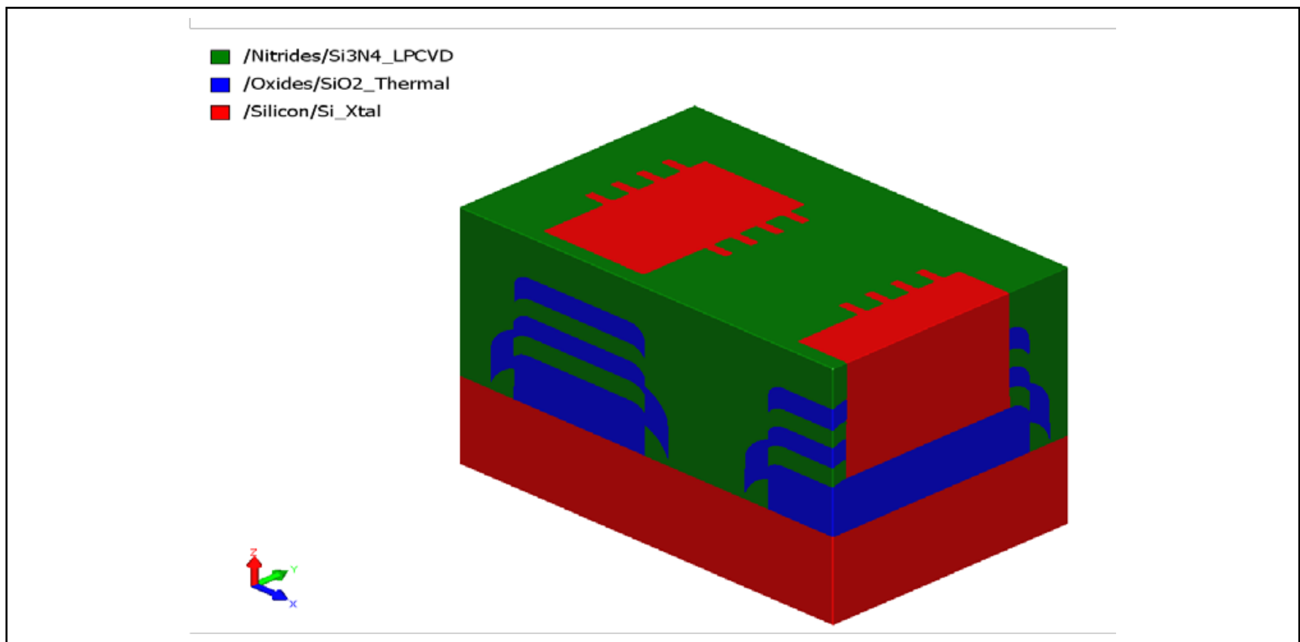
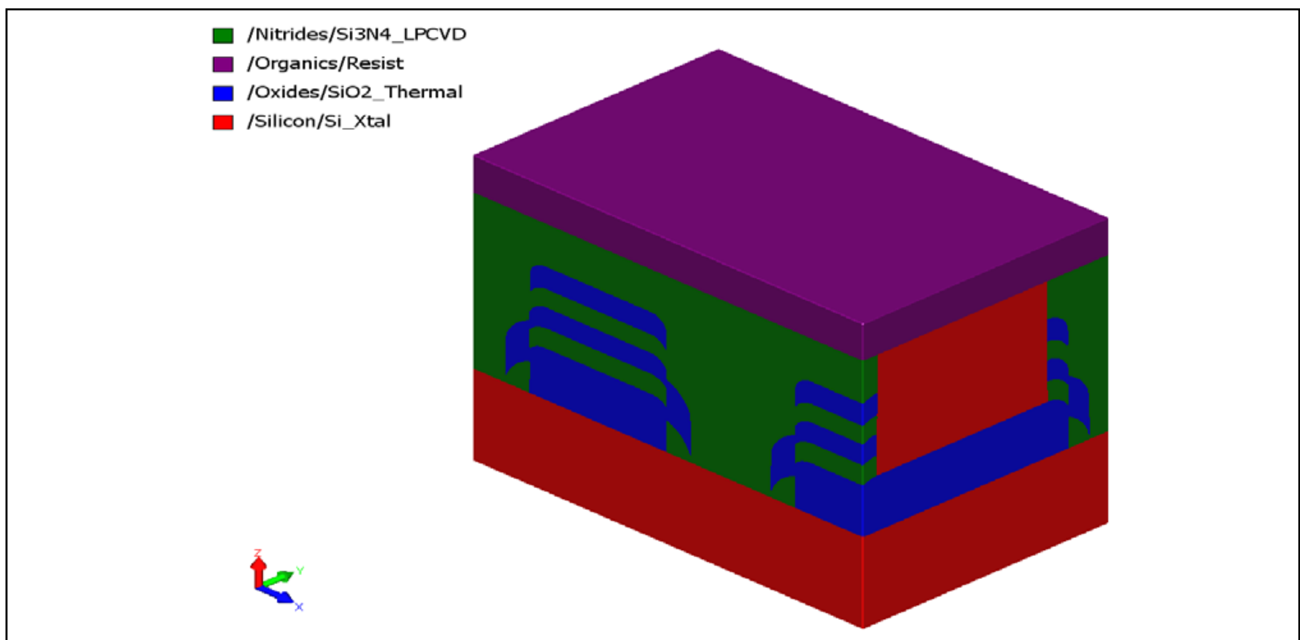


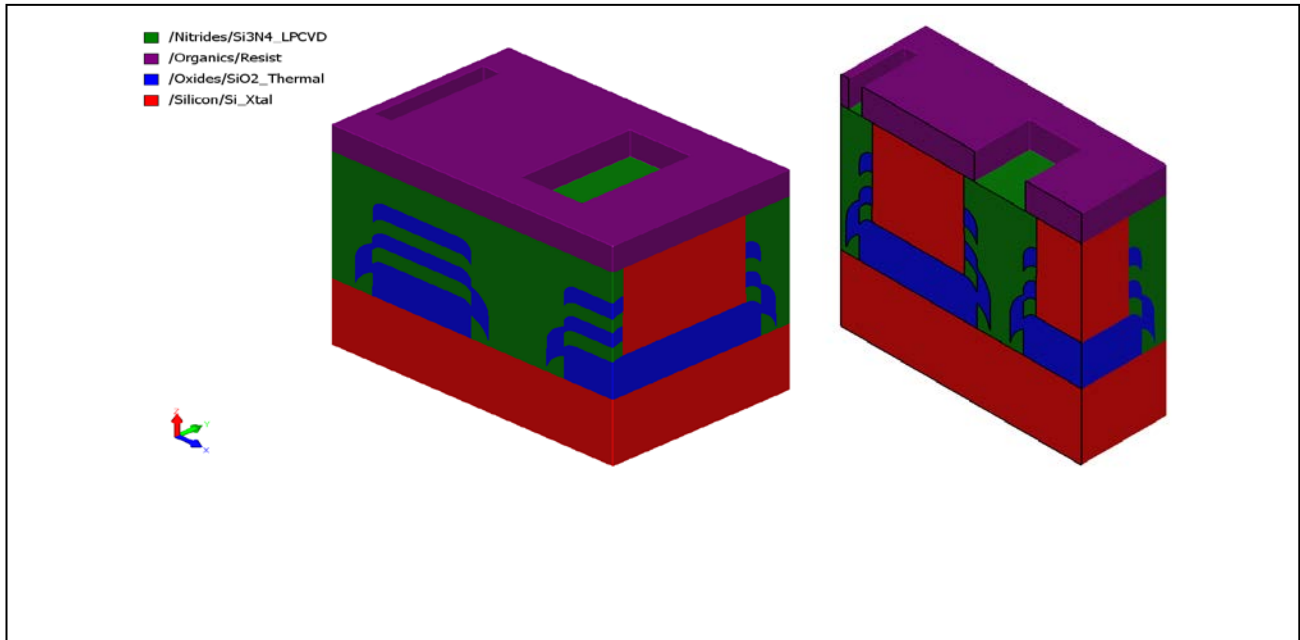
4.2.2.11. Planar Deposit



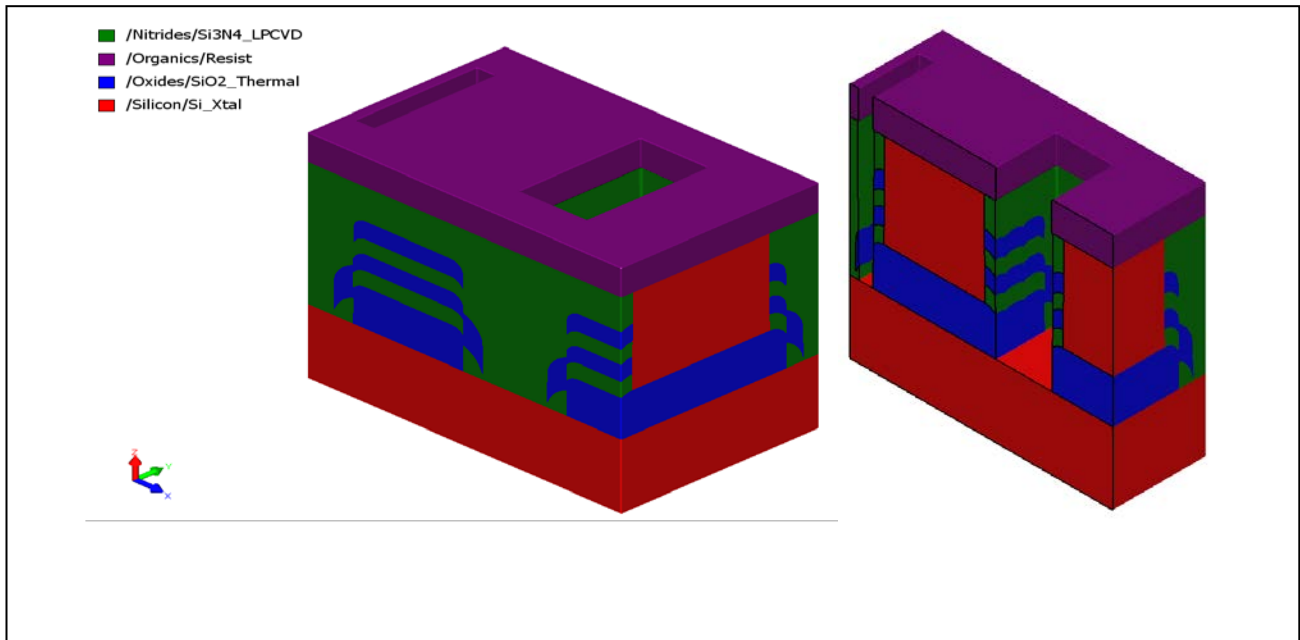
4.2.2.12. Planar Deposit



4.2.2.13. Expose Material



4.2.2.14. Basic Etch



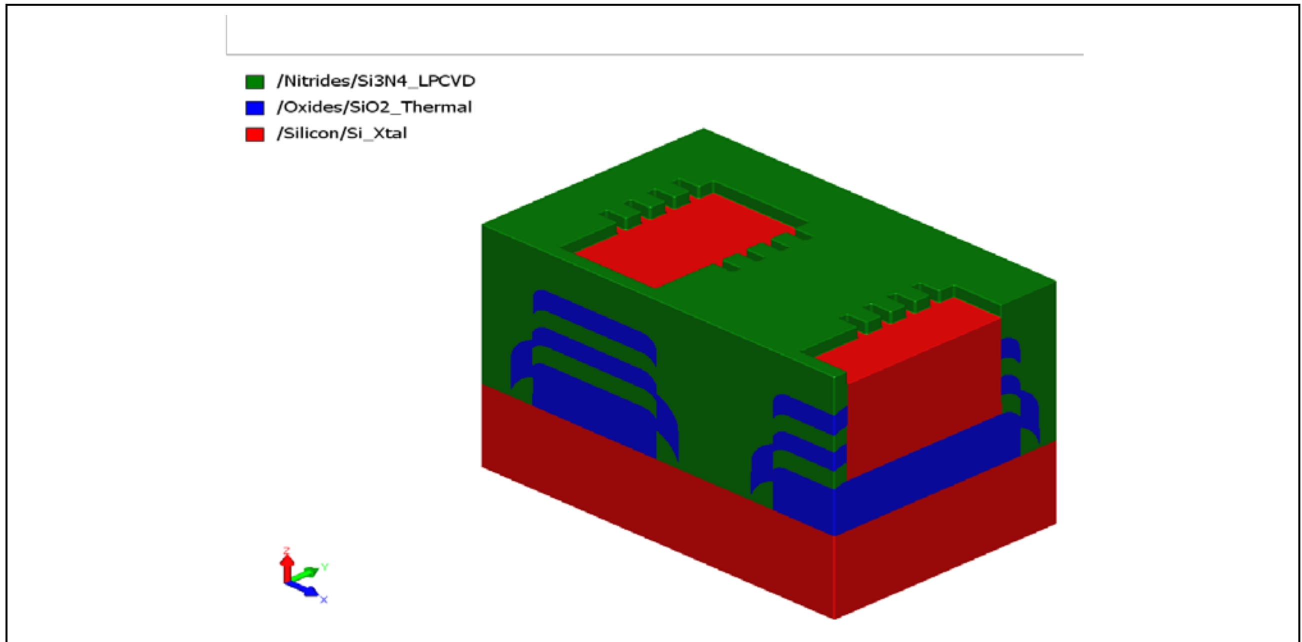
4.2.2.15. Remove Materials

/Nitrides/Si3N4_LPCVD
/Oxides/SiO2_Thermal
/Silicon/Si_Xtal

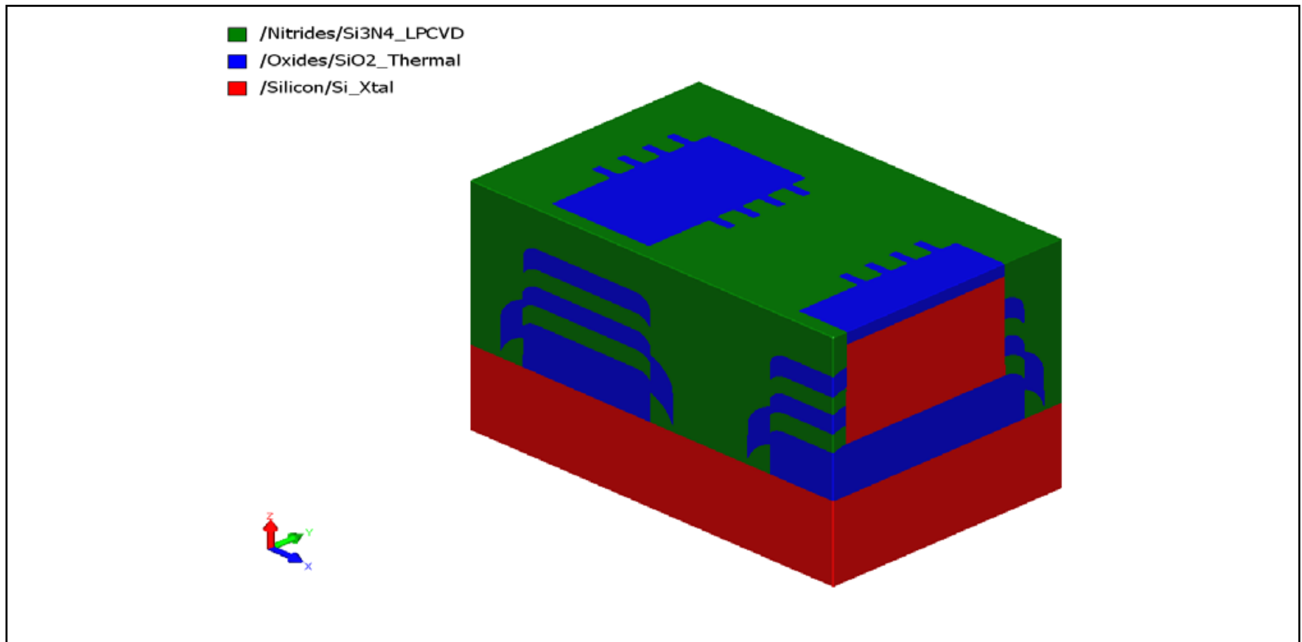
4.2.2.16. Planar Deposit

/Nitrides/Si3N4_LPCVD
/Oxides/SiO2_Thermal
/Silicon/Si_Xtal

4.2.12. Basic Etch

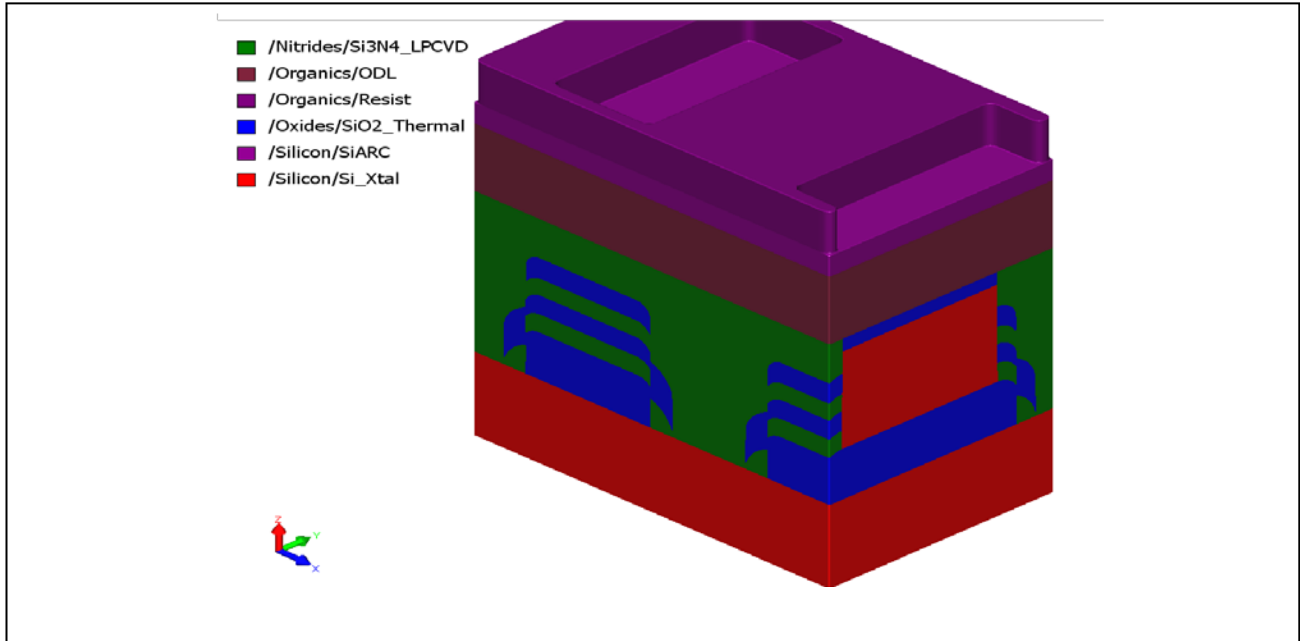


4.2.13. Planar Deposit

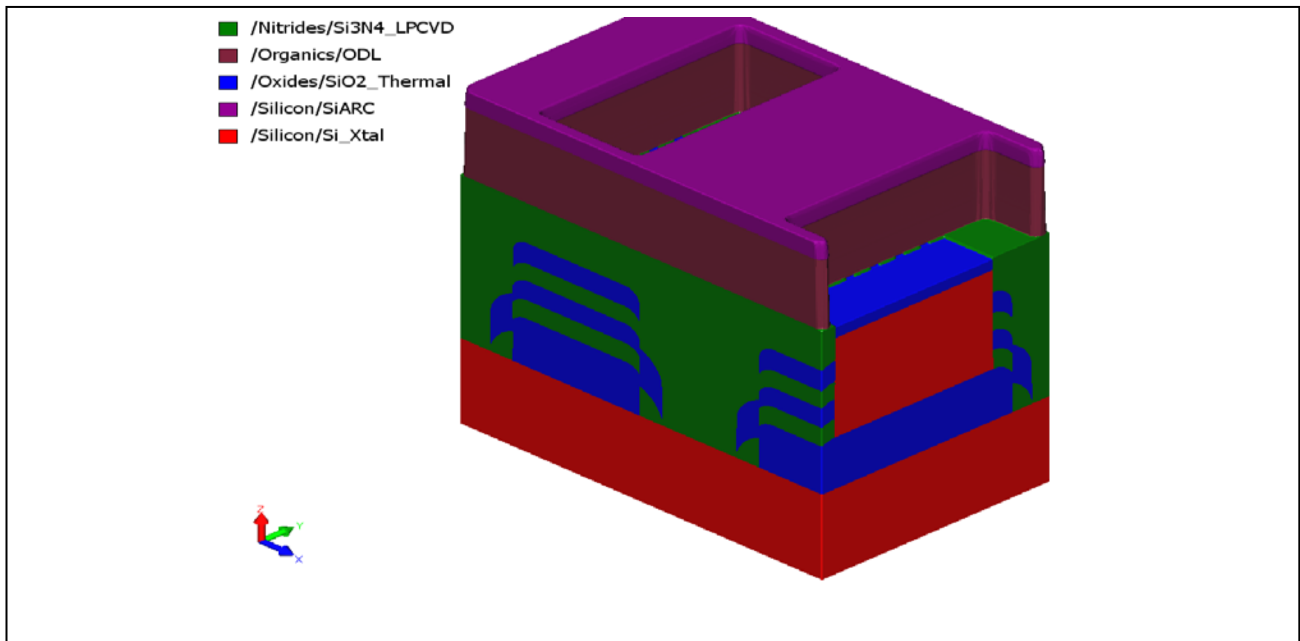


Dummy Gate module

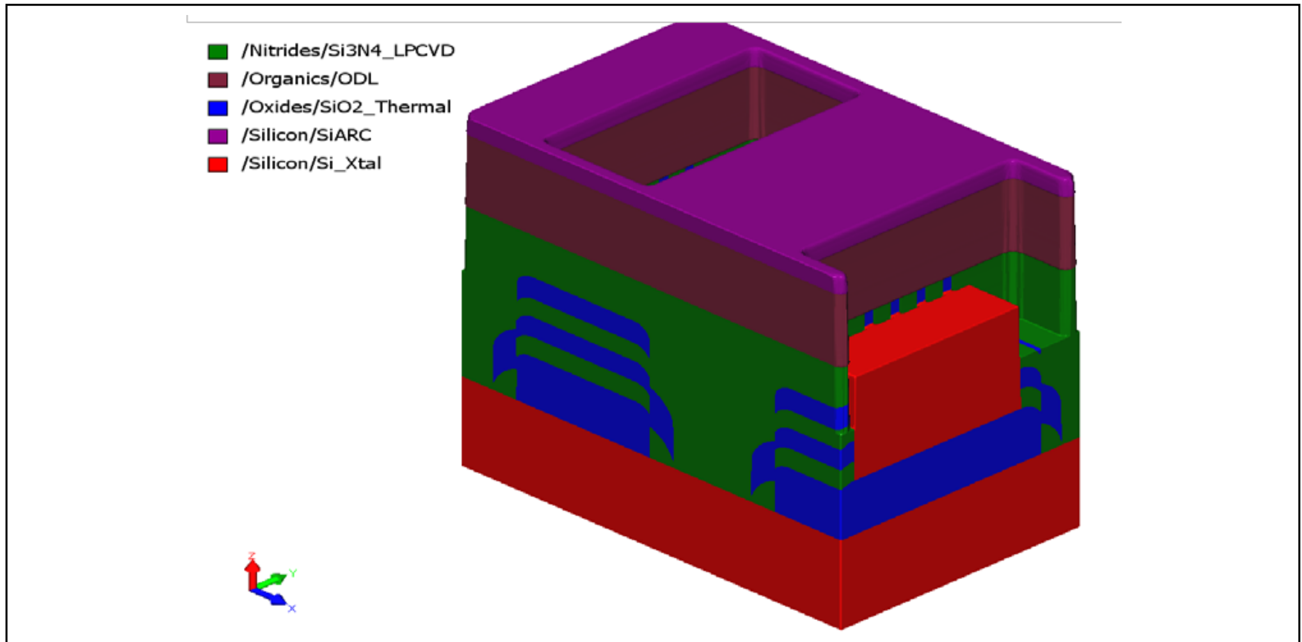
4.3.4. LTH Gate



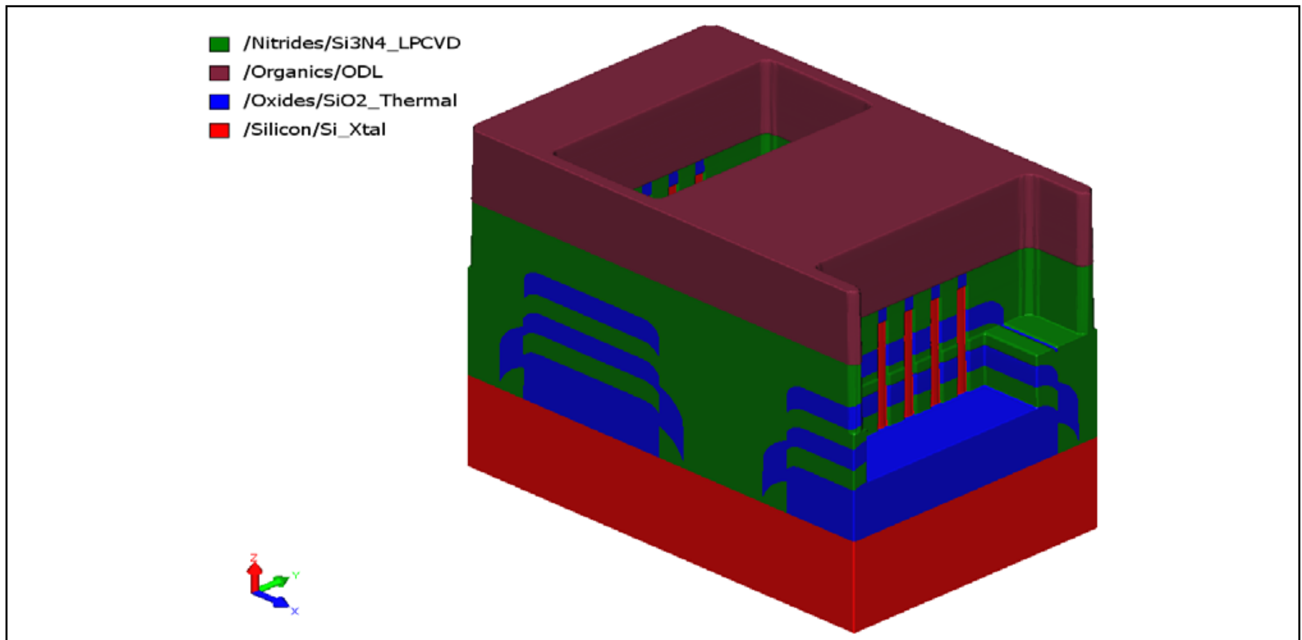
4.3.9.2. RIE ODL



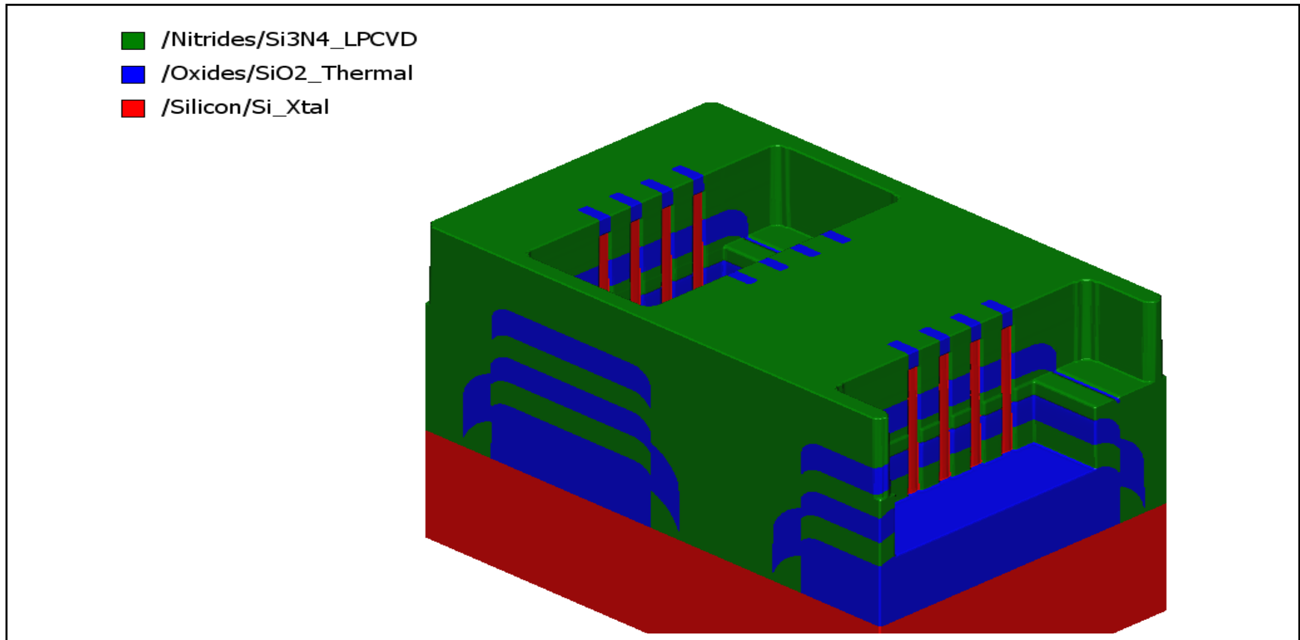
4.3.9.4. RIE Oxide BT



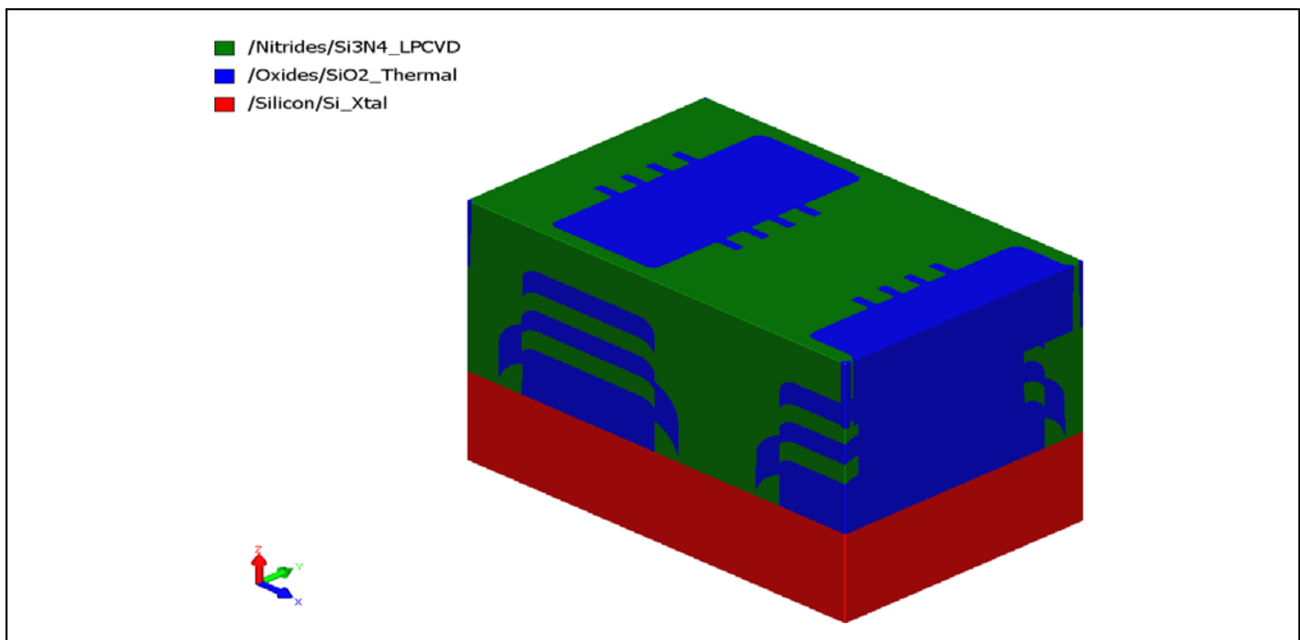
4.3.9.5. RIE Oxide BT



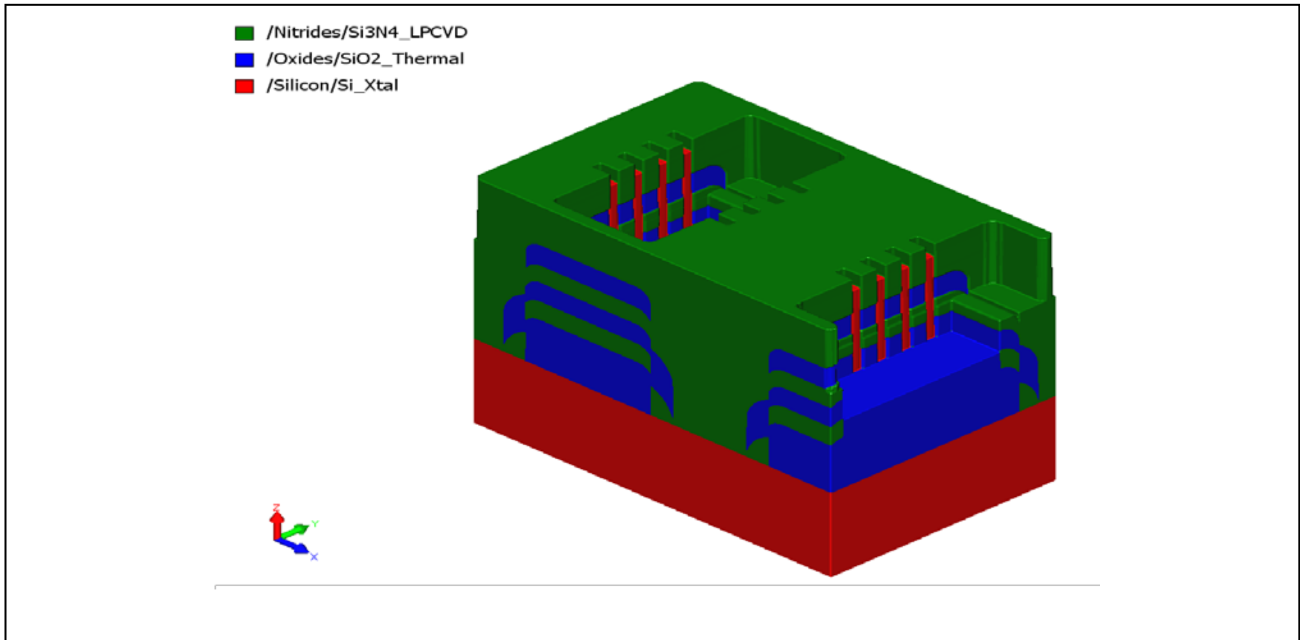
4.3.9.6. Remove Materials



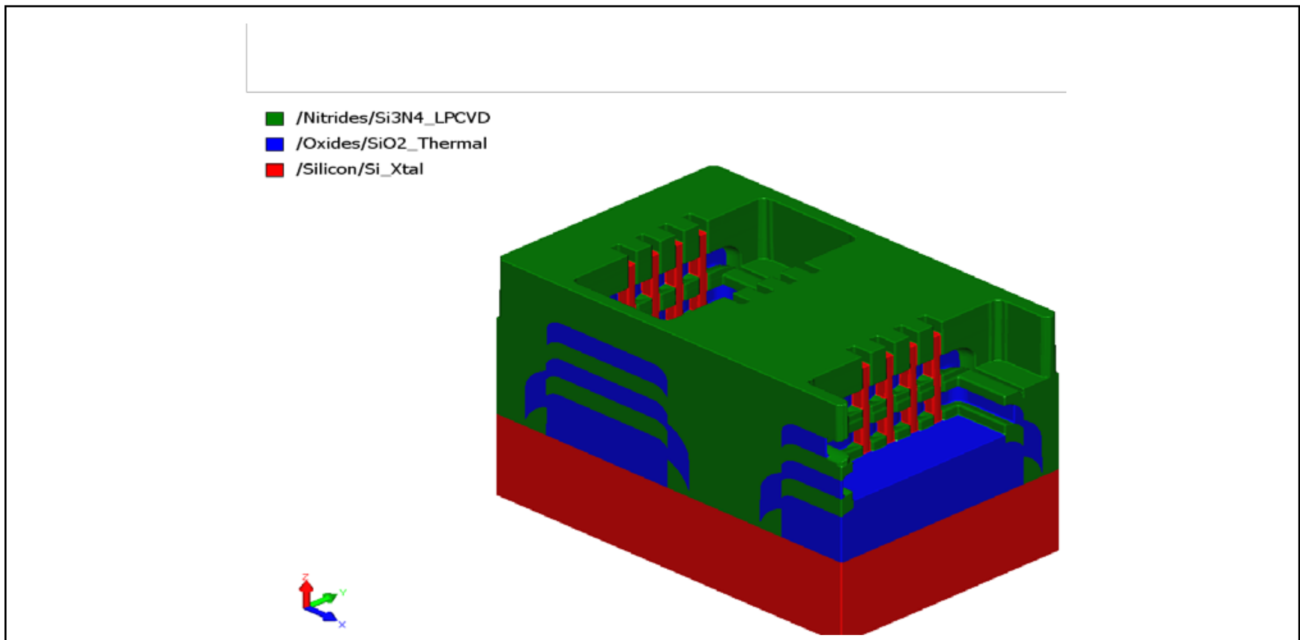
4.3.9.7. Planar Deposit



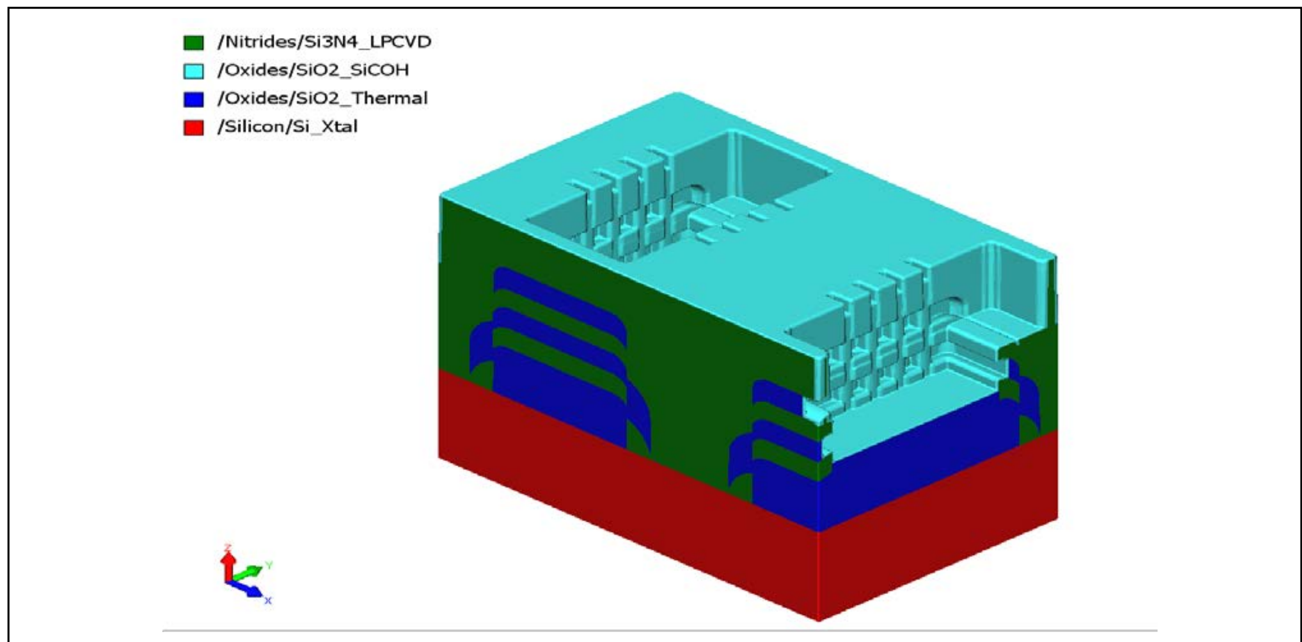
4.3.9.8. Oxide recess



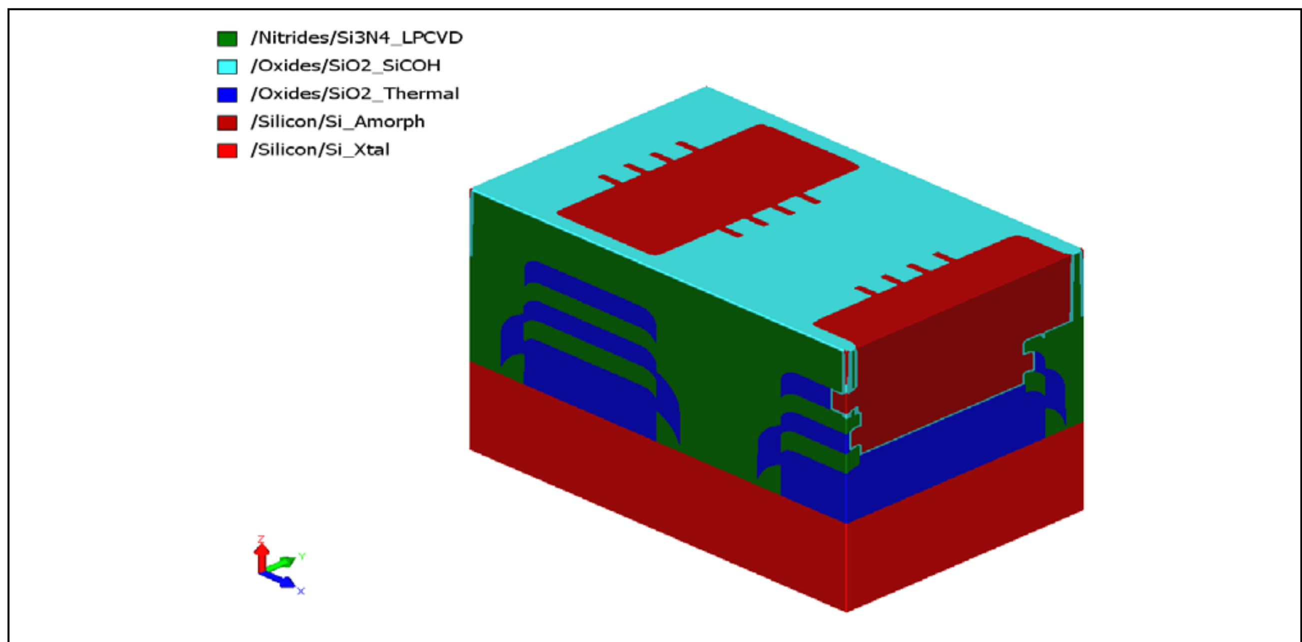
4.3.9.9. Oxide recess



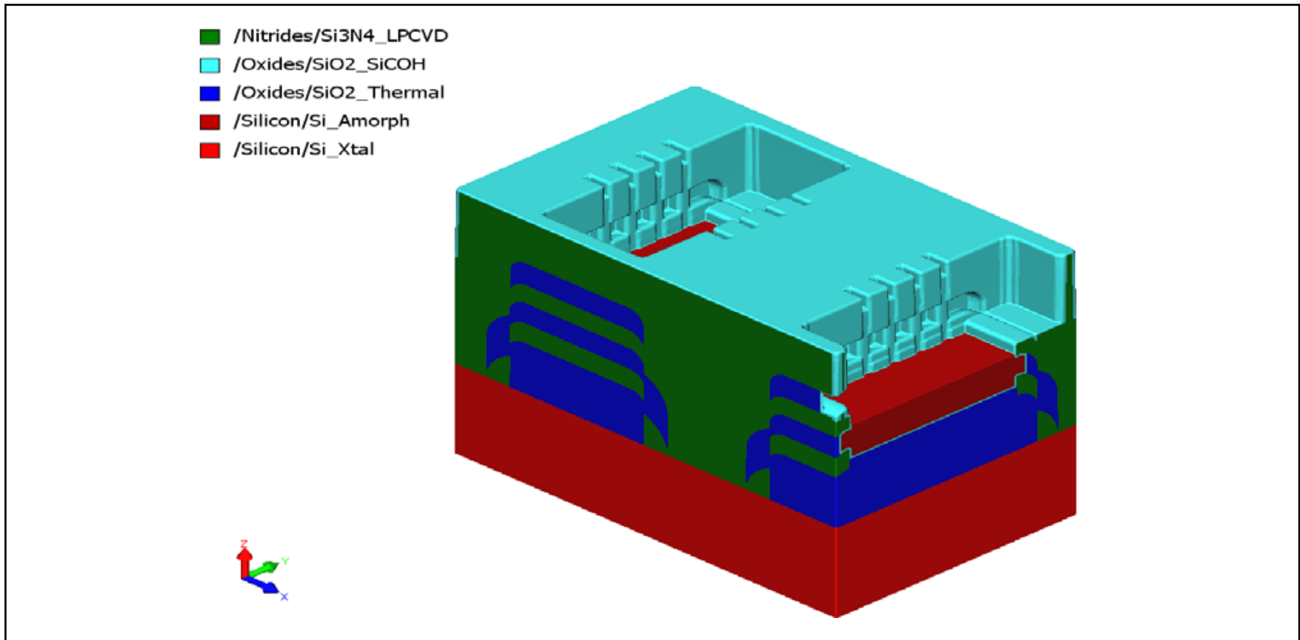
4.3.9.13. Conformal Deposit



4.3.9.14. Planar Deposit



4.3.9.15. Basic Etch



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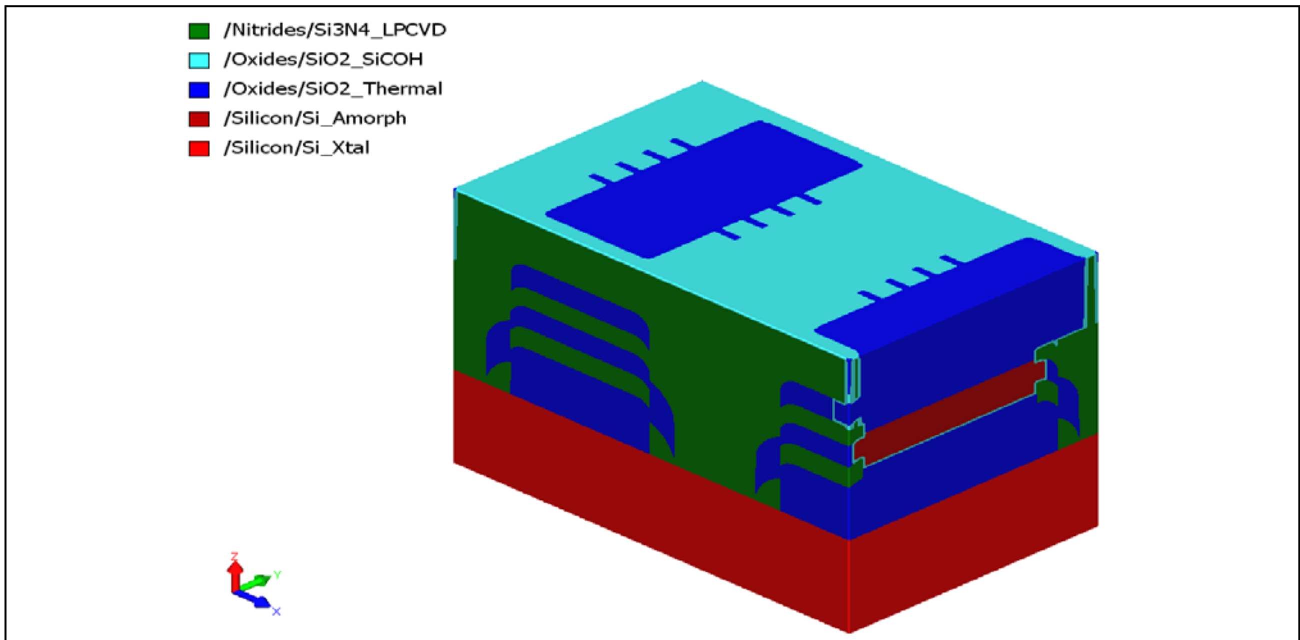
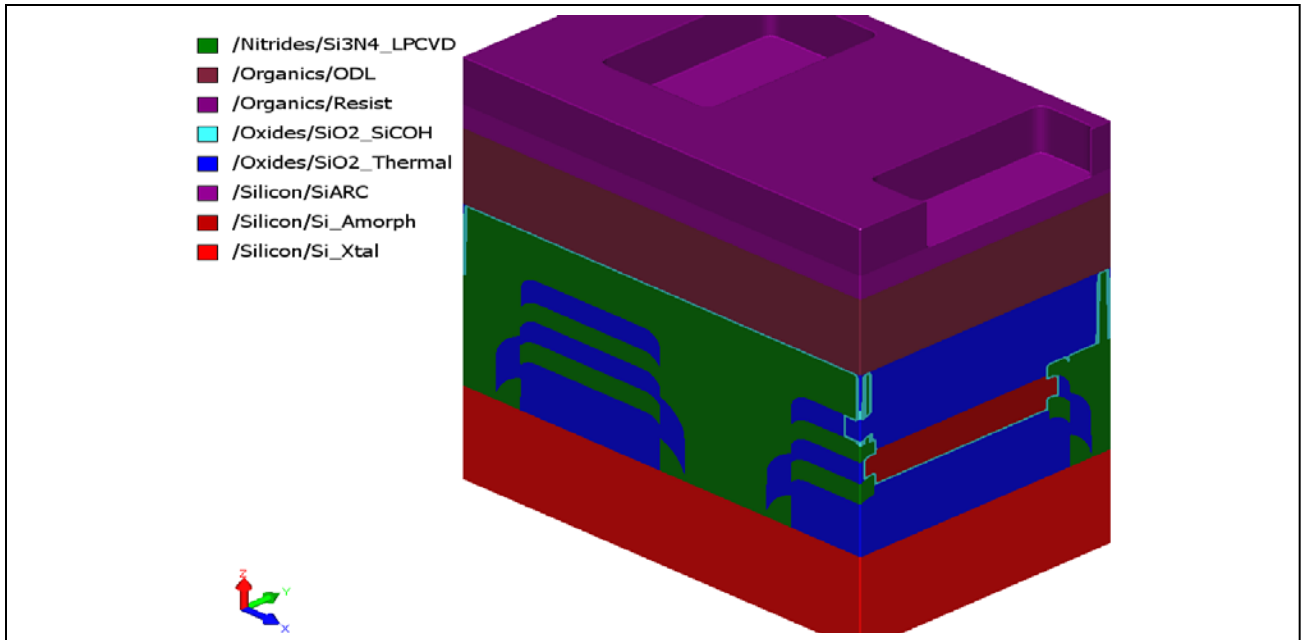
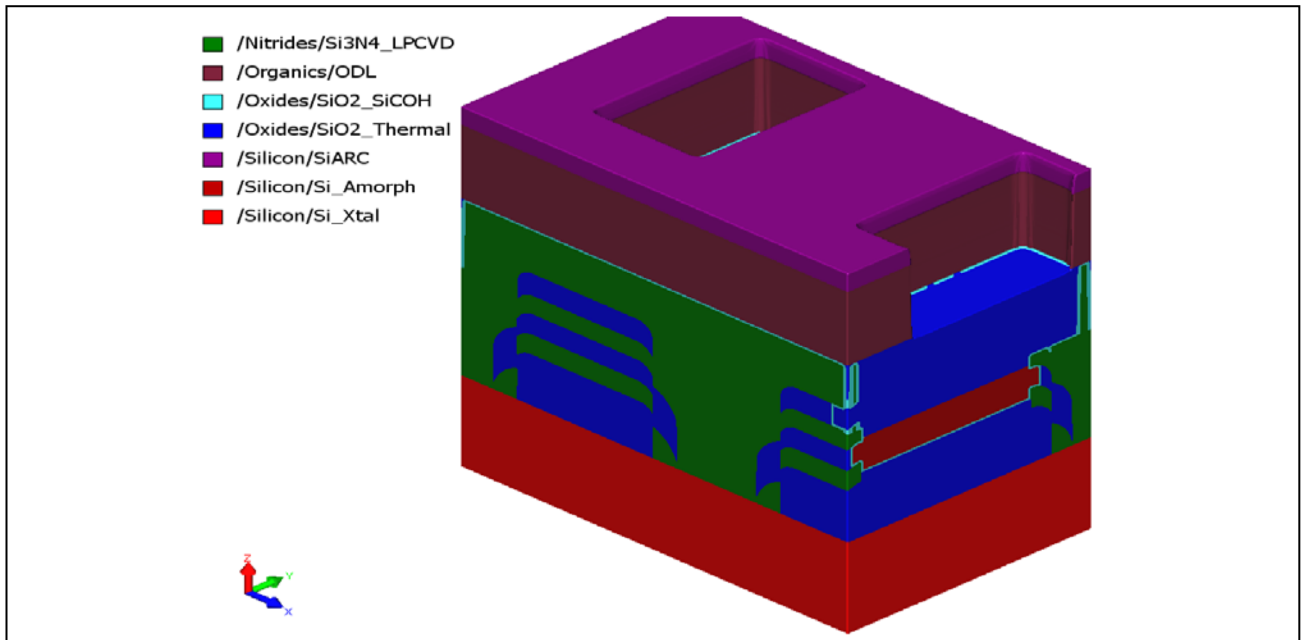


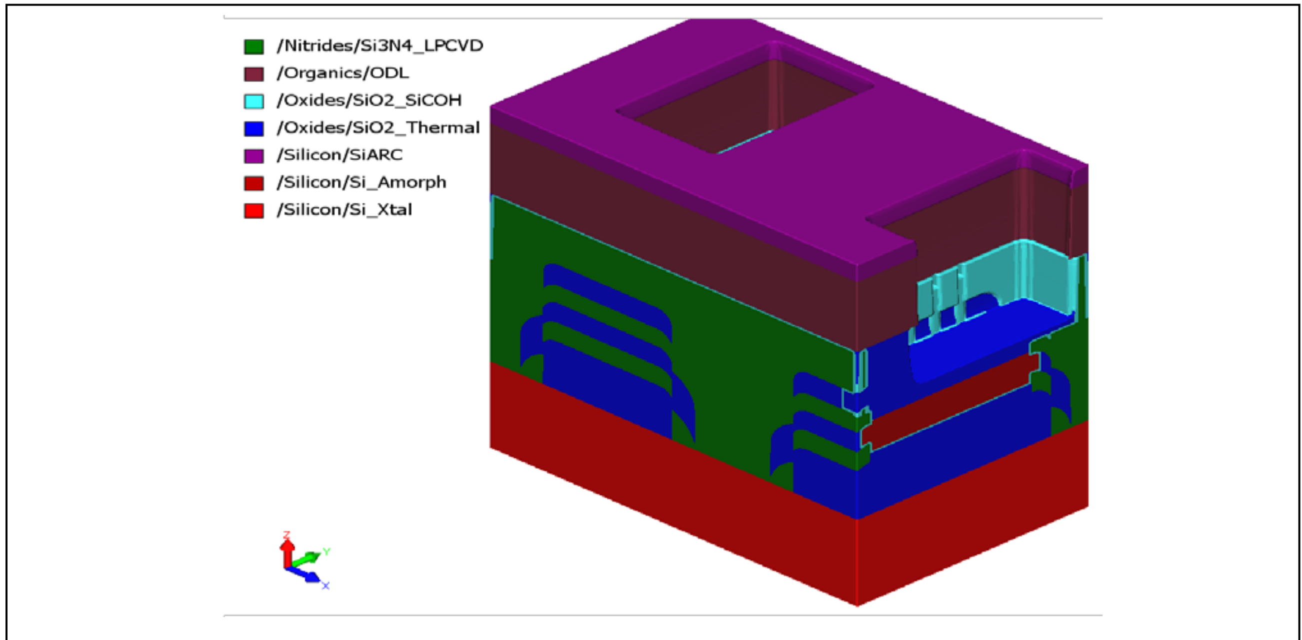
4.3.9.20. LTH Gate



4.3.9.22. RIE ODL



4.3.9.23. Basic Etch



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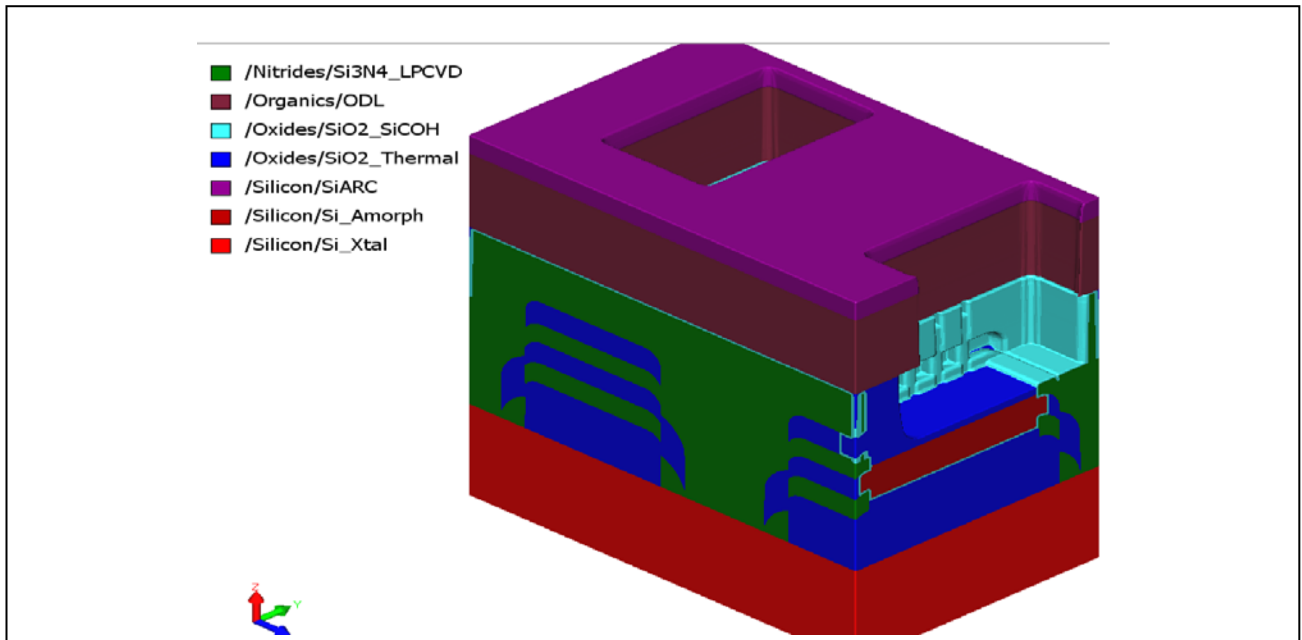
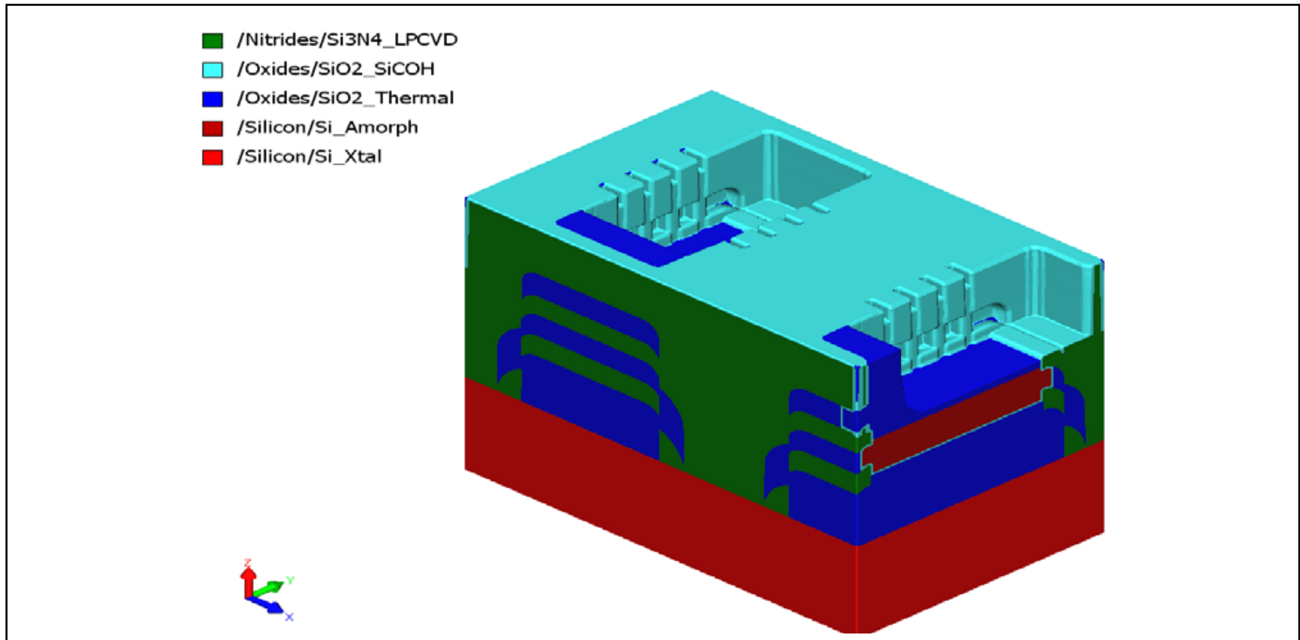


4.3.9.25. Remove Materials



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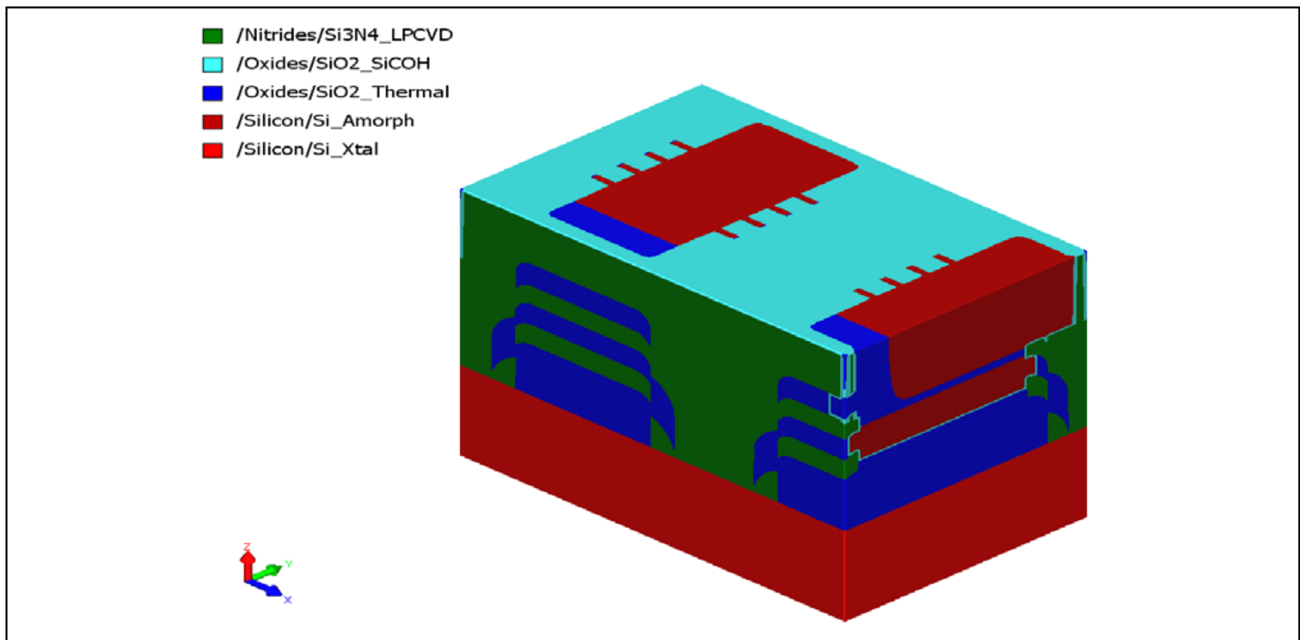

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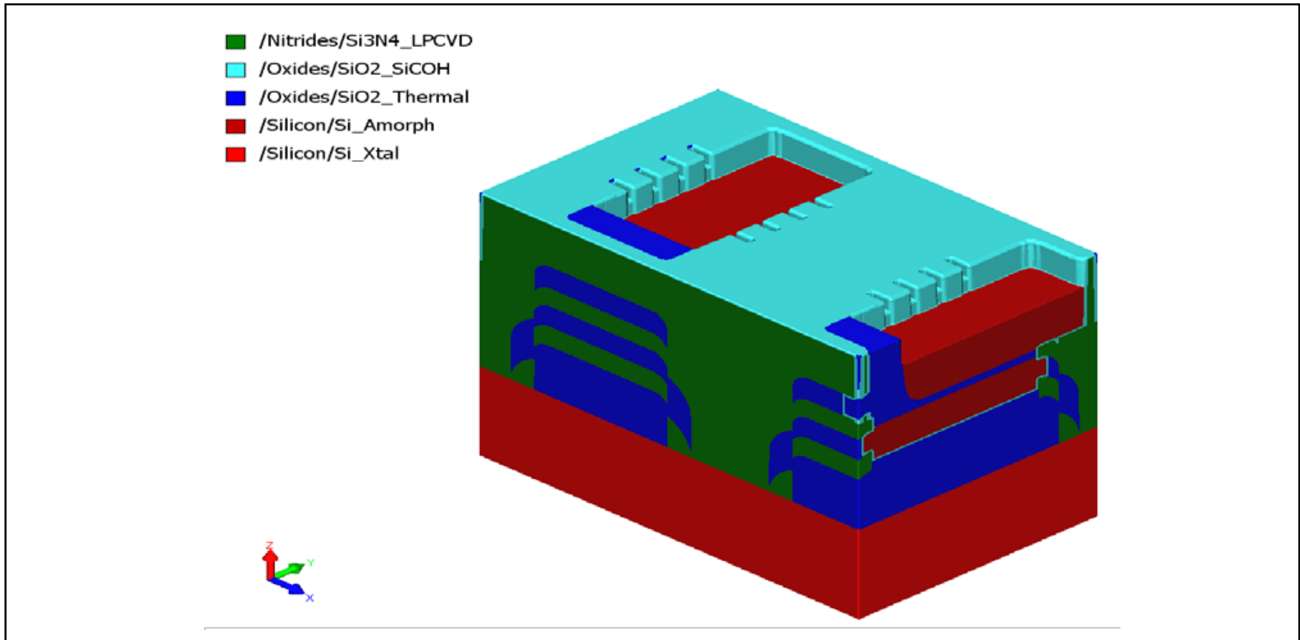

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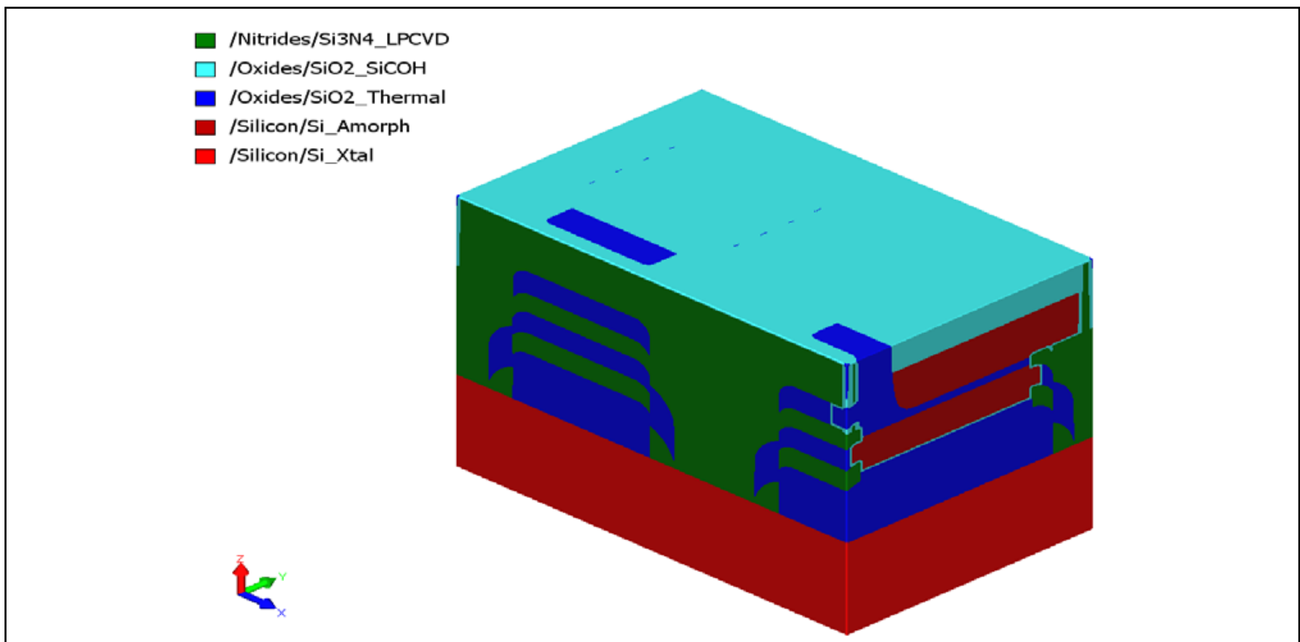
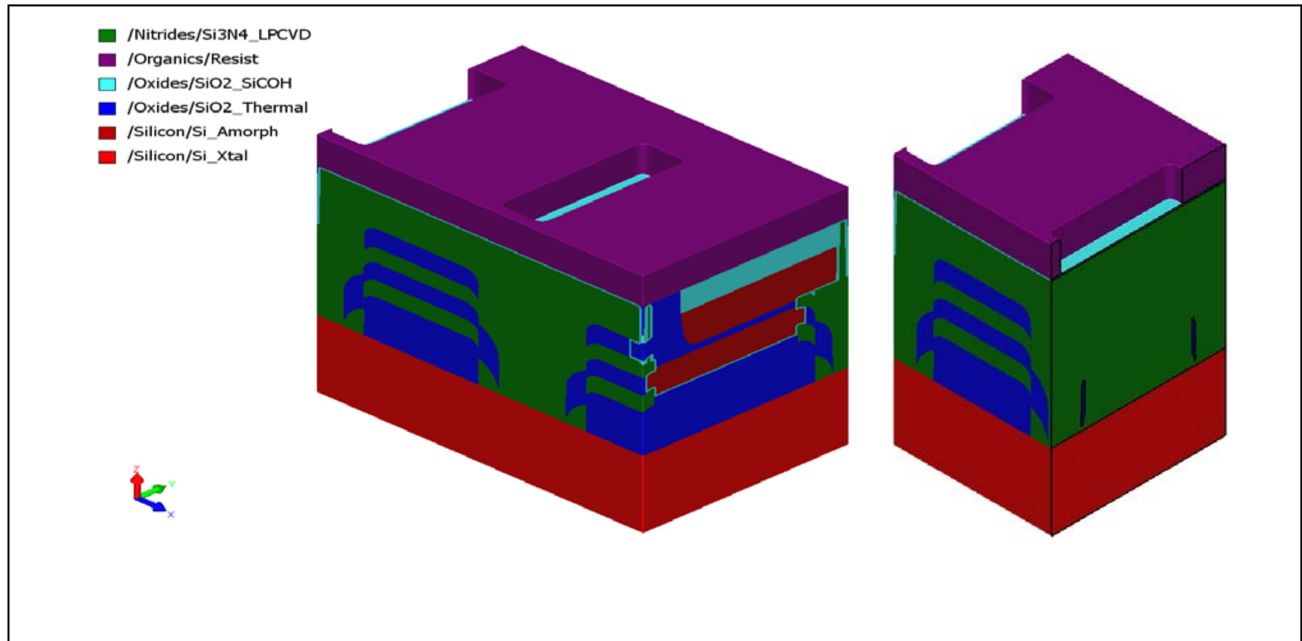


SD EPI

4.4.3. Expose Material



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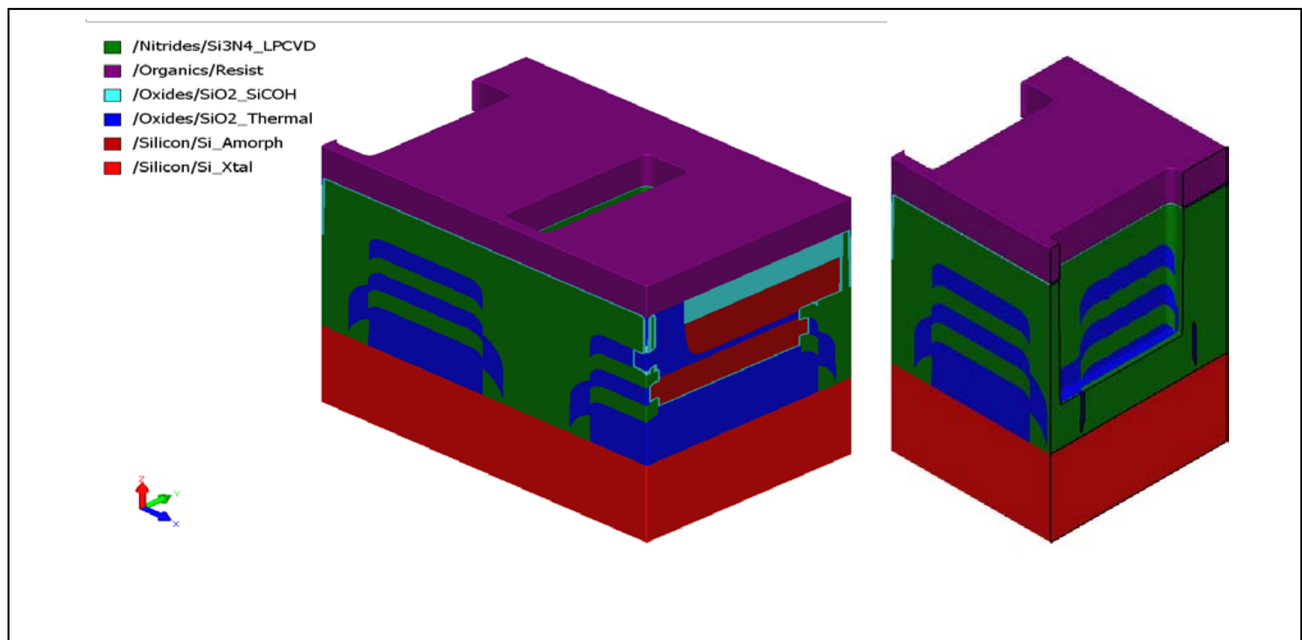

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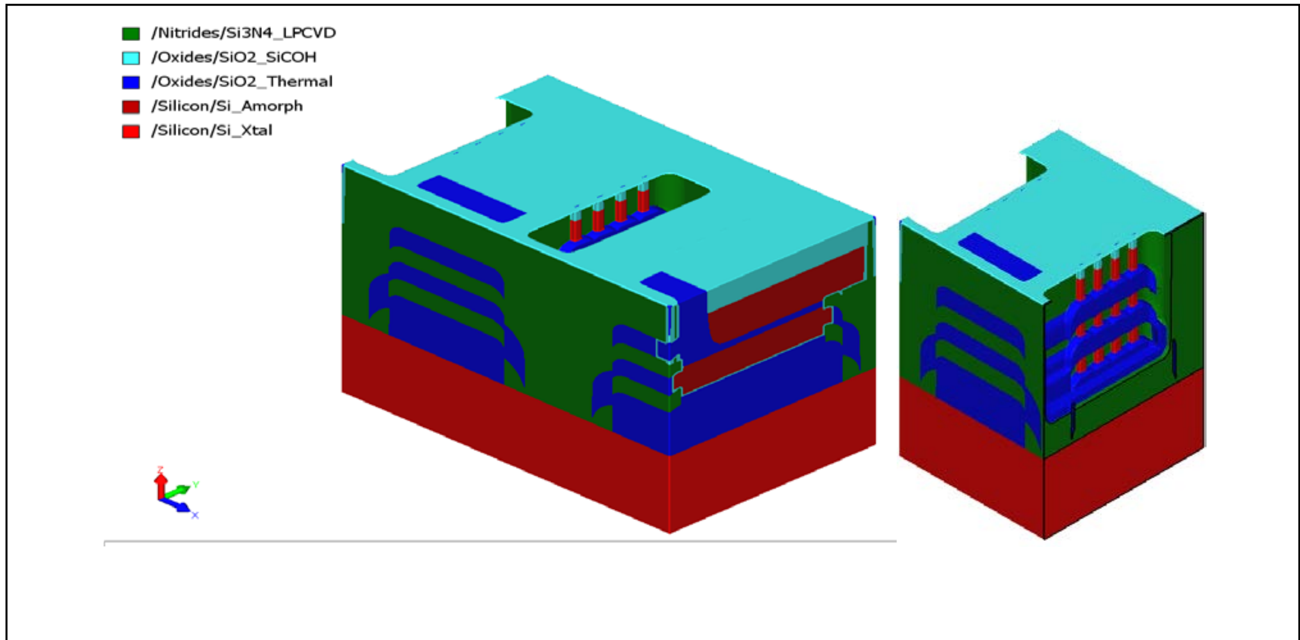
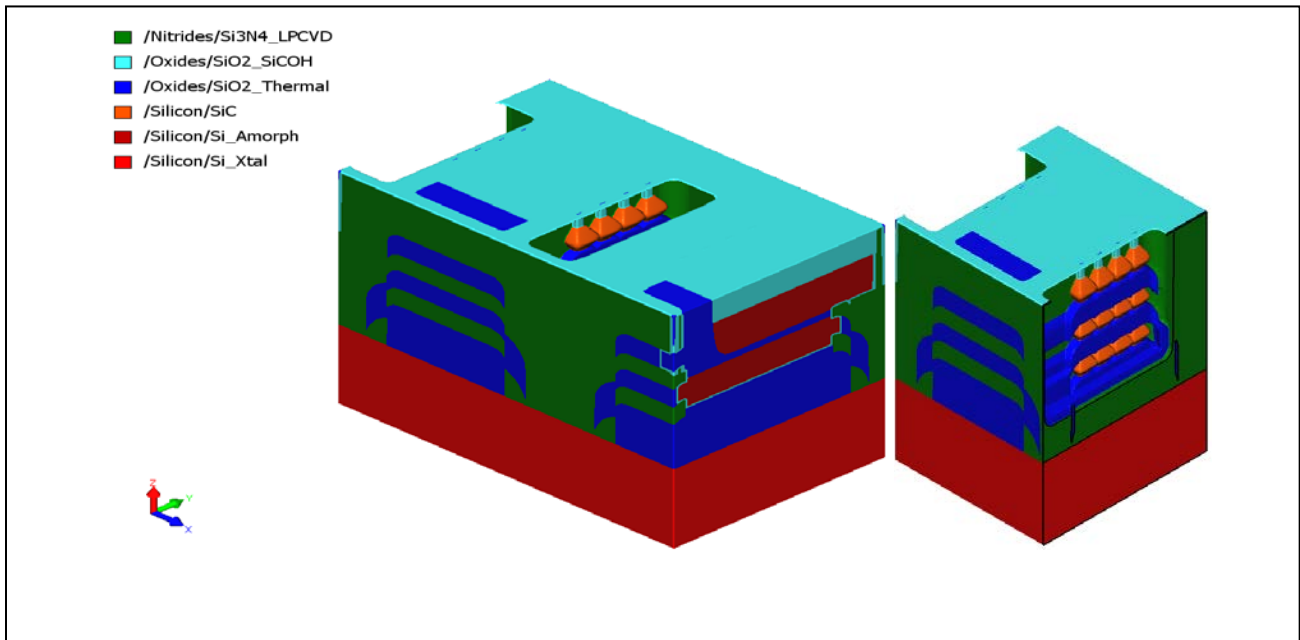


4.4.11. Selective Epitaxy (Requires Advanced Modeling)



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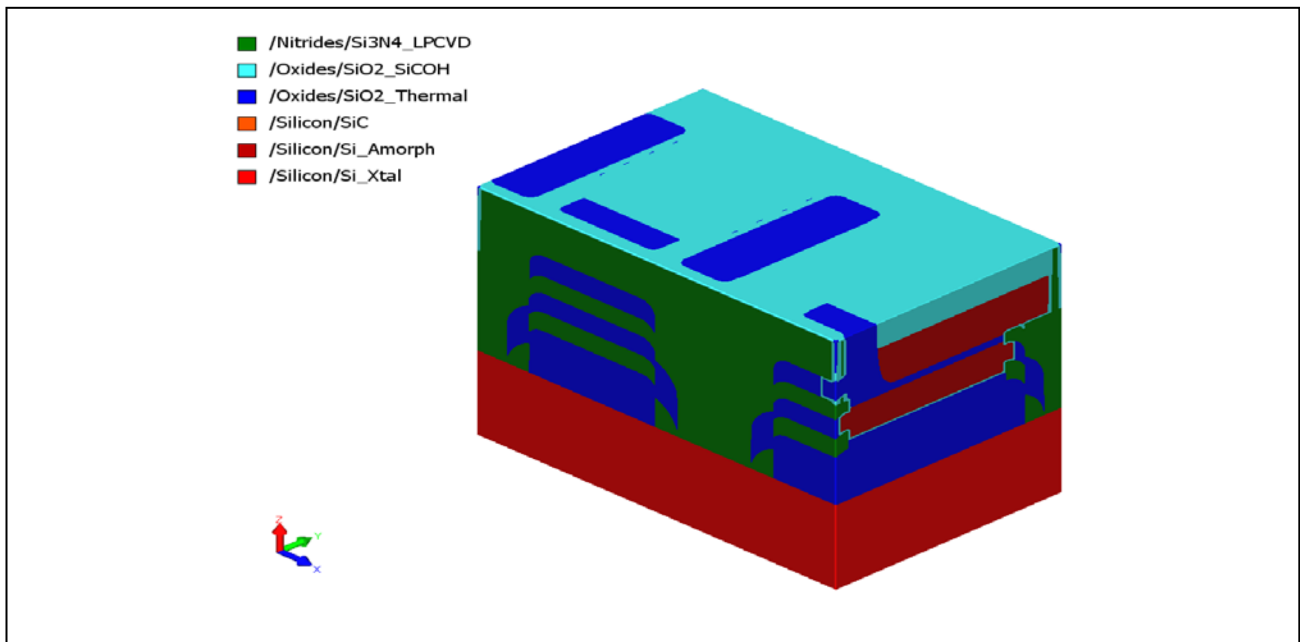
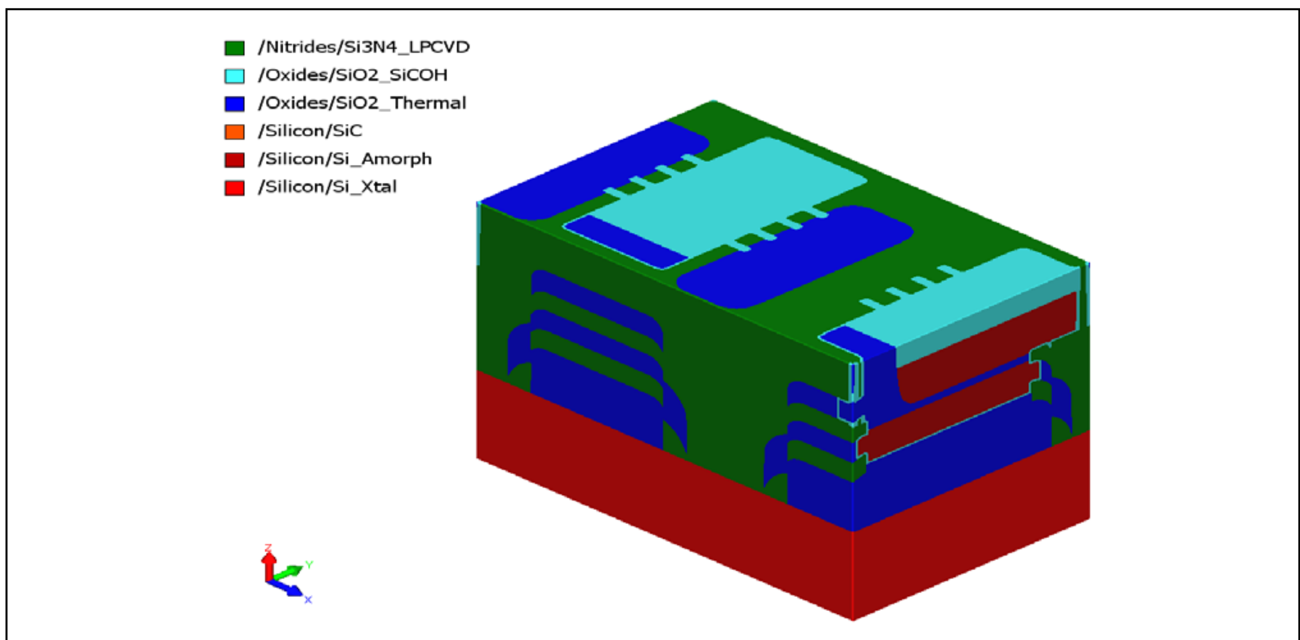
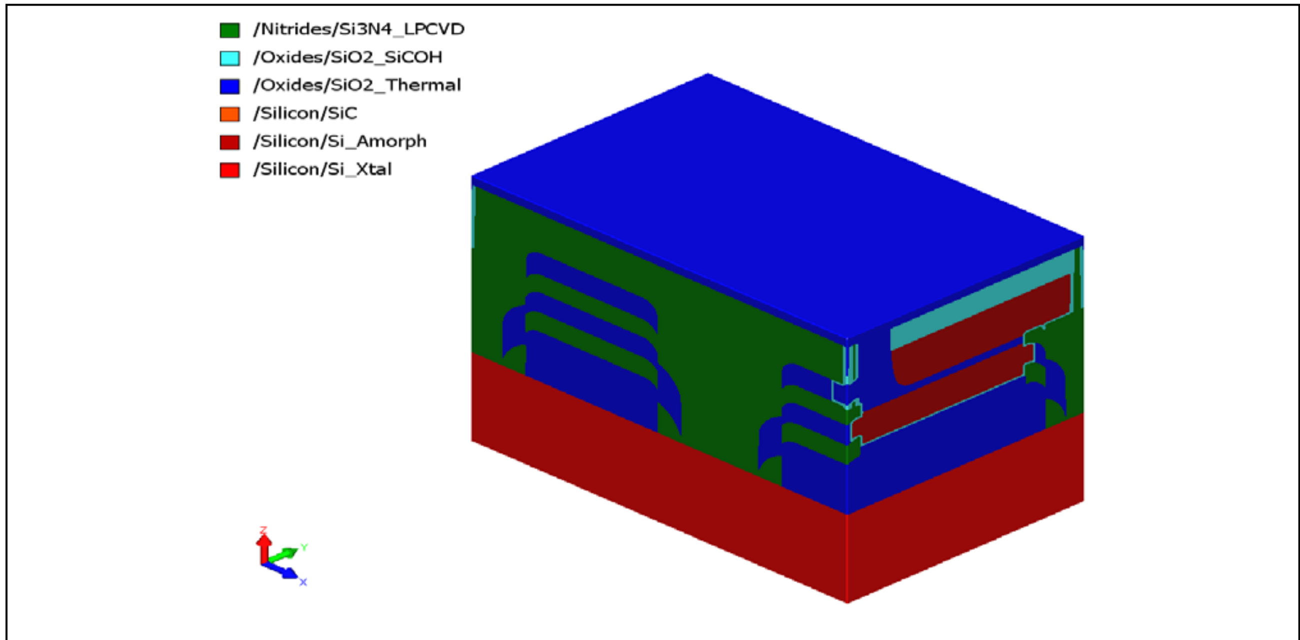


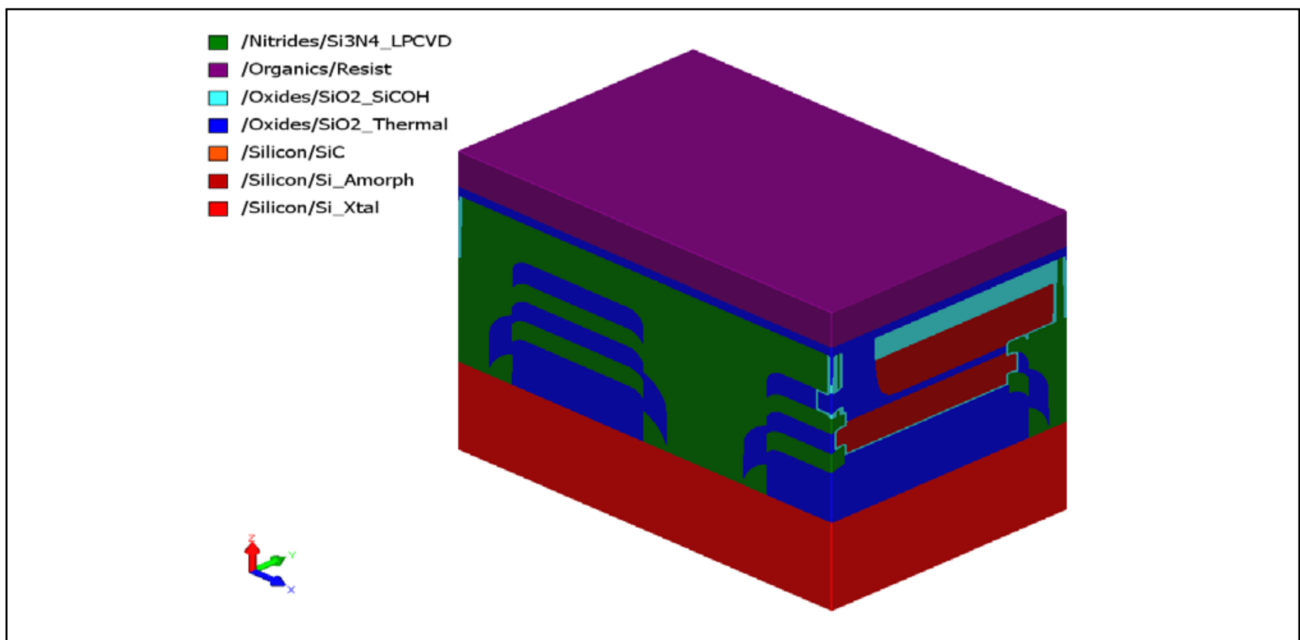
4.4.13. Stopping CMP



4.5.1. Planar Deposit



4.5.2. Straight Deposit



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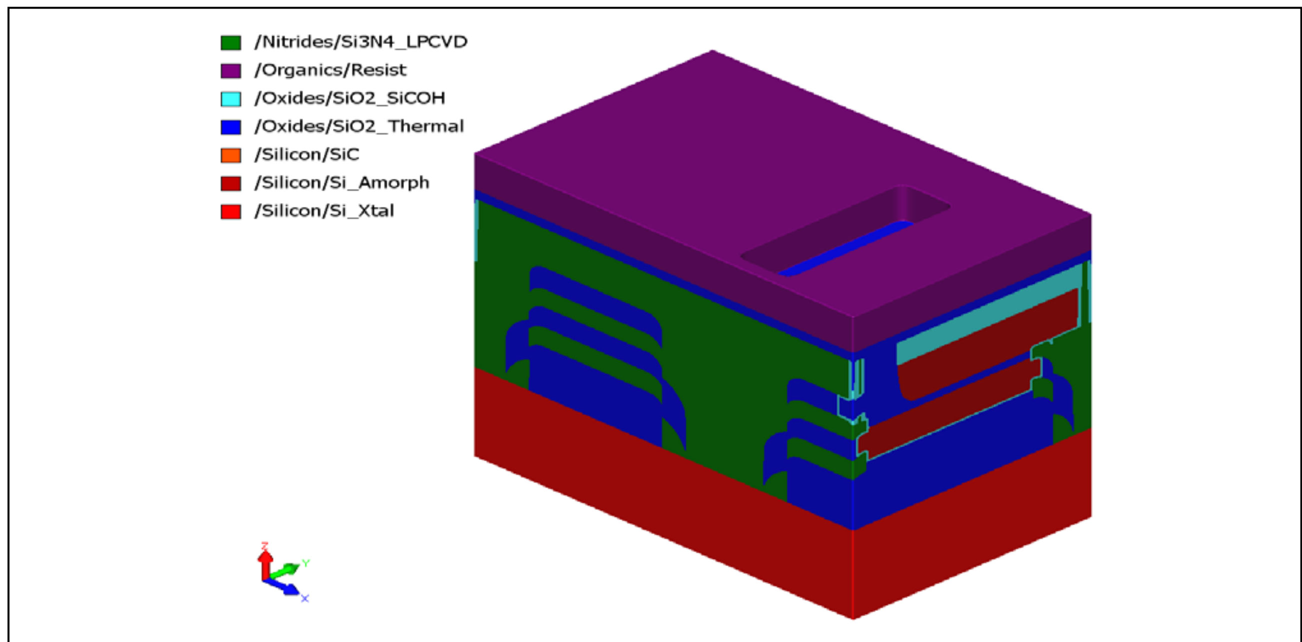
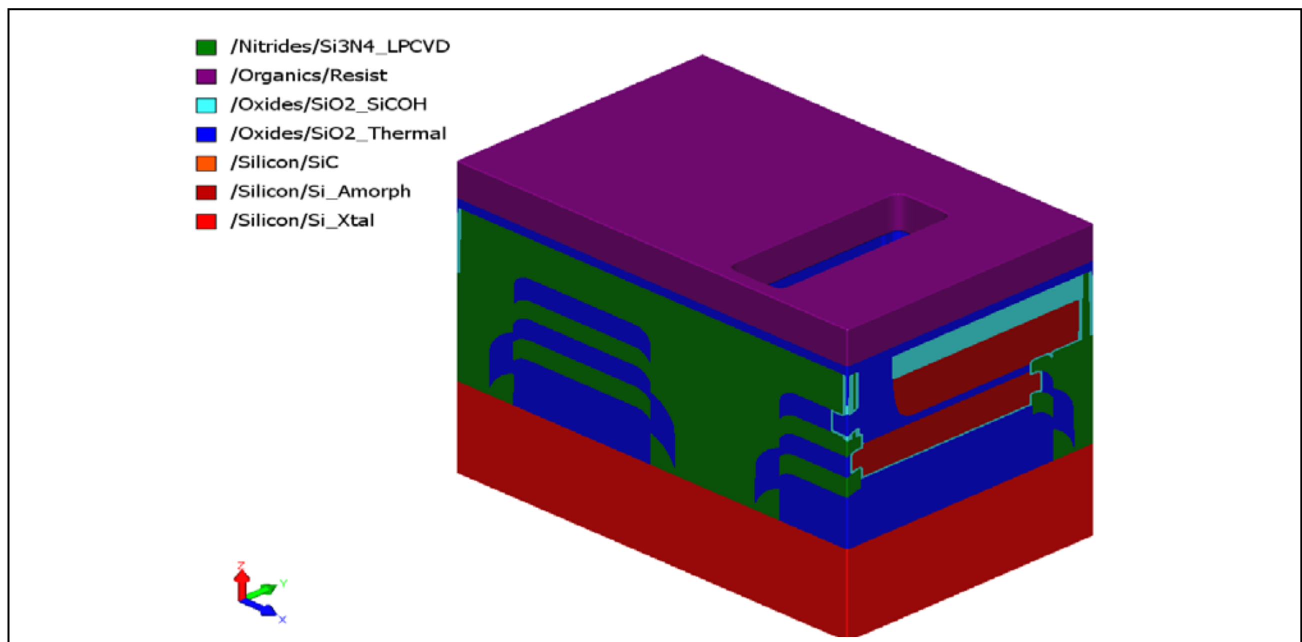


4.5.4. Basic Etch



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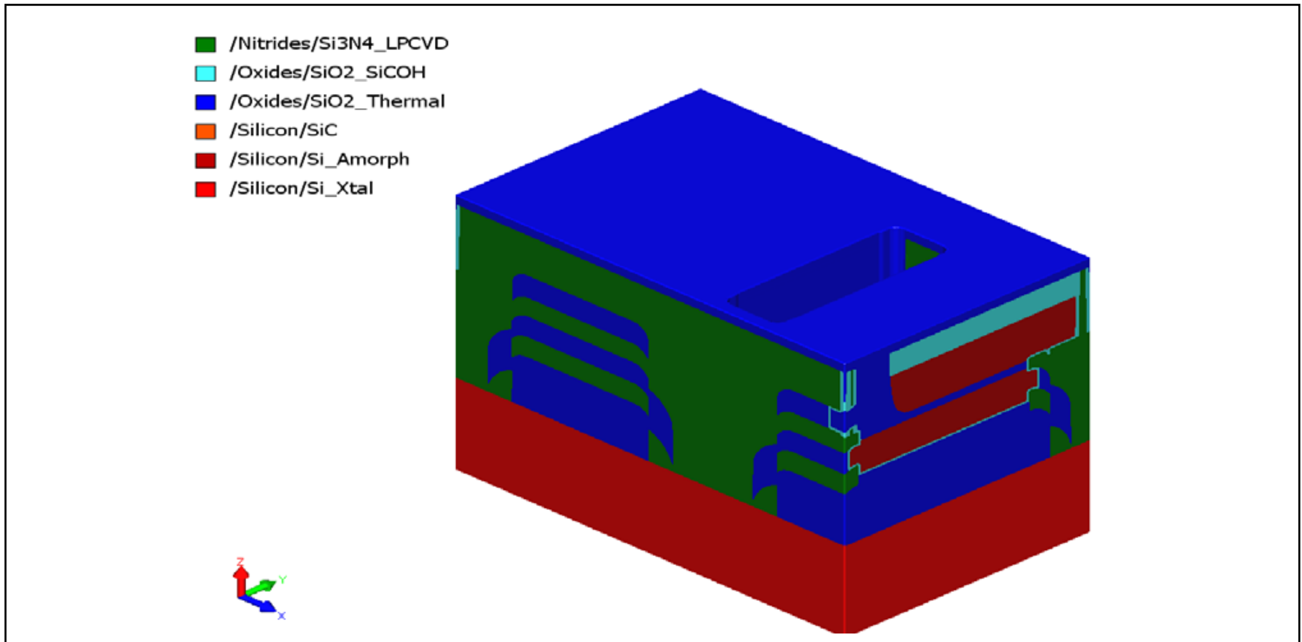
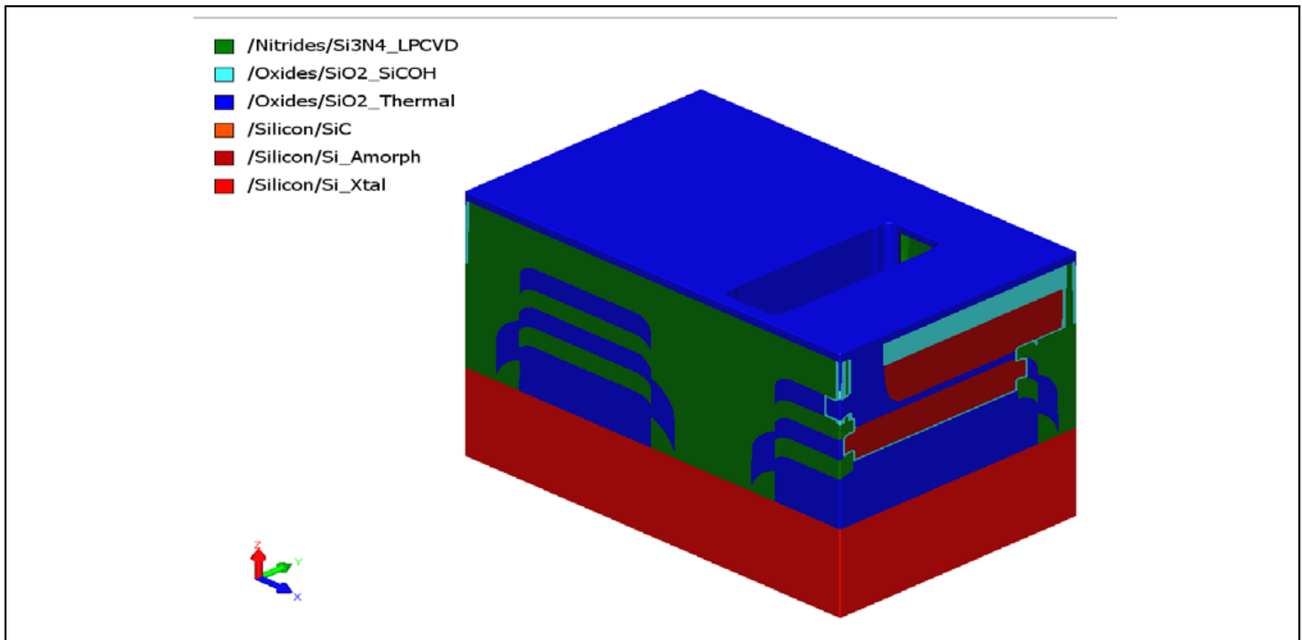
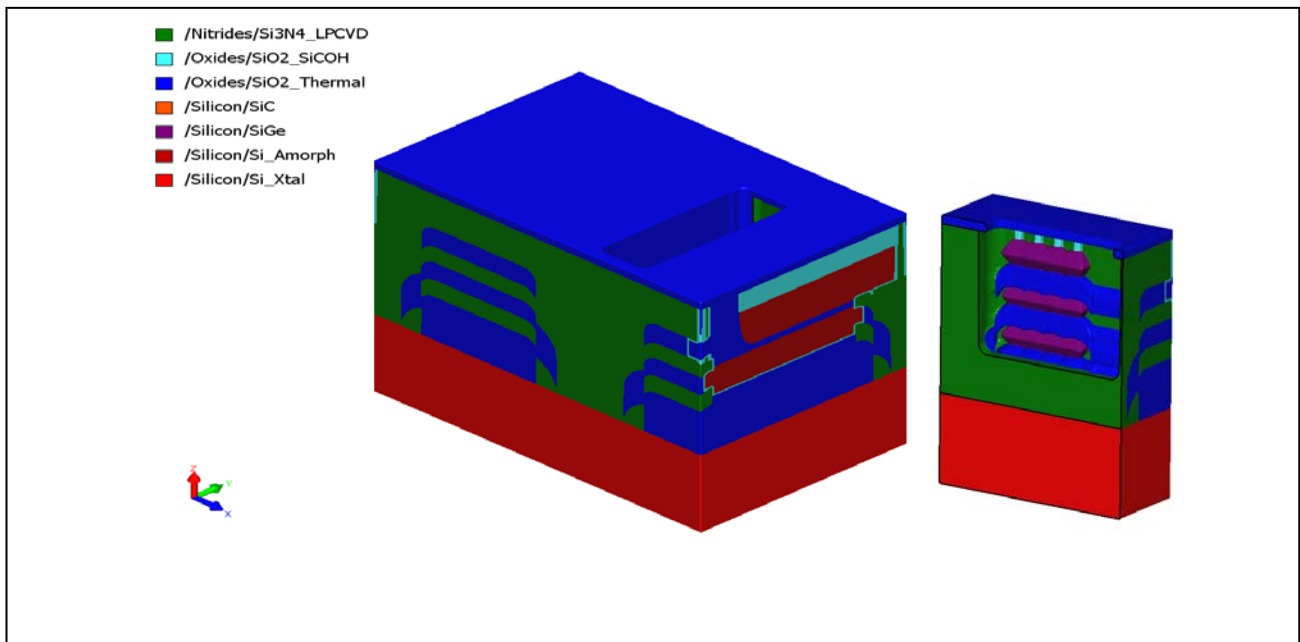


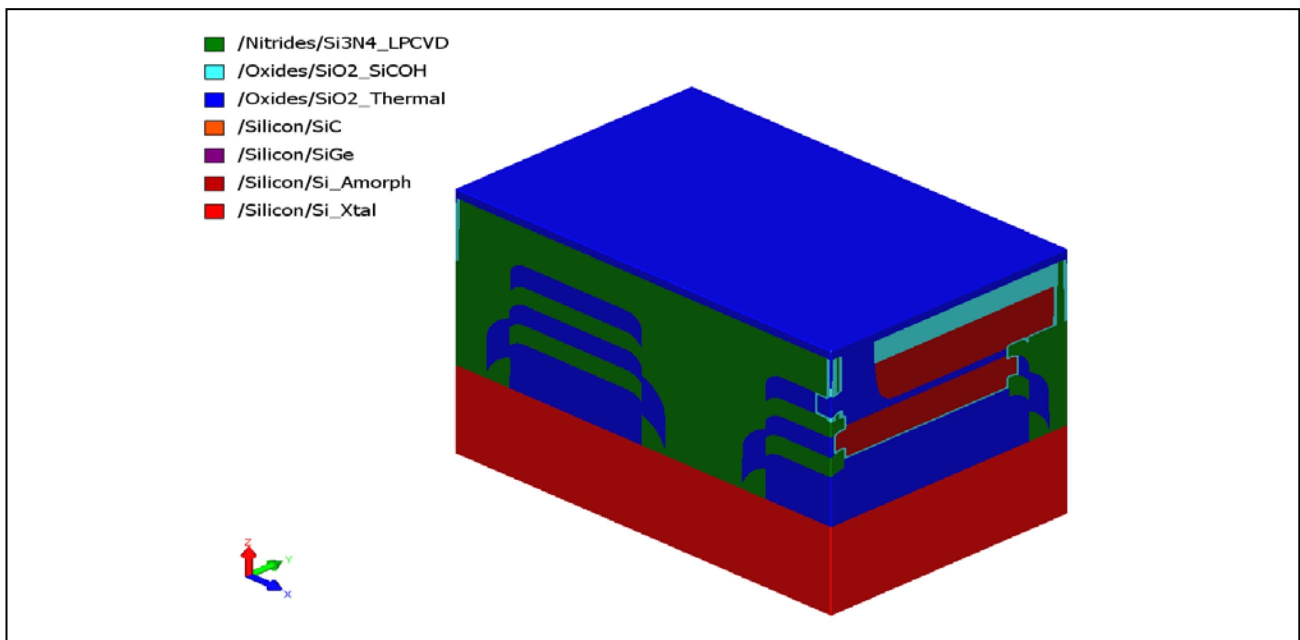
4.5.6. Basic Etch



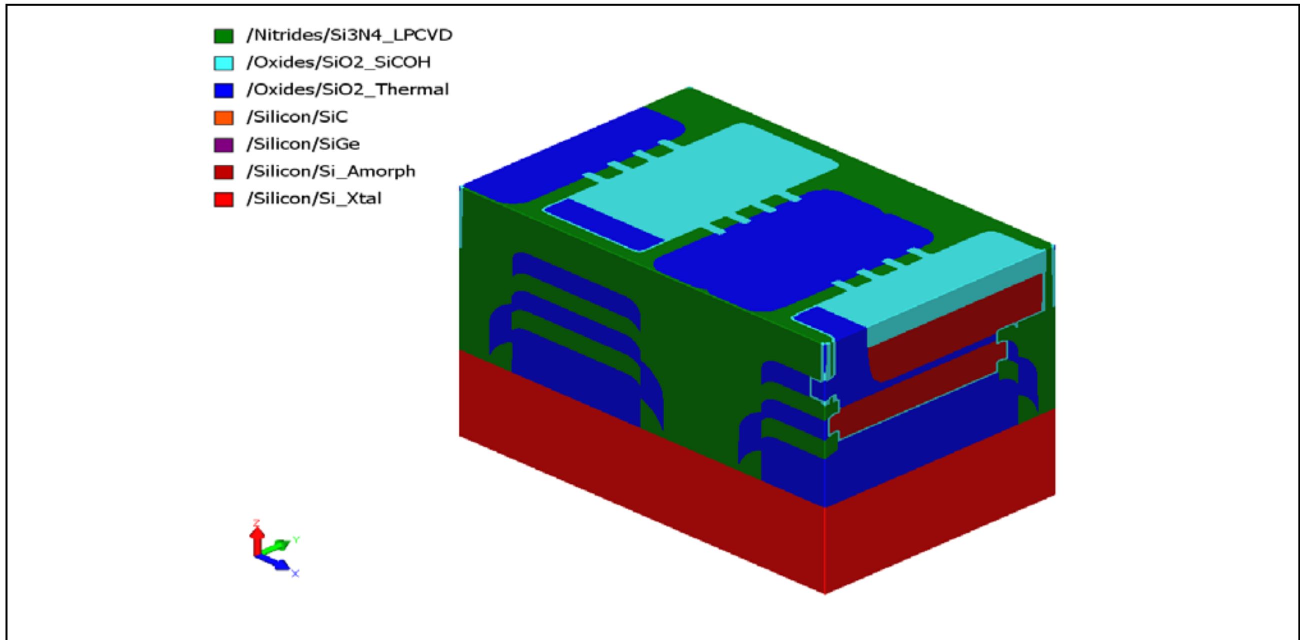
4.5.8. Selective Epitaxy (Requires Advanced Modeling)



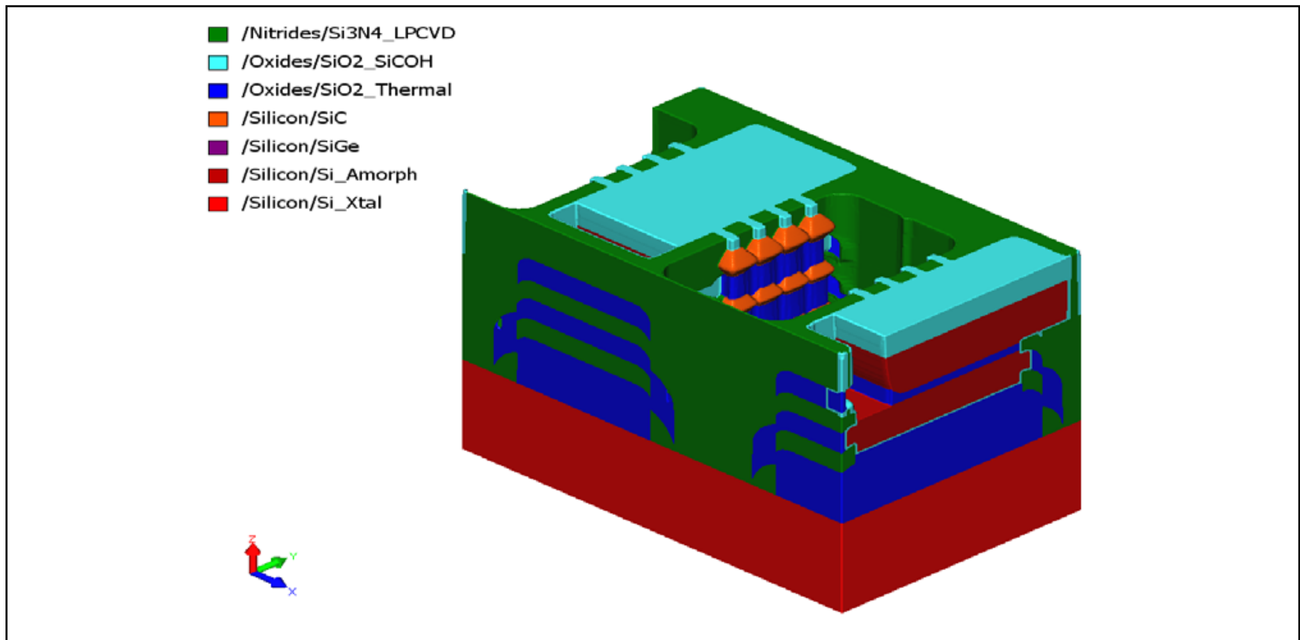
4.5.9. Planar Deposit



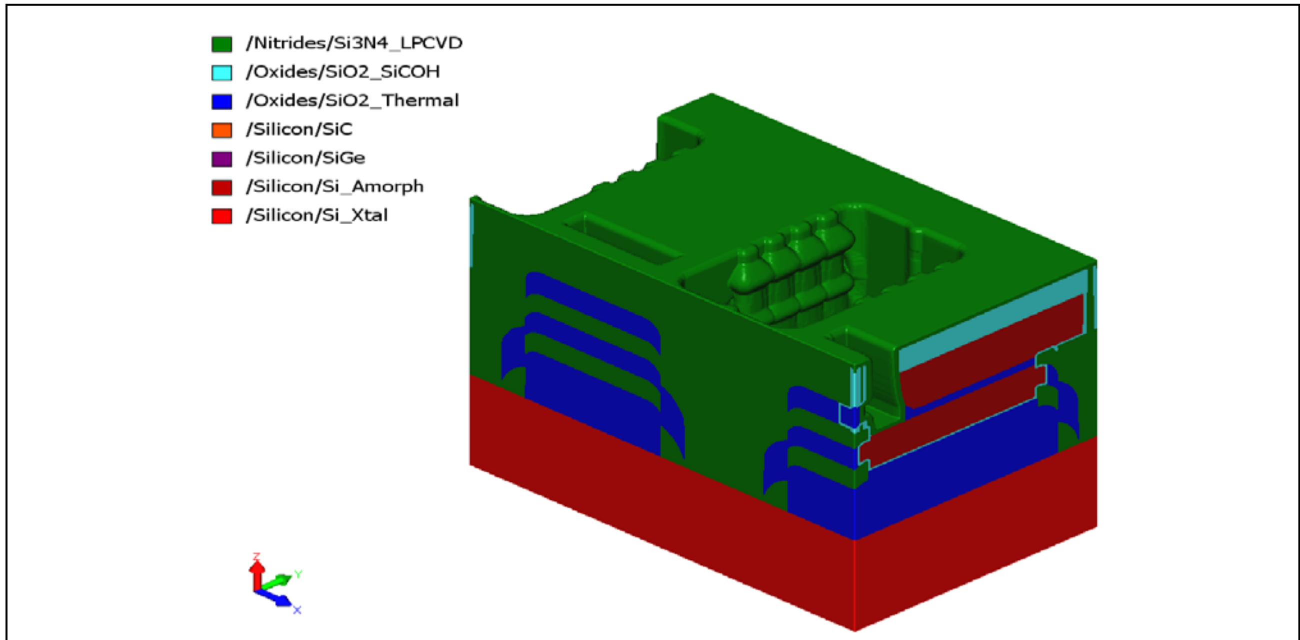
4.5.10. Stopping CMP



4.5.14. Basic Etch



4.5.17. Conformal Deposit



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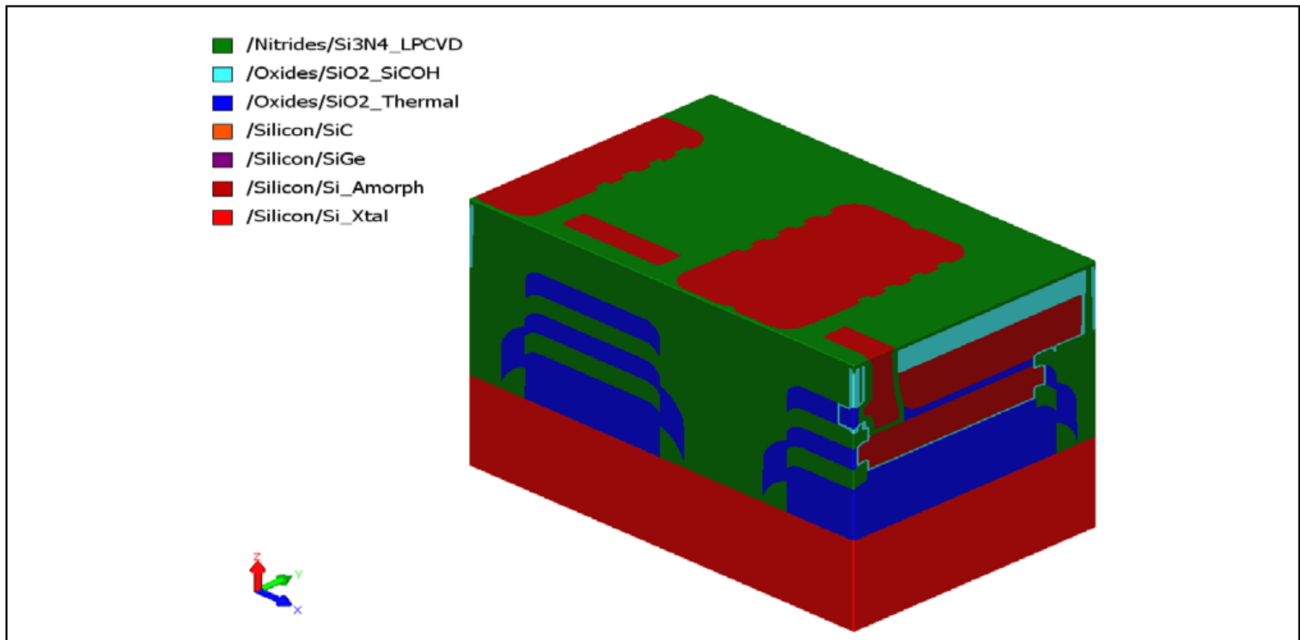
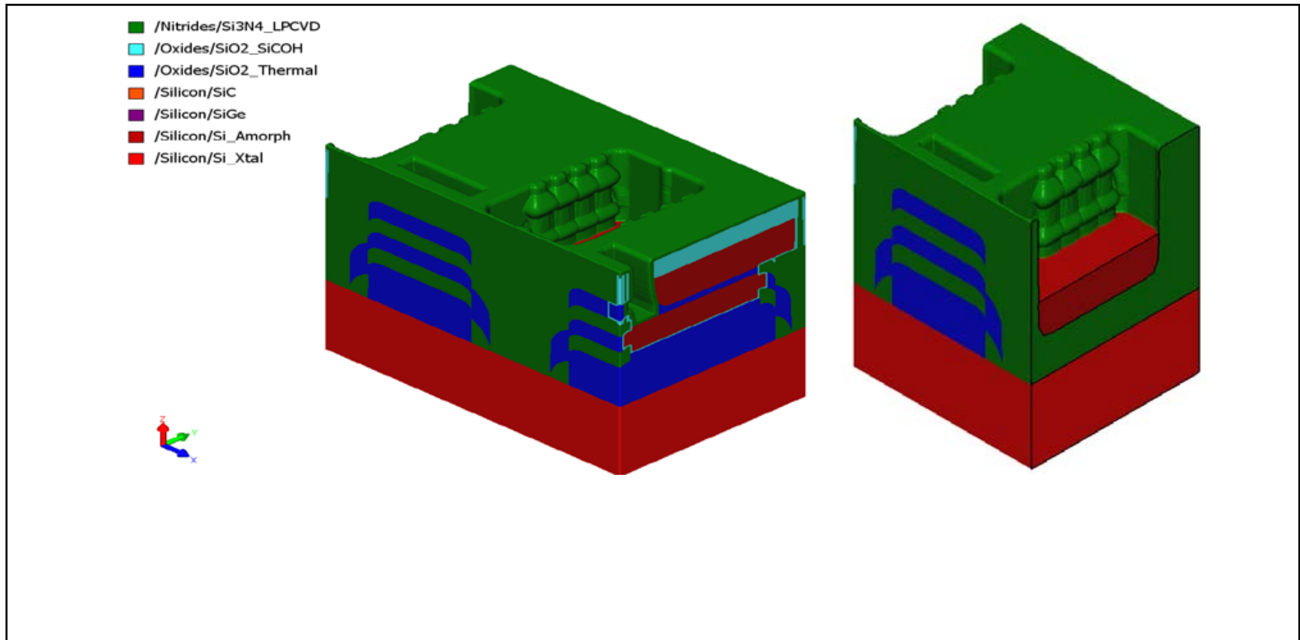


4.5.19. Basic Etch



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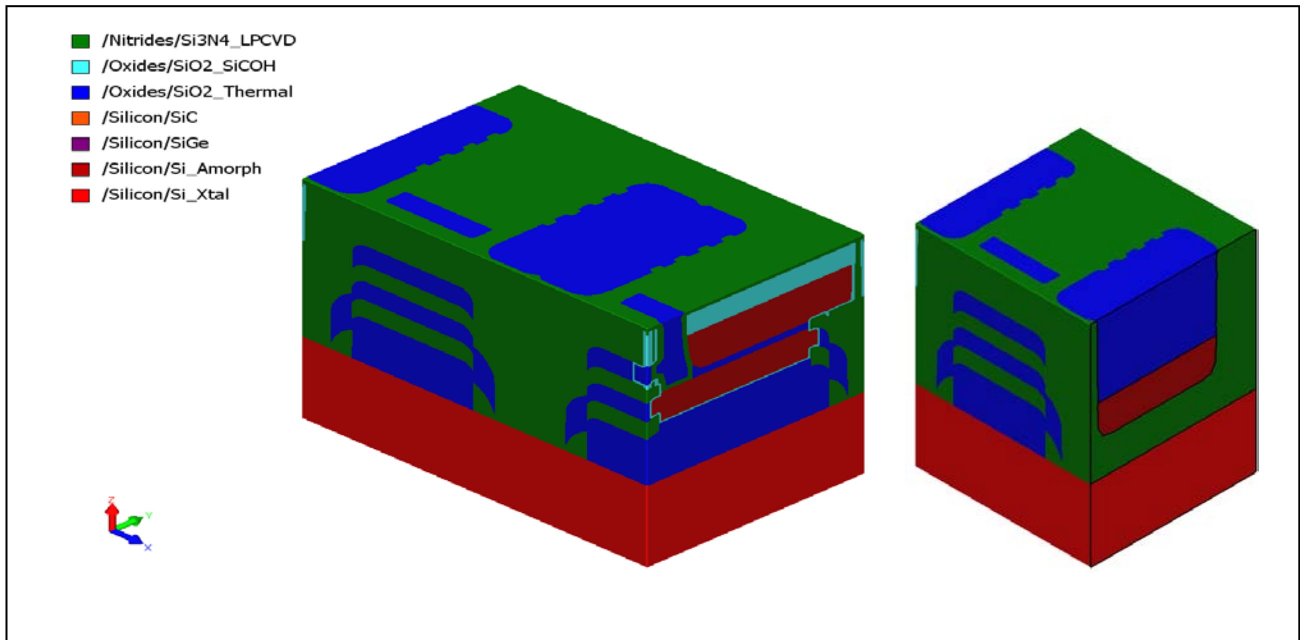
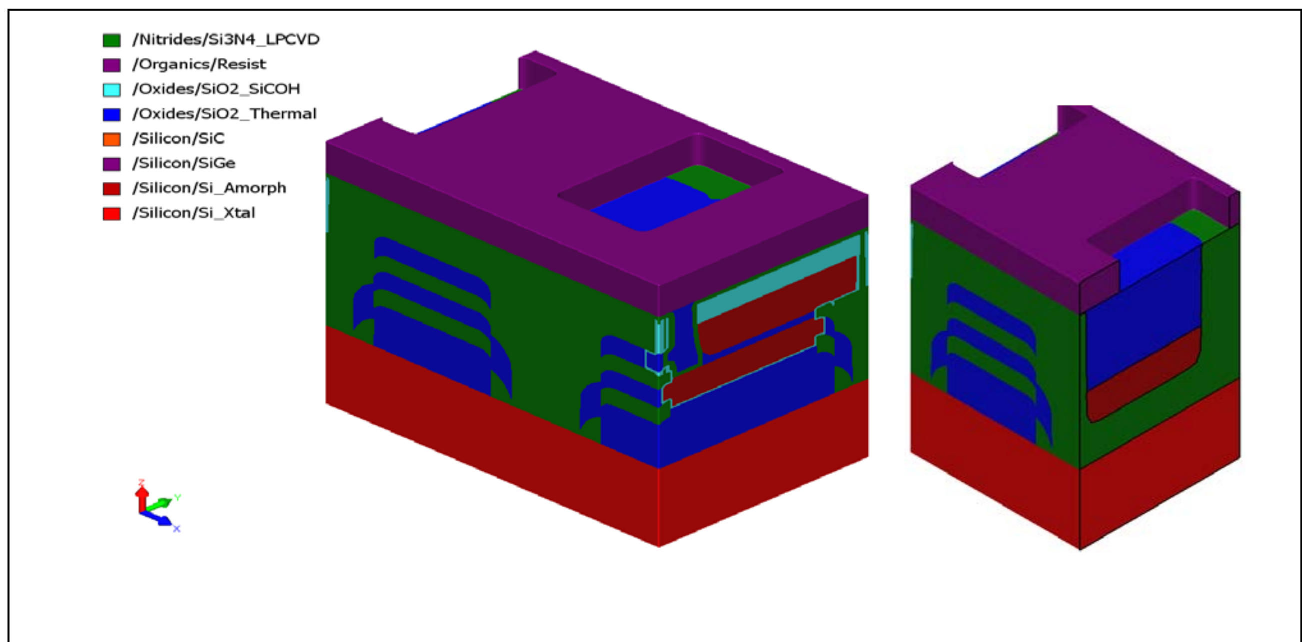
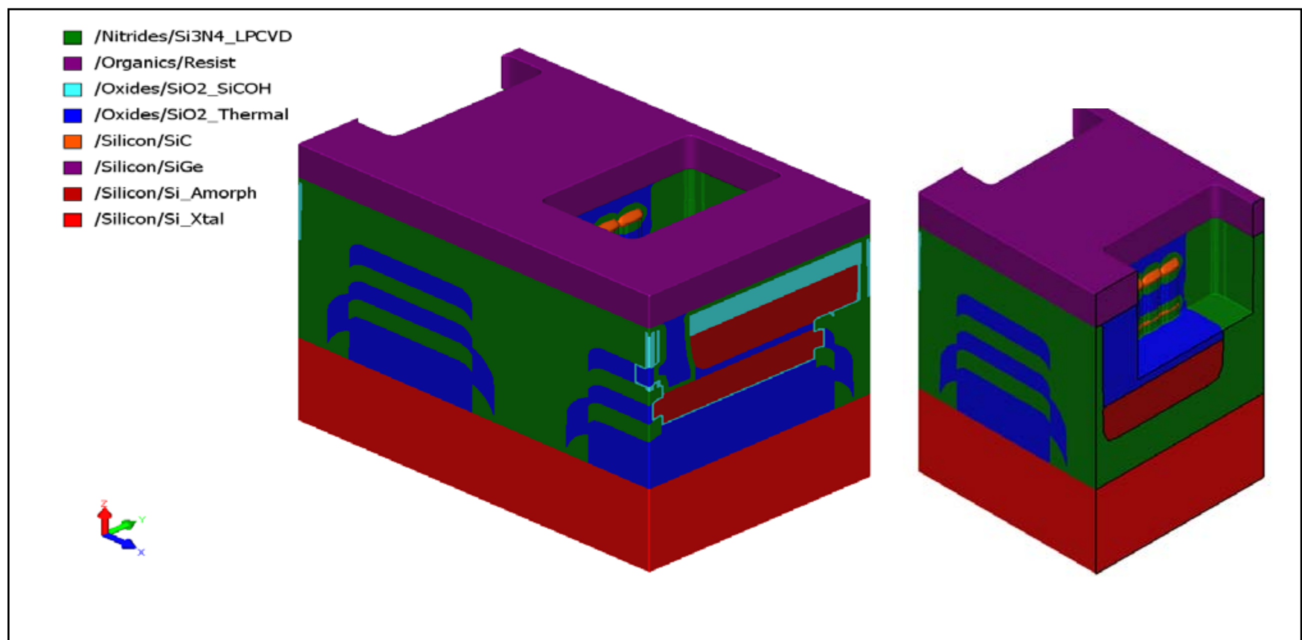


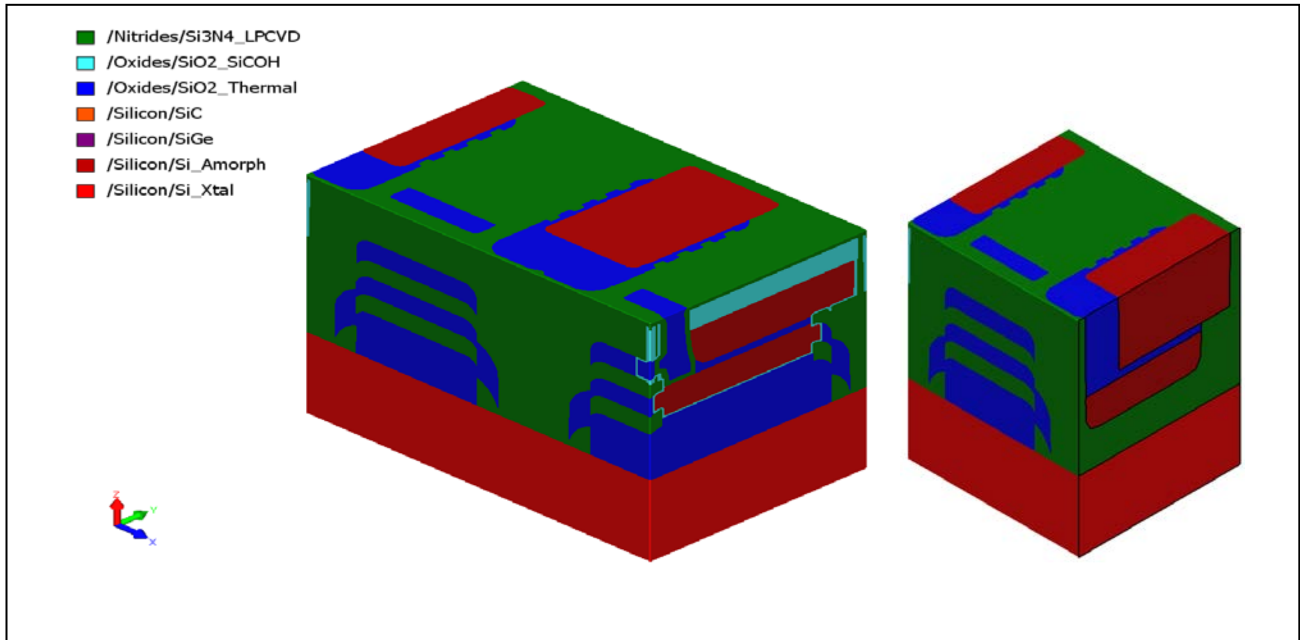
4.5.22. Expose Material



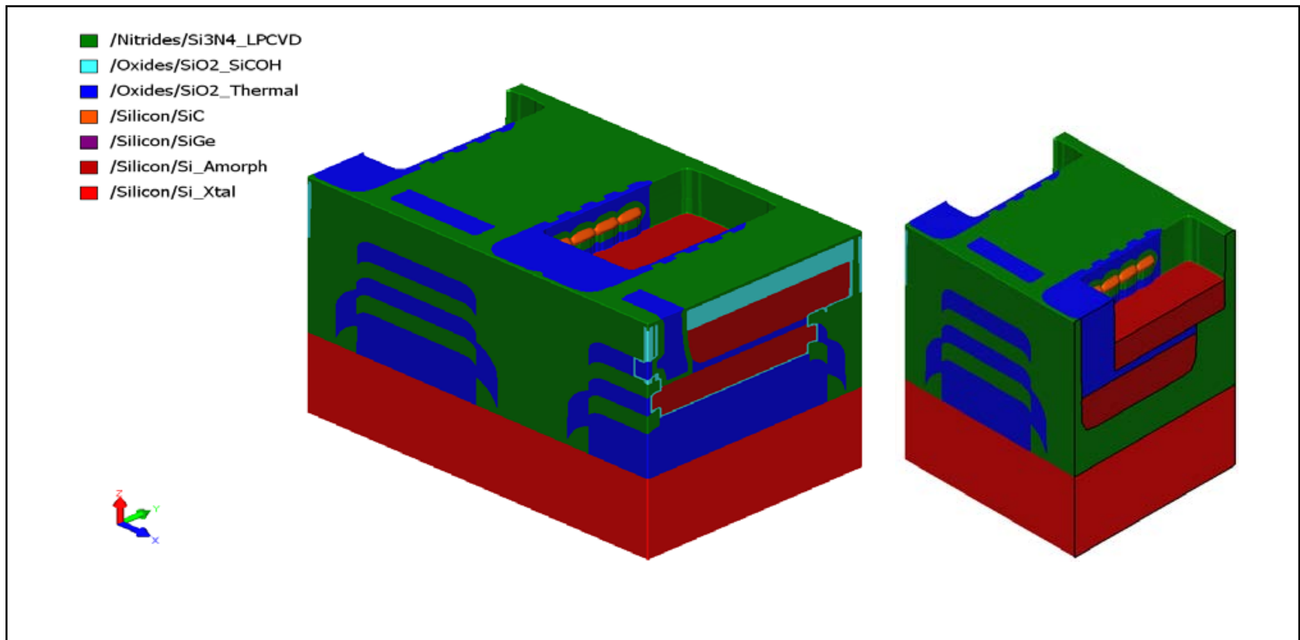
4.5.23. Basic Etch



4.5.25. Planar Deposit



4.5.26. Basic Etch

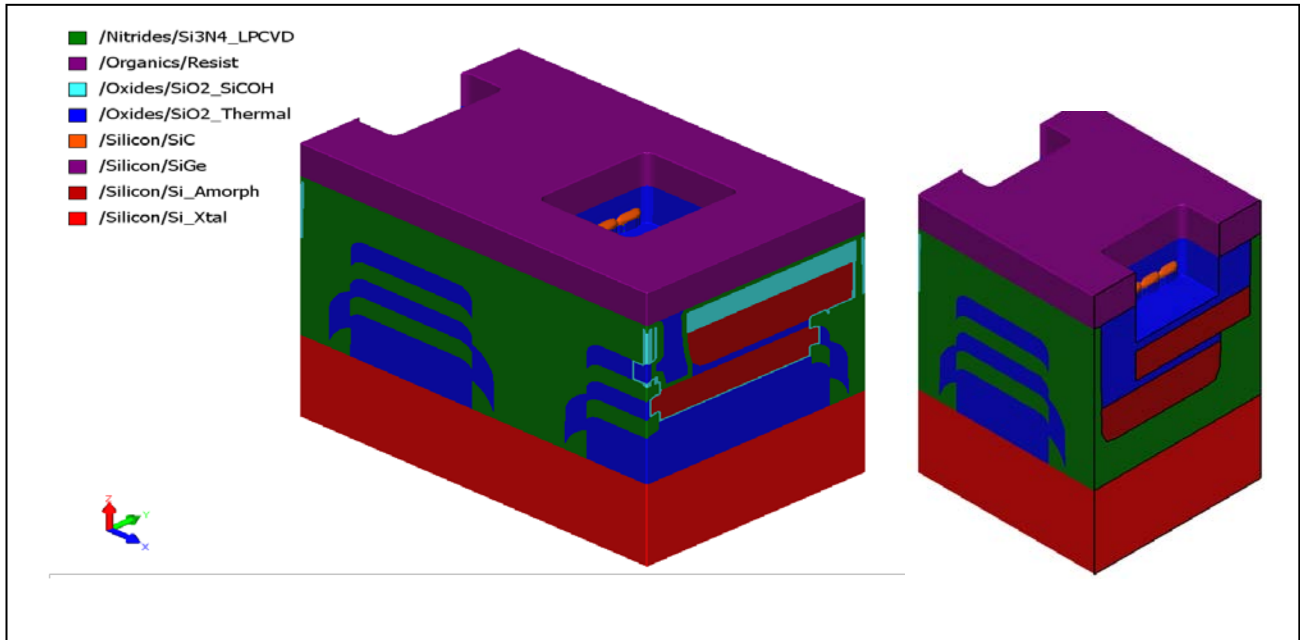


4.5.27. Planar Deposit

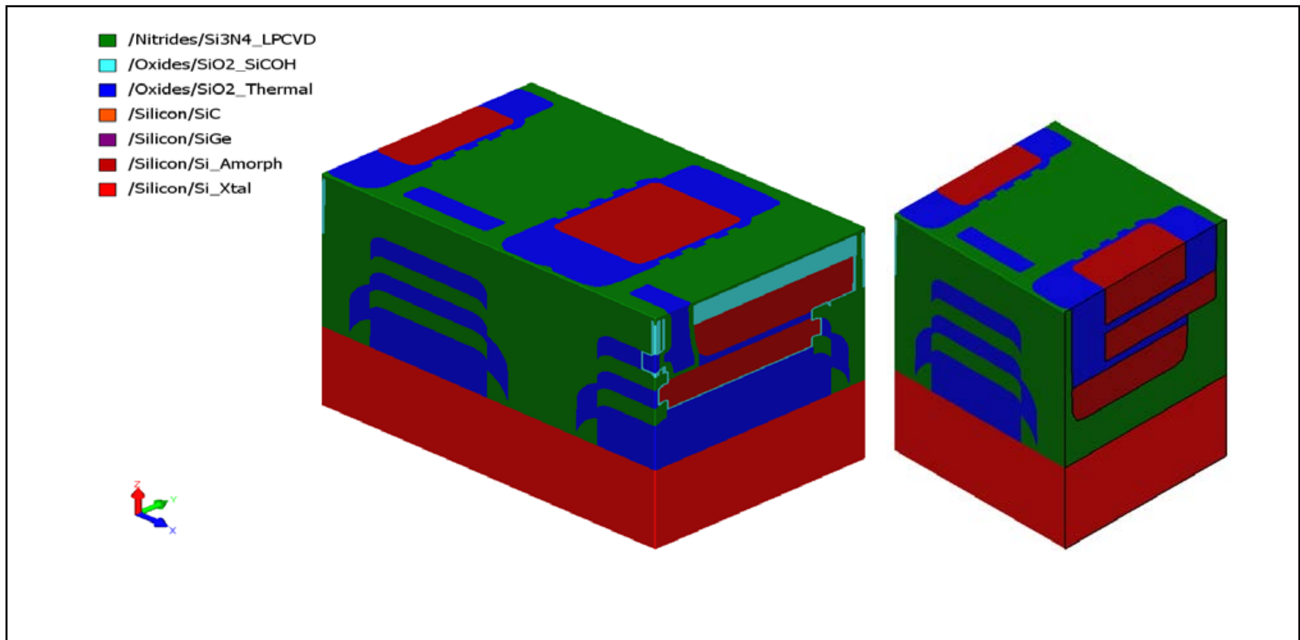
RMG module

4.5.29. Expose Material

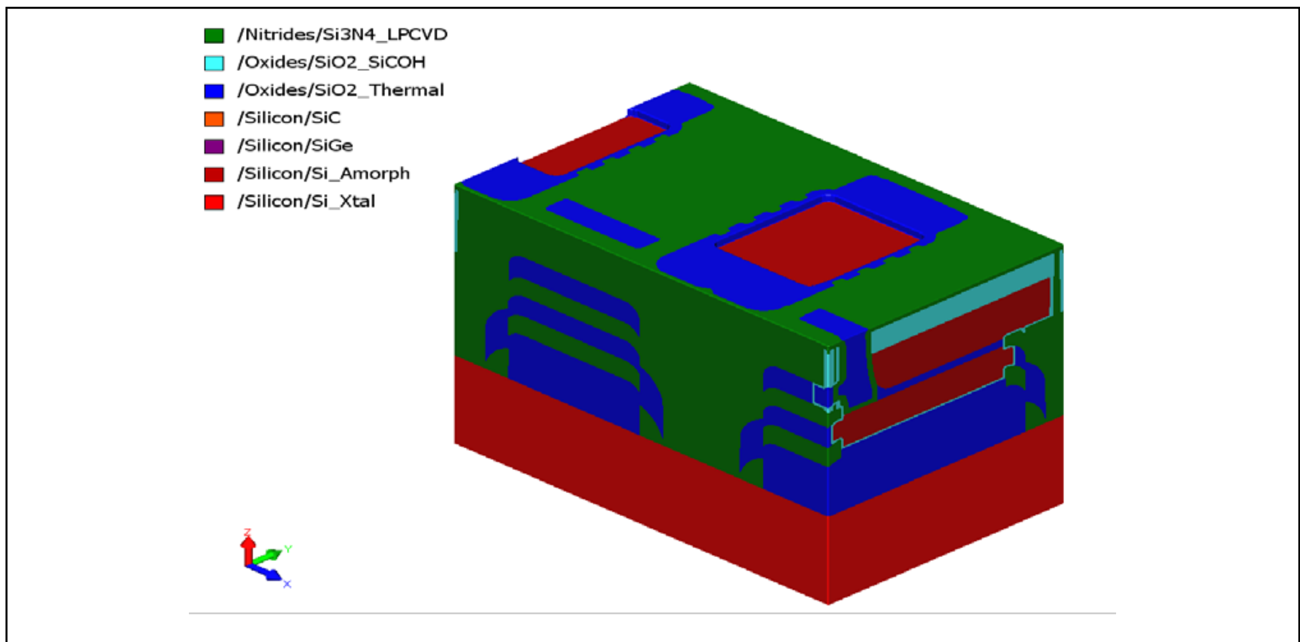
4.5.30. Basic Etch



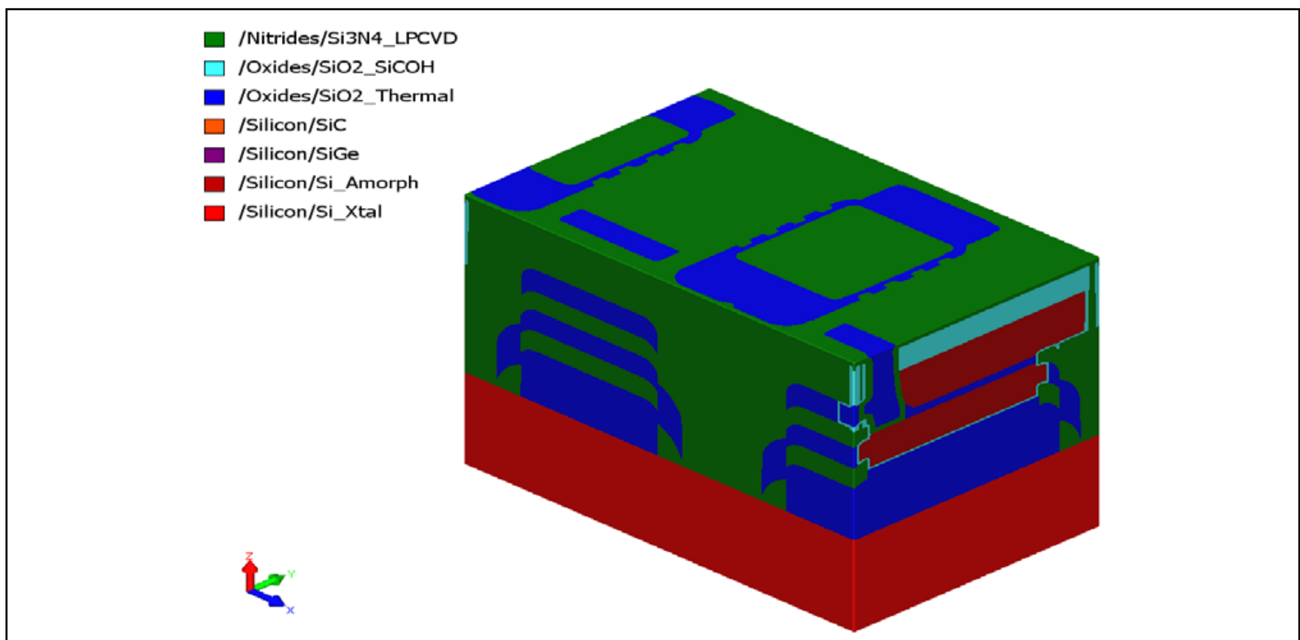
4.5.32. Planar Deposit



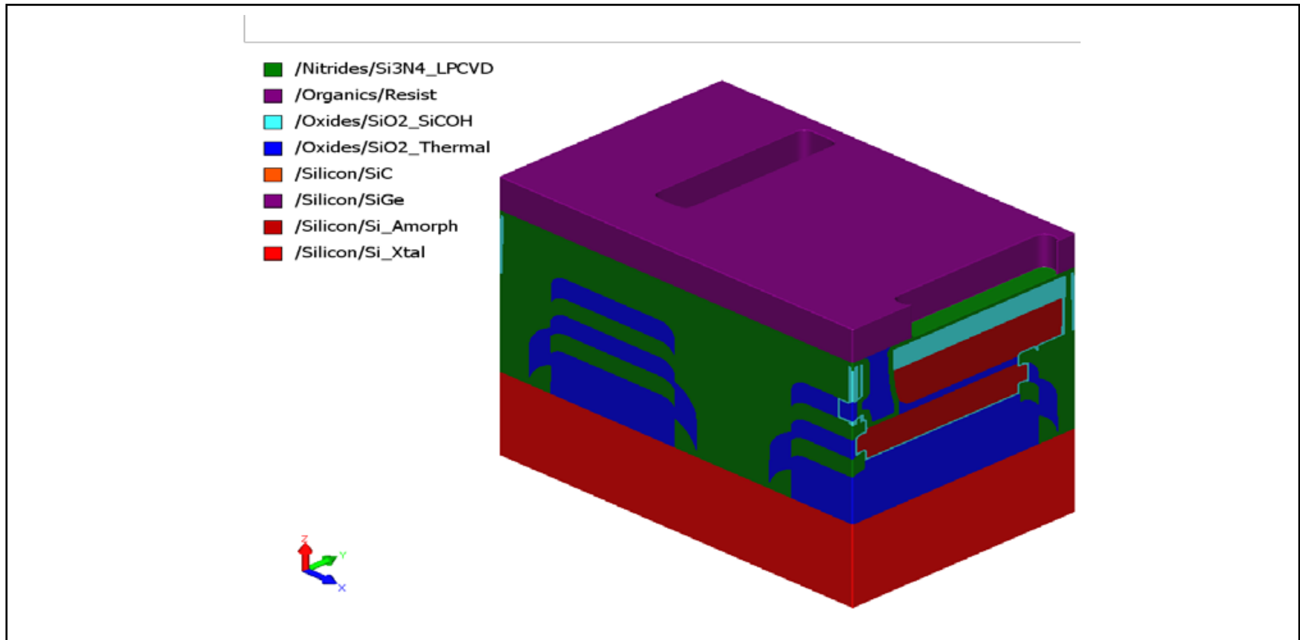
4.5.37. Basic Etch



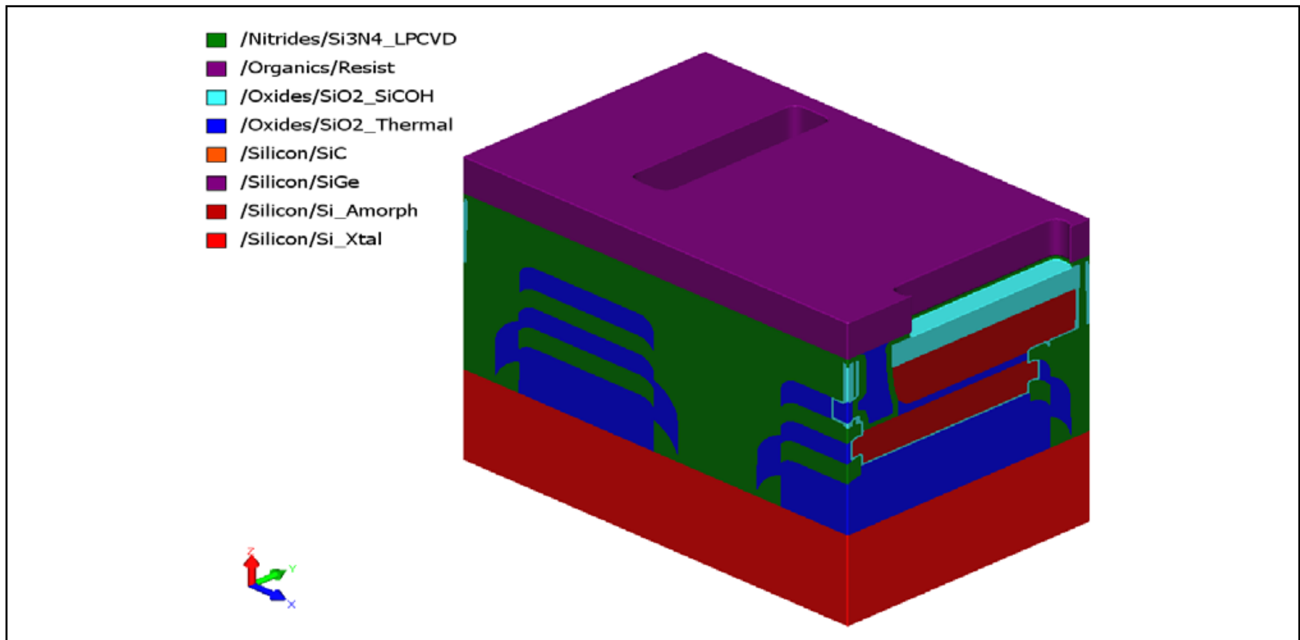
4.5.38. Planar Deposit



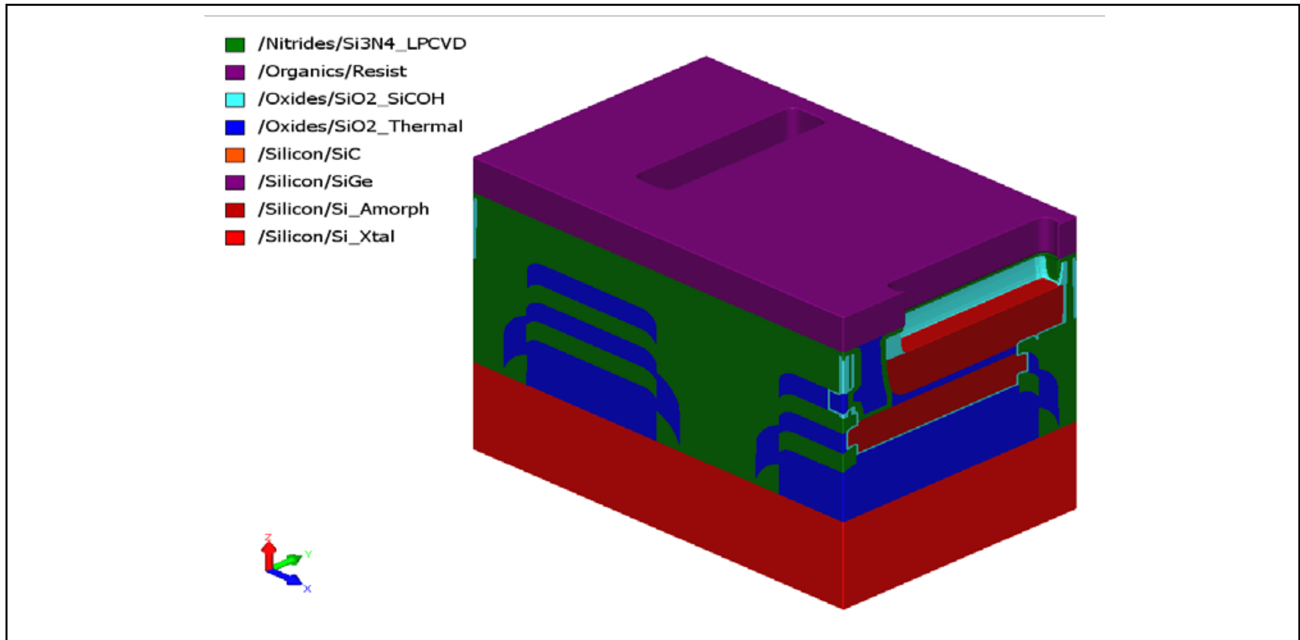
4.6.4. Expose Material



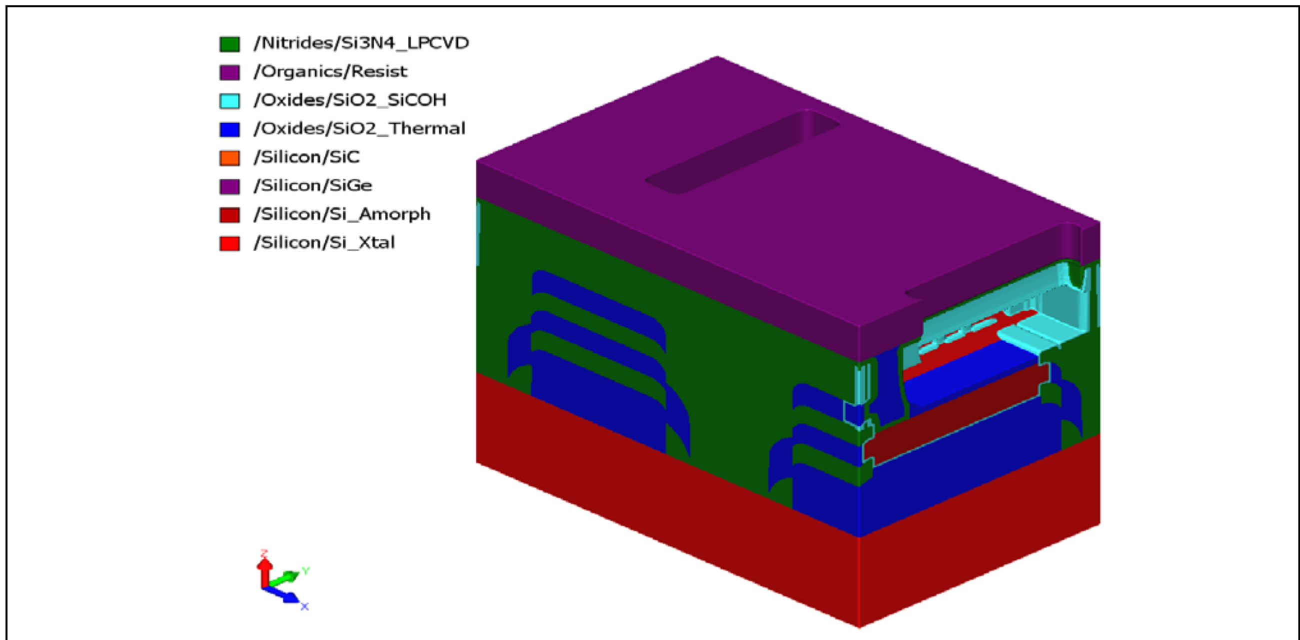
4.6.5. Basic Etch



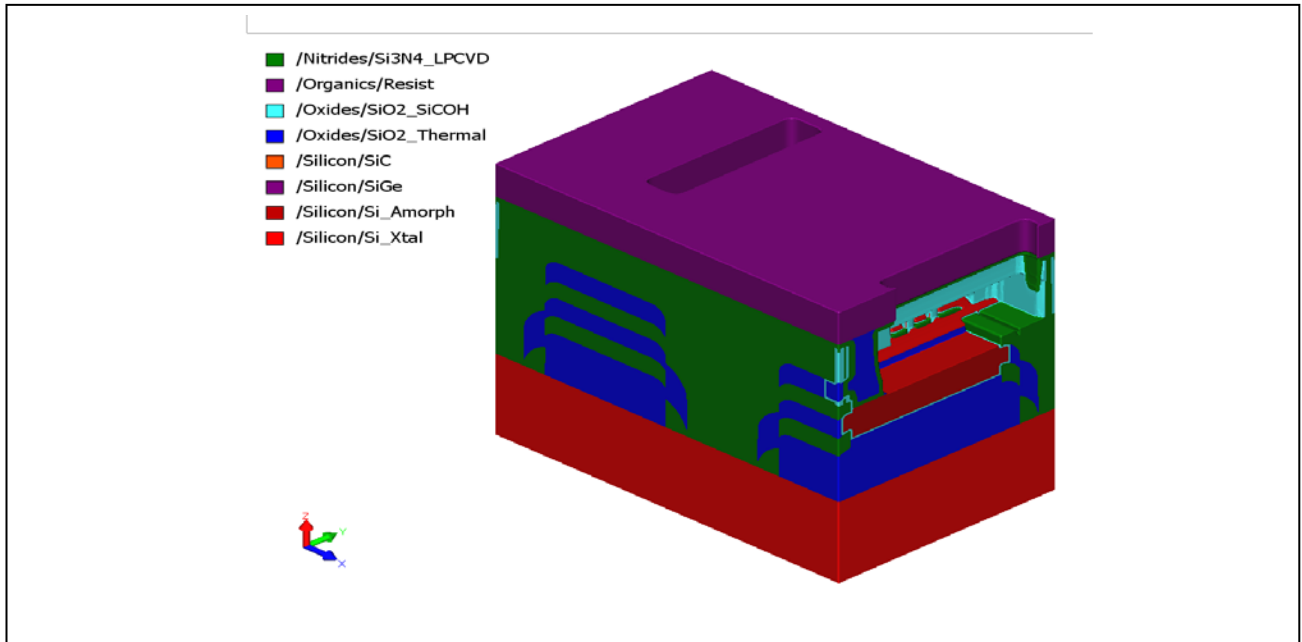
4.6.6. Basic Etch



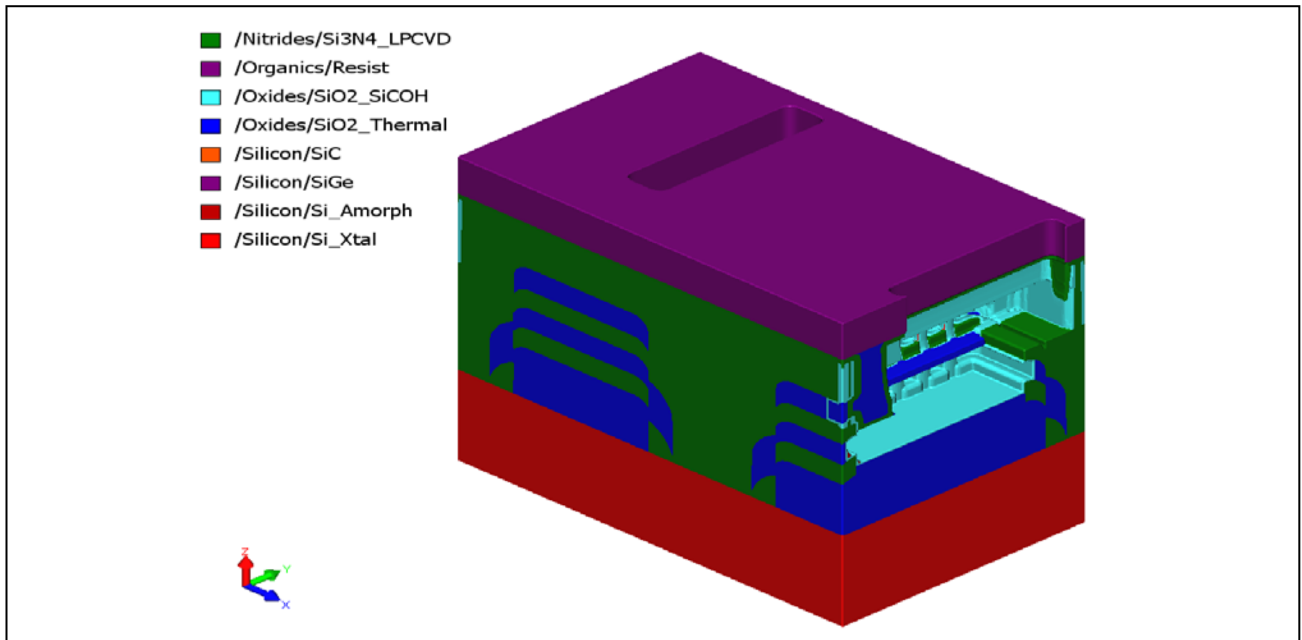
4.6.7. Basic Etch



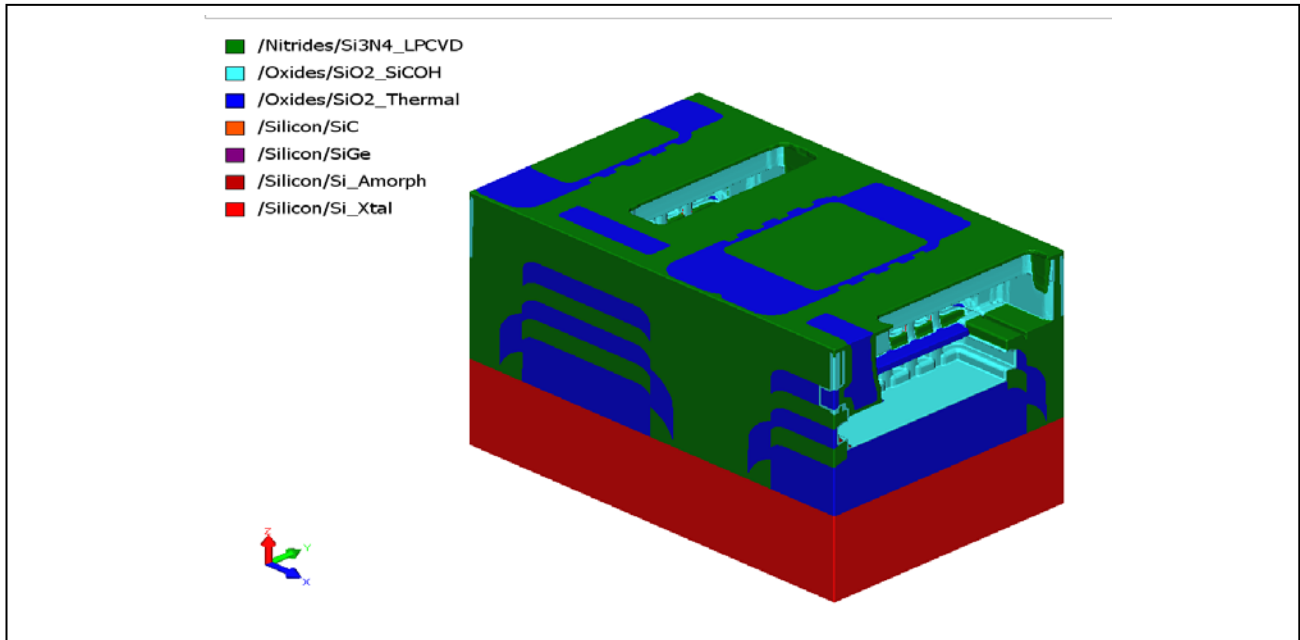
4.6.8. Basic Etch



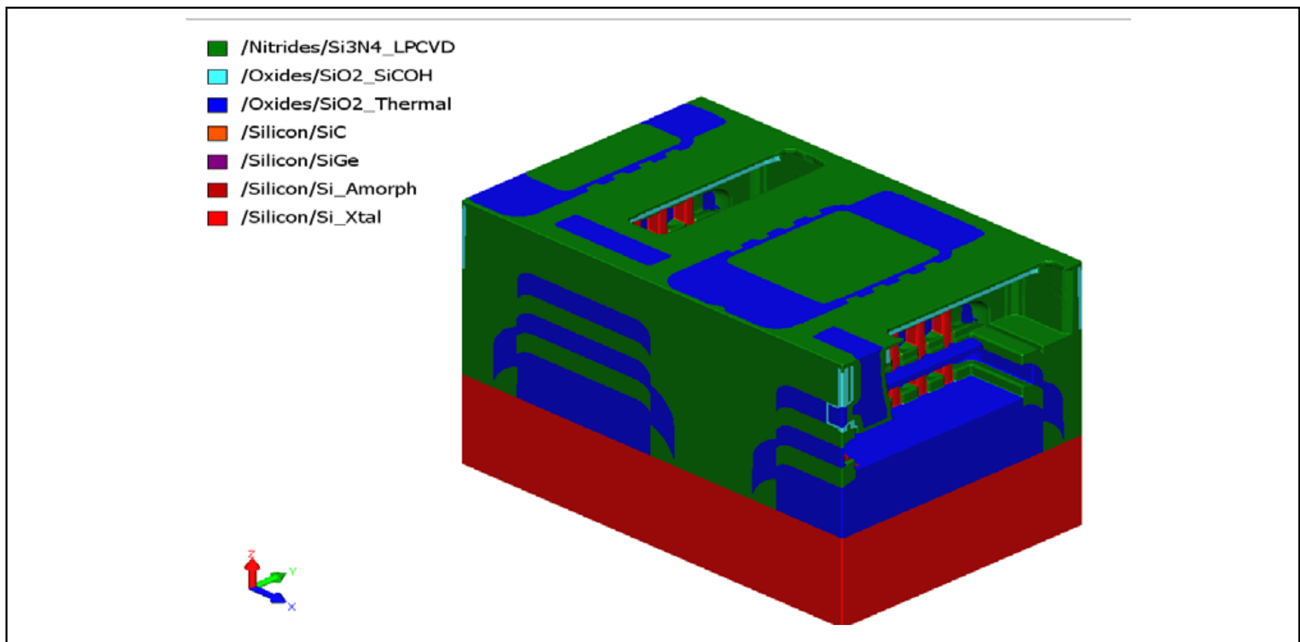
4.6.9. Basic Etch



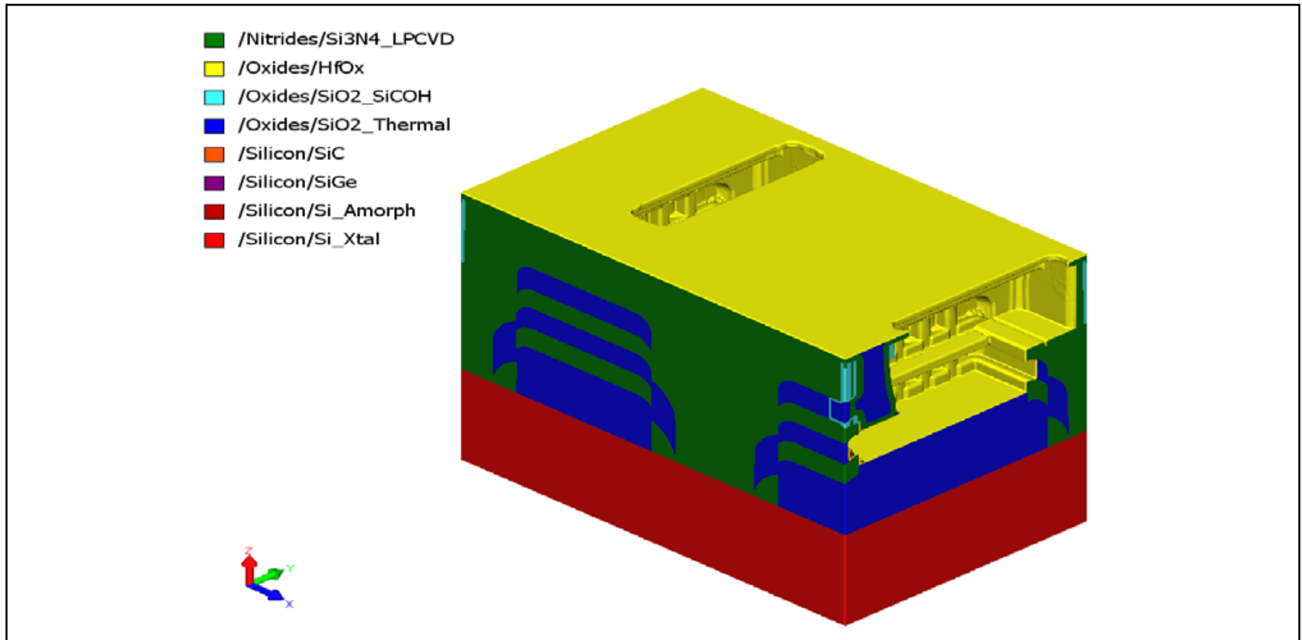
4.6.11. Remove Materials



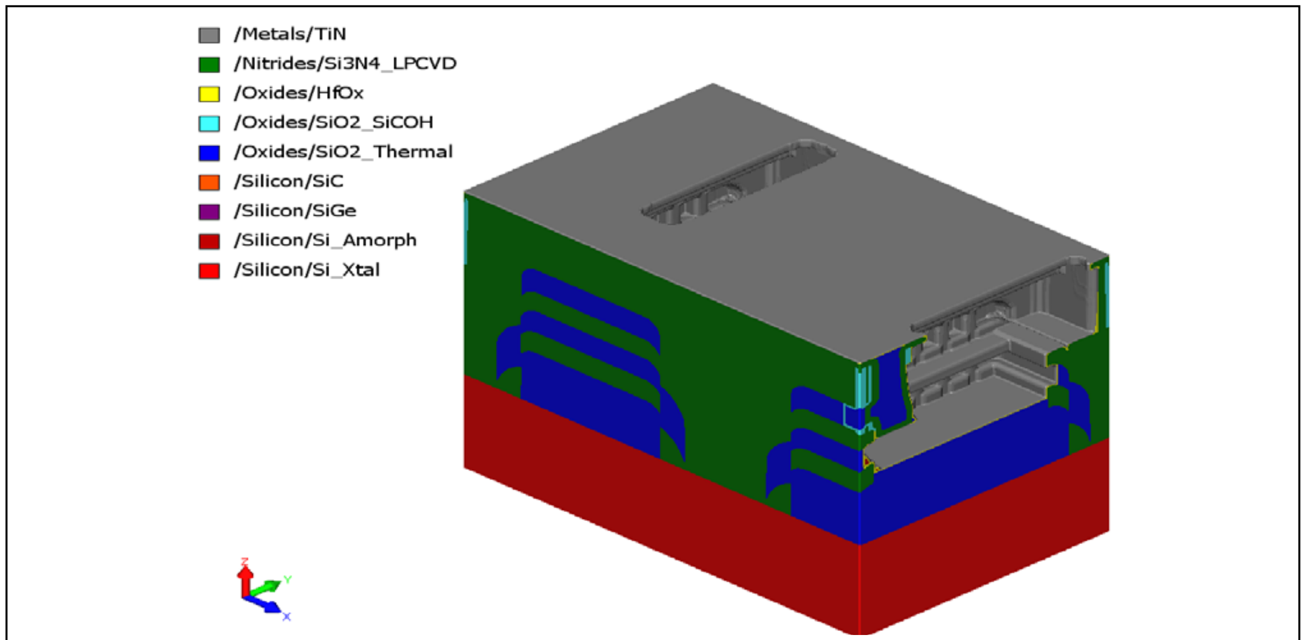
4.6.17. Basic Etch



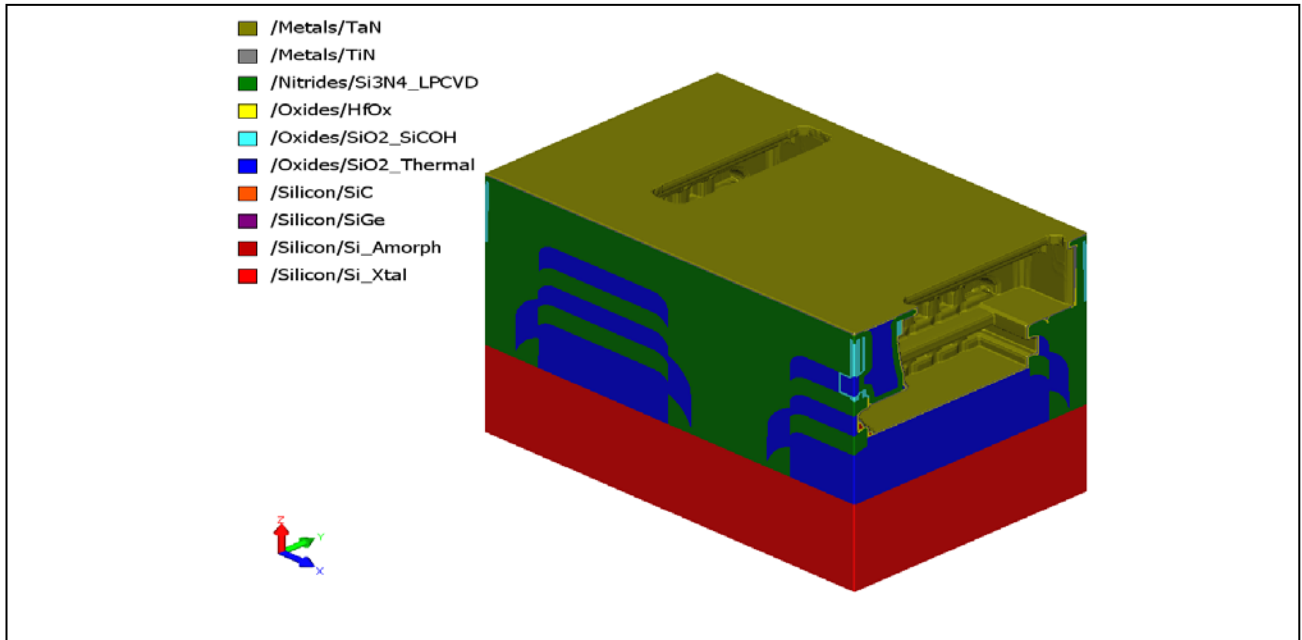
4.6.18. Conformal Deposit



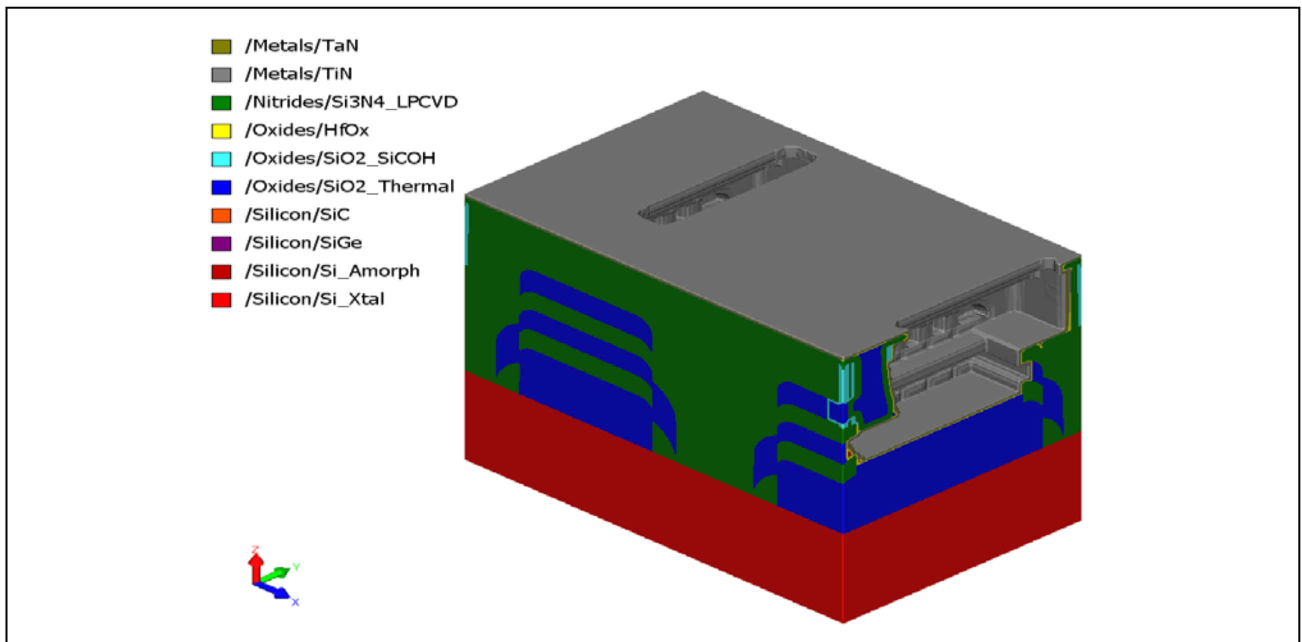
4.6.19. Conformal Deposit



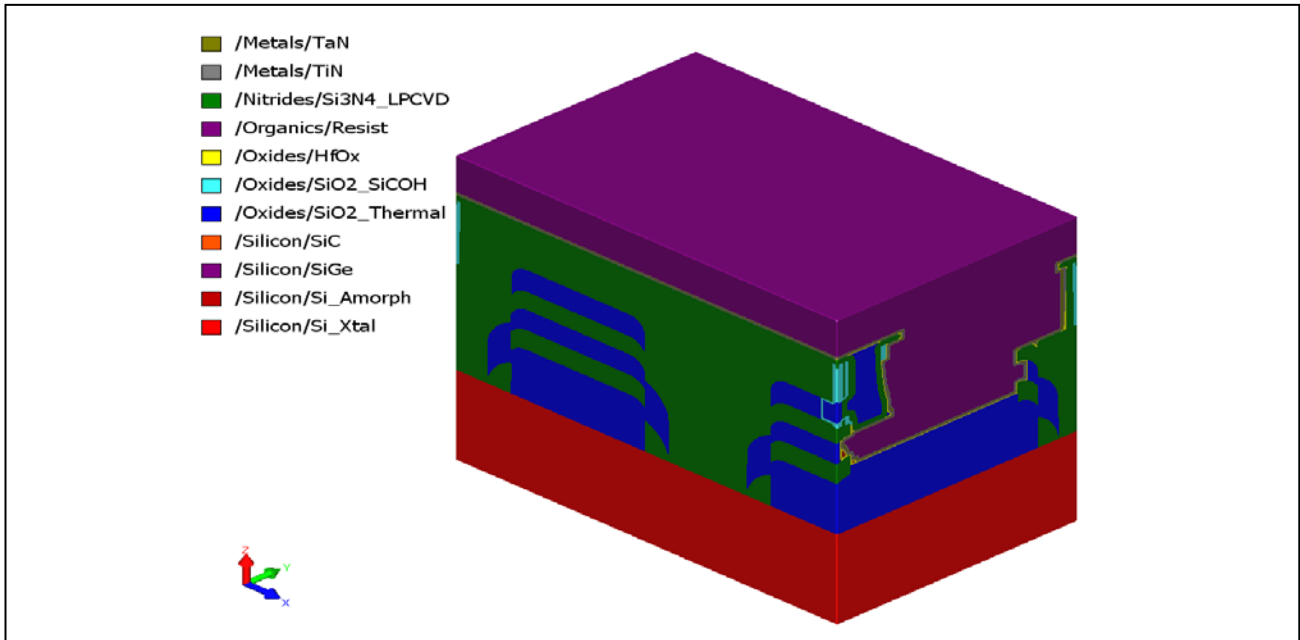
4.6.20. Conformal Deposit



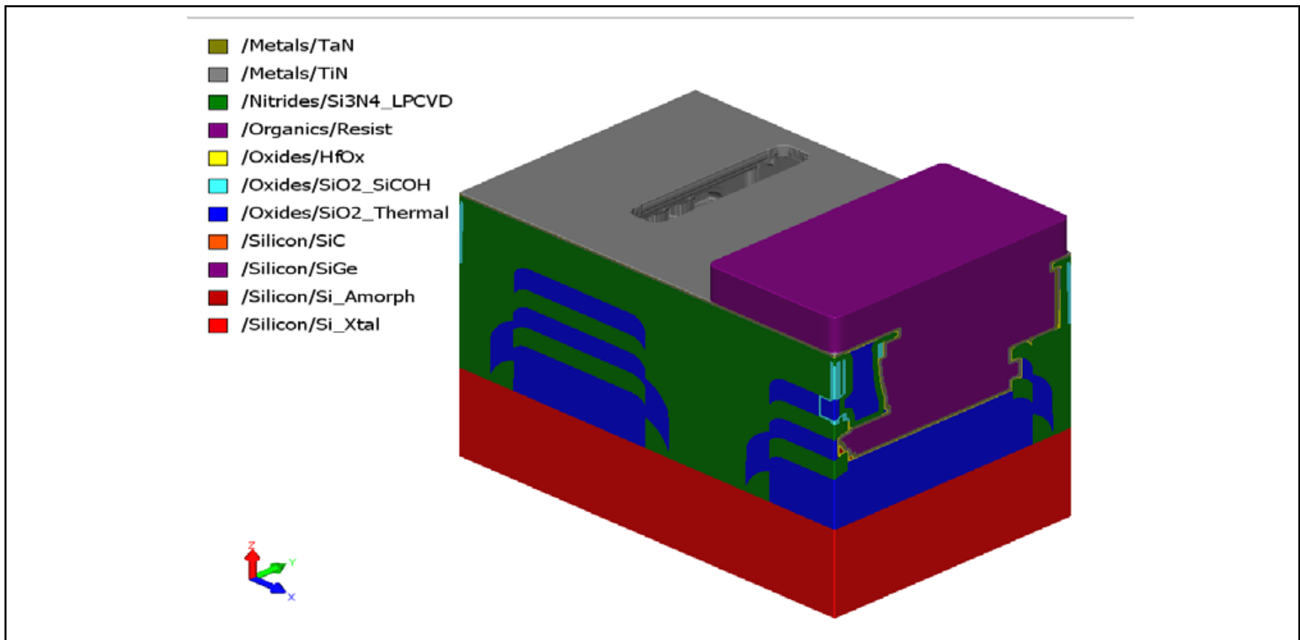
4.6.21. Conformal Deposit



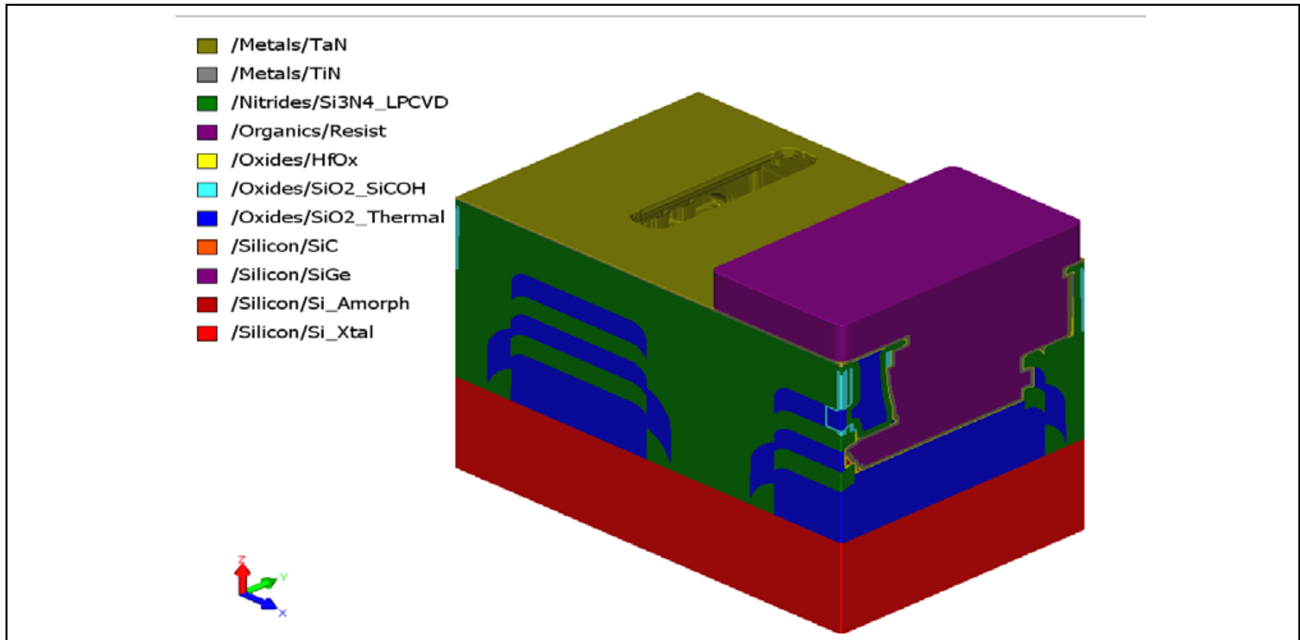
4.6.22. Straight Deposit



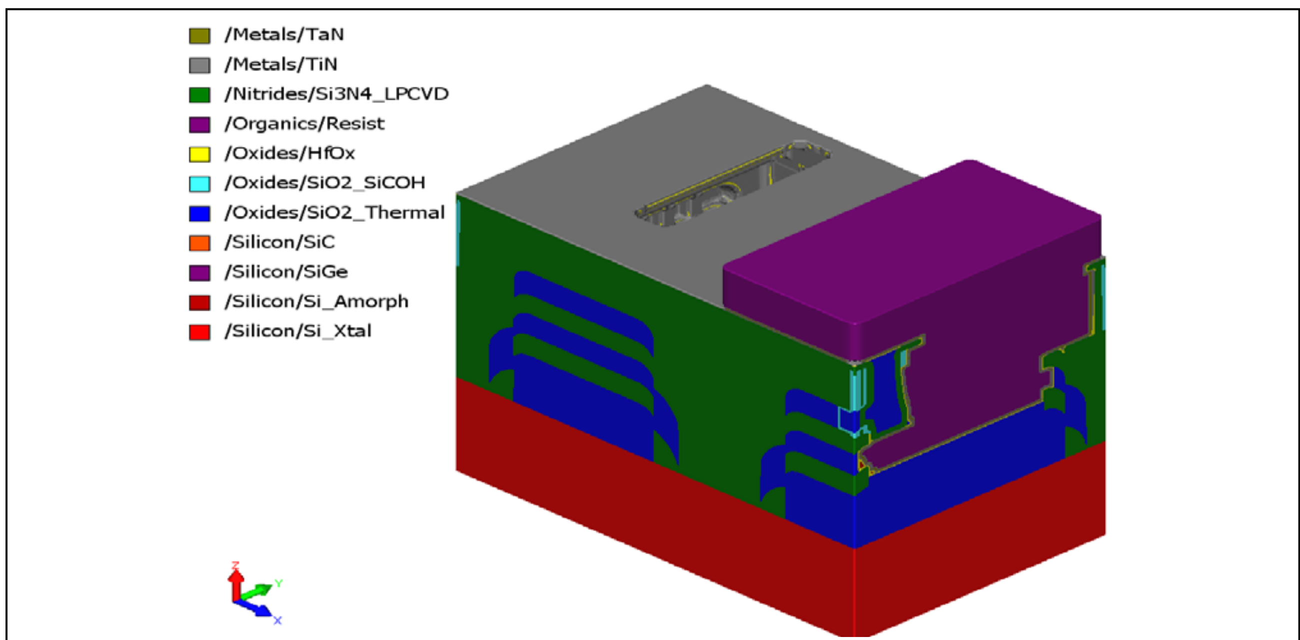
4.6.23. Expose Material



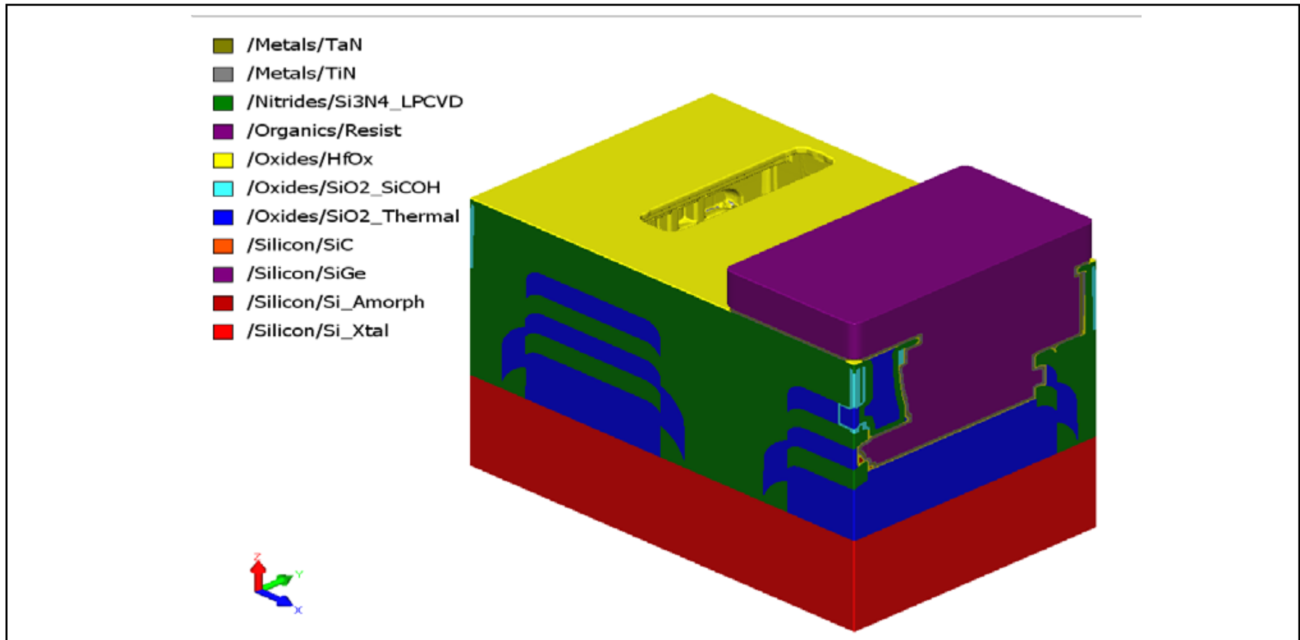
4.6.25. Basic Etch



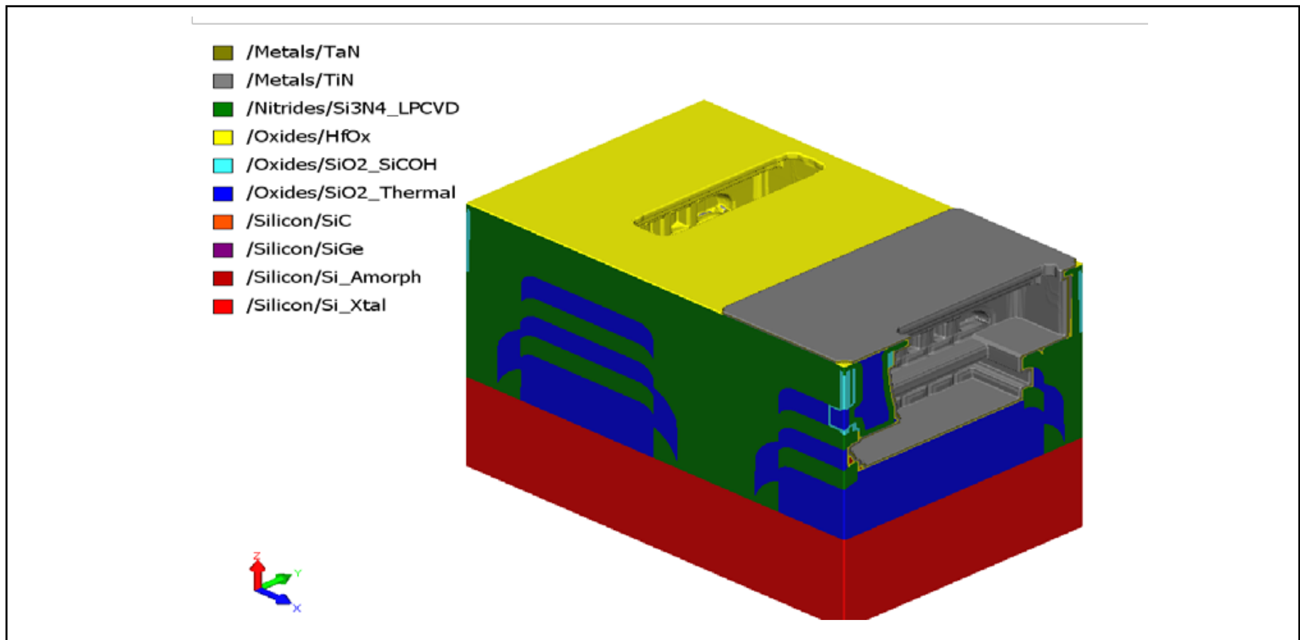
4.6.26. Basic Etch



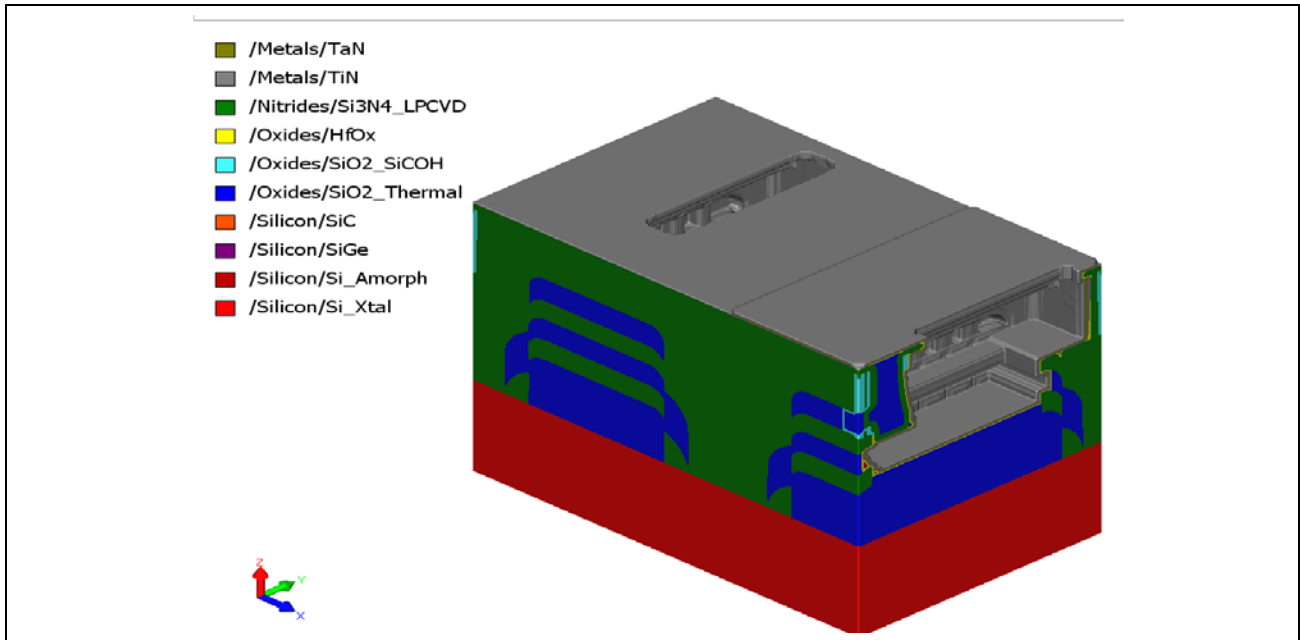
4.6.27. Basic Etch



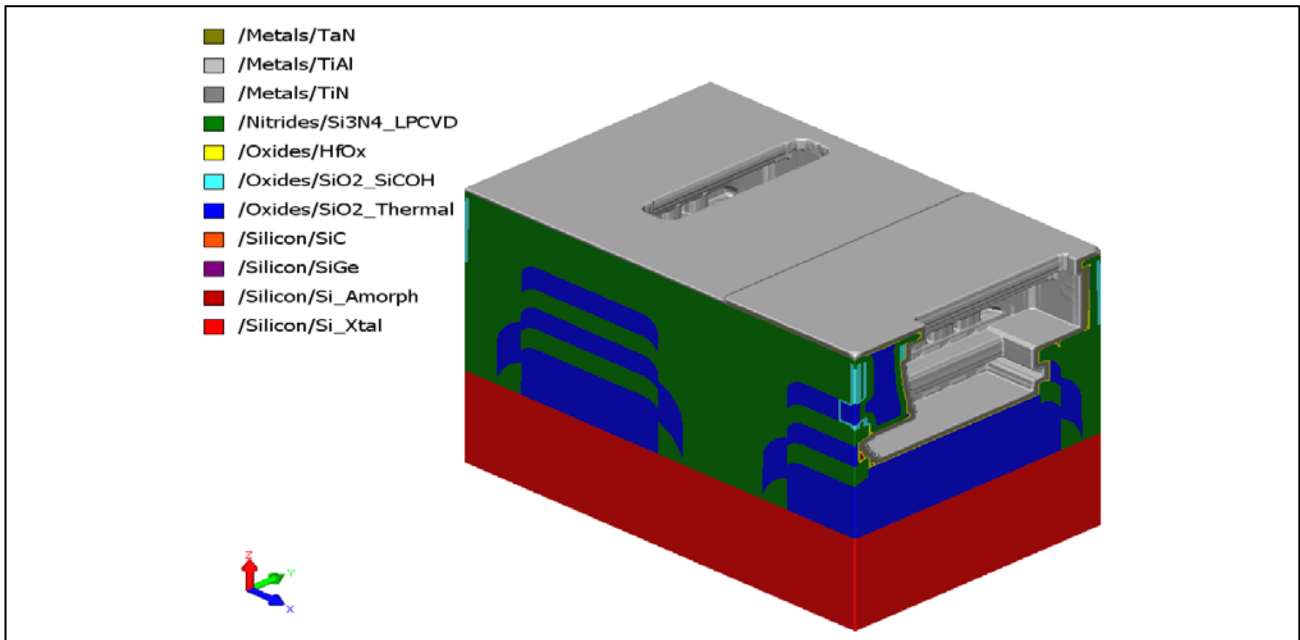
4.6.28. Remove Materials



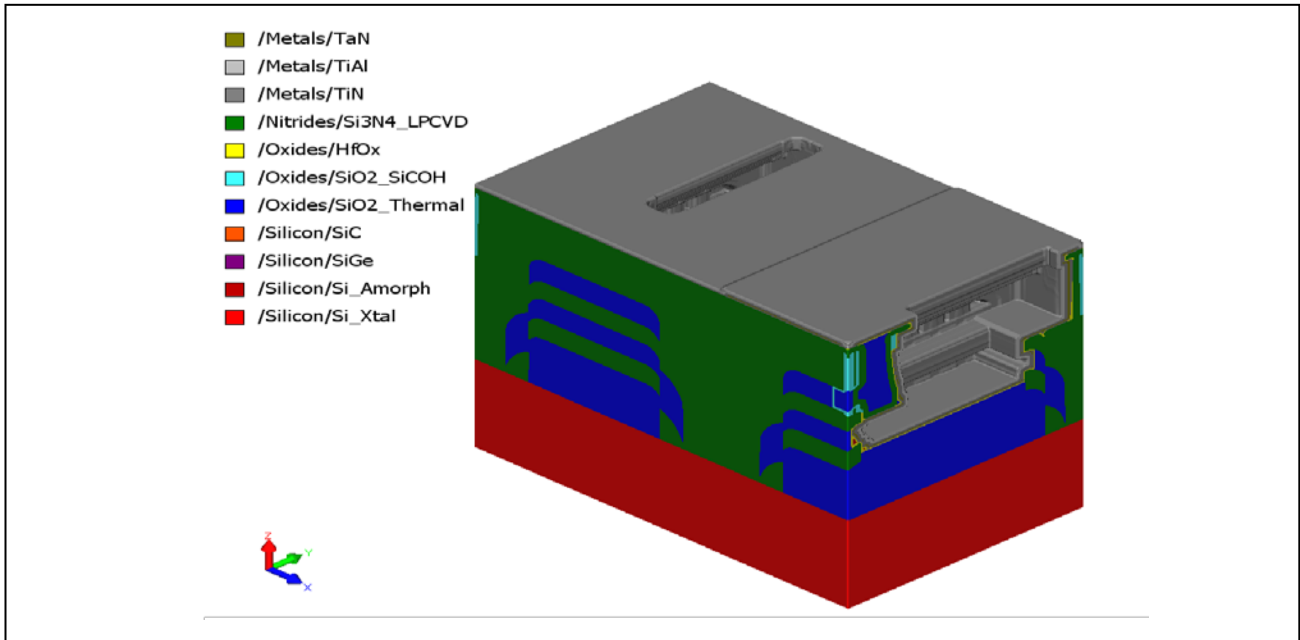
4.6.29. Conformal Deposit



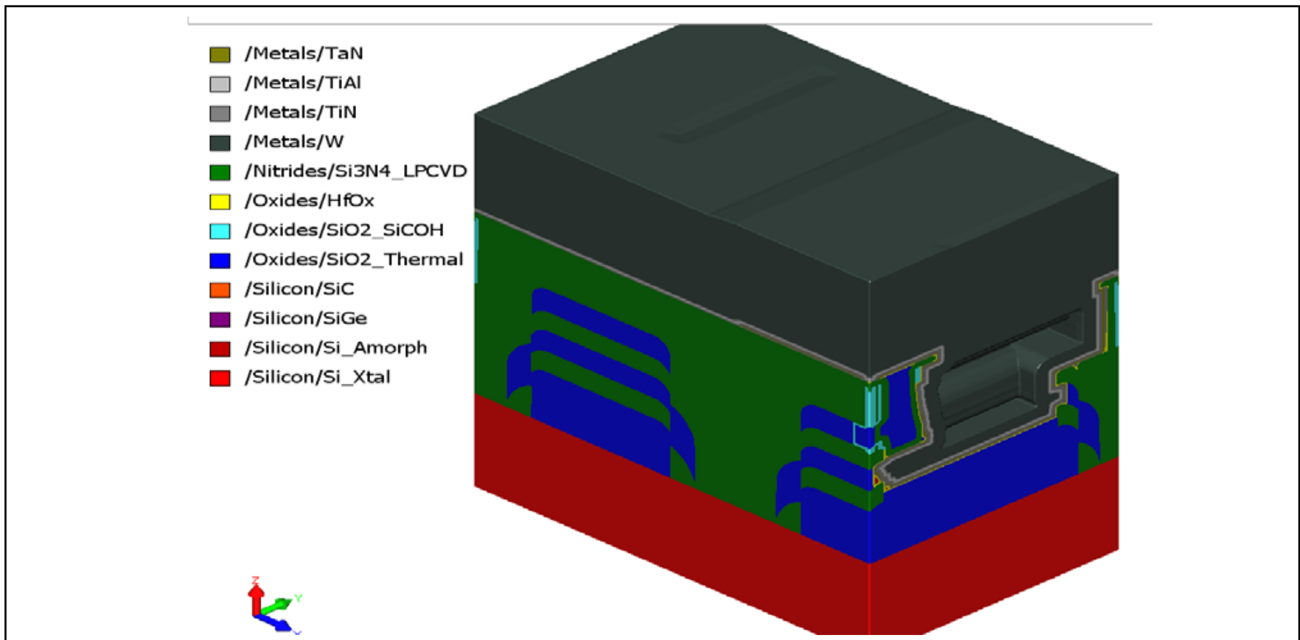
4.6.30. Conformal Deposit



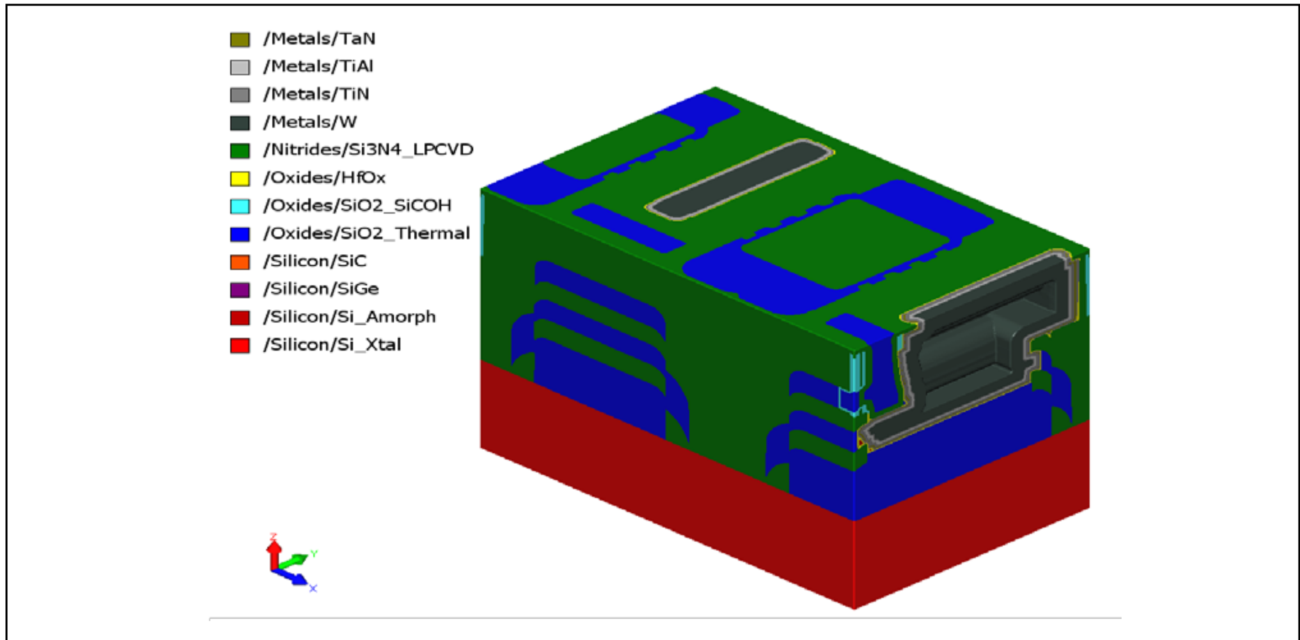
4.6.31. Conformal Deposit



4.6.32. Conformal Deposit

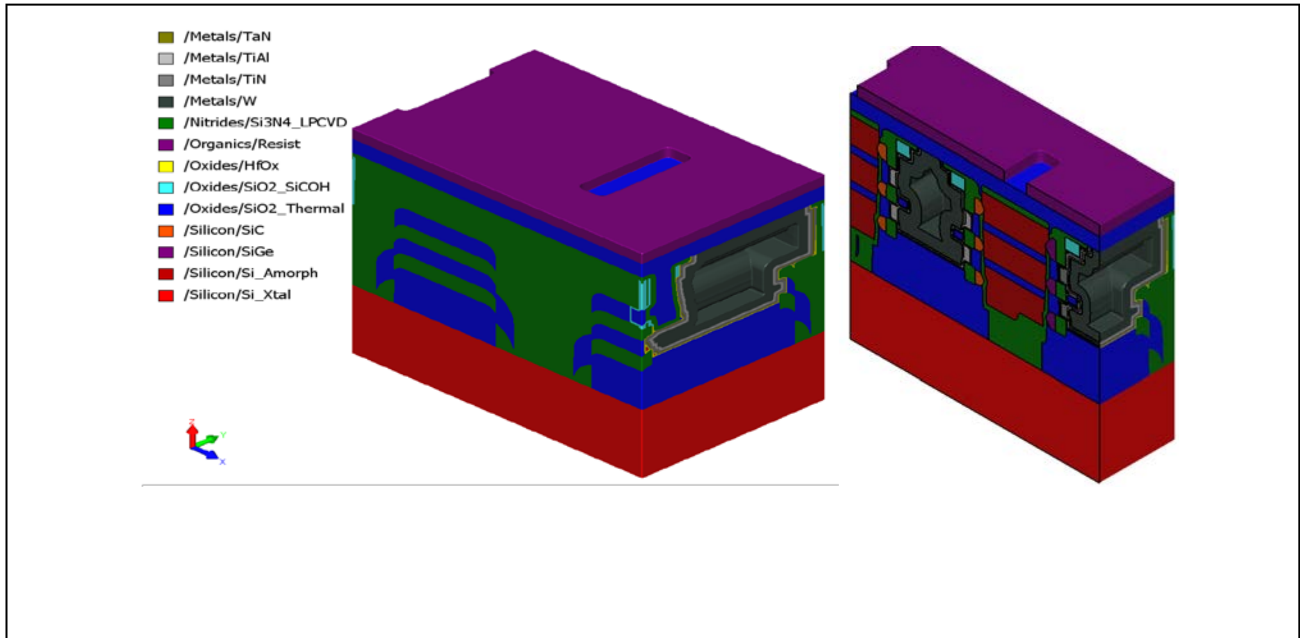


4.6.33. Reference CMP

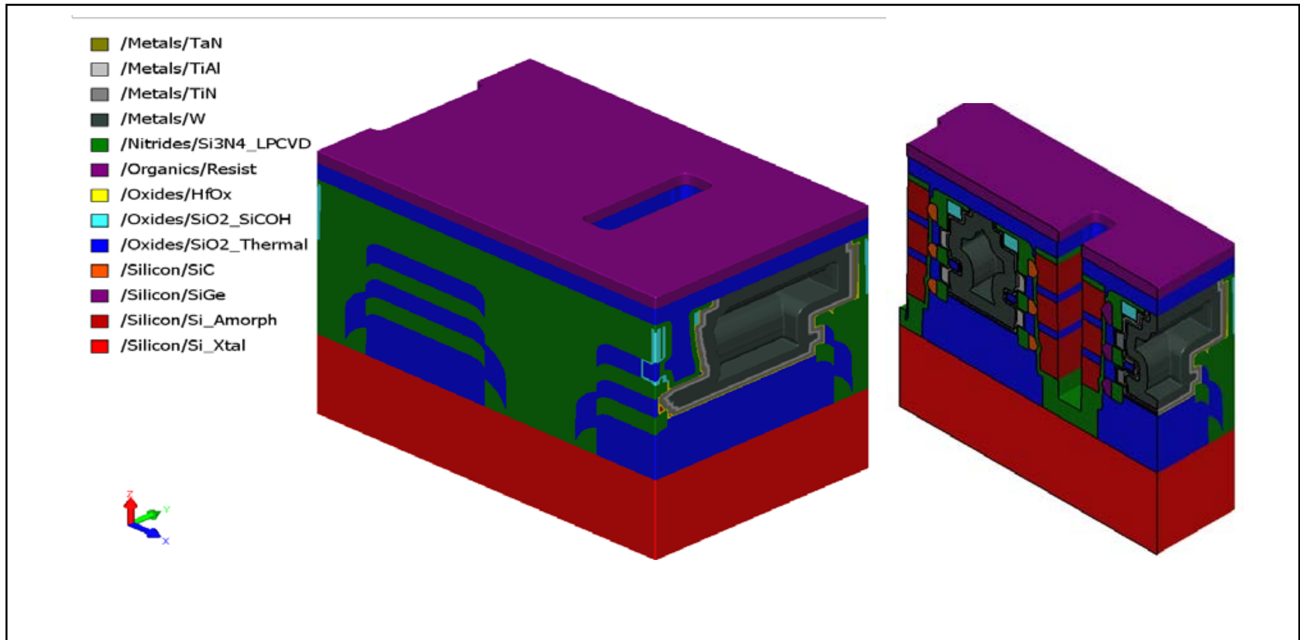


SD Contact module

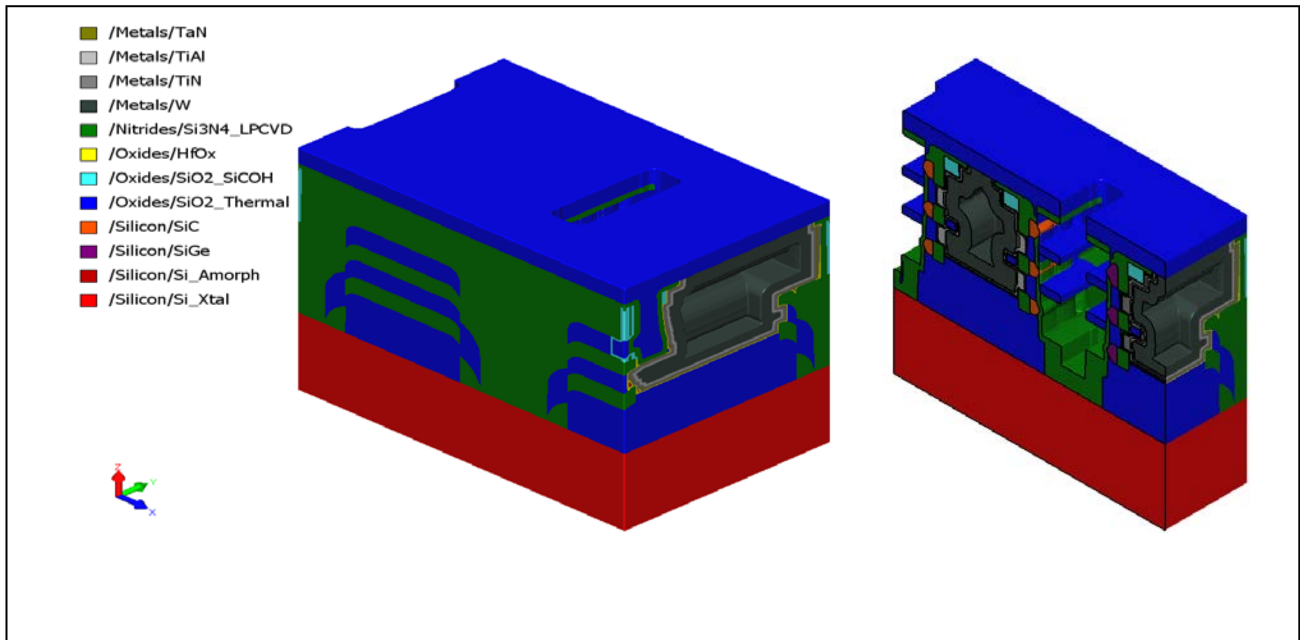
4.9.4. Expose Material



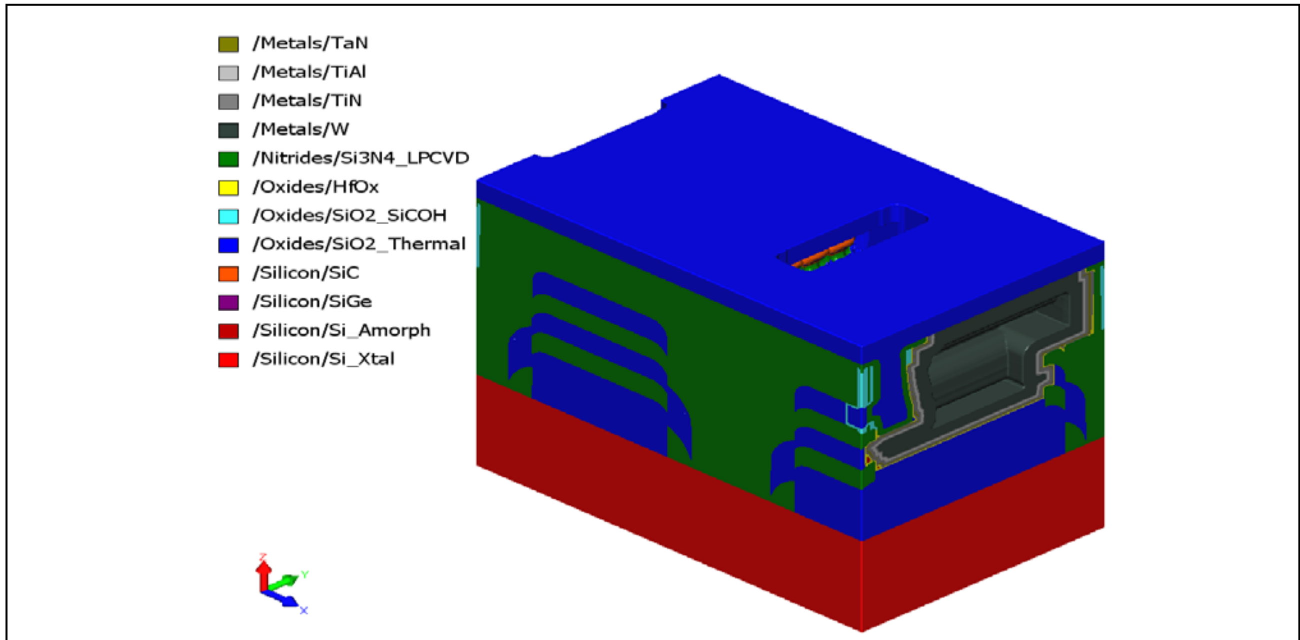
4.9.5. Basic Etch



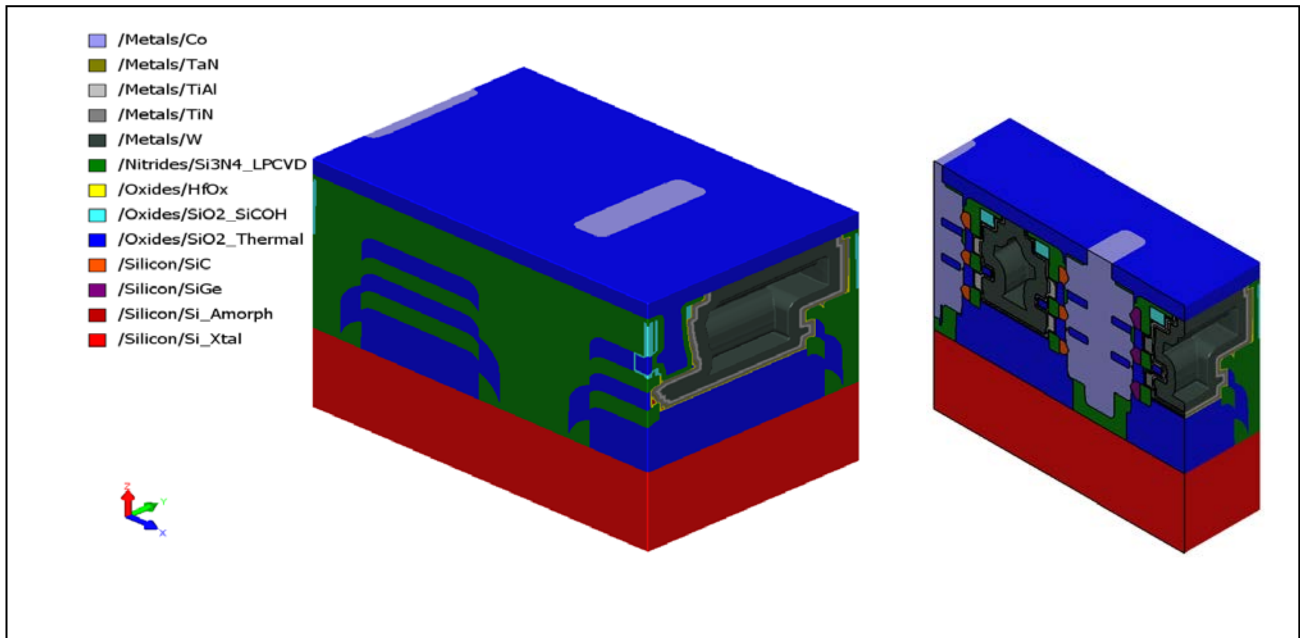
4.9.29. Basic Etch



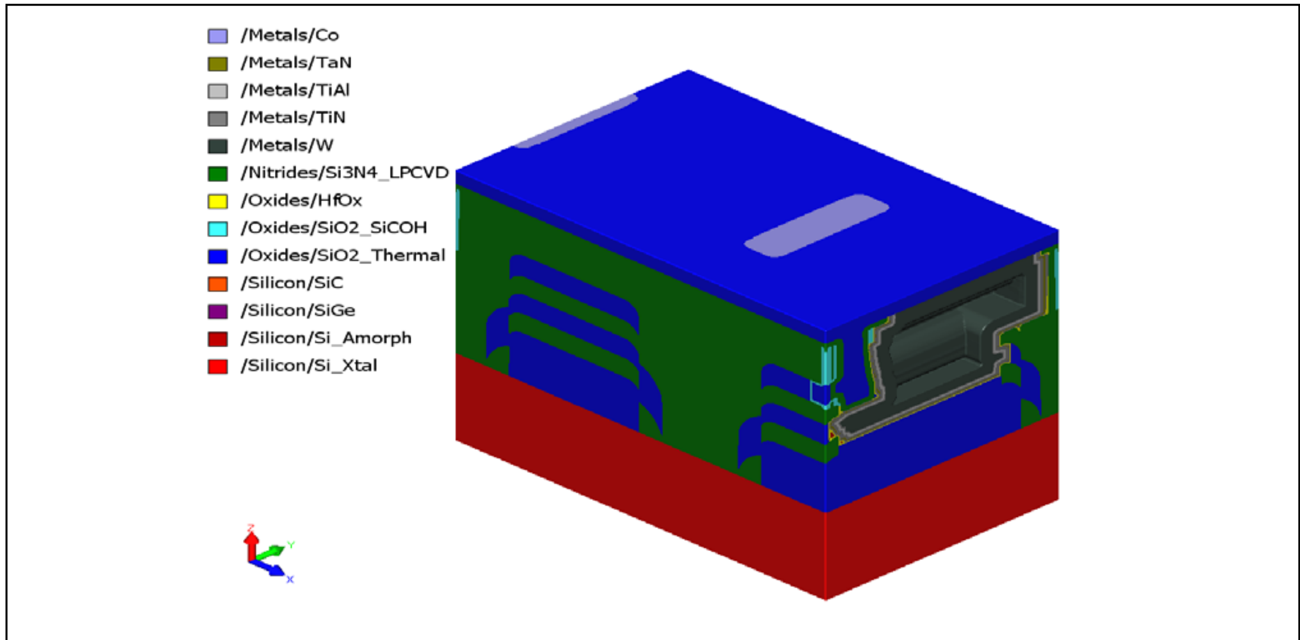
4.9.32. Straight Etch



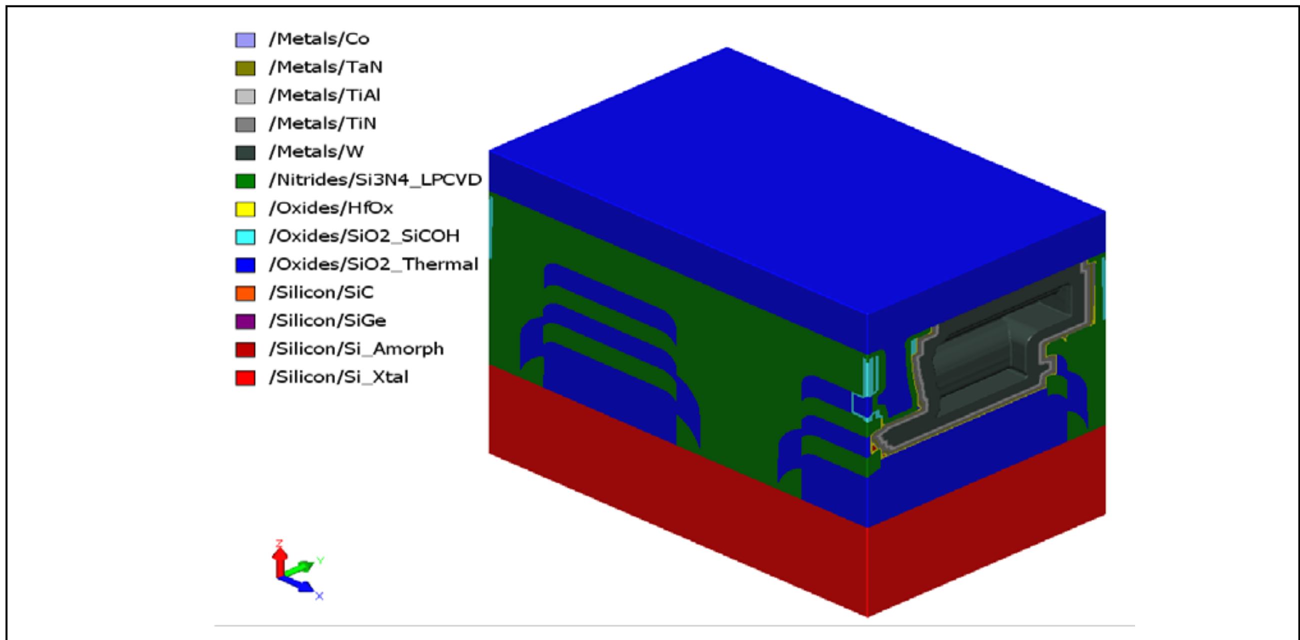
4.9.33. Planar Deposit



4.9.34. Reference CMP

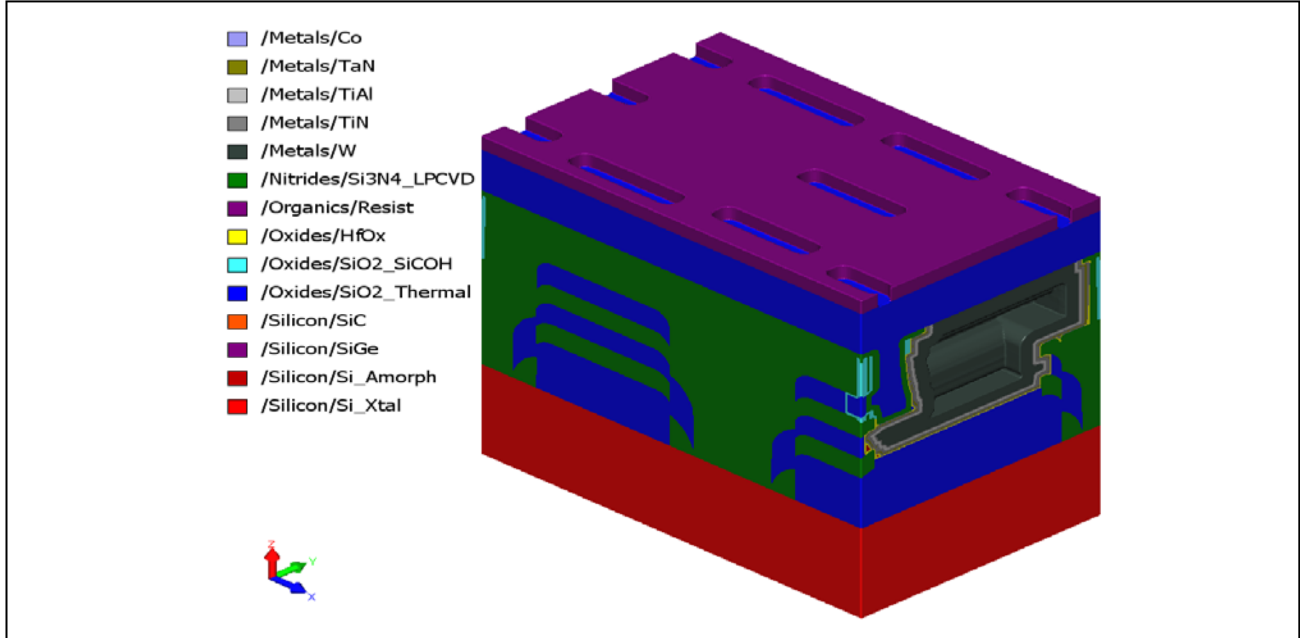


4.10.1. Straight Deposit

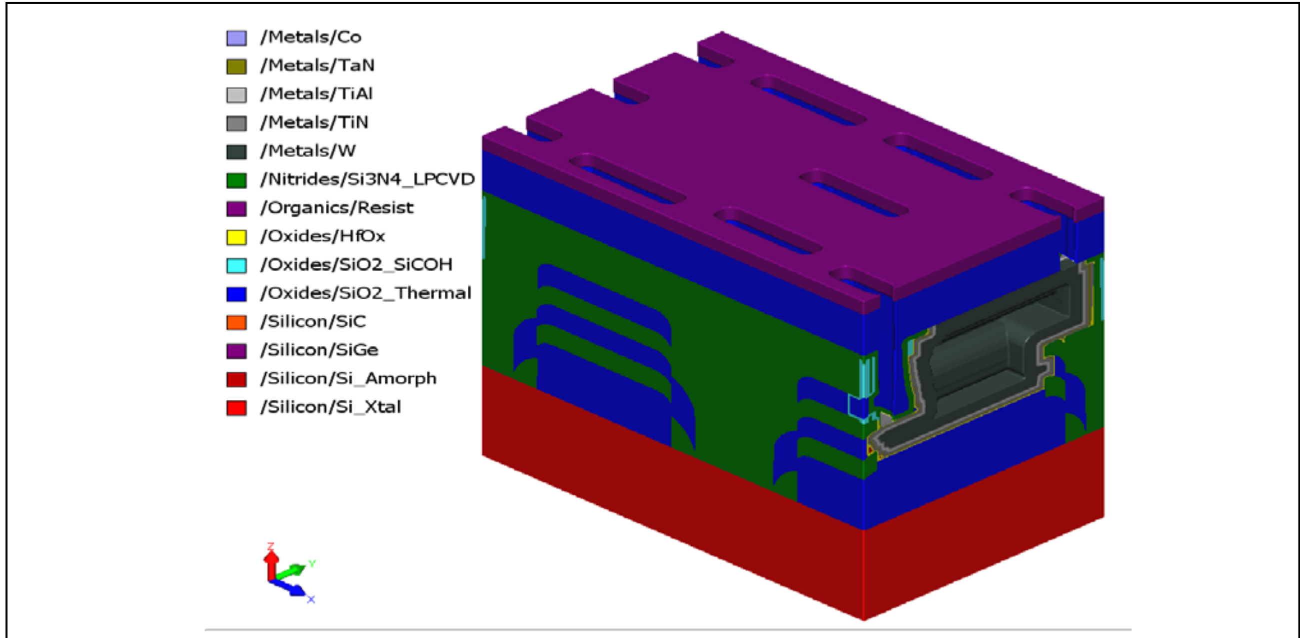


Contact Via and separation module

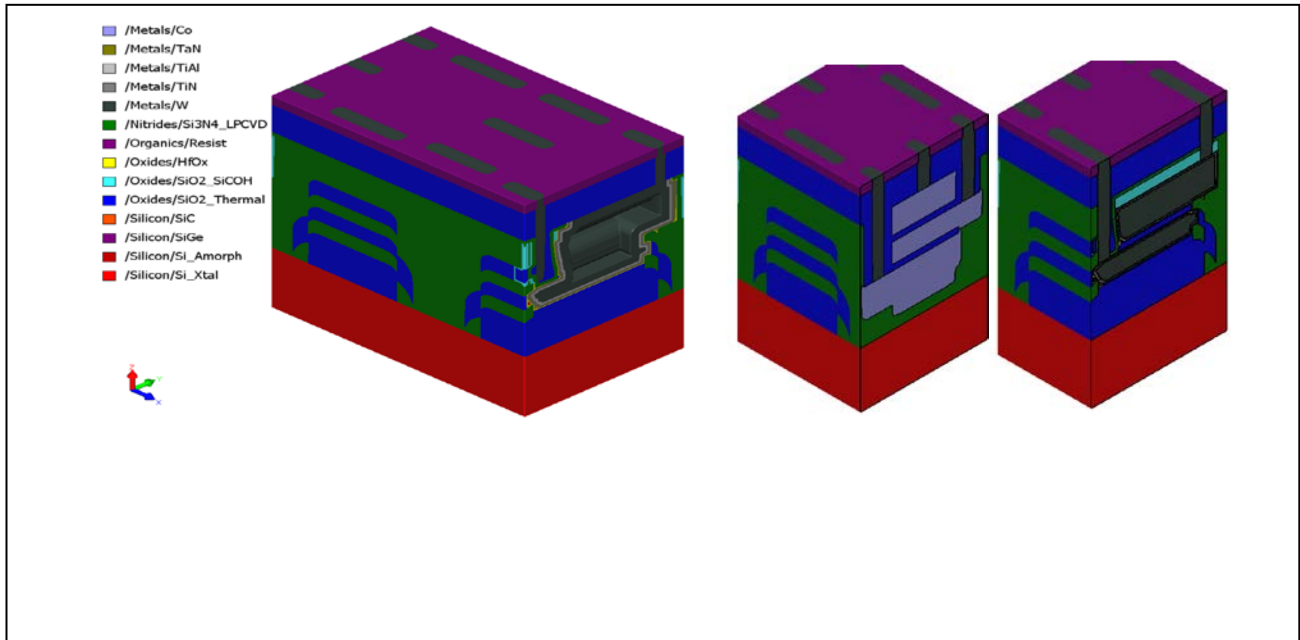
4.10.3. Expose Material



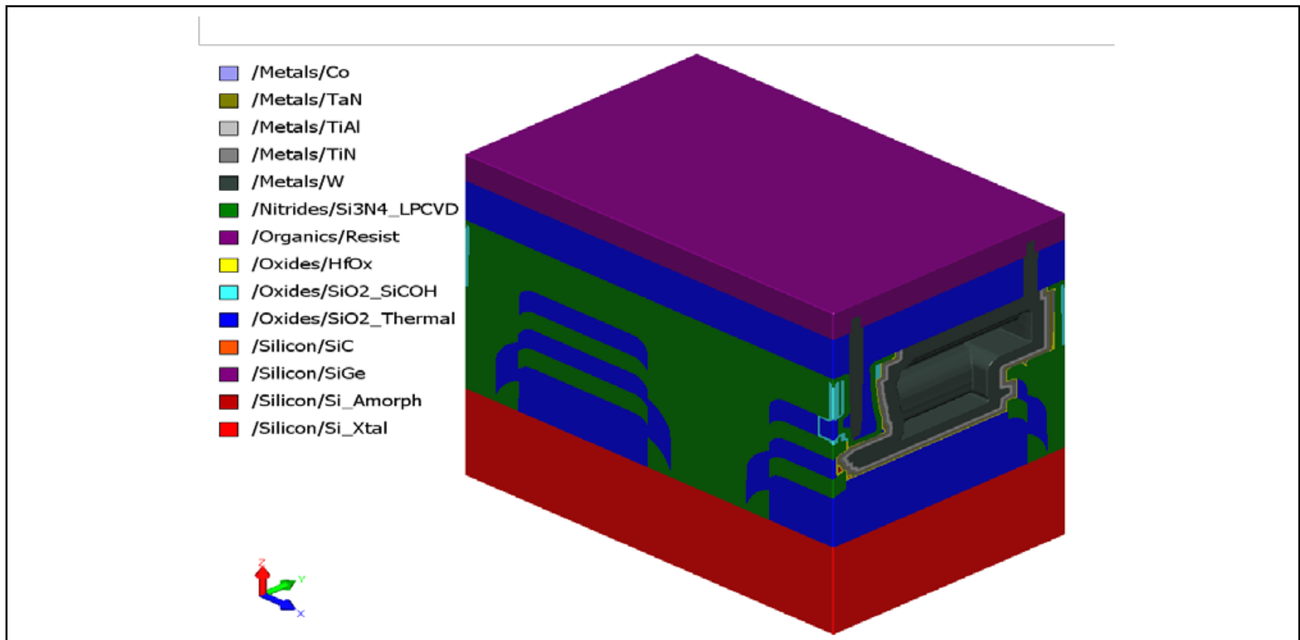
4.10.4. Basic Etch



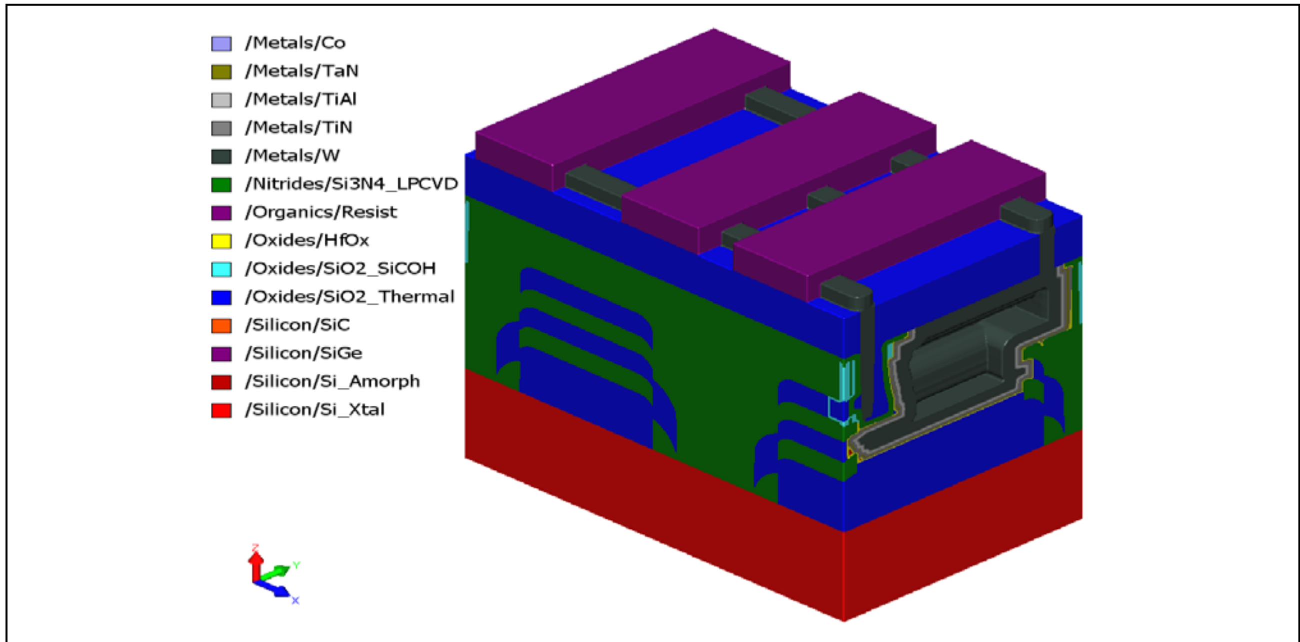
4.10.7. Planar Deposit



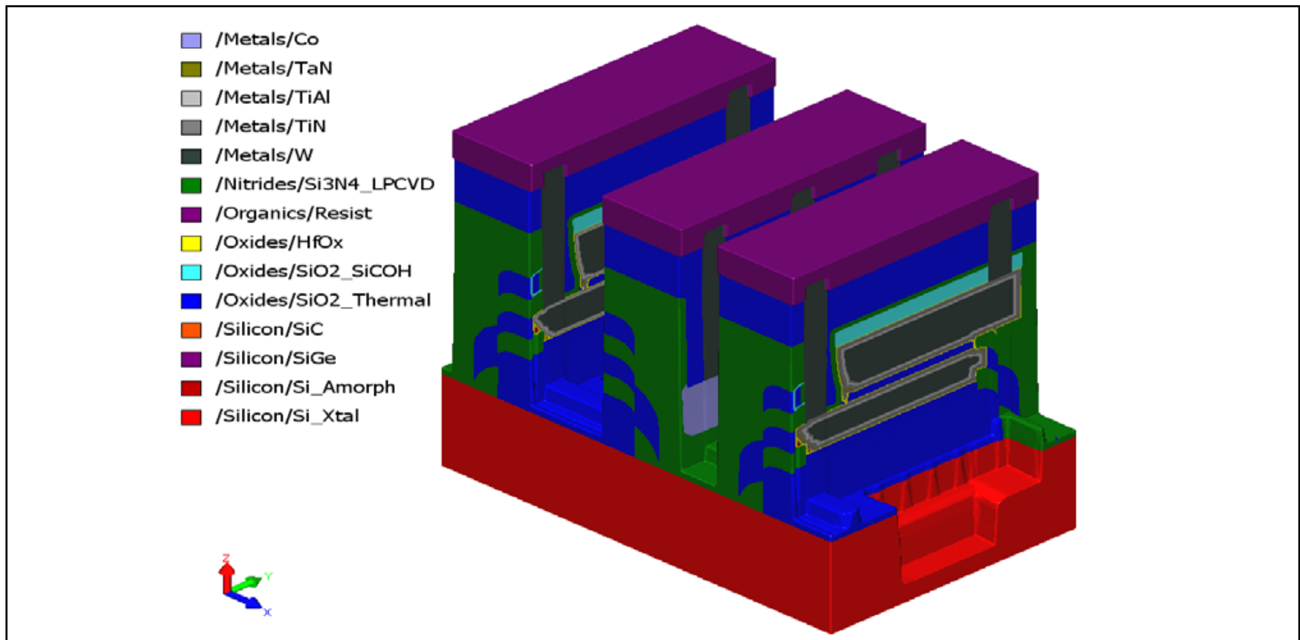
4.10.8. Straight Deposit



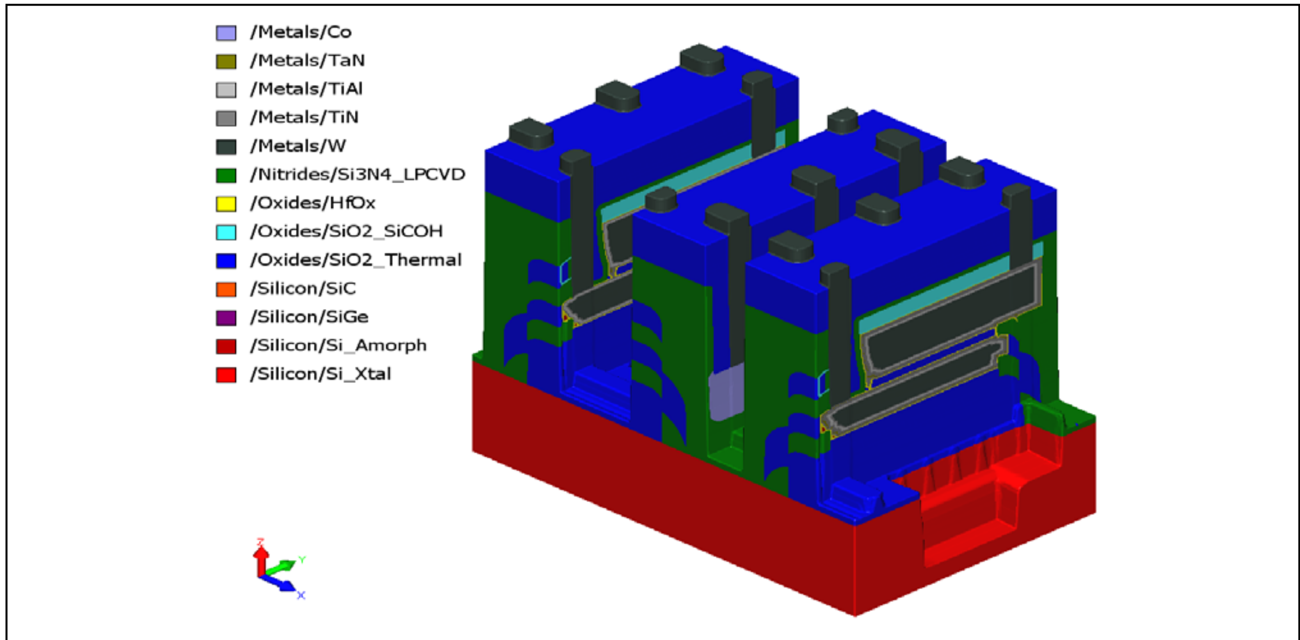
4.10.9. Expose Material



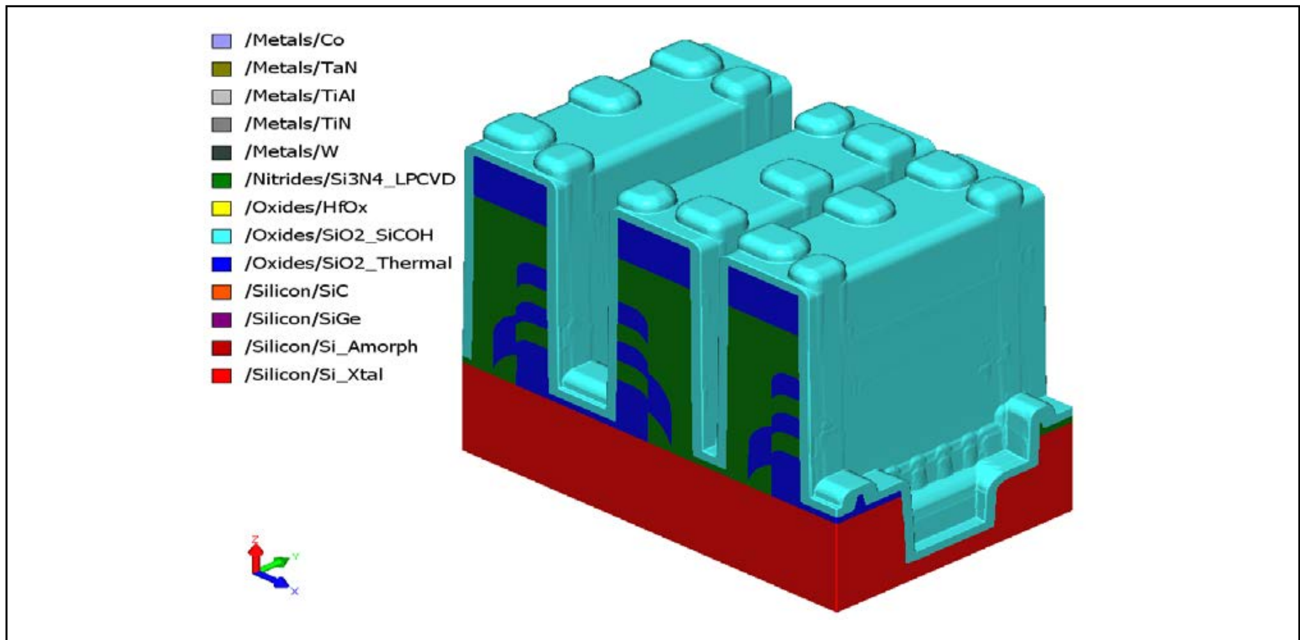
4.10.10. Basic Etch



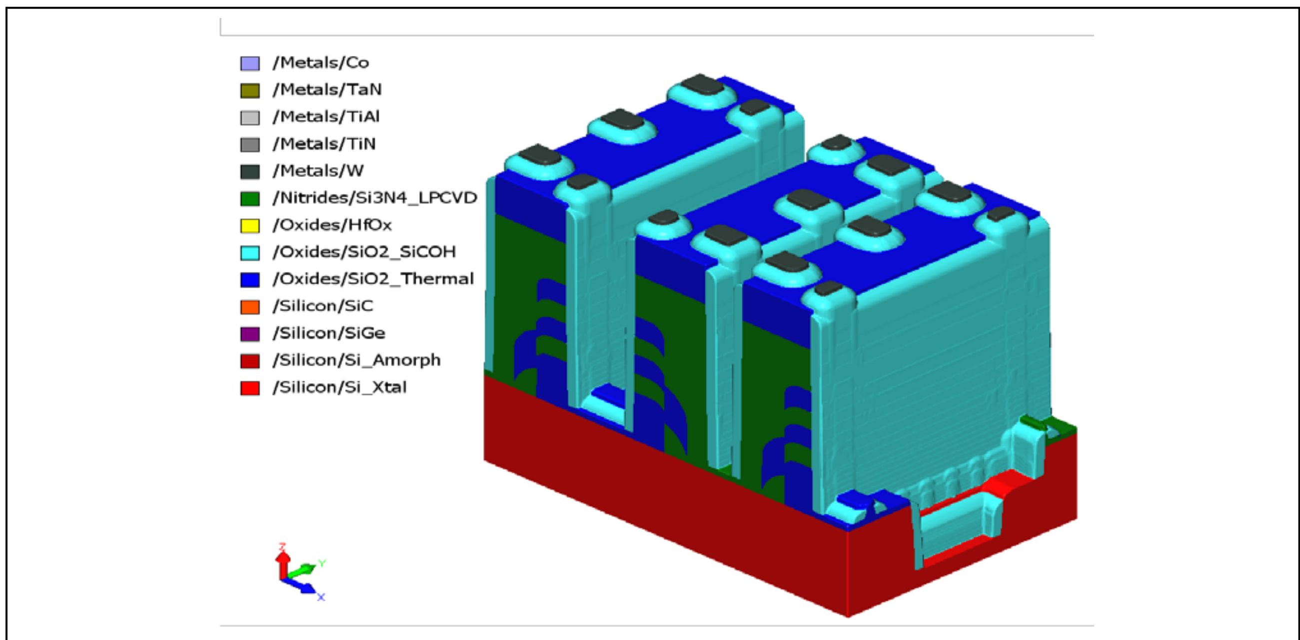
4.10.11. Remove Materials



4.10.12. Conformal Deposit



4.10.13. Straight Etch



4.10.14. Planar Deposit