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# Zigzag Double Forksheet Field Effect Transistor Architecture

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ZIGZAG DOUBLE FORKSHEET FIELD EFFECT TRANSISTOR ARCHITECTURE

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Abstract

Logic Forksheet is considered to be the evolution of FinFET technology after nanosheet architecture. The Forksheet architecture uses a forksheet gate that crosses multiple stacked nanosheets. Source/drain epitaxy is usually grown next to the gates requiring gate spacer formation, which causes potentially high parasitic capacitance between gate and source/drain. One approach is to move source/drain epitaxy also in a forksheet geometry on the opposite side of the gate to avoid spacer formation and reduce parasitic capacitance. This approach, however, is not scalable with a classical design due to an isotropic etch process in the process flow. The solution proposed below allows scaling down using double Forksheet architecture to less than the 3nm node using a zigzag shape during fin patterning.

Problem

Scaling of transistors has consistently produced increased performance, area gains, power reduction and decreased cost. To continue the scaling path, manufacturers are switching from planar MOSFET to 3D FinFET transistor architectures. In a FinFET device, the channel between the source and drain terminals is in the form of a fin. The gate wraps around the 3D channel and provides control from 3 sides of the channel. The multi-gate structure eliminates short-channel effects, which started to degrade performance at reduced gate lengths.

The 3D nature of the FinFETs allows increased fin height to produce higher device drive current in the same footprint. As scaling is pushed beyond 5nm, FinFETs are expected to encounter problems. At reduced gate length, the FinFET structure fails to provide enough electrostatic control. Lower track height standard cells require a transition to single-fin devices, which cannot provide sufficient drive current even when fin height is increased.

Vertically stacked nanosheet transistors include a FinFET that is arranged on its side and divided into separate horizontal sheets or channels. A gate fully wraps around the channel. The gate-all-around nature of the nanosheet provides superior channel control as compared to the multi-gate FinFET. At the same time, the more optimal distribution of the channel cross-section in the 3D volume optimizes the effective drive per footprint.

The migration to nanosheet devices becomes optimal at low cell track heights of 6T and 5T, where fin depopulation degrades drive current in traditional FinFET-based cells. Reducing track heights (and cell area) from 6T to 5T cannot happen without introducing structural scaling boosters such as buried power rails and wrap-around contacts.

Power rails, providing power to the different components of the chip, are traditionally implemented as metal lines in the chip's back end of line (BEOL). In that location, however, they occupy considerable space. In a buried power rail construct, the power rails are buried in the chip's front-end-of-line (FEOL) to help free up routing resources for the interconnects. Moreover, they provide a lower resistive local distribution of the current to a technology that suffers from increasing BEOL resistance with pitch scaling. By removing the power rails from the back-end-of-line, the standard cell height can be further reduced from 6T to 5T.

Smaller track heights require reduction of cell height and much tighter spacing between nFET and pFET devices within the cell. However, for both FinFET and nanosheet devices, process limitations pose a limit on spacing. In FinFET architectures, for example, 2 dummy fin spacings are typically required between n and p, consuming up to 40-50% of the total available space.

To extend scalability, a forksheet device has been introduced. The forksheet is an extension of the nanosheet device. Unlike nanosheet devices, the sheets are now controlled by a forked gate structure, which is realized by introducing a dielectric wall in between the p- and nMOS devices before gate patterning. This wall physically isolates the p-gate trench from the n-gate trench, allowing a much tighter n-to-p spacing.

A ZIGZAG DOUBLE FORKSHEET FIELD EFFECT TRANSISTOR ARCHITECTURE
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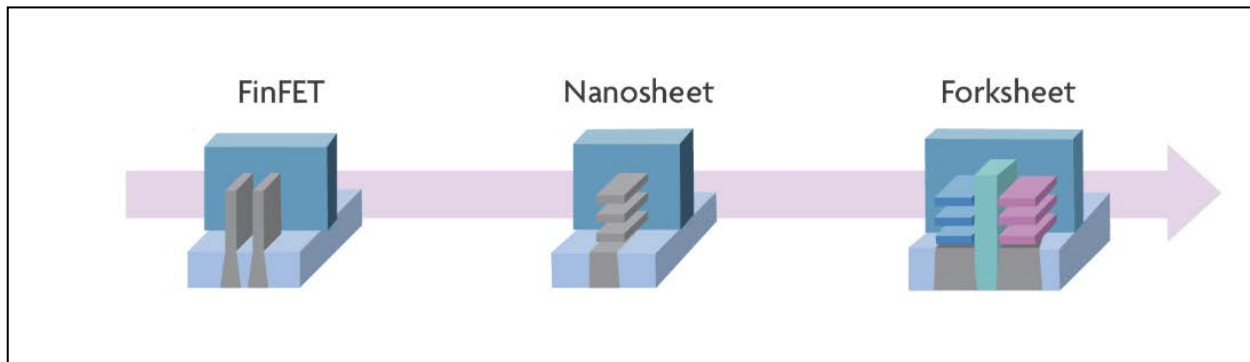
In a forksheet FET, source/drain epitaxy is grown on the sides of the gate (similar to the FinFET case). This approach requires formation of a spacer on the gate to isolate the gate from the source/drain epitaxy. This in turn causes high parasitic gate-to-source/drain capacitance due to proximity effect. The parasitic capacitance limits the number of nanosheets that can be used (currently, a maximum of 3 nanosheets can be used).
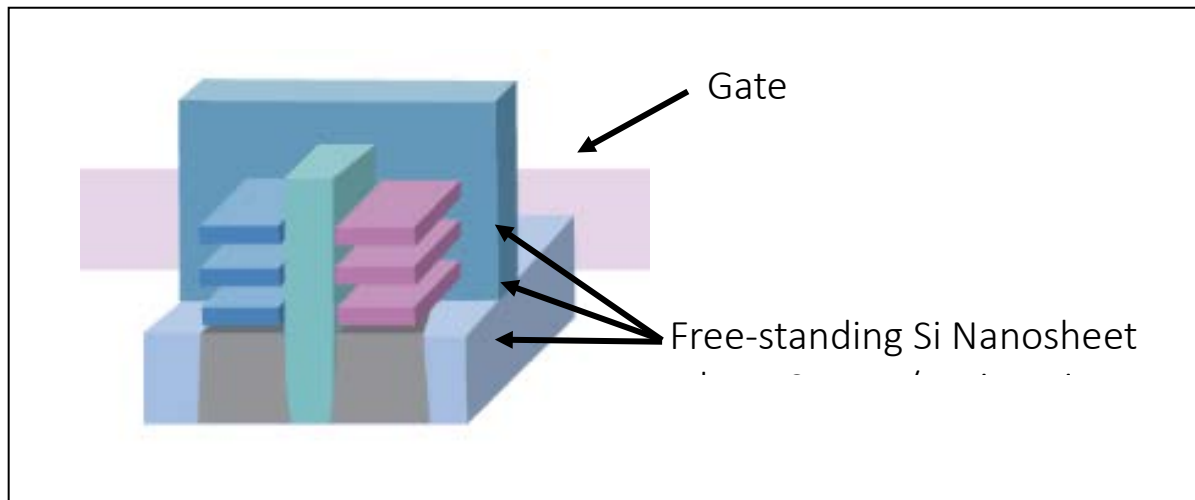


One solution is to also form the source/drain EPI on the opposite side of the gate using a forksheet approach.

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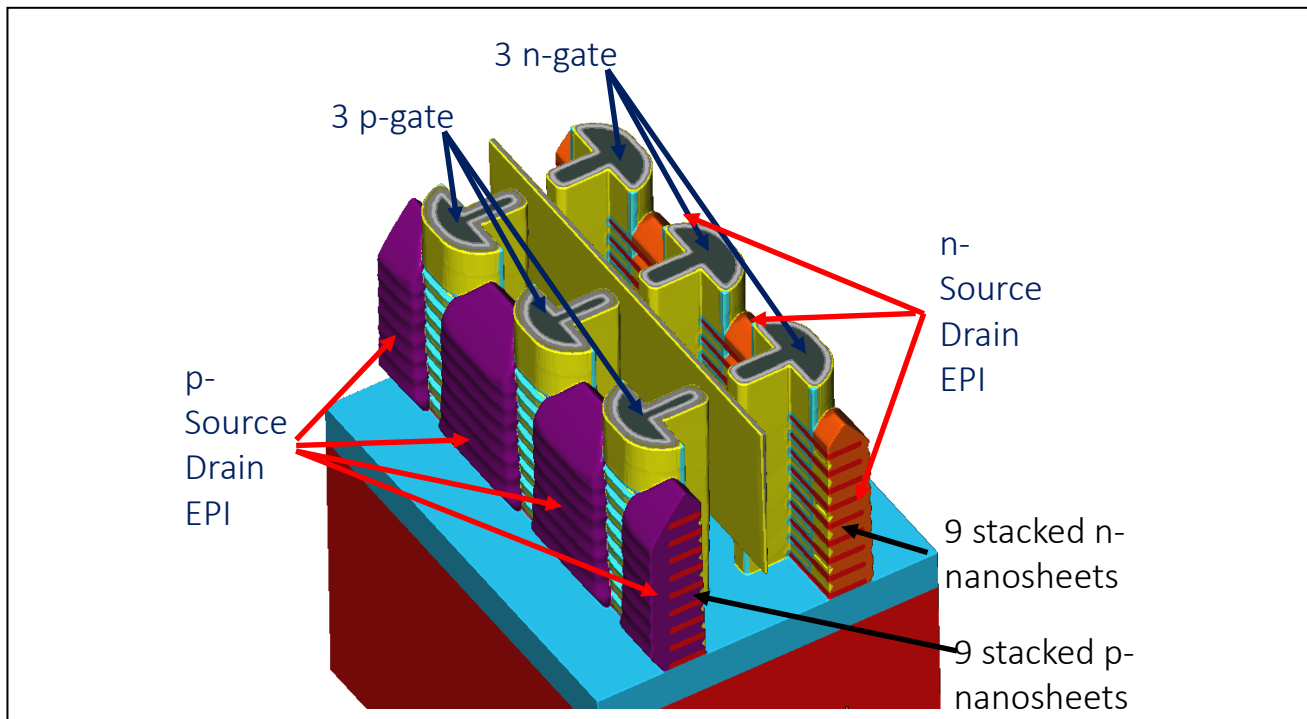
One concern with this approach is scalability. Dummy gate is performed by filling a cavity formed by isotropic lateral etch of the sacrificial SiGe layers present in between the Si nanosheets. This isotropic etch induces an "umbrella" shape for the dummy gate.

Space in-between the dummy gate is required to introduce source/drain EPI. Tight contact poly pitch (CPP) below 42nm cannot be achieved for 10-15nm wide nanosheets.
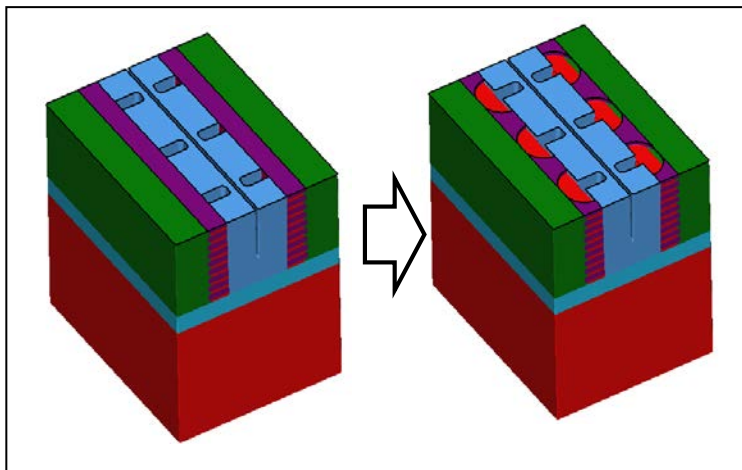


In order to allow scalability of the double forksheet approach, the umbrella shape needs to be modified. There is no practical solution for changing the etch isotropy. One option that has been proposed is to add

dopant implantation to slow down the lateral etch rate.  However, this solution has not been easy to implement.

## Description

The present disclosure relates to an improved double forksheet approach using a zig-zag shape during Fin patterning.  This approach has two key benefits.  Additional distance can be created in between the gate forksheet and the source/drain forksheets without impacting the gate contact poly pitch.  The dummy gate "umbrella profile" can be modified by starting the etch from a corner interface allowing reducing contact poly pitch (CPP).  This allows the architecture to scale down to CPP < 42nm (31nm), Fin pitch=35nm, Fin width=10-15nm.



ZigZag Fin patterning

Dummy gate formation
(acces opening, SiGe lateral etch, a-Si filling)

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Source/Drain EPI          Replacement Metal Gate
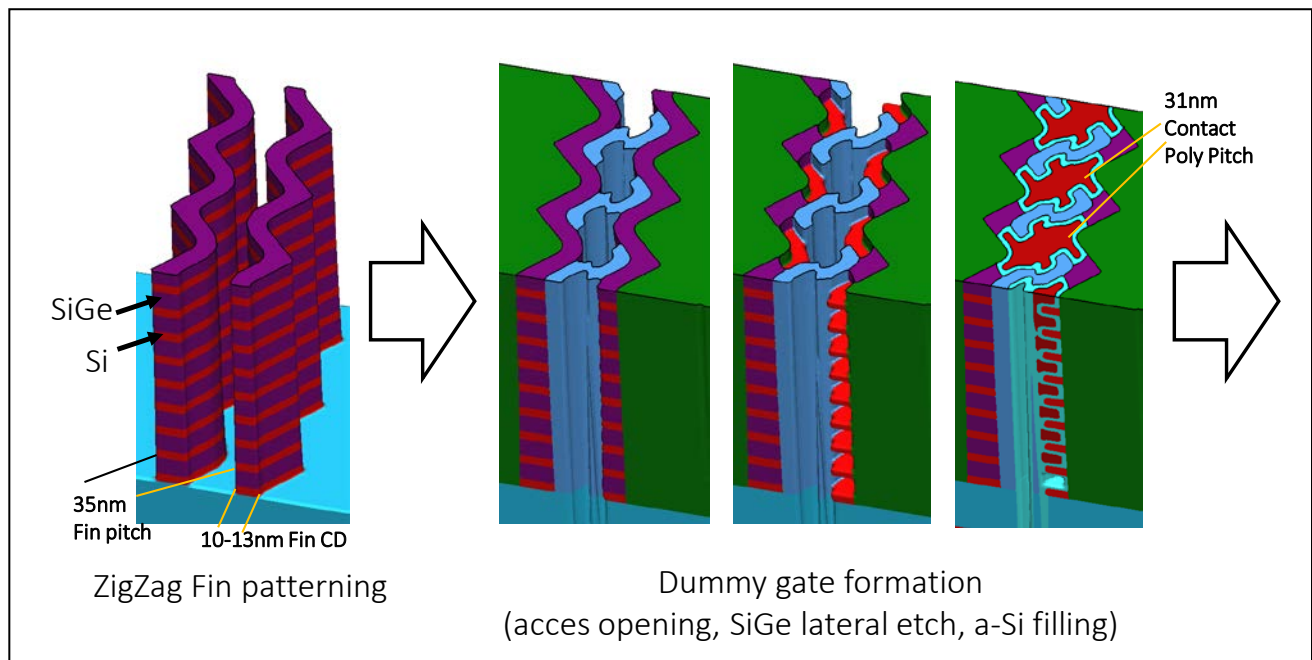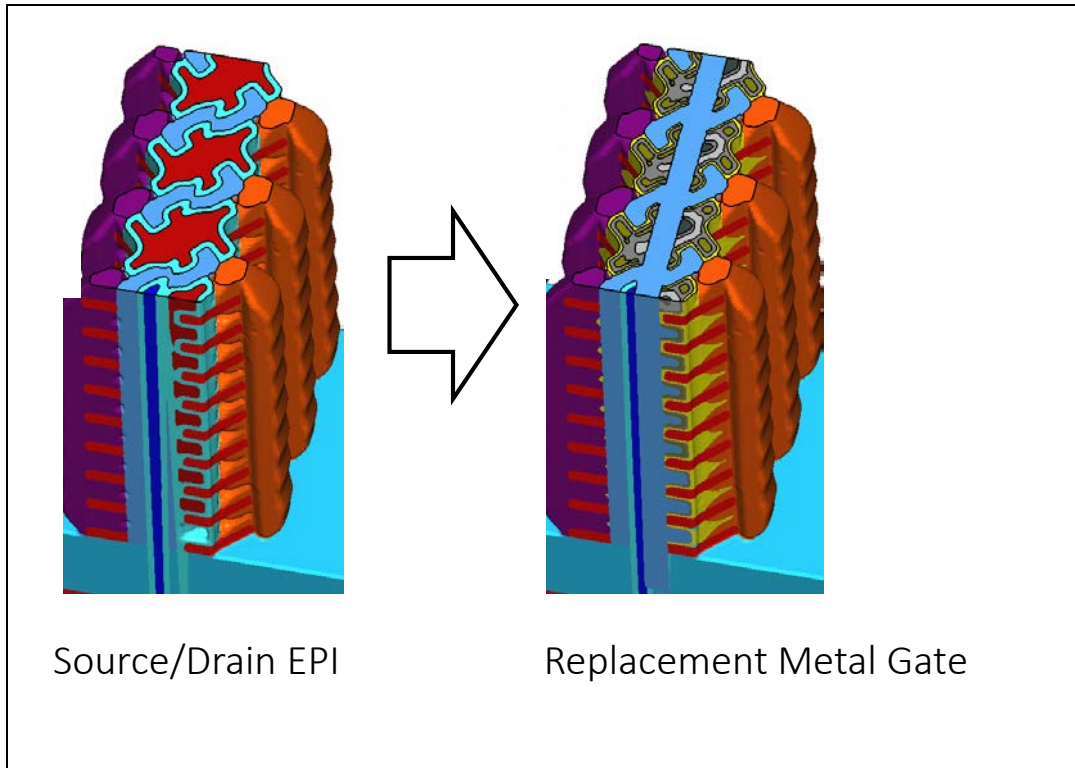
The following example relates to 6T-SRAM fabrication.

**1.      Fin patterning module**

SOI starting material:
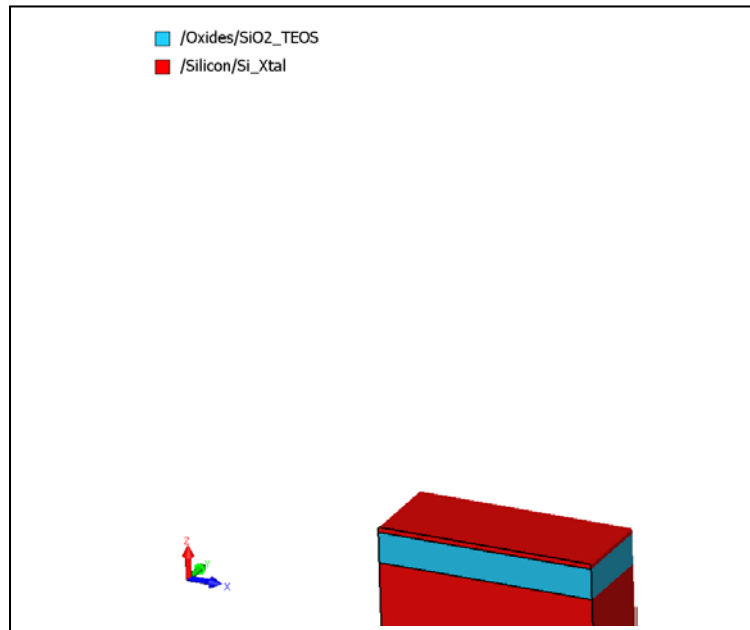
Si/SiGe EPI growth + Nitride deposition:

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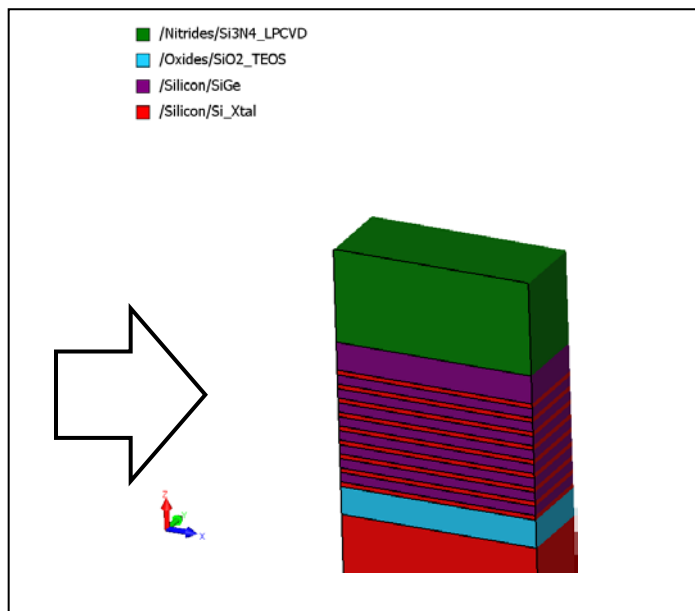
Zig-Zag mandrel patterning for Self Aligned Double Patterning:



- /Nitrides/Si3N4_LPCVD
- /Organics/ODL
- /Organics/Resist
- /Oxides/SiO2_TEOS
- /Silicon/SiARC
- /Silicon/SiGe
- /Silicon/Si_Xtal

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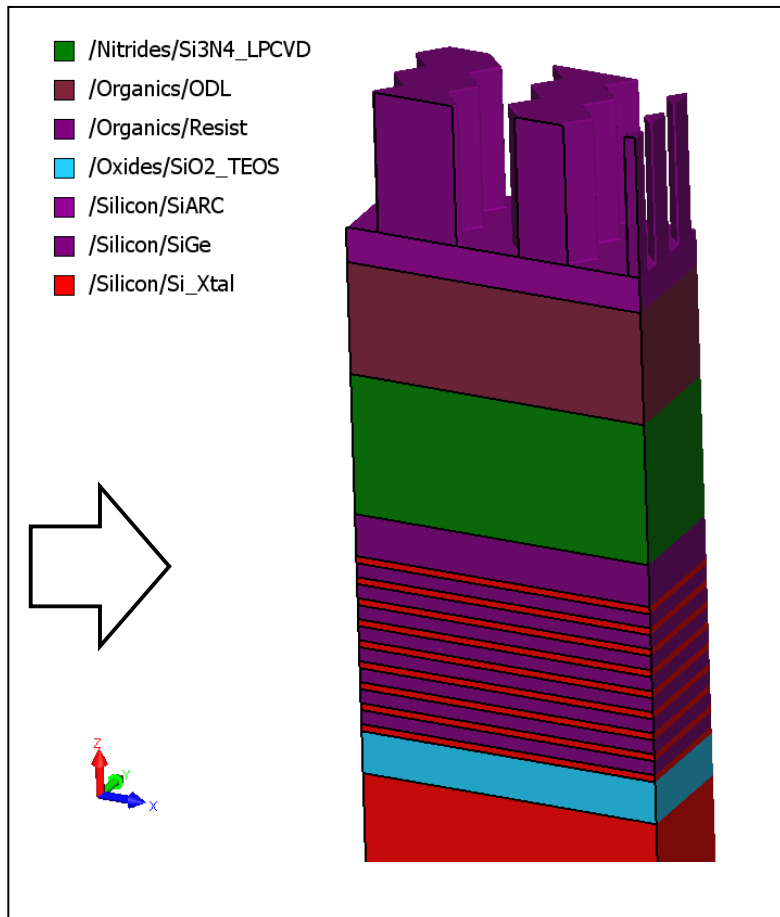
**2.        Fin etch and cladding**

Hard mask formation (spacer deposition, etch and resist removal)



Si/SiGe/Nitride etch

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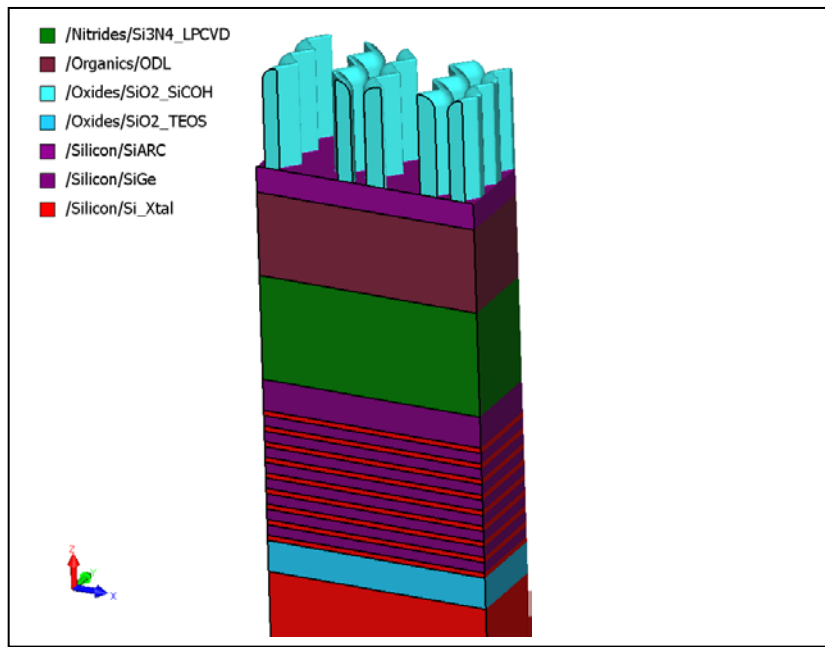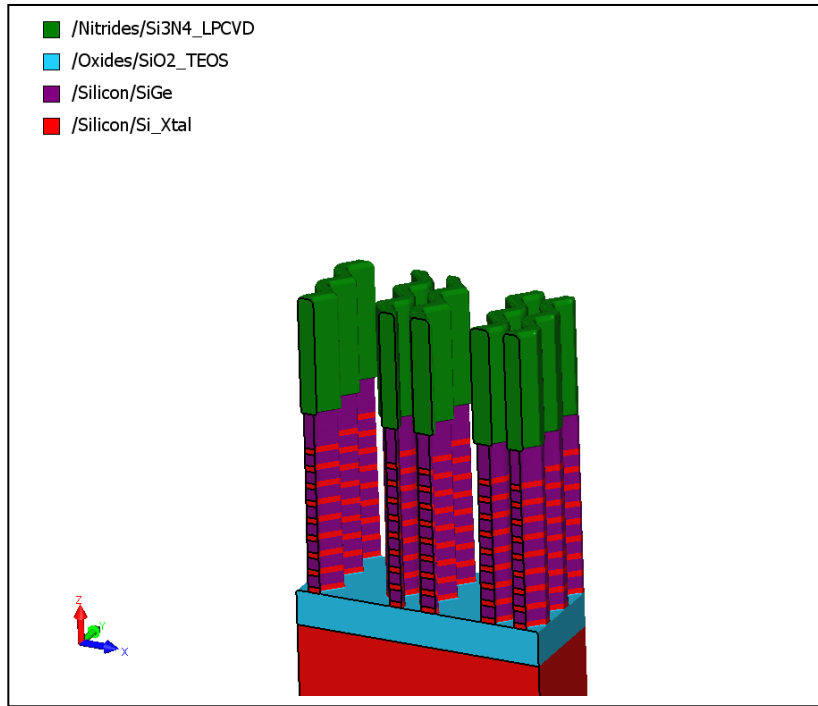
Oxide conformal deposition
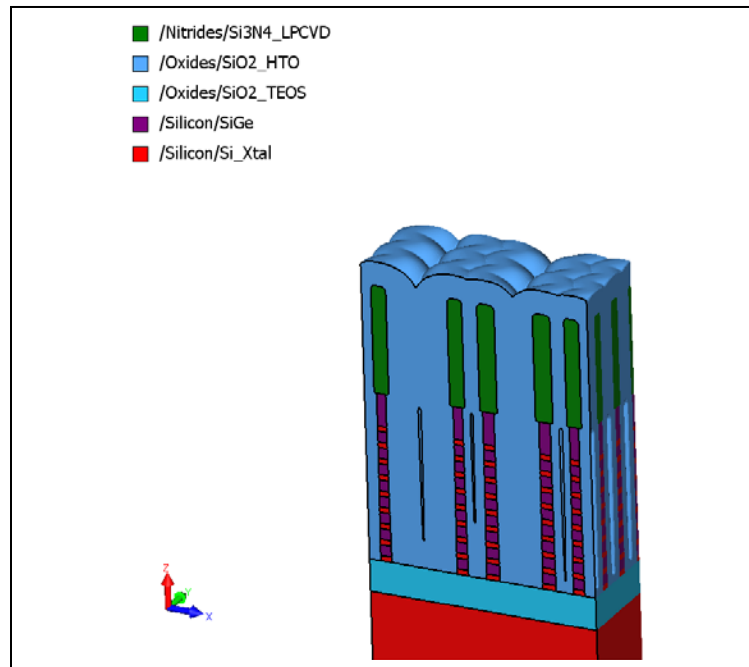


In some examples, the fins have 2 different fin pitches (1 and 2). Fin pitch can be controlled using lithography.

### 3.     Wall formation and Nitride cladding

Oxide wall formation by oxide etch:

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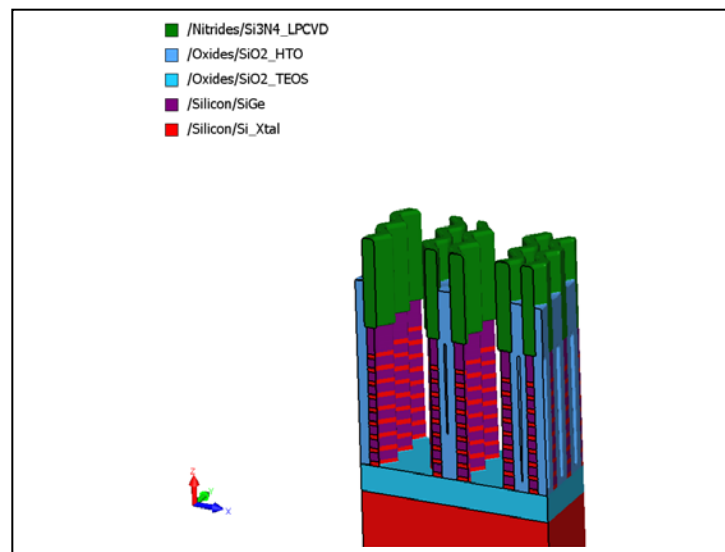
Nitride deposition and CMP:
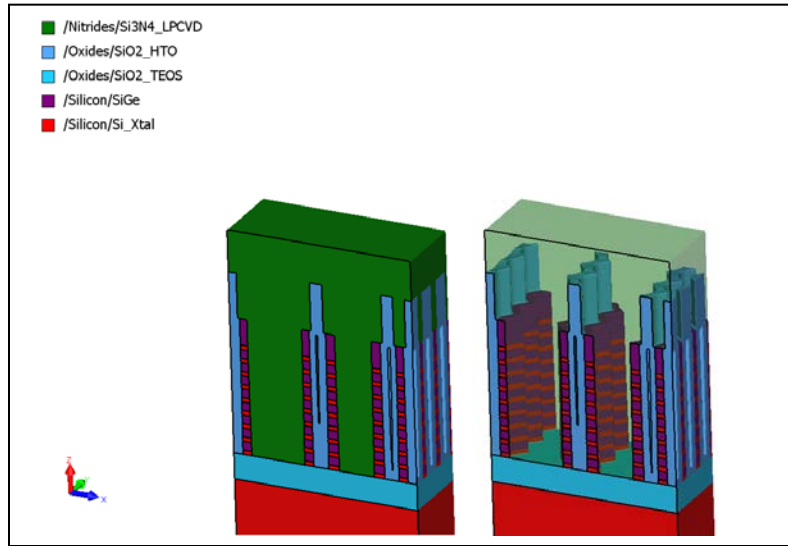


## 4. Dummy Gate patterning module:

The lithography pattern is tilted 45deg in order to i) create a large opening by merging n- and –p-gate and ii) maintain isolation between adjacent gates:

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Nitride etch:



Oxide etch:

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SiGe isotropic etch:

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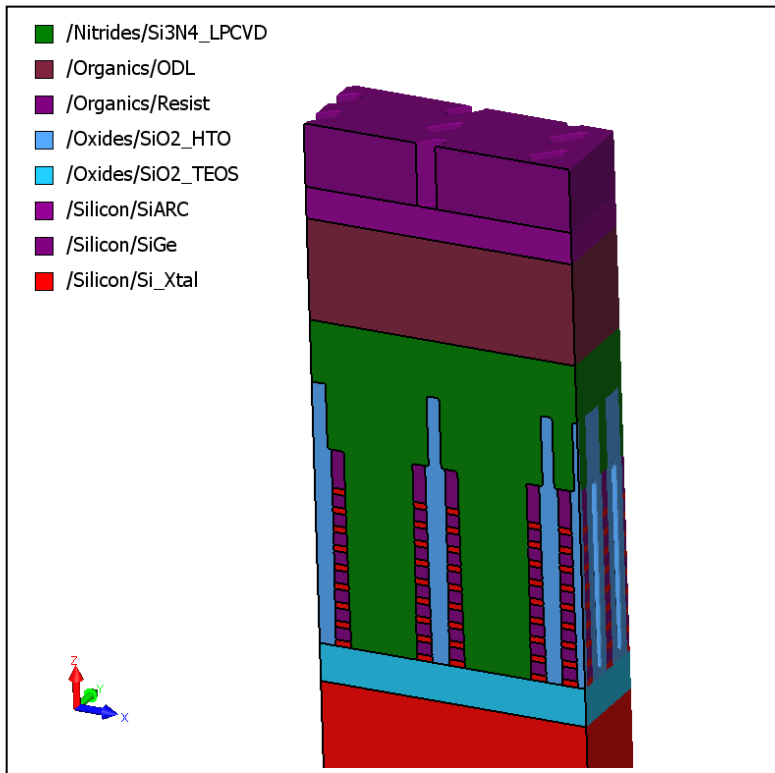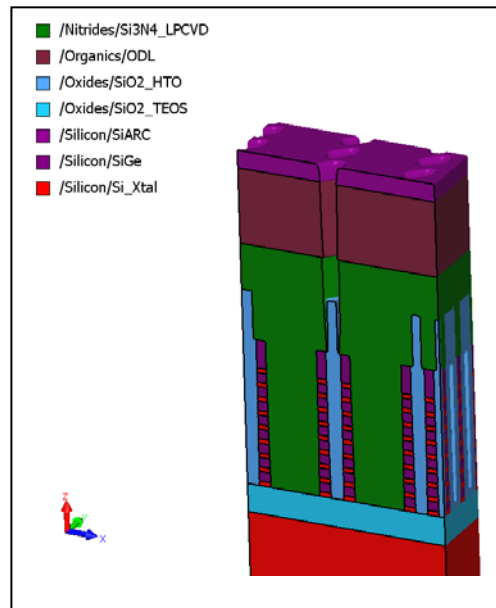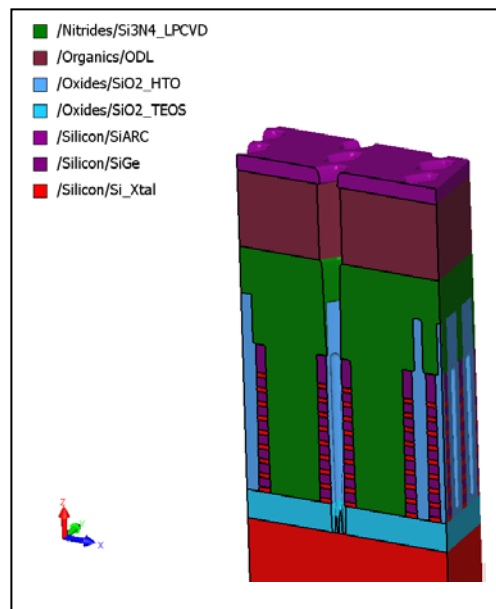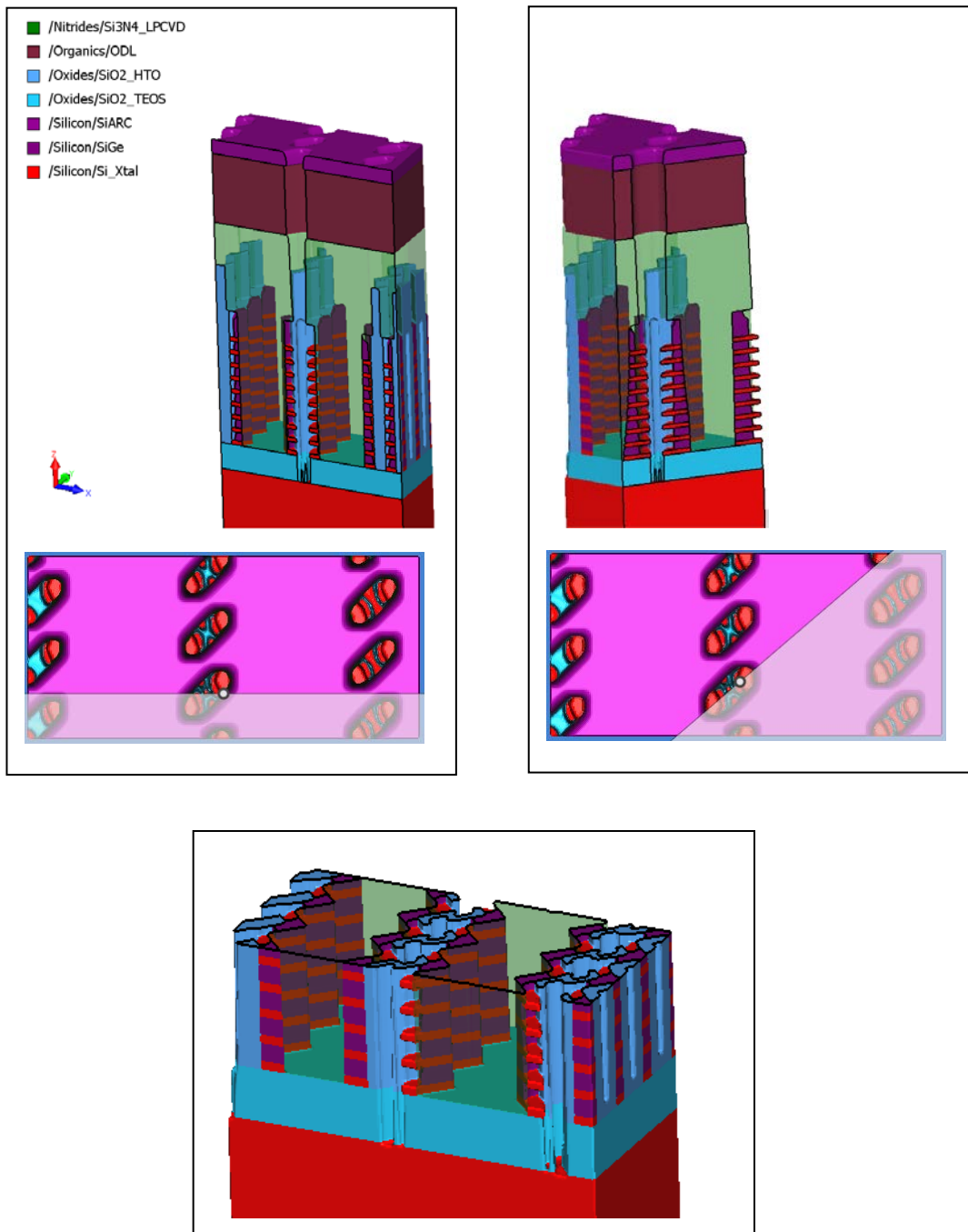
## 5.      Dummy gate filling (with amorphous Si) and capping

Cavity filled with a-Si:
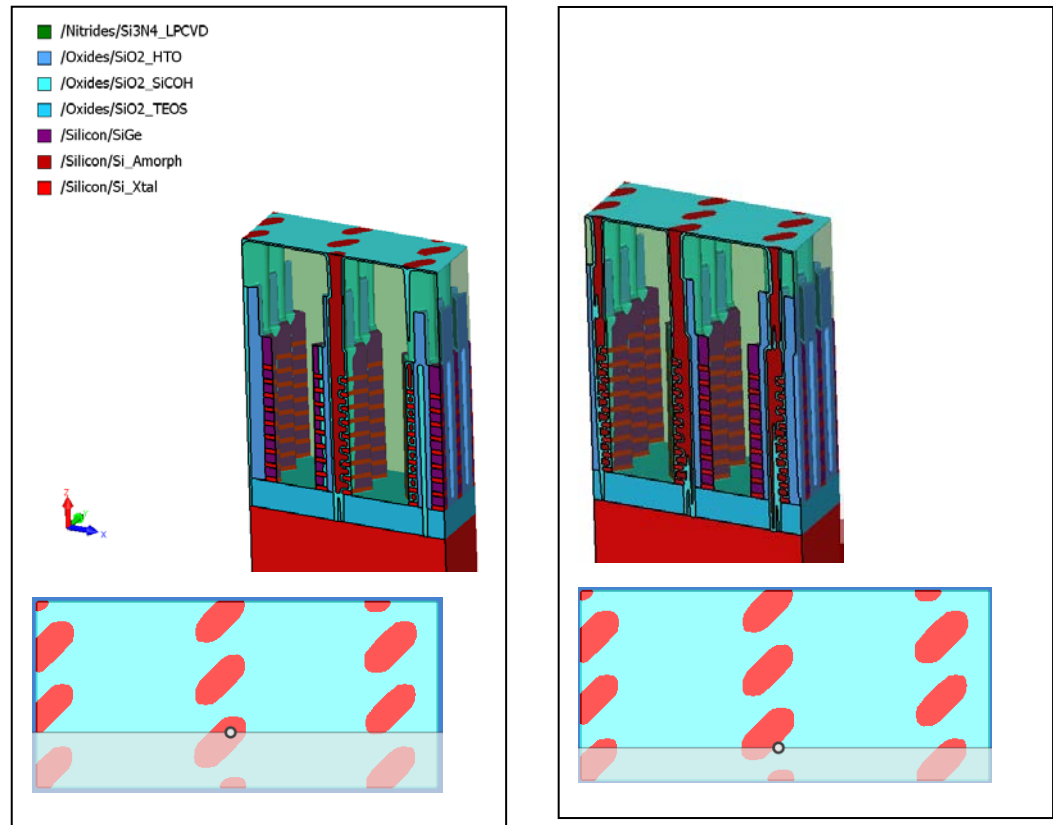


A-Si recess and oxide plug formation:
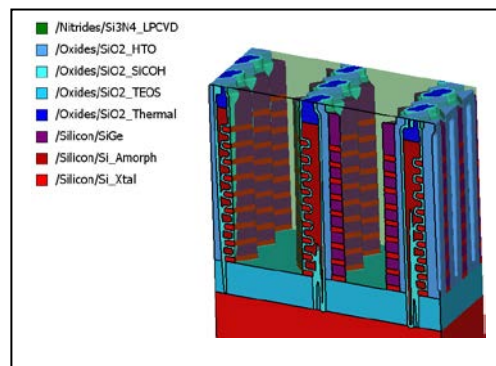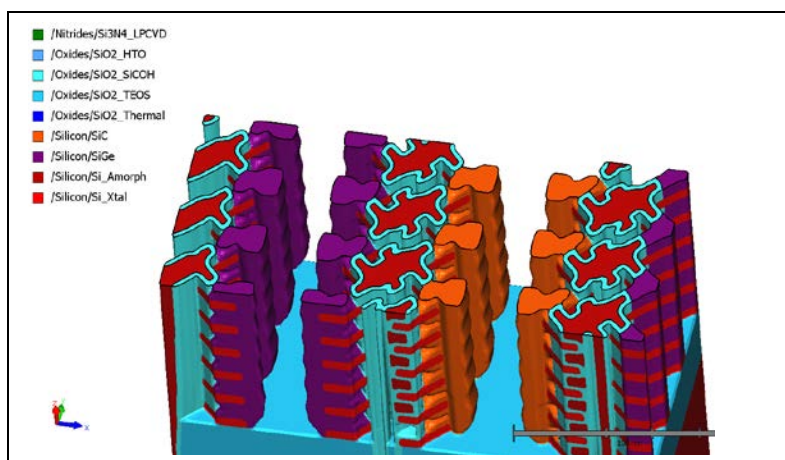
## 6.        n- and p- Source/Drain EPI

n- Source/Drain EPI:
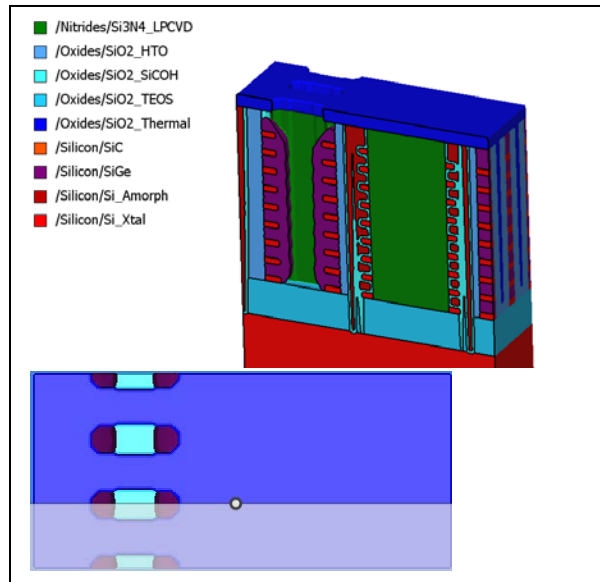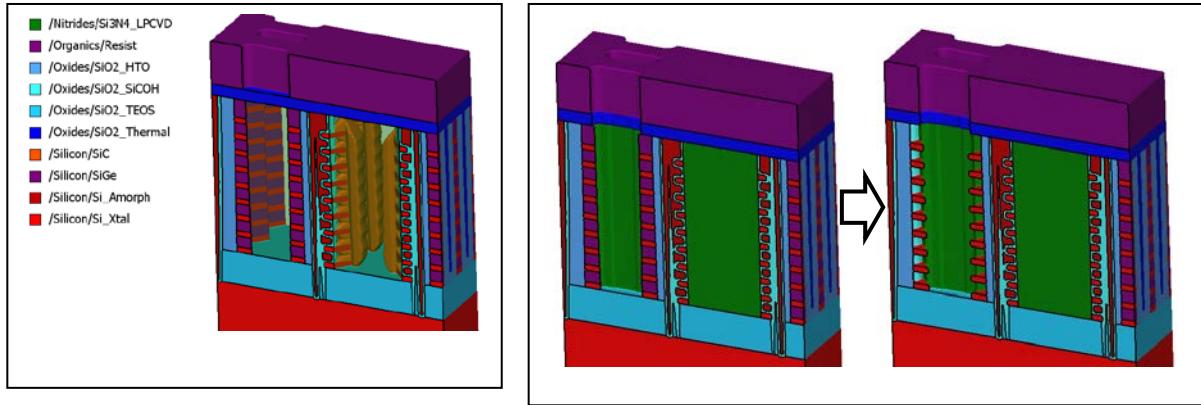
p- Source/Drain EPI
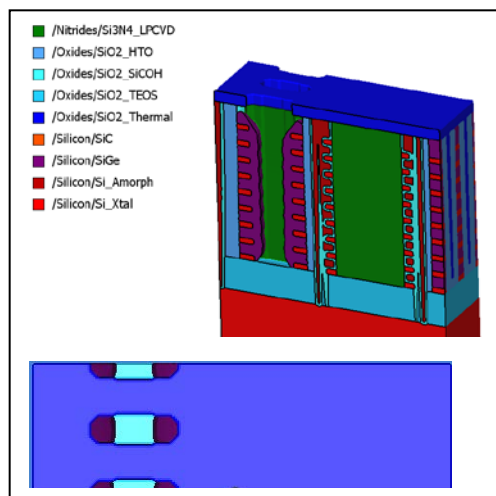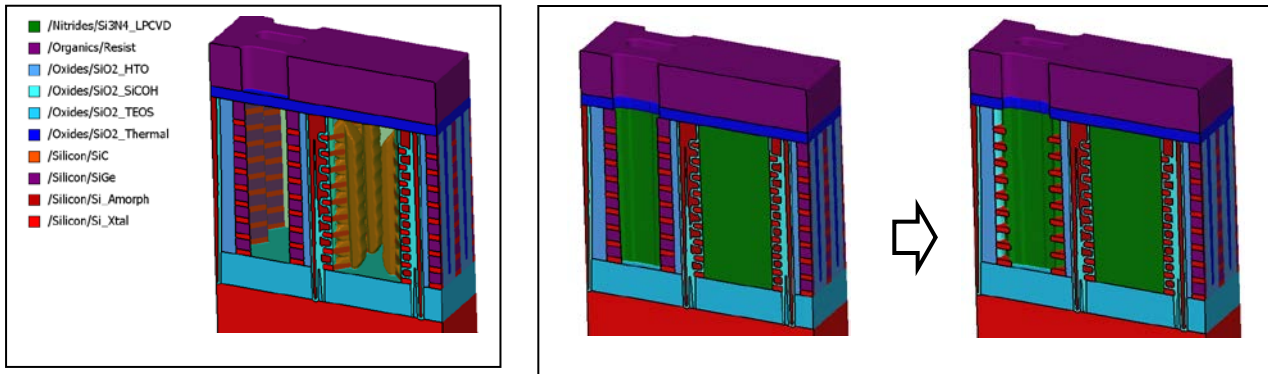




The following are different views of the structure after S/D EPI (with dielectric materials made invisible):
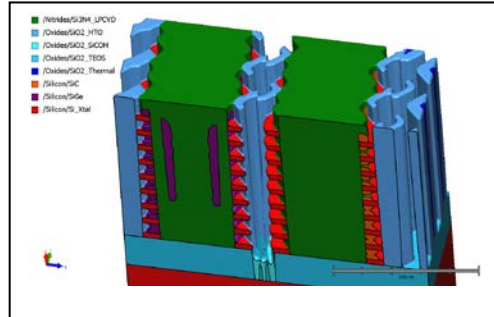
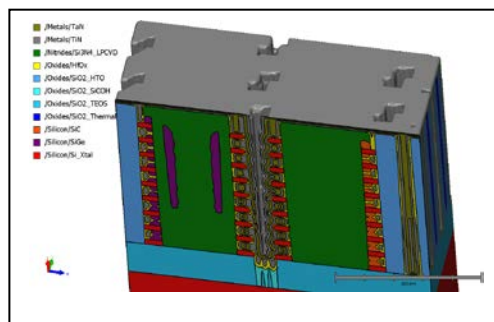A ZIGZAG DOUBLE FORKSHEET FIELD EFFECT TRANSISTOR ARCHITECTURE
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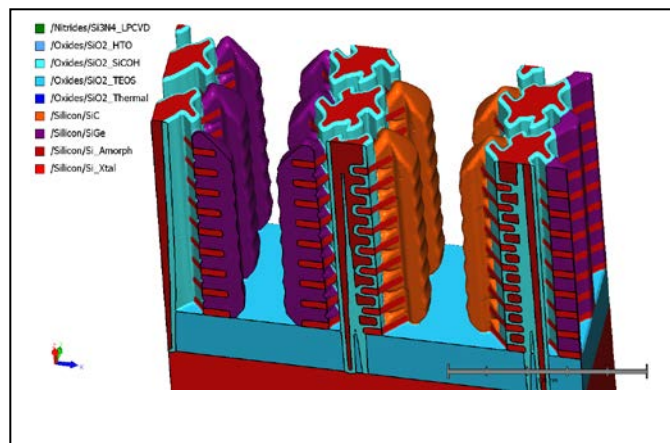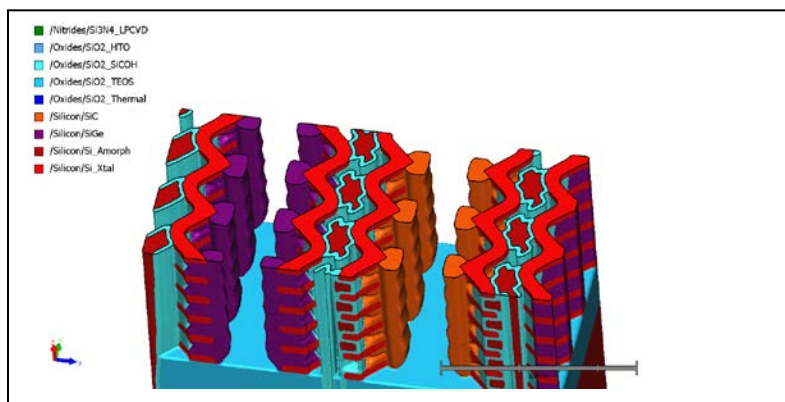
**7.       Replacement Metal Gate module:**

RMG sequence

Dummy gate material removal
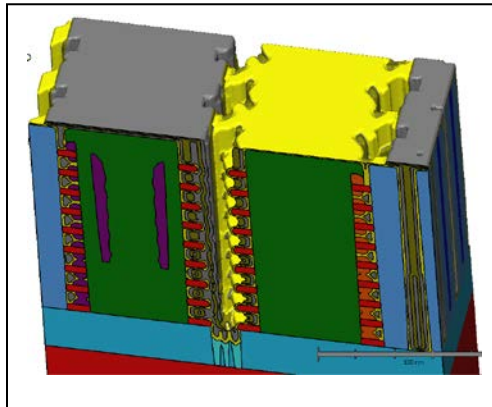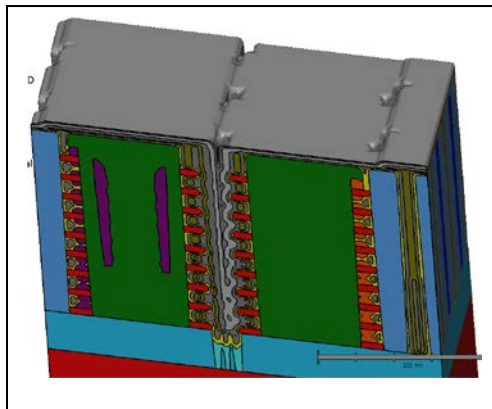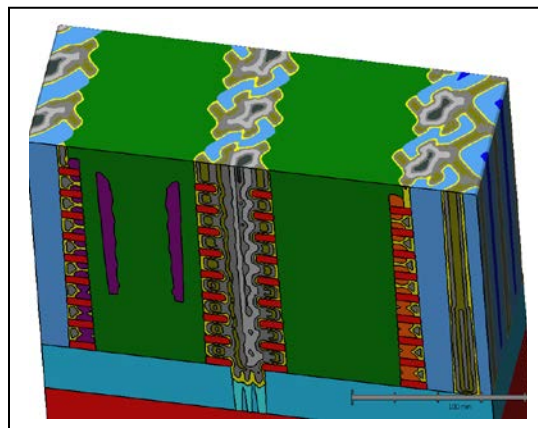


p-WF metal deposition



Opening n-side
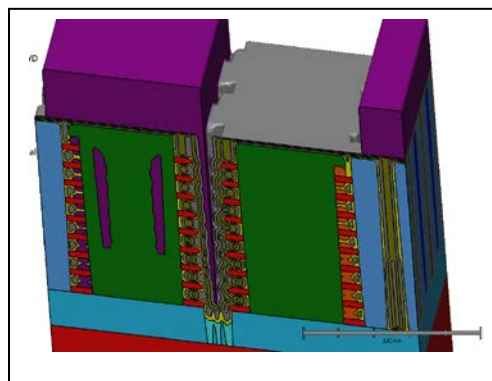
p-WF metal (partial) removal



n-WF metal deposition
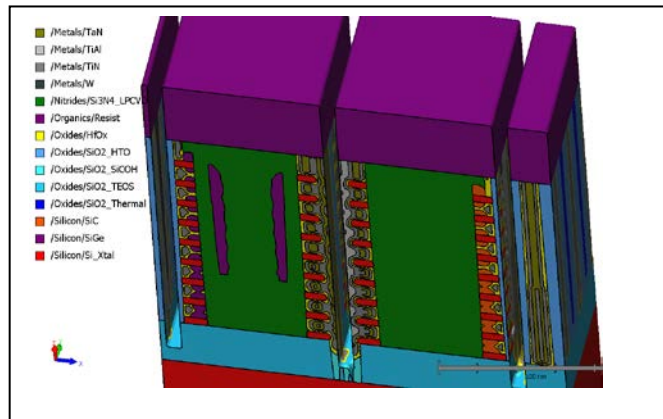


Tungsten deposition

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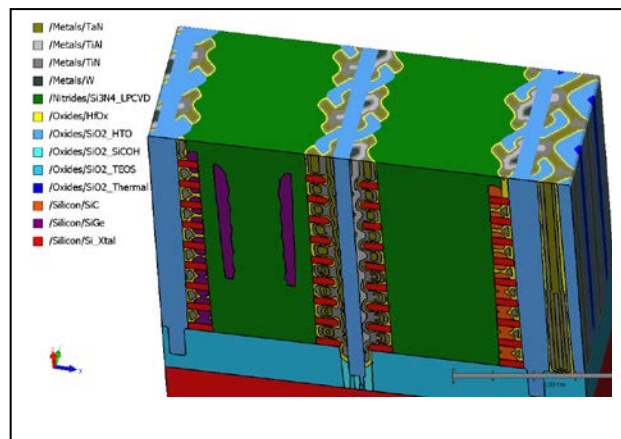Benjamin Vincent

## 8.     Gate cut

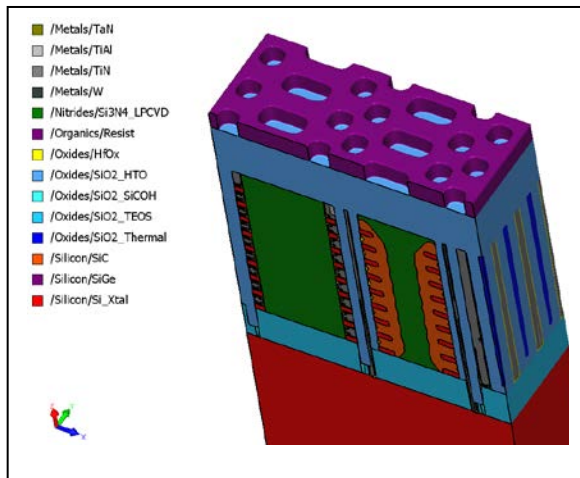Trench etch to isolate n- and p- gates



Dielectric deposition in the trench and CMP:

## 9.       Contact formation

Contact Litho:



Contact etch and metal filling + CMP:

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