Mekathoti Sirisha* et al.
(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH
Volume No.8, Issue No.6, October – November 2020, 9732-9734.

Design Of High Speed Shift Registers Using Pulsed Latches

MEKATHOTI SIRISHA
M.Tech Student, Dept of ECE, Priyadarshini Institute of Technology and Management, Pulladigunta, Guntur, A.P, India

P.SANJAI KRISHNAMAL
Associate Professor, Dept of ECE, Priyadarshini Institute of Technology and Management, Pulladigunta, Guntur, A.P, India

Abstract: **Record this design change using TSPC pulse latches and clock generator circuit with GDI AND gate and single delay cell. The proposed method reduces waste of space and energy with the Mentor Graphics 130nm tool. Here, the proposed method is compared with the two conventional shift register methods. In a traditional method, the shift register was designed using a PPCFF (Power-PC style flip-flop). The flip-flop based shift register required a one hour signal per flip to work. In the second method, the shift register was designed using SSASPL (Static Differential Sense Amplifier Pulse Lock) and a clock generator circuit with a simple AND gate and some delay cells. To operate the pulse latch, the pulse clock signals (part of the clock signal) are sufficient. The gateway must continue to move forward and reverse data sources can also be recovered from returns. At the point where the device meets these two conditions, the second law of thermodynamic elements ensures that heat does not spread. Fans can't go out and recharge. Reverse logic applications have applications in various fields, including quantum computing, optical computing, nanotechnology, computer graphics, VLSI technology, etc. Low speed as reverse logic has recently gained its importance due to its low power characteristic. In addition, a relative review of waste performance, quantitative cost, and input quantities is provided. The circuit was implemented and recreated using Xilinx programming. Reverse logic is today's advanced field of view. The aim of this article is to get acquainted with the different types of combinational circuits such as whole circuits, whole circuits, and multiplexes, and to compare using a reverse decoder circuit at the lowest quantitative cost.**

Keywords: **Pulsed Latch; Pulsed Clock; Flip- Flop; Area; Power Dissipation; Shift Register;**

INTRODUCTION

To design an N-bit shift register with flip-flops or spring latches, they must be connected in series. To reduce the area, the shift register must be specified with fewer transistors. Among the different types of flip-flops and pulse latches, the proposed TSPC pulse latch has fewer transistors. Therefore, the proposed shift register reduces the space [1]. It also reduces the proposed shift register power dissipation due to the use of the TSPC pulse latch and the GDI clock generator circuit which contains the GDI gate and also less delay cells. In this article, the proposed transform register is compared to two conventional shift register methods designed with PPCFF and SSASPL in terms of area and power dissipation and the transform register is designed for low area and power dissipation using the Mentor tool. 130 nm graphics. The proposed shift register is modulated by a TSPC pulse latch and a clock generator circuit to generate the pulse clock signals. There are two common design formats for shifting, namely gear shifting and logarithmic gear shifting. Gallery gear transmission breaks down the catalyzed transmission into individual transmission bit lines that act on all information estimates. At each point of intersection, the gate will or will not allow the information stimulus to travel to the production line, which is controlled by a bit transmission line. The benefit of this scheme is that there is only one entry between the information lines and the return information lines, so it is fast [2]. The drawbacks to this scheme are the basic condition of the decoder and the way each line sees a stack of information from each line of the transport bit. The structure of the proposed shift register using the TSPC pulse latch as shown in Figure 4 is the same as that of the conventional shift register using SSASPL. The TSPC pulse latch register also requires a clock generator circuit [3]. The number of transistors on this latch is reduced to 6 and the clock generator circuit used in this proposed shift register has fewer delay cells and the AND gate of GDI. So that space is reduced and power is dissipated by almost half of the conventional SSASPL designed shift register. When the clock rings loud, the clock pulses are generated and the latch is in a transparent position and corresponds to two attached reflectors; The latch is not reversed and distributes the input to the output. When the clock is low, both inverters are on standby and only the pull-out louvers are active and the pull-down louvers are disabled [4]. As a result, no signal from the latch input to the output can propagate in this position. The main feature of this proposed latch is the use of a single phase clock.

RELATED STUDY

The conventional N-bit 2-bit shift register architecture using SSASPL is divided into sub-shift

registers as shown in Figure 2. Each shift register subset consists of five pulse latches. The shift register output is taken from the first four latches, and the last latch acts as a temporary latch. Therefore, to design the N-bit shift register, an N + 1 pulse latch is required. The five non-interlaced clock pulses of the clock generator circuit enable five pulse latches. These five pulse clock signals are enough to design any shift register length. The clock pulses are applied in reverse order to the latches in the shift register. Therefore, the data is also updated in the reverse order of the latches. Although the power dissipation of a clock generator is higher, it is not taken into account because the same circuit is used to design any bit shift register. The pulse latch requires only a part of the clock signal to function [5]. The clock generator circuit used in conventional shift register 2 consists of five delay cells and a basic AND gate to generate a single pulse clock signal. The generated clock signals have a bit more delay than the previous one.

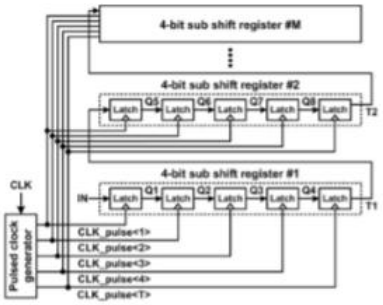

Fig.2.1: Conventional method 2 shift register using SSASPL

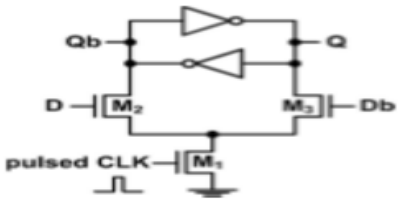

Fig.2.2: Schematic of SSASPL

AN OVERVIEW OF PROPOSED SYSTEM

Structure of the shift register proposed using the TSPC pulse latch as with the conventional shift register using SSASPL. The TSPC pulse latch register also requires a clock generator circuit. The number of transistors in this latch is reduced to 6 and the clock generator circuit used in this proposed shift register has fewer delay cells and a GDI AND gate, so the space and power dissipation are reduced to about the half of the conventional shift register designed with SSASPL. When the clock rings loud, the clock pulses are generated and the latch is in a transparent position and corresponds to two attached reflectors; The latch is not reversed and distributes the input to the output. When the clock is low, both inverters are on standby and only the pull-out louvers are active and the pull-down louvers are disabled. As a result, no signal from the latch input to the output can propagate in this position. The main feature of this proposed latch is the use of a single phase clock. PPCFF and simulation results [6]. The PPCFF is a passive edge that is powered by master-slave data. When the clock signal is applied, the output follows the input.

PARAMETERS	FLIP FLOP	PULSED LATCHES	% IMPROVEMENT
Total number of transistors	16	7	43.75%
Number of transistors connected to clock	8	1	12.5%
Area	9600	5530	57.6%
Power	0.786mW	0.184mW	23.4%
Maximum Clock frequency	2.8GHZ	483MHZ	17.25%

TABLE 1: COMPARISION OF PROPOSED SHIFT REGISTER**.**

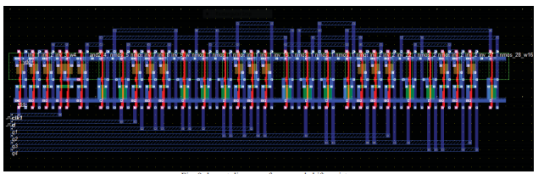

Fig.3.1: LAYOUT DIAGRAM OF PROPOSED SHIFT REGISTER**.**

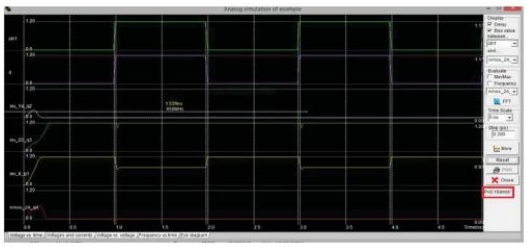

Fig. 3.2: WAVE FORMS OF PROPOSED SHIFT REGISTER.

CONCLUSION

It is proposed to design and analyze the shift register using a low power, low area pulse latch. To reduce space, traditional data flip-flops are replaced by spring latches. The use of non-overlapping pulse clock signals substituted for conventional single pulse clock signals by this design solves the timing problem in pulse latches. In the standard system, the shift register uses a single pulse clock signal to transmit data, which consumes additional power. The shift register uses a small number of pulse clock signals and combines the latches with various substream registers and takes advantage of more buffer latches. To reduce power consumption, it is proposed to design a non-interfering multi-pulse clock signal to synchronize the data in a multi-bit shift register.

REFERENCES

[1] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, "New protection techniques against SEUs for moving average filters in a radiation environment," IEEE Trans. Nucl. Sci., vol.54, no. 4, pp.957-964, Aug.2007.

[2] M. Hatamian et al., "Design considerations for gigabit ethernet 1000 base-T twisted pair transceivers," Proc. IEEE Custom Integr. Circuits Conf., pp. 335–342, 1998.

[3] H.Yamasaki and T.Shibata, "Areal-time image-featureextraction and vector-generation vlsi employing arrayed-shift-register architecture," IEEE J.SolidState Circuits,vol.42,no.9,pp.2046–2053, Sep. 2007.

[4] S.-H.W. Chiang and S. Kleinfelder, "Scaling and design of a16-megapixel CMOS image sensor for electron microscopy," in Proc. IEEE Nucl. Sci. Symp.Conf.Record (NSS/MIC), 2009,pp.1249–1256.

[5] S. Heo, R. Krashinsky, and K. Asanovic, "Activitysensitive flip-flop and latche selection for reduced energy," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol.15,no.9,pp.1060 – 1064,Sep. 2007.

[6] S. Naffziger and G. Hammond, "The implementation of the next generation 64 bit aniummicro processor," in IEEE Int.Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,Feb.2002 ,pp. 276–504.

