Control of a Buck dc/dc Converter using Approximate Dynamic Programming and Artificial Neural Networks

Weizhen Dong, *Student Member, IEEE*, Shuhui Li, *Member, IEEE*, Xingang Fu, *Member, IEEE*, Zhongwen Li, *Member, IEEE*, Michael Fairbank, and Yixiang Gao, *Student Member, IEEE*

***Abstract* –This paper proposes a novel artificial neural network (ANN) based control method for a *dc/dc* buck converter. The ANN is trained to implement optimal control based on approximate dynamic programming (ADP). Special characteristics of the proposed ANN control include: 1) The inputs to the ANN contain error signals and integrals of the error signals, enabling the ANN to have PI control ability; 2) The ANN receives voltage feedback signals from the dc/dc converter, making the combined system equivalent to a recurrent neural network; 3) The ANN is trained to minimize a cost function over a long time horizon, making the ANN have a stronger predictive control ability than a conventional predictive controller; 4) The ANN is trained offline, preventing the instability of the network caused by weight adjustments of an on-line training algorithm. The ANN performance is evaluated through simulation and hardware experiments and compared with conventional control methods, which shows that the ANN controller has a strong ability to track rapidly changing reference commands, maintain stable output voltage for a variable load, and manage maximum duty-ratio and current constraints properly.**

***Index Terms* – dc/dc buck converter, artificial neural network, approximate dynamic programming, optimal control**

I. Introduction

WITH the fast developments of microgrids, electric vehicles and renewable generations, *dc/dc* converters have been widely used to regulate output *dc* voltage and power from the distributed energy sources [1-3]. In these applications, the controller design of *dc/dc* converters is still facing the challenge to accurately and rapidly maintain desired output voltages due to the low switching frequency normally required in high-power converters, load variations, *dc* input voltage disturbances, parameter deviation, and current and PWM saturation constraints of the converters [2-4].

W. Dong, S. Li, and Y. Gao are with the Department of Electrical and Computer Engineering, the University of Alabama, Tuscaloosa, AL 35487 USA (e-mail: wdong5@crimson.ua.edu; sli@eng.ua.edu; ygao43@crimson.ua.edu).

X. Fu is with the Department of Electrical Engineering and Computer Science, Texas A&M University Kingsville, Kingsville, TX 78363 USA (e-mail: xingang.fu@tamuk.edu).

Z. Li is with Zhengzhou University, Zhengzhou 450001 China (e-mail: lzw@zzu.edu.cn).

M. Fairbank is with University of Essex, ColchesterCO4 3SQ UK (e-mail: m.fairbank@essex.ac.uk).

Two types of conventional control methods, voltage mode control (VMC) and current mode control (CMC), are typically used for the control of a *dc/dc* converter. The traditional VMC uses PI, Type II, or Type III compensators, and has a single control loop with voltage feedback [5, 6]. The implementation is simple, but the load-disturbance rejection ability is poor. The CMC improves the performance through a cascade structure, by introducing an inner inductor current-control loop. This structure has the ability to limit the inductor current due to the introduction of the inner current-loop controller. However, the response speed of the output voltage control could be affected due to the two-nested-loop configuration.

In recent years, various advanced control techniques for *dc/dc* converters have been developed [7-13]. Sliding-mode control (SMC) is a popular method developed in recent years for *dc/dc* converter control. The technology has been shifted from early first-order SMC [7] to recent second-order SMC [8-10]. Second-order SMC improves performance measures such as transient response, in comparison to first-order SMC, but an extra capacitor current sensor is usually needed to achieve this. Conventionally, hysteresis-modulation (HM) based SMC isused for control of a *dc/dc* converter, but one of the major problems is that the switching frequency is not constant [7-9]. Recently, PWM-based SMC was developed to overcome the variable switching frequency issue [10, 11]. In [10], a nested SMC strategy is adopted in both voltage and current control loops for DC/DC converters. With this design, the robustness of the paralleled converter system is improved. In [11], a disturbance observer is integrated with a PWM-based sliding mode approach to improve the voltage tracking performance. But the PWM-based SMC typically requires high switching frequency and high sampling rate in order to assure a good dynamic response, which can cause excessive losses and complicated filter designs, and is not suitable for high-power converters. A few research articles show the use of model predictive control (MPC) for control of *dc/dc* converters, because of its fast dynamic response [12, 13]. However, a weakness of the MPC is it would become unstable when the model parameters differ from the actual values.

Artificial neural networks (ANNs) have been applied to *dc/dc* converter control in recent years. Nevertheless, ANNs have not been developed to implement predictive and optimal control of the *dc/dc* converter based on approximate dynamic programming (ADP). In [14], a feedforward ANN is proposed to assist the sliding-mode based control of a *dc/dc* Cuk converter, which is fundamentally still a sliding-mode based

controller. In [15], the authors introduced a neural network to improve the performance of a fuzzy-controlled *dc/dc* converter. In [16], an adaptive fuzzy-neural-network control scheme is designed based upon the SMC for the voltage tracking of a *dc/dc* boost converter. Similar to [14] though, the overall control structure is a sliding-mode based controller, while the purpose of the fuzzy-neural-network scheme is to help improve the SMC performance.

Although significant research has been conducted in optimal control of nonlinear systems based on ADP [17-21], none focuses on *dc/dc* converter control. In [21], an ANN control strategy was developed for control of *dc/ac* inverters based on ADP [17] while how to implement ADP-based ANN control for *dc/dc* converters remains unknown. The authors in [20] proposed an ADP-based optimal switching strategy for *dc/dc* converter control without using ANNs. However, the ADP-based power-converter switching mechanism is similar to a hysteresis switching strategy used in SMC [7, 8]. As a result, the switching frequency varies depending on the optimal action generated by the ADP strategy proposed in [19], which is difficult to implement in practical applications.

This paper develops ADP-based ANN control in the PWM switching framework for *dc/dc* buck converters. Some special features of the proposed method include: 1) The control objective of a *dc/dc* buck converter is defined based on ADP and implemented via an ANN; 2) The complete system dynamic equation for the *dc/dc* converter is integrated into the ANN development to achieve the ADP-based optimal control; 3) A recurrent network structure is formulated by integrating the *dc/dc* converter feedback and the ANN as an integrated system; 4) Error signals and integrals of error signals are used as network inputs to let the ANN gain PI control ability; 5) The ANN is trained offline to avoid the instability of the ANN at runtime that could be caused by network weight adjustments of a real-time training algorithm. On the other hand, compared to the conventional control methods, there are two main limitations associated with the proposed control method. One is that training of the ANN controller is needed in the design stage of the controller. The other one is that more computing time is needed in the implementation stage of the controller. However, it is appropriate to point out that since the proposed ANN controller is trained offline, the proposed ANN controller can be easily implemented using a low-cost DSP as demonstrated by the hardware experiment shown in Section VI of the paper.

The rest of the paper is structured as follows: Section II reviews conventional control methods of a buck converter, Section III presents the proposed ANN-based control of the buck converter. Section IV shows how to train the ANN to implement the ADP-based optimal control for the *dc/dc* buck converter. Section V presents simulation evaluation, and the hardware experiment evaluation is presented in Section VI. Finally, Section VII summarizes with conclusions.

II. Conventional Control of Buck Converter

A. Buck Converter Model

A basic buck converter is shown in Fig. 1, where V_{dc} represents the input *dc* voltage. Using the converter average model and the generator sign convention, the voltage and current-balance equations across the smoothing inductor and capacitor of the *dc/dc* converter are

$$v_A = R_L i_L + L \cdot di_L/dt + v_o \quad (1a)$$

$$C \cdot dv_c/dt = i_L - v_o/R \quad (1b)$$

$$v_o = R_C\left(i_L - v_o/R\right) + v_c \quad (1c)$$

where R_L and L are the resistance and inductance of the inductor, R_C and C are the resistance and capacitance of the capacitor, v_A represents the average voltage at the diode, v_C is the capacitor voltage, and v_o is the output voltage to the load R, and i_L is the current flowing through the inductor.

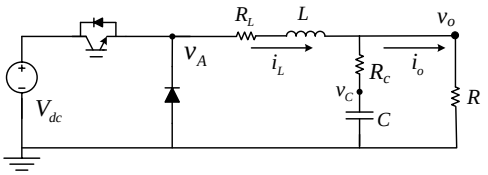

Fig. 1. A dc/dcbuck converter with loads

In typical controller design of a buck converter, the impact of the capacitor resistance is generally neglected, making the model of the buck converter (1) as follows:

$$v_A = R_L i_L + L \cdot di_L/dt + v_o \quad (2a)$$

$$C \cdot dv_o/dt = i_L - v_o/R \quad (2b)$$

Also, a graphic representation of (2) is usually used for the design of a conventional controller [8], as shown in Fig. 2.

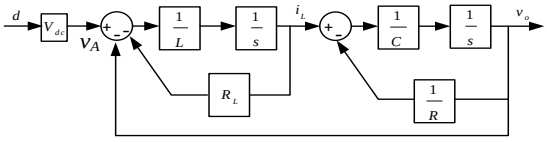

Fig. 2. Buck converter graphic model

B. VMC based Control

VMC-based control typically has one voltage control loop. To design a VMC controller, a transfer function is needed between the buck-converter output voltage v_o and the control voltage v_A generated by the VMC. This is obtained from (2) or Fig. 2 as follows:

$$\frac{V_o(s)}{V_A(s)} = \frac{V_o(s)}{d \cdot V_{dc}} = \frac{1}{s^2 LC + s\left(R_L C + L/R\right) + R_L/R + 1} \quad (3)$$

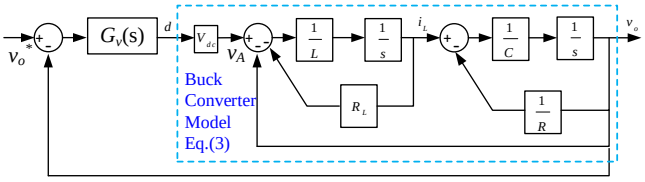

Fig. 3. Buck converter VMC model

In terms of the buck-converter graphic model shown in Fig. 2, the block diagram of the closed-loop control system can be obtained as shown in Fig. 3, in which $G_v(s)$ represents the transfer function of the VMC controller, and v_o^* is the

reference output voltage of the *dc/dc* converter. A Type-III compensator is usually employed [5, 6]. To design the VMC controller $G_v(s)$ using the Bode plot design approach, the cutoff frequency of the controller is generally selected as one to two orders smaller than the converter switching frequency.

C. CMC based Control

CMC typically has a cascade control structure [5]. The overall block diagram of the cascade control is shown in Fig. 4, which consists of an inner current-loop controller, plus an outer voltage-loop controller. Typically, decoupling between the voltage v_o and the current i_L is needed [5, 22, 23]. Thus, the transfer function between the buck-converter output current i_L and the control voltage v_A generated by the current-loop controller is:

$$\frac{I_L(s)}{V_A(s)} = \frac{I_L(s)}{d \cdot V_{dc}} = \frac{1}{s \cdot L + R_L} \tag{4}$$

In terms of the buck-converter graphic model shown in Fig. 2, the block diagram of the current-loop control system is represented by the inner-block enclosed by the dashed green line shown in Fig. 4, in which $G_i(s)$ represents the transfer function of the inner current-loop controller, and i_L^* is the reference current generated by the voltage-loop controller.

Typically, the current-loop controller is much faster than the voltage-loop controller, and is generally assumed to be ideal. Hence, the transfer function of the current-loop is assumed to be 1 during the design of the voltage-loop controller [5, 22, 23]. To design the voltage-loop controller, the transfer function between the buck-converter output voltage v_o, and the control action i_L generated by the voltage-loop controller, is obtained from (2b) as follows:

$$\frac{V_o(s)}{I_L(s)} = \frac{1}{s \cdot C + 1/R} \tag{5}$$

In terms of the graphic illustration shown in Fig. 4, $G_v(s)$ represents the transfer function of the outer voltage-loop controller, which is designed according to (5), and i_L^* is the reference current generated by the voltage-loop controller.

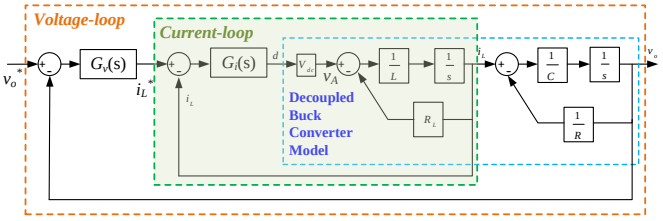

Fig. 4. Buck converter CMC cascade voltage-current control model

Using the Bode-plot approach, the cutoff frequency of the voltage-loop controller is normally one order smaller than that of the current-loop controller. As a result, under the same switching frequency, the response speed of the output voltage for the cascade control strategy is generally slower than that of the VMC approach.

D. Sliding-mode based Control

Fig. 5 shows a PWM-based second-order SMC approach [24], which can overcome the variable switching frequency issue associated with traditional SMC, and also can use low switching frequency and sampling rate for control of the *dc/dc* buck converter. Similar to the CMC, a cascade SMC control structure is employed, which includes a second-order current-loop SMC and a second-order voltage-loop SMC. The sliding surfaces for the current- and voltage-loop SMCs are defined as (6a) and (6b), respectively, as shown by

$$S_i = e_i + \lambda_i \cdot \int e_i dt \tag{6a}$$

$$S_v = e_v + \lambda_v \cdot \int e_v dt \tag{6b}$$

where $e_i = i_L^* - i_L$ and $e_v = v_o^* - v_o$. Here v_o^* and i_L^* represent output voltage and inductor current references, respectively. According to (2a) and (2b), the control actions generated by the current- and voltage-loop SMCs are designed as (7a) and (7b), respectively, as shown by

$$i_L^* = C \cdot \frac{dv_o^*}{dt} + \frac{v_o}{R} + C \cdot \left(\lambda_v e_v + a_v \cdot \mathrm{sgn}(S_v) + b_v \cdot S_v\right) \tag{7a}$$

$$u = \frac{L}{V_{dc}} \frac{di_L^*}{dt} + \frac{i_L R_L}{V_{dc}} + \frac{v_o}{V_{dc}} + \frac{L}{V_{dc}} \left(\lambda_i e_i + a_i \cdot \mathrm{sgn}(S_i) + b_i \cdot S_i\right) \tag{7b}$$

where a_v, b_v and λ_v are the parameters of the voltage-loop SMC, a_i, b_i and λ_i are the parameters of the current-loop SMC, and u is the duty ratio. Details about the PWM-based cascade SMC control design and analysis are provided in [24].

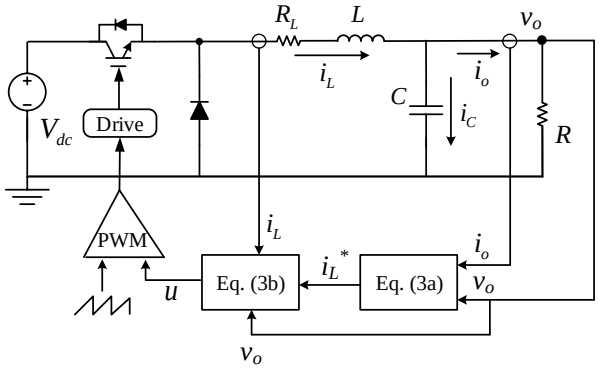

Fig. 5. A PWM-based cascade SMC for Buck converter

III. ANN Control of Buck Converter

A. Buck Converter State-Space Model

The ANN controller is developed based on the complete state-space model of the buck converter, which is obtained from (1) by first rearranging (1c) to get $v_c = v_o - R_C\left(i_L - v_o/R\right)$. Substituting this into (1b) and combining with (1a) gives the state-space model in terms of i_L and v_o, as follows:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} -R_L/L & -1/L \\ \dfrac{\left(L - CR_LR_C\right)R}{\left(R+R_C\right)CL} & -\dfrac{L + CRR_C}{\left(R+R_C\right)CL} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L \\ \dfrac{RR_C}{\left(R+R_C\right)L} \end{bmatrix} v_A \tag{8}$$

where the system states are i_L and v_o, and v_A is proportional to the output of the ANN controller [25].

As the ANN controller is a digital controller, a discrete model of (8) is needed. This is obtained via a zero- or first-order hold discrete equivalent mechanism as [26]:

$$\begin{bmatrix} i_L(kT_s+T_s) \\ v_o(kT_s+T_s) \end{bmatrix} = \mathbf{A}\begin{bmatrix} i_L(kT_s) \\ v_o(kT_s) \end{bmatrix} + \mathbf{B}\begin{bmatrix} v_A(kT_s) \\ 0 \end{bmatrix} \quad (9)$$

in which T_s represents the sampling time, **A** is the system matrix, and **B** is the input matrix. Note: matrices**A** and **B** are obtained from (8) based on a chosen discrete equivalent mechanism [26]. Since T_s is present on both sides, (9) can be simplified as (10) where k is an integer time step.

$$\begin{bmatrix} i_L(k+1) \\ v_o(k+1) \end{bmatrix} = \mathbf{A}\begin{bmatrix} i_L(k) \\ v_o(k) \end{bmatrix} + \mathbf{B}\begin{bmatrix} v_A(k) \\ 0 \end{bmatrix}, \quad (10)$$

B. ANN Control Structure

The overall ANN control structure is shown in the lower part of Fig. 6, in which the ANN is a feedforward network. The ANN consists of four different layers: an input layer, two hidden layers, and an output layer. The input layer contains two inputs: the error term and the integral of the error term as defined by:

$$e_{v_o}(k) = v_o(k) - v_o^*(k),\ s_{v_o}(k) = \int_0^{kT_s} e_{v_o}(t)dt, \quad (11)$$

where $v_o^*(k)$ is the reference output voltage of the *dc/dc* converter. The two inputs are divided by their appropriate gains, and then processed through a hyperbolic tangent activation function. Each gain is selected as 4 for the simulation and experimental Buck converter setup shown in Sections V and VI. The input layer then feeds into the hidden layers. Each of the two hidden layers contains six nodes. Each node at the hidden layers uses a hyperbolic-tangent activation function. Finally, the output layer gives $v_A^*(k)$, the output of the ANN. This output is multiplied by a gain, k_{PWM}, which represents the PWM gain, to obtain the final control action, v_A, of the *dc/dc* converter given by:

$$v_A(k) = k_{PWM} \cdot A\left(e_{v_o}(k), s_{v_o}(k), \vec{w}\right), \quad (12)$$

where $\vec{w}$ represents the network's overall weight vector, and $A(\bullet)$ denotes the whole ANN. The error signal and integral of the error signal as the network inputs would enable the ANN to gain important PI control characteristics. Besides, there are hundreds of 'PI' gains for the ANN controller instead of two gains for a conventional PI controller, and the training of the network should enable its performance to match, and potentially exceed, that of an optimal "PI" controller.

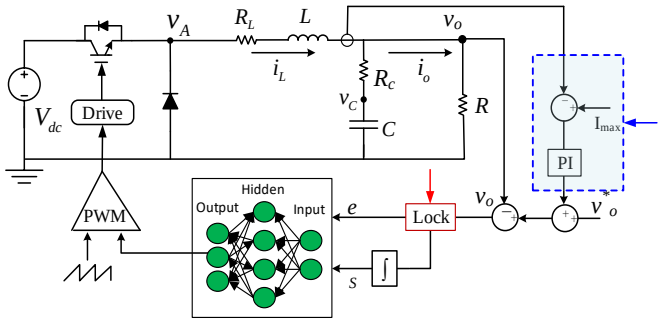

Fig. 6. ANN control for buck *dc/dc* converter

It is also important to point out that although the ANN is a feedforward network, the feedback signal of the *dc/dc* converter applied as the input to the ANN makes the combined ANN and *dc/dc* converter equivalent to a recurrent neural network. This property is considered properly and accurately in training the ANN as shown in Section IV, which would allow the ANN to gain important predictive control ability.

C. Maximum Duty-ratio and Current Limitations

During the real-time control stage, it is possible that the controller output voltage may be beyond the maximum duty cycle constraint, or the inductor current may be beyond the maximum inductor current limitation.

To handle the maximum duty cycle constraint, a locking mechanism (Fig. 6) is developed with the ANN controller. The mechanism first detects whether the controller output voltage is beyond the PWM saturation limit. If so, the error signal passed to the ANN controller will be blocked and the controller just maintains the output voltage at the maximum duty cycle until there is a potential to draw the ANN controller out of the PWM saturation limit.

To handle the maximum inductor current constraint, a PI regulation block (Fig. 6) is added to adjust the reference output voltage of the *dc/dc* converter. However, this PI regulation block is only initiated when the actual inductor current is over the maximum current constraint and stops when the actual inductor current is about 2% below the maximum current constraint. Here, 2% is a dead-band margin to assure that the PI controller for the maximum current limitation does not turn on and off constantly at the maximum current constraint. Later, it will be demonstrated by the simulation and hardware experiments shown in Sections V and VI that the proposed ANN controller correctly handles the maximum current constraint, even using such a small dead-band margin.

IV. Training ANN to Implement ADP-based Control

A. ADP-based Control

ADP employs the principle of Bellman's optimality [17] and is a very useful tool for solving optimization and optimal control problems. The typical structure of discrete-time ADP includes a discrete-time state-space system model and a performance index or cost associated with the system [17, 18]. For the ADP-based control of the *dc/dc* converter, the discrete-time state-space model is (10) and the performance index or cost is

$$C(v_o) = \sum_{k=1}^{N} \sqrt[\alpha]{\left[v_o(k) - v_o^*(k)\right]^2} \quad (13)$$

where N is the trajectory length and α is a fractional number. The objective of the ADP-based control for the *dc/dc* converter is to determine a sequence of control actions $v_A(k)$, k=1, 2, ..., N, such that the ADP cost (13) is minimized. Compared to the cost function normally used for the conventional MPC methods, the ADP cost function emphasizes minimizing the difference between the actual and reference voltages over a much longer time horizon, instead of the one-step ahead that is normally used in the conventional

MPC [13]. Thus, ADP-based control would provide a much stronger predictive control ability than conventional MPC.

B. Training ANN to Implement ADP

The ADP-based control is achieved through the ANN that is trained to minimize the ADP cost function (13). We used the Levenberg-Marquardt (LM) algorithm [27] to train the ANN, and the Jacobian matrix needed by the LM algorithm is calculated via a Forward Accumulation Through Time (FATT) algorithm [28]. Similar to many other neural network training algorithms, the most important part of the training algorithm is the calculation of the gradient of (13) regarding the weight vector. Define $U(k)=\sqrt[\alpha]{\left[v_o(k)-v_o^*(k)\right]^2}$ and $V(k)=\sqrt{U(k)}$, then, the gradient $\partial C/\partial \vec{w}$ can be written in matrix form as

$$\frac{\partial C}{\partial \vec{w}}=\frac{\partial\sum_{k=1}^{N}[V(k)]^2}{\partial \vec{w}}=\sum_{k=1}^{N}2V(k)\frac{\partial V(k)}{\partial \vec{w}}=2J(\vec{w})^T\vec{V} \tag{14}$$

where the Jacobian matrix $J(\vec{w})$ is

$$J(\vec{w})=\begin{bmatrix}\frac{\partial V(1)}{\partial w_1} & \cdots & \frac{\partial V(1)}{\partial w_M}\\ \vdots & \ddots & \vdots\\ \frac{\partial V(N)}{\partial w_1} & \cdots & \frac{\partial V(N)}{\partial w_M}\end{bmatrix},\ \vec{V}=\begin{bmatrix}V(1)\\ \vdots\\ V(N)\end{bmatrix} \tag{15}$$

Therefore, the weight update can be expressed by

$$\Delta\vec{w}=-\left[J(\vec{w})^T J(\vec{w})+\mu\mathbf{I}\right]^{-1}J(\vec{w})^T\vec{V} \tag{16}$$

Here μ>0 is an adaptable parameter set by the LM algorithm [28]. The network weights are updated by

$$\vec{w}_{\text{update}}=\vec{w}+\Delta\vec{w} \tag{17}$$

Note: the combination of the ANN and the *dc/dc* converter is equivalent to a recurrent network as explained in Section III-B. Also, the ANN is trained offline, meaning that there is no further training involved at the real-time control stage. A more detailed description about training a recurrent network using LM and FATT algorithms is provided in [28]. In general, in each experiment, training continued until one of the following three stopping criteria were met [28]: 1) when the training epoch reaches the maximum number of training epochs, 2) when μ is larger than $\mu_{\max}$, a predefined maximum μ value, or 3) when the smallest gradient of (14) is less than a predefined minimum gradient.

V. Simulation Evaluation

The parameters of the *dc/dc* buck converter used in both the simulation and experiment evaluation are as follows: R_L=0.3Ω, L=5.63mH, R_C=0.02Ω, and C=5μF. The nominal input voltage is 42V.

A. Tuning of Conventional Controller

The conventional VMC and CMC controllers were tuned based on the description shown in Sections II-B and II-C using the phase-margin of 60°. In the simulation, the converter switching frequency was 20kHz. To reject the switching noises and disturbances, the crossover frequency of the VMC Type-III compensator is selected lower than the switching frequency, usually from $0.1f_{sw}$ to $0.05f_{sw}$. Therefore the bandwidth of the VMC compensator was selected as 1000 Hz. For the CMC, a cascade PI configuration was used. To limit the switching noise in the current loop, the bandwidth of the current PI controller was selected as 1000 Hz. Then the bandwidth of the outer voltage loop was selected as 1000/10 = 100 Hz. The SMC controller was tuned according to Section II-D and [24].

B. Training of ANN Controller

The ANN was trained to implement ADP-based control through multiple training experiments. In each experiment, the ANN was trained repeatedly to track a variety of randomly generated reference voltage trajectories. The procedure of each training experiment is as follows: 1) randomly generate a sample reference output voltage trajectory; 2) randomly generate a sample initial state $v_o(1)$ where the value 1 indicates a start time; 3) unroll the converter output voltage trajectory from the initial state; 4) train the ANN as detailed in Section IV-B; and 5) repeat the process for other randomly generated reference voltage trajectories and sample initial states. In each training experiment, a dozen randomized reference voltage trajectories were created to train the network. Each reference trajectory duration was 1 second, with a sampling time of Ts=0.1ms, and was changed randomly every 0.1 seconds. The training of each experiment for all randomly generated reference output voltage trajectories continued until reaching a stop criterion (Section IV-B). Each training experiment started with randomly generated network weights, which were initially randomized using a uniform distribution within ±0.1. The impact of load and input voltage variations are considered as noises in each training experiment. Each training experiment took about 10 to 30 minutes to complete on a PC with a 2.3GHz CPUand 16GB RAM. Since each experiment starts with randomly generated weights, each may converge to a different ADP cost. The final network weights were selected from the training experiment having the lowest ADP cost. Compared to the conventional control methods, the trained ANN controller has a very strong adaptive ability to withstand circuit parameter changes that may appear in real-life conditions, such as the increase or decrease of L and C values beyond the nominal values, as shown in the subsection below.

C. Control Evaluation within System Constraints

The tuned conventional controllers shown in Section V-A and the trained ANN controller shown in Section V-B are first evaluated and compared via simulation. The simulation models of traditional and ANN-controlled *dc/dc* buck converter were built by using SimPowerSystems. Again, the switching frequency was 20kHz. The evaluation focuses on the output voltage and inductor current under different conditions using conventional and ANN control techniques as presented in Sections II to IV.

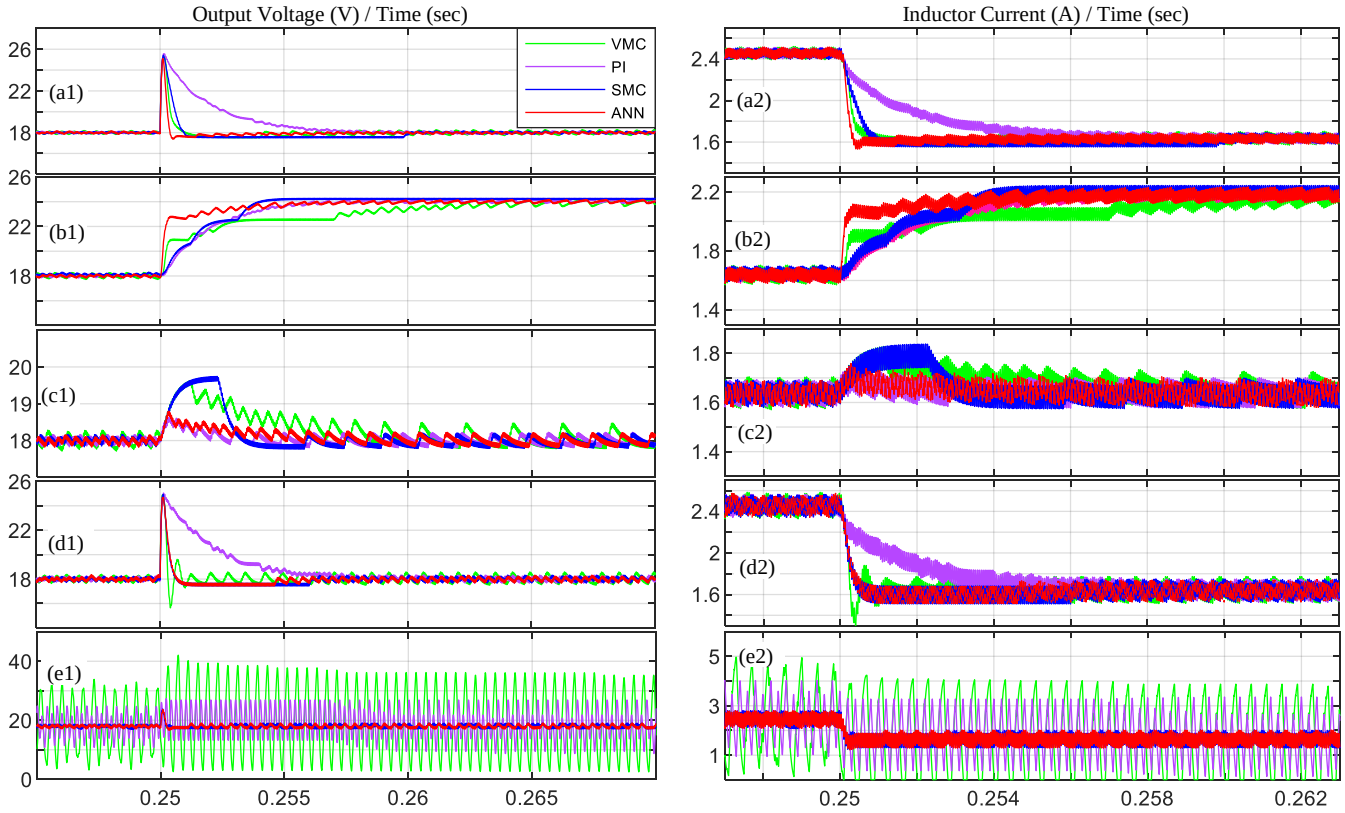

Fig. 7. Simulated results for ANN vs. VMC Type III, CMC cascade PI, and cascade SMC:a) a load change from 7.33Ω to 11Ω, b) a reference voltage change from 18V to 24V, c) an input voltage change from 42V to 47V, d) the same load change as (a) when L decreases by 50%, e) the same load change as (a) when L decreases by 85%

Fig. 7a) compares the control of the buck converter under a load change from 7.33Ω to 11Ωusing VMC-Type III, CMC-Cascade PI, Cascade SMC, and ANN. The comparison shows both the conventional VMC and the proposed ANN controller responding faster to maintain the output voltage at a constant level than the cascade PI and SMC control. This is due to the fact that there are two control loops for the CMCand SMC approaches. Thus, the response speed of the external voltage loop would be slower than that of a single voltage control loop according to the design rules presented in Section II. Overall, the ANN controller shows the best performance and fastest response speed, demonstrating the higher bandwidth of the ANN controller than that of others.

Fig. 7b) compares the control of the buck converter under a reference-voltage change from 18V to 24V using VMC, CMC, SMC, and ANN. The comparison shows that the ANN controller has the fastest response speed to track a reference voltage change than other control methods.

Fig. 7c) compares the control of the buck converter as the input voltage changes from 42V to 47V, to examine how the four different control methods behave in maintaining output-voltage stability when there is a disturbance in the supply voltage. Since there is no load or reference output voltage change, the CMC-Cascade PI has better performance than the VMC-Type III. However, the ANN still has the best performance, demonstrating its strong adaptive ability to manage a system condition variation.

Figs. 7d) and 7e) compare the control of the buck converter when the inductance value is different from the inductance value used in tuning conventional controllers and training the ANN controller. Normally, the performance of the controllers would be worse as the inductance value reduces, because this would make the *dc/dc* converter more likely to get out of continuous-conduction mode. Although more oscillations are shown with all the four control methods, the ANN has the smallest degradation in performance, especially for a large parameter variation away from its nominal value (Fig. 7e), demonstrating its strong robust ability under system parameter variations.

D. Control Evaluation beyond System Constraints

Physical system constraints of the *dc/dc* converter are an important issue that needs to be addressed. Typically, there are two constraints: maximum duty-ratio constraint and inductor current constraint. Fig. 8 evaluates the performance of the *dc/dc* converter using the ANN and conventional control strategies under the two physical constraint conditions. It is assumed in the simulation that the maximum inductor current is 2A. Also, the *dc* supply voltage is 30V.

For a fair comparison, the mechanism used to handle the PWM saturation limit shown in Fig. 6 is applied to all the conventional methods. However, the mechanism used to handle the current limitation shown in Fig. 6 cannot be applied to VMC, as this would result in high oscillations of the output voltage. For both the CMC and SMC, the current limit control is handled by the inner-loop current controller.

For the ANN controller (Fig. 8d), when the inductor current is over the maximum current limit, the controller is

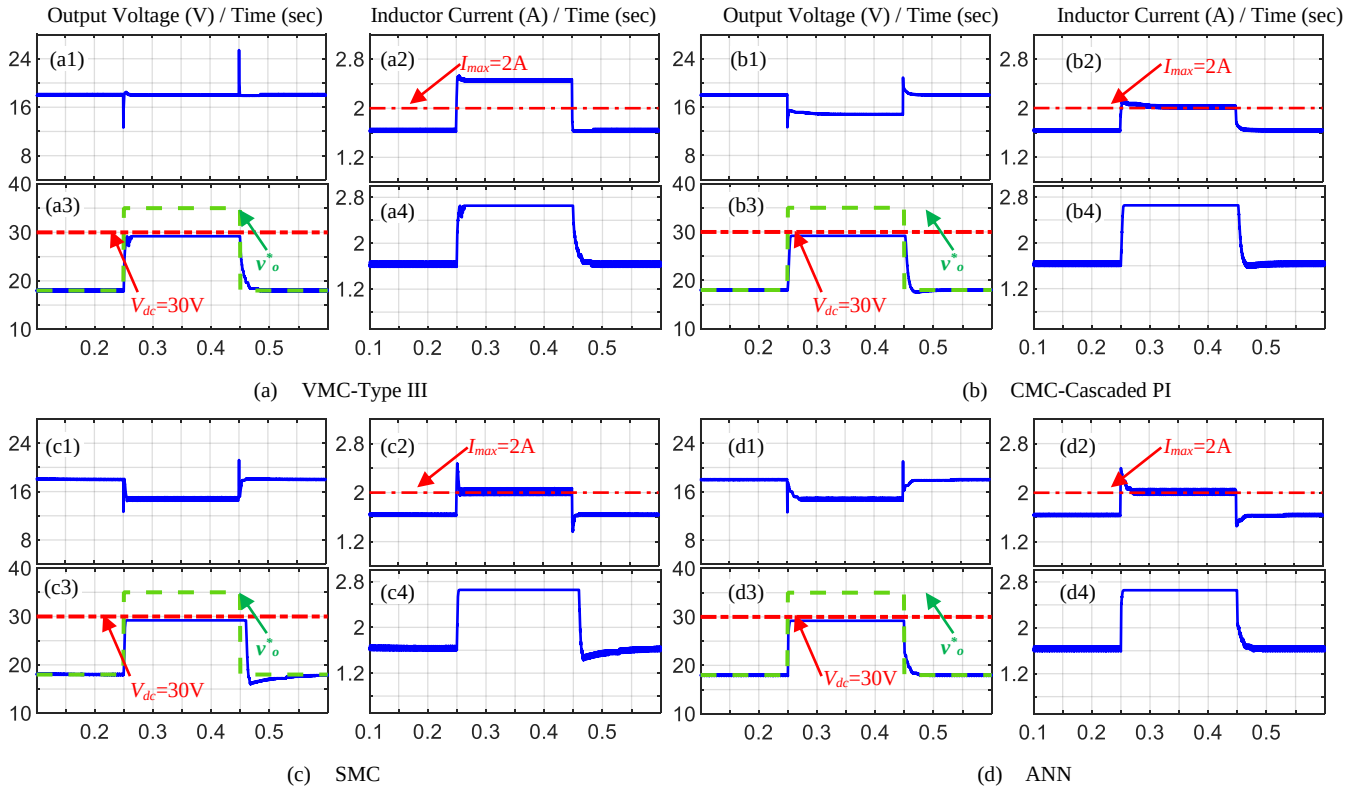

Fig. 8. Simulated results for ANN vs. VMC Type III, CMC cascaded PI, and SMC under: a maximum inductor current constraint of 2A (a1)-(a2), (b1)-(b2), (c1)-(c2), & (d1)-(d2); b) the maximum duty-ratioconstraint (a3)-(a4), (b3)-(b4), (c3)-(c4), & (d3)-(d4)

able to react immediately to maintain the output voltage at a lower value, while preventing the inductor current from exceeding the maximum limit; when a high reference voltage command is presented to the controller, the ANN can maintain the output voltage at the highest voltage that can be outputted by the converter, while stability and controllability of the *dc/dc* converter are not affected before and after the maximum duty-ratio operation period.

The CMC cascade-PI and cascade SMC control structures can properly prevent the inductor current from exceeding the maximum inductor current limit too. But, the VMC Type III controller is unable to limit the inductor current, because the current limit control used for the ANN cannot be applied to the VMC as explained above. When using the locking mechanism presented in Fig. 6 and Section III-C, all the three conventional methods can manage the PWM saturation constraint properly.

VI. Hardware Experiment Evaluation and Validation

A. Experiment Setup

To further validate the proposed ANN controller, a DSP-based digital control systemwas implemented. The experimental setup (Fig. 9) consists of four main parts: (i) a*dc/dc* Buck converter built by using a three-phase converter board from Vishay HiRel Systems which has the maximum allowable switching frequency of 20kHz, (ii) a LabVolt LC circuit module representing the inductor and capacitor of the Buck converter, (iii) a dSPACE DS1103 controller board to collect inductor current and output voltage/current of the *dc/dc* converter, and (iv) a sensor board to convert measured voltage and current to dSPACE compatible format. The converter switching frequency is 10kHz and the controller sampling time is 0.1ms.

B. Experiment Results

Fig. 10 shows the comparison of VMC-Type III, CMC-Cascade PI, cascade SMC and ANN for control of the *dc/dc* Buck converter. The left side of Fig. 10 shows the Buck converter's ability to follow a reference voltage change from 18V to 24V. Again, in the experiment condition, the ANN controller shows less overshoot and faster response speed than the conventional control methods in tracking the reference output voltage change. The right side of Fig. 10 shows the Buck converter's ability to maintain a constant output voltage under a load change. As shown in the figure, the ANN controller presents a much stronger ability in maintaining output voltage stability under the variable load condition.

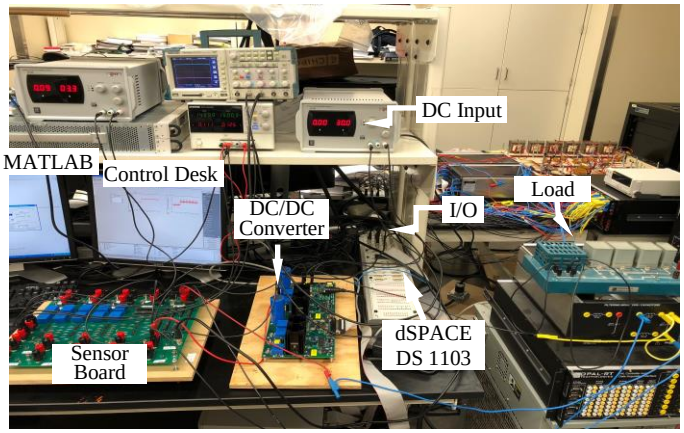

Fig. 9. Hardware laboratory testing and control systems

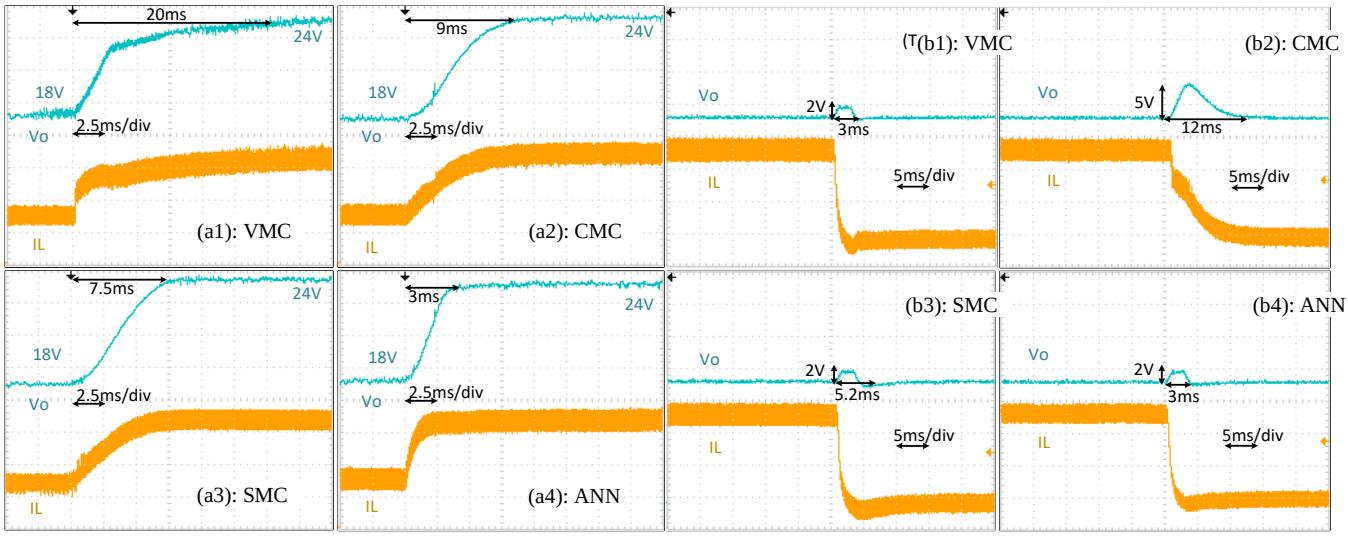

Fig. 10. Hardware results for VMC vs. CMC Cascade PI vs. Cascade SMC vs. ANN: a) Change of v^*_o from 18V to 24V, b) Load change from 7.33Ω to 11Ω

Fig. 11 shows the experiment results of the ANN controller when considering the maximum inductor current (2A) and duty-ratio constraints. In Fig. 11a, when a load change causes the inductor current to be over the maximum current limit, the output voltage of the *dc/dc* converter is dropped automatically to regulate the inductor current within the maximum current limitation. In Fig. 11b, when the reference voltage increases and makes the duty-ratio over the maximum duty-ratio constraint, the output voltage is automatically limited; and when the reference voltage reduces, the ANN controller is able to return to its normal condition.

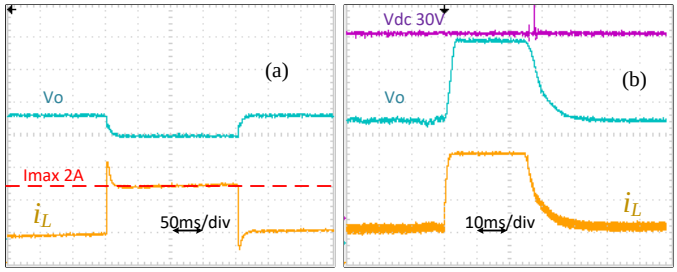

Fig. 11. Hardware results for ANN under a) inductor current constraint; b) duty-ratioconstraint

VII. Conclusion

This paper presents an ANN-based optimal and predictive control based on ADP for *dc/dc* Buck converters. Compared to conventional control methods, the ANN controller shows better performance in various aspects. In addition, the ANN controller can handle the control of the *dc/dc* converter properly under both the maximum inductor current and duty ratio constraints, while a conventional controller needs to have an inner-current loop through a cascade control structure to handle the current limit control. Compared to the conventional control methods, the ANN controller responds faster and maintains a more stable output voltage. The hardware experiment confirmed that the ANN controller is able to track reference commands, maintain output voltage stability under variable load and input voltage conditions, and manage the control of the *dc/dc* converter correctly under the maximum duty-ratio and inductor current constraints. The study shows that it is feasible to implement the ANN-based control for practical *dc/dc* Buck converters.

The proposed ANN control method can be extended to other dc/dc converters, such as Boost and Buck-Boost converters. However, since the state-space models of the Boost and Buck-Boost converters are different from that of the Buck converter, the training algorithms for each of the other dc/dc converters need to be redesigned and revalidated. We plan to extend the proposed ANN-ADP control method to other dc/dc converters through future research.

References

[1] P. J. d. S. Neto, T. A. d. S. Barros, J. P. C. Silveira, E. R. Filho, J. C. Vasquez and J. M. Guerrero, "Power Management Strategy Based on Virtual Inertia for DC Microgrids," in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12472-12485, Nov. 2020, doi: 10.1109/TPEL.2020.2986283.

[2] W. W. A. G. Silva, T. R. Oliveira and P. F. Donoso-Garcia, "An Improved Voltage-Shifting Strategy to Attain Concomitant Accurate Power Sharing and Voltage Restoration in Droop-Controlled DC Microgrids," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2396-2406, Feb. 2021, doi: 10.1109/TPEL.2020.3009619.

[3] Z. Xia and J. Abu Qahouq, "State-of-charge Balancing of Lithium-ion Batteries with State-of-health Awareness Capability," in *IEEE Transactions on Industry Applications*, doi: 10.1109/TIA.2020.3029755.

[4] M. S. Sadabadi, "A Distributed Control Strategy for Parallel DC-DC Converters," in *IEEE Control Systems Letters*, vol. 5, no. 4, pp. 1231-1236, Oct. 2021, doi: 10.1109/LCSYS.2020.3025411.

[5] N. Mohan, *Power Electronics: A First Course*, Wiley, 2011

[6] R.A. Mammano, *Fundamentals of Power Supply Design*, Texas Instruments, 2017.

[7] S. Tan, Y. M. Lai and C. K. Tse, "General Design Issues of Sliding-Mode Controllers in DC–DC Converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1160-1174, March 2008.

[8] M. Ordonez, M. T. Iqbal and J. E. Quaicoe, "Selection of a curved switching surface for buck converters," *IEEE Trans. on Power Electron.*, vol. 21, no. 4, pp. 1148-1153, July 2006.

[9] R. Ling, D. Maksimovic and R. Leyva, "Second-Order Sliding-Mode Controlled Synchronous Buck DC–DC Converter," *IEEE Trans. on Power Electron.*, vol. 31, no. 3, pp. 2539-2549, March 2016.

[10] Cheng, Zhiping, et al. "A novel cascaded control to improve stability and inertia of parallel buck-boost converters in DC microgrid." *International Journal of Electrical Power & Energy Systems* 119 (2020): 105950.

[11] Z. Wang, S. Li and Q. Li, "Continuous Nonsingular Terminal Sliding Mode Control of DC–DC Boost Converters Subject to Time-Varying

Disturbances," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 11, pp. 2552-2556, Nov. 2020

[12] B. Wang, V. R. K. Kanamarlapudi, L. Xian, X. Peng, K. T. Tan and P. L. So, "Model Predictive Voltage Control for Single-Inductor Multiple-Output DC–DC Converter With Reduced Cross Regulation," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4187-4197, July 2016.

[13] Z. Liu, L. Xie, A. Bemporad and S. Lu, "Fast Linear Parameter Varying Model Predictive Control of Buck DC-DC Converters Based on FPGA," in *IEEE Access*, vol. 6, pp. 52434-52446, 2018, doi: 10.1109/ACCESS.2018.2869043.

[14] J. Mahdavi, M.R. Nasiri, A. Agah, and A. Emadi, "Application of neural networks and state-space averaging to DC/DC PWM converters in sliding-mode operation," *IEEE/ASME Trans. Mechatronics*, 10(1), 2005 pp. 60-67.

[15] A. Rubaai, A.R. Ofoli, L. Burge, and M. Garuba, "Hardware implementation of an adaptive network-based fuzzy controller for DC-DC converters," *IEEE Trans. Ind. Appl*., 41(6), 2005, pp.1557-1565.

[16] R.J. Wai and L.C. Shih, "Adaptive fuzzy-neural-network design for voltage tracking control of a DC–DC boost converter," *IEEE Trans. Power Electron*., 27(4), 2012, pp.2104-2115.

[17] Dimitri P. Bertsekas, " Dynamic Programming and Optimal Control: Approximate Dynamic Programming," 4th Ed., Athena Scientific, 2012.

[18] F.L. Lewis and D. Liu (eds.), *Reinforcement Learning and Approximate Dynamic Programming for Feedback Control*, IEEE Press / Wiley, 2012, pp. 474-493.

[19] H. Zhang, C. Li, X. Zhang, and Y. Luo, "Data-Driven Robust Approximate Optimal Tracking Control for Unknown General Nonlinear Systems Using Adaptive Dynamic Programming Method," *IEEE Trans. Neural Netw*., 22(12), 2011, pp. 2226-2236.

[20] A. Heydari, "Optimal Switching of DC–DC Power Converters Using Approximate Dynamic Programming," in *IEEE Transactions on Neural Networks and Learning Systems*, vol. 29, no. 3, pp. 586-596, March 2018.

[21] S. Li, M. Fairbank, C. Johnson, D.C. Wunsch, E. Alonso, and J.L. Proao, "Artificial neural networks for control of a grid-connected rectifier/inverter under disturbance, dynamic and power converter switching conditions," *IEEE Trans. Neural Netw. Learn. Syst*., 25(4), 2014, pp. 738–750.

[22] E. d. C. Gomes, L. A. de S. Ribeiro, J. V. M. Caracas, S. Y. C. Catunda and R. D. Lorenz, "State space decoupling control design methodology for switching converters," 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, 2010, pp. 4151-4158, doi: 10.1109/ECCE.2010.5617741.

[23] K.M. Tsang, and W.L. Chan. "Cascade controller for DC/DC buck convertor." *IEE Proc. Electr, Power Appl*., 152(4), (2005), pp. 827-831.

[24] Z. Li, C. Zang, P. Zeng, H. Yu, S. Li and J. Bian, "Control of a Grid-Forming Inverter Based on Sliding-Mode and Mixed H2/{H∞ Control," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3862-3872, May 2017.

[25] N. Mohan, T.M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd Ed., John Wiley & Sons Inc., Oct. 2002.

[26] G.F. Franklin, J.D. Powell, M.L. Workman, *Digital control of dynamic systems*, 3rd edition, Addison-Wesley, 1998.

[27] M. Hagan and M. Menhaj, "Training feedforward networks with the Marquardt algorithm," *IEEE Trans. Neural Netw.*, vol. 5(6), pp. 989-993, Nov. 1994.

[28] X. Fu, S. Li, M. Fairbank, D. C. Wunsch, and E. Alonso, "Training recurrent neural networks with the Levenberg-Marquardt algorithm for optimal control of a grid connected converter," *IEEE Trans. Neural Netw. Learn. Syst.*, Oct. 2014.