

A Compact Trench-Assisted Space-Modulated JTE Design for High-Voltage 4H-SiC Devices

T. Dai¹, L. Zhang, O. Vavasour, A. B. Renz, V. A. Shah, M. Antoniou¹,
P. A. Mawby, *Senior Member, IEEE*, and P. M. Gammon¹, *Senior Member, IEEE*

Abstract—This article proposes a compact trench-assisted space-modulated junction termination extension (TSM-JTE) design for high-voltage 4H-silicon carbide (SiC) devices. In this design, trench structures are introduced into the JTE region to effectively split the termination region into three functional zones. The proposed termination structure is cost effective in terms of the chip area it occupies; for devices rated at 10 kV, the termination structure extends the edge of the device by only 250 μm . Requiring only one implant, it is relatively cheap to fabricate, while a wide implantation dose window endures that is relatively insensitive to variations in dose that may occur during processing. The same advantages occur at 20 kV, the TSM-JTE proving to have the best tradeoff between maximum breakdown voltage and implantation window, compared with other single implant termination designs, achieving this in 500 μm of termination length. At 3.3 kV, a 110- μm TSM-JTE retains its advantages over the other JTE designs, but floating field rings are expected to consume less area, though this is not the case at the higher voltages.

Index Terms—10 kV, 20 kV, junction termination extension (JTE), power device, silicon carbide (SiC).

I. INTRODUCTION

THE superior electrical and thermal properties of silicon carbide (SiC) have made it an excellent candidate for high power applications. 4H-SiC devices rated above 10 kV are an attractive prospect for grid applications, in order to reduce the number of devices required in, for example, voltage-source converters. The realization of these high-voltage devices is based on the continual improvement in the epitaxial growth of thick 4H-SiC ($>100 \mu\text{m}$), with a marked improvement in defect densities [1]; however, the starting wafers remain expensive. As a result, in order to reduce device cost, it is important to maximize device yield and to minimize the area given over to the termination region.

Manuscript received November 13, 2020; revised December 19, 2020; accepted December 22, 2020. This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) under Grant EP/R00448X/1. The review of this article was arranged by Editor T. Kimoto. (*Corresponding author: T. Dai.*)

The authors are with the School of Engineering, University of Warwick, Coventry CV4 7AL, U.K. (e-mail: tianxiang.dai@warwick.ac.uk; luyang.zhang.1@warwick.ac.uk; o.vavasour.1@warwick.ac.uk; a.renz@warwick.ac.uk; vishal.shah@warwick.ac.uk; marina.antoniou@warwick.ac.uk; p.a.mawby@warwick.ac.uk; p.m.gammon@warwick.ac.uk).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TED.2020.3047348>.

Digital Object Identifier 10.1109/TED.2020.3047348

The termination region surrounds the perimeter of a power device chip's active, current carrying central region. Its primary purpose is to alleviate the electric field at the edge of a device, so maximizing the breakdown voltage. However, if the termination is not optimized, breakdown can occur prematurely. This termination region can also be very large, accounting for a large proportion of a chip. Therefore, the following principles must be applied in designing the device's termination: First, the termination must be effective, maximizing the breakdown voltage. Second, its fabrication should be manufacturable and repeatable. This requires a wide implantation dose window for a Junction termination extension (JTE) termination in order to counter variations in dose that can occur between wafers, or wafer lots. Third, to lower costs, the termination should use minimal semiconductor area, requiring a small termination length, L_{term} . Fourth, a minimum number of expensive implant steps should be used.

Floating field ring (FFR) termination is an effective and repeatable design choice at lower voltages, but the chip area they occupy in high-voltage designs is relatively large. A 27-kV 4H-SiC IGBT was reported in 2014 [2], a proof of concept device that used a conventional FFR design that extended the active area by 1500 μm radially, occupying 65% of the 20-A chip area. A more optimized design for 14-kV 4H-SiC p-i-n diode was fabricated [3] with an advanced multiple expansion ratio FFR termination. While this design was 99% efficient, it required a termination length of 720 μm . JTE is another popular option that attracts attention due to the small chip area requirement at high voltage. Implanted single-zone JTE (SZ-JTE) and multizone JTE (MZ-JTE) structures with and without etched steps have been studied extensively [4], [5], while advanced structures such as space-modulated JTE (SM-JTE) and multiple-floating-zone JTE (MFZ-JTE) have been shown to simplify the fabrication process and reduce the implantation cost [4], [6]. In [4], a 15-kV SM-JTE design achieves a wide implantation window ($\pm 56\%$ above 10 kV), using a single implant in 600 μm of extension. In [6], a 10-kV MFZ-JTE was produced in 450 μm of extension with a considerable implantation window ($\pm 41\%$ above 8 kV) compared with conventional SZ-JTE. The design in this article is based on similar principles to the etched JTE with FFRs and middle rings presented in [7]. In this, a 200- μm -long JTE design, optimized for 15-kV devices, was shown to offer an effective solution with a relatively wide implantation

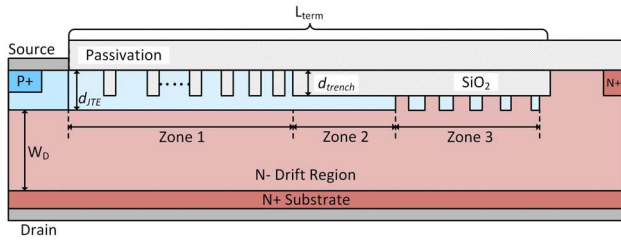


Fig. 1. Proposed TSM-JTE design.

window. Elsewhere, two novel single implant designs have been proposed. A tapered JTE design targeting at 6 kV [8], produced using greyscale photolithography, is $>90\%$ efficient, and occupies $250\ \mu\text{m}$. In [9], an intricate 120 zone JTE is produced utilizing a single mask and a single implant that achieved a breakdown voltage of 12 kV, with termination length over $500\ \mu\text{m}$.

The trench-assisted space-modulated JTE (TSM-JTE) structure introduced in this article is designed to minimize chip area for SiC devices rated to 10 kV and higher. Its novelty lies in the use of space-modulated regions, created by a single implant and a single trench etch into these, making it cheap to produce with a wide implantation window, as well as maximizing the breakdown. This study focuses initially on the development of the TSM-JTE and its optimization at 10 kV, while the results of structures optimized for 20- and 3.3-kV devices are also presented.

II. SIMULATION METHODOLOGY

The TSM-JTE structure proposed in this article is shown in Fig. 1. This structure, and the other structures in this article, were simulated and optimized using TCAD Silvaco. The proposed structure is notionally at the edge of a MOSFET (as in [10]), though the design is applicable to p-i-n diodes [4], [6], [7] and IGBTs [11].

Initially, this structure is optimized for a 10-kV device, using an epitaxial drift region with a width (W_D) of $100\text{-}\mu\text{m}$ layer and a doping of $3.5 \times 10^{14}\ \text{cm}^{-3}$, grown upon an $N + (1 \times 10^{19}\ \text{cm}^{-3})$ substrate. This structure has a theoretical (1-D) maximum breakdown voltage of 15 kV. Both the p-body depth and the JTE depth (d_{JTE}) are 700 nm, presuming a box profile implant. The doping of the JTE region, determined by the implantation dose, is varied in the simulations in order to determine the maximum possible breakdown voltage (V_{BD}) and the implantation window. The implantation window reported is the maximum percentage error in the dose that will maintain the target V_{BD} . The proposed TSM-JTE design is benchmarked to SZ-JTE, SM-JTE, and MFZ-JTE designs, each of which is fabricated with only one implantation step.

The new TSM-JTE design comprises of several trench structures etched into the JTE region with controlled depth (d_{trench}), width, and spacing. This effectively splits the JTE region into three functional zones, which greatly widens the implantation dose window, just as in a MZ-JTE design, except with only one region of implantation. The structure in Fig. 1, when optimized for 10 kV, has 12 trenches etched into the JTE region and filled with silicon dioxide. The outermost trench is

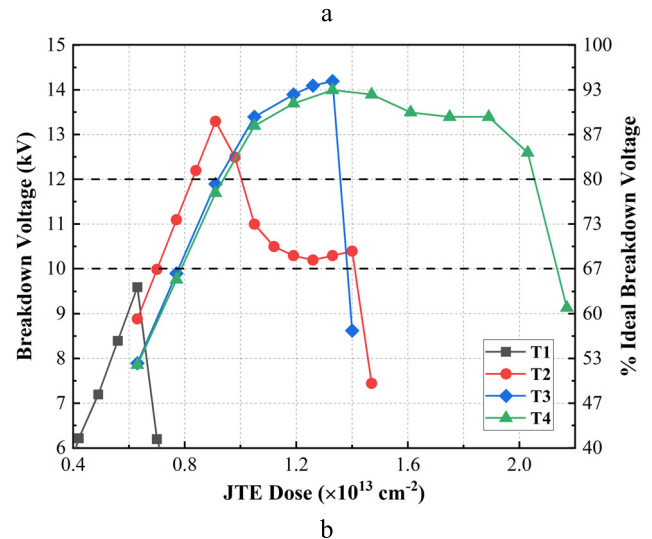
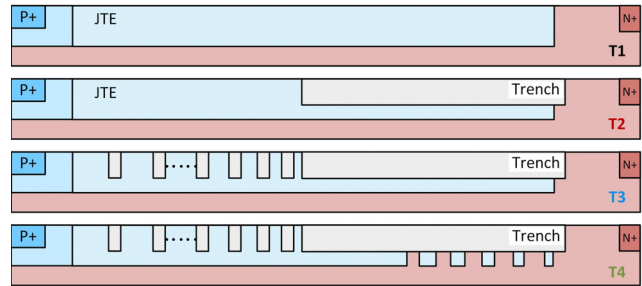


Fig. 2. TSM-JTE (T4) design process, showing (a) incremental designs and (b) their simulated breakdown voltage versus JTE dose.

$130\ \mu\text{m}$ wide while the 11 narrow trenches are all $2\ \mu\text{m}$ wide. The space between the wide trench and the outermost narrow trench is $2\ \mu\text{m}$, with the space to each consecutive small trench incrementing by $1\ \mu\text{m}$ (e.g., 3, 4, and $5\ \mu\text{m}$) every step closer to the center of the device. Five SM-JTE rings are located at the end of termination region which forms Zone 3 in Fig. 1. Their pitch (the sum of the ring width and space) is fixed at $10\ \mu\text{m}$. The initial ring space starts at $3\ \mu\text{m}$, increasing by $1\ \mu\text{m}$ per ring space. The target total termination length L_{term} for the 10-kV devices is $250\ \mu\text{m}$, just $2.5\times$ the drift region width.

III. RESULTS AND DISCUSSION

A. TSM-JTE Optimization

To understand the TSM-JTE, it is important to trace its development. The primary motivation for the work was to improve the design of termination structures that require only one implant, in order to reduce fabrication cost. As a result, the optimization started with a conventional SZ-JTE ($L_{\text{term}} = 250\ \mu\text{m}$) as a reference. This is T1 in Fig. 2(a). Its breakdown voltage and process window are plotted in Fig. 2(b) and summarized in Table I. Quite evidently, an SZ-JTE is not appropriate for high-voltage termination design due to a peak V_{BD} of just 9.6 kV and an extremely narrow process window.

The optimization begins in T2 by etching the wide trench structure into the JTE region, to a depth, d_{trench} , 400 nm from the surface. This simple modification significantly enhances the breakdown voltage, to a peak of 13.3 kV, 89% of the

TABLE I
SUMMARY OF 10-kV SIMULATION RESULTS

Structure	d_{trench} (nm)	Peak V_{BD} (kV)	Dose Window @10 kV	Dose Window @12 kV
SZ-JTE (T1)	-	9.6	-	-
SM-JTE	-	14.1	$\pm 23\%$	$\pm 13\%$
MFZ-JTE	-	12.3	$\pm 28\%$	$\pm 8\%$
T2	400	13.3	$\pm 33\%$	$\pm 10\%$
T3	400	14.2	$\pm 27\%$	$\pm 19\%$
TSM-JTE	300	14.4	$\pm 39\%$	$\pm 29\%$
TSM-JTE (T4)	400	14.0	$\pm 46\%$	$\pm 37\%$
TSM-JTE	500	13.1	$\pm 56\%$	$\pm 18\%$

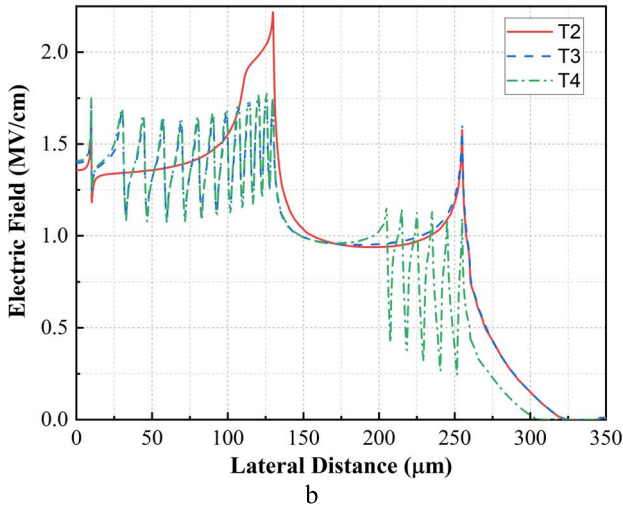
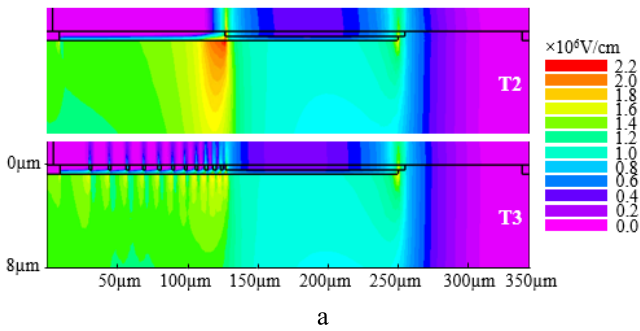


Fig. 3. Simulated (a) electric field distribution and (b) electric field cutline below the JTE/n-drift region junction for structures T2, T3, and T4 all at a reverse voltage of 10 kV.

ideal maximum. The implantation window, at 10 kV, is also improved, to $\pm 33\%$, due to the space modulation effect of the trench, which leads to a near flat tail in the breakdown voltage versus dose curve. However, the window for achieving the peak breakdown voltage is relatively narrow, just $\pm 10\%$ at 12 kV.

When the dose is above $0.9 \times 10^{13} \text{ cm}^{-2}$ the breakdown voltage of T2 structure decreases rapidly. In Fig. 3(a), the electric field distribution of a T2 structure with a dose of $1.1 \times 10^{13} \text{ cm}^{-2}$ is plotted at a reverse voltage of 10 kV. Here, the location of the breakdown can be seen, at the bottom-left

corner of the wide trench, where there is an abrupt change in the geometry. The electric field crowding at this point limits the breakdown voltage for T2.

To relieve the field at the inside edge of the wide trench, the 11 small trenches are inserted to the left of the wide trench, with expanding space between them, resulting in layout T3. The technique used here for spreading the electric field is like an FFR design, though the expansion of the spacing between the trenches is contrary to FFRs, the trench spacing expanding toward the center from right to left. The dose- V_{BD} profile of T3 is improved from T2, having a much higher average breakdown voltage, the peak of which is 14.2 kV, and a window of $\pm 19\%$ at 12 kV. It is also clear from Fig. 3 that the electric field at the bottom-left corner of the wide trench has been distributed between the trenches and the peak electric field reduced.

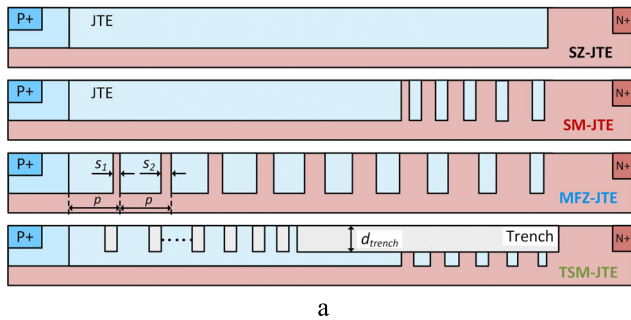
Finally, the addition of the five space-modulated floating JTE rings to the end of the JTE termination leads to the proposed TSM-JTE design, T4 in Fig. 2. This greatly widens the process window, to $\pm 37\%$, by smoothing out the second electric field peak located at $250 \mu\text{m}$ in Fig. 3 (the outer edge of the wide trench), which was responsible for breakdown at doses above $1.3 \times 10^{13} \text{ cm}^{-2}$.

In summary, in the full structure shown in Fig. 1, zones 2 and 3 provide the double space modulation, while zone 1 is mainly responsible for electric field smoothing. The results from all the simulations in Fig. 2 are summarized in Table I.

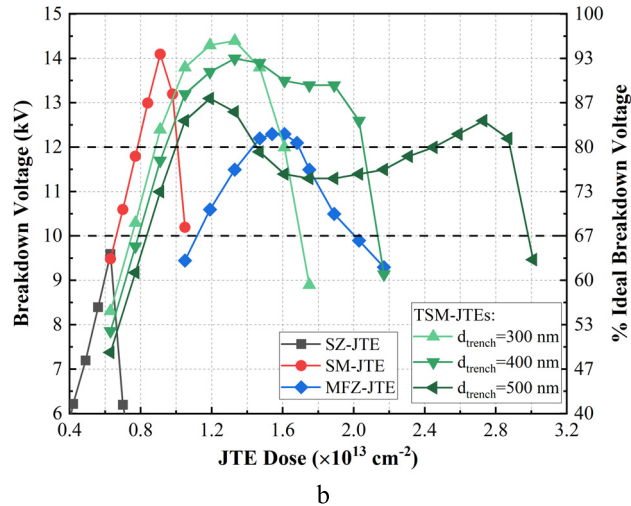
B. Trench Depth Optimization and Benchmarking

The trench depth, d_{trench} , is a critical parameter for the TSM-JTE structure. In Fig. 4 and Table I, simulation results are presented in which d_{trench} is varied from 300 to 500 nm, while the JTE depth is maintained at 700 nm. In the same figure, the proposed TSM-JTE is benchmarked to optimized SZ-JTE, SM-JTE, and MFZ-JTE structures, all of which are illustrated in Fig. 4(a). The JTE implanted region of the SM-JTE structure is the same as that used in the TSM-JTE. The simulated MFZ-JTE structure has 36 JTE zones with a fixed pitch (ring width and space), p , of $7 \mu\text{m}$ per zone. The starting space, s_1 , is set to $2 \mu\text{m}$, with an expansion ratio of 1.02 ($s_{n+1} = 1.02s_n$). The results of the SZ-JTE are plotted again for benchmarking.

The SM-JTE structure achieves a peak breakdown voltage of 94% of the 15 kV maximum, but with a very narrow window. The MFZ-JTE structure offers a larger process window of $\pm 27\%$ at 10 kV, but with a significant reduction of the peak breakdown voltage, down to 82% of the maximum. The center of the process window increases from 9×10^{12} to $1.6 \times 10^{12} \text{ cm}^{-2}$ when an MFZ-JTE is used in place of an SM-JTE. This is due to the enhanced space modulation effect for the MFZ-JTE, where the effective dose is reduced across the entire termination area. There is a close relationship between the SM-JTE and MFZ-JTE. SM-JTE can be treated as an MFZ-JTE with the first grounded JTE being much larger; according to the same principle, MFZ-JTE can be treated as an SM-JTE with the space modulation expanding all the way toward the p-base transition region. Both designs rely on the space modulation effect. However, none of the conventional



a



b

Fig. 4. TSM-JTE with varying d_{trench} benchmarked against 10-kV SZ-JTE, SM-JTE, and MFZ-JTE designs. In (a), these structures are shown and in (b), their simulated breakdown voltage versus JTE dose.

one-implant termination designs simulated herein could be optimized to reach the peak V_{BD} or window of the TSM-JTE designs. From Fig. 4(b), the TSM-JTE design with a d_{trench} of 300 nm offers the highest breakdown voltage of up to 96% of the maximum. However, its process window of $\pm 29\%$ at 12 kV can be improved to $\pm 37\%$ when d_{trench} is increased to 400 nm, with the peak breakdown voltage dropping to 93%. Further increasing d_{trench} to 500 nm causes a further reduction of the peak V_{BD} to 87% of the maximum, but facilitates a very large process window of $\pm 56\%$ at 10 kV.

A trend can be observed across the three TSM-JTE structures, with the process window widening and the peak V_{BD} dropping as d_{trench} increases. The reason for this is as follows: As d_{trench} increases, the effective dose in Zones 2 and 3 reduces. A greater JTE dose is, therefore, required for these two regions to reach their maximum V_{BD} . However, the V_{BD} peak of Zone 1 is less affected by trench depth and its peak remains at the same dose. With a d_{trench} of 300 nm, the peak V_{BD} of all three zones occurs at the same dose, resulting in its large, narrow peak observed in Fig. 4. As d_{trench} increases and the peak voltage associated with Zones 2 and 3 shifts to higher dose, so the process window broadens and the maximum voltage reduces. A d_{trench} of 500 nm is an extreme case in which the two peaks associated with Zone 1, and Zones 2 and 3 have shifted apart so far that there is a significant dip in the breakdown voltage in the center of the process window. This results in the two very narrow peaks at 12 kV.

TABLE II

SUMMARY OF 20-kV SIMULATION RESULTS

Structure	Peak V_{BD} (kV)	Dose Window @20 kV
SZ-JTE	13.7	n/a
SM-JTE	23.8	$\pm 13\%$
MFZ-JTE	21.7	$\pm 12\%$
TSM-JTE	24.3	$\pm 32\%$

As a result, the TSM-JTE structure with a trench depth of 400 nm offers the best tradeoff between the V_{BD} and the process window. However, with a well trialed, controlled implantation process, the use of the TSM-JTE with a trench depth of 300 nm may be preferred.

While this article has focused on the simulation of these structures, the fabrication of the proposed TSM-JTE structure is relatively simple. It adds one extra photolithography and dry etching step after the JTE is implanted. The extra fabrication process is much cheaper compared with ion implantation. The trench depth must be controlled between 400 and 500 nm (preferably close to 400 nm), which can be achieved by the accurate tuning of the dry etching process.

C. Optimizing the TSM-JTE Design for 20-kV Devices

The applicability of the TSM-JTE design has been investigated for even higher voltage devices (> 20 kV). In this section, the n-drift region doping is $2.3 \times 10^{14} \text{ cm}^{-3}$ with a thickness, W_D of 186 μm . This has a theoretical maximum of 25.8 kV.

The same material parameters have been used in published work previously [12], in which the JTE used was a two-Zone SM-JTE with an L_{term} of 600 μm . Here, we shall use the new TSM-JTE to reduce this to 500 μm , while only one implantation will be used, reducing the fabrication cost.

The JTE implanted region of the SM-JTE structure is the same as that used in the TSM-JTE. The simulated MFZ-JTE structure has 50 JTE zones with a pitch of 10 μm for each zone. The starting space is set to 2 μm , and the expansion ratio for the spaces is 1.026.

At 20 kV, the TSM-JTE structure comprises of 17 small trenches and one wide trench. As before, the trench spacing between the wide trench and the first small trench is 2 μm with every consecutive space 1 μm wider than the last. The wide trench is 160 μm wide. Four SM-JTE rings are located at the end of the termination region with ring width fixed at 3 μm and ring space starts at 3 μm and expands by 1 μm per ring. The trench depth remains 400 nm.

The results are shown in Fig. 5 and summarized in Table II. Just as at 10 kV, the similar SM-JTE and MFZ-JTE structures have a high V_{BD} but a narrow window. In contrast, the proposed TSM-JTE design offers the best V_{BD} (24.3 kV; 92% of maximum) and a process window of $\pm 32\%$ at 20 kV, therefore, offering a high likelihood of achieving the targeted breakdown voltage.

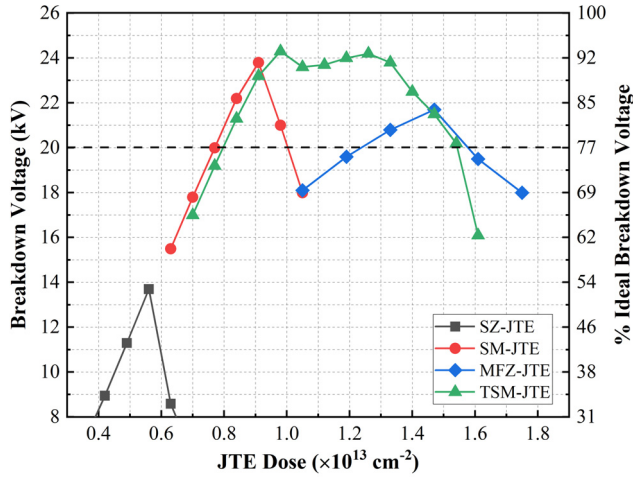


Fig. 5. Simulated breakdown voltage versus JTE dose of the TSM-JTE, compared with SZ-JTE, SM-JTE, and MFZ-JTE optimized for 20 kV.

D. Optimizing the TSM-JTE Design for 3.3-kV Devices

Although the TSM-JTE was designed initially for high-voltage devices, the proposed termination design can also be applied to a lower voltage range. The performance is again benchmarked to the SZ-JTE, SM-JTE, and MFZ-JTE, single implant layouts.

In this section, the n-drift region doping is $3 \times 10^{15} \text{ cm}^{-3}$ with a thickness, W_D of $28 \mu\text{m}$. This has a theoretical maximum of 4.02 kV. There are six small trenches in total having $2\text{-}\mu\text{m}$ trench width. The trench space starts at $2 \mu\text{m}$ and expands by $1 \mu\text{m}$ per trench. For the 3.3-kV rating, only three floating JTE rings are employed with a pitch of $6 \mu\text{m}$, the ring space incrementing from 2 to $4 \mu\text{m}$. The total length of the termination for the TSM-JTE is $110 \mu\text{m}$ (Zone 1 = $70 \mu\text{m}$, Zone 2 = $22 \mu\text{m}$, and Zone 3 = $18 \mu\text{m}$). As mentioned earlier, Zone 1 smooths the electric field around the bottom corner of the big trench and, therefore, it is not possible to reduce Zone 1 proportionally in line with the voltage rating.

The simulated SM-JTE has the same JTE implantation pattern as the TSM-JTE. For the MFZ-JTE, the termination region has been separated into 15 zones with one grounded JTE and 14 floating JTE rings. Their pitch is fixed at $7 \mu\text{m}$, the ring spacing starting at $2 \mu\text{m}$, increasing with an expansion ratio of 1.08. Unlike at 10 and 20 kV, the MFZ-JTE at 3.3 kV does not have a steep breakdown voltage drop after reaching its maximum breakdown voltage. This occurs because of the approximate equivalence in optimal design lengths (L_{term}) at 3.3 kV between the JTE and FFR terminations. As the doping in the MFZ-JTE design is increased beyond its optimal value, the rings begin to behave instead like FFRs, maintaining a high V_{BD} . This does not occur in the MFZ-JTE designs at 10 and 20 kV, because the optimal FFR design would occupy a much wider L_{term} than the MFZ-JTE.

Comparing the JTE designs, similar conclusions to those previous voltage ratings can be drawn from the simulation results shown in Fig. 6 and Table III. The proposed TSM-JTE design offers the best tradeoff between maximizing V_{BD} (3.91 kV, 97%) and the process window ($\pm 54\%$ at 3 kV). It is also more compact than other JTE designs proposed at a

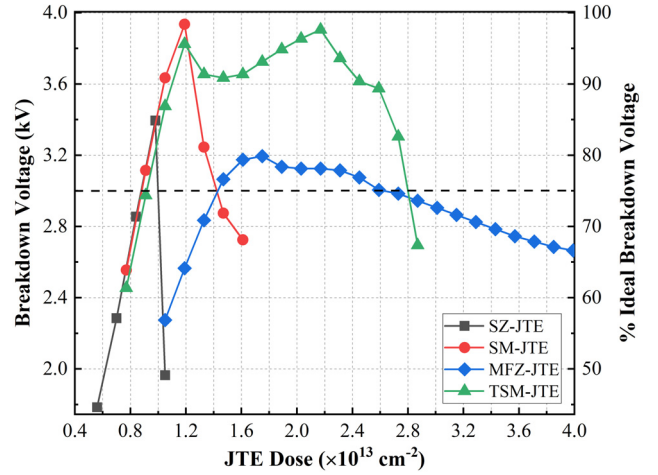


Fig. 6. Simulated breakdown voltage versus JTE dose of the TSM-JTE, compared with SZ-JTE, SM-JTE, and MFZ-JTE optimized for 3.3 kV.

TABLE III
SUMMARY OF 3.3-kV SIMULATION RESULTS

Structure	Peak V_{BD} (kV)	Dose Window @3 kV
SZ-JTE	3.40	$\pm 7\%$
SM-JTE	3.94	$\pm 24\%$
MFZ-JTE	3.20	$\pm 30\%$
TSM-JTE	3.91	$\pm 54\%$

similar voltage [13]. However, as mentioned before, in contrast to the higher voltages before, one must also consider FFR designs at 3.3 kV, which can be implanted at the same time as the p+ source contact. A $25\text{-}\mu\text{m}$ drift region in [14] reached 2.8 kV, 80% of the theoretical maximum, in under $50 \mu\text{m}$ of termination, suggesting that JTE designs at 3.3 kV may not be optimal.

IV. CONCLUSION

The proposed TSM-JTE structure is a novel termination design requiring only one implantation that is appropriate for high-voltage SiC devices. As well as the benefit of requiring only one implant, the TSM-JTE can maximize V_{BD} , requiring only a relatively narrow termination length. Furthermore, its wide implantation dose window means it is practically realizable.

The TSM-JTE has been benchmarked to other single-implant JTE structures, the SZ-JTE, SM-JTE, and MFZ-JTE, at 10, 20, and 3.3 kV. At 10 kV, the optimal TSM-JTE achieves a peak breakdown voltage of 14 kV (93% of the theoretical maximum) with an implantation window of $\pm 46\%$. This is achieved with a termination length of just $250 \mu\text{m}$, with the SM-JTE and MFZ-JTE design at this length unable to match V_{BD} and implantation window. In comparison with published work, the TSM-JTE termination length is much narrower, 58% and 44% of the SM-JTE [4] and MFZ-JTE [6] designs. Compared with the TSM-JTE, the termination length of the 15-kV trench design in [7] is narrower by $50 \mu\text{m}$, but the

implantation window is narrower and the fabrication process more complex.

In optimizing the termination structures for 20 kV, the TSM-JTE offers the highest V_{BD} (24.3 kV; 92% of maximum) and a process window of $\pm 32\%$ in a termination length of 500 μm . This compares well with a two-step implanted SM-JTE in the literature [12], which has a 20-kV window of $\pm 35\%$, a termination length 20% wider, and twice the implantation cost. At 3.3 kV, the TSM-JTE remains the best JTE design, particularly, its dose window, but the chip area reduction is less significant when compared with FFRs.

The introduction of trench structures into the termination region will likely result in interface charge on the trench sidewalls. However, in this article, the impact of interface and oxide charge on the dose window shift has not been studied. In the future, the simulation will be calibrated to account for these effects, using experimental results.

REFERENCES

- [1] M. Yazdanfar, I. G. Ivanov, H. Pedersen, O. Kordina, and E. Janzén, "Reduction of structural defects in thick 4H-SiC epitaxial layers grown on 4° off-axis substrates," *J. Appl. Phys.*, vol. 113, no. 22, 2013, Art. no. 223502, doi: [10.1063/1.4809928](https://doi.org/10.1063/1.4809928).
- [2] E. van Brunt *et al.*, "27 kV, 20 A 4H-SiC n-IGBTs," *Mater. Sci. Forum*, vols. 821–823, pp. 847–850, Jun. 2015, doi: [10.4028/www.scientific.net/MSF.821-823.847](https://doi.org/10.4028/www.scientific.net/MSF.821-823.847).
- [3] X. Deng *et al.*, "A near ideal edge termination technique for ultrahigh-voltage 4H-SiC devices with multi-zone gradient field limiting ring," in *Proc. 1st Workshop Wide Bandgap Power Devices Appl. Asia (WiPDA Asia)*, Xi'an, China, May 2018, pp. 144–148, doi: [10.1109/WiPDAAsia.2018.8734553](https://doi.org/10.1109/WiPDAAsia.2018.8734553).
- [4] G. Feng, J. Suda, and T. Kimoto, "Space-modulated junction termination extension for ultrahigh-voltage p-i-n diodes in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 414–418, Feb. 2012, doi: [10.1109/TED.2011.2175486](https://doi.org/10.1109/TED.2011.2175486).
- [5] C.-N. Zhou, R.-F. Yue, Y. Wang, J. Zhang, G. Dai, and J.-T. Li, "10-kV 4H-SiC gate turn-off thyristors with space-modulated buffer trench three-step JTE," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1199–1202, Aug. 2018, doi: [10.1109/LED.2018.2849829](https://doi.org/10.1109/LED.2018.2849829).
- [6] W. Sung, E. Van Brunt, B. J. Baliga, and A. Q. Huang, "A new edge termination technique for high-voltage devices in 4H-SiC—multiple-floating-zone junction termination extension," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 880–882, Jul. 2011, doi: [10.1109/LED.2011.2144561](https://doi.org/10.1109/LED.2011.2144561).
- [7] X. Zou, R. Yue, and Y. Wang, "Etched junction termination extension with floating guard rings and middle rings for ultrahigh-voltage 4H-SiC PiN diodes," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Hong Kong, Aug. 2016, pp. 418–421, doi: [10.1109/EDSSC.2016.7785297](https://doi.org/10.1109/EDSSC.2016.7785297).
- [8] E. A. Imhoff *et al.*, "High-performance smoothly tapered junction termination extensions for high-voltage 4H-SiC devices," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3395–3400, Oct. 2011, doi: [10.1109/TED.2011.2160948](https://doi.org/10.1109/TED.2011.2160948).
- [9] V. Veliadis *et al.*, "Process tolerant single photolithography/implantation 120-zone junction termination extension," *Mater. Sci. Forum*, vols. 740–742, pp. 855–858, Jan. 2013, doi: [10.4028/www.scientific.net/MSF.740-742.855](https://doi.org/10.4028/www.scientific.net/MSF.740-742.855).
- [10] S.-H. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, and A. Hefner, "10 kV, 5A 4H-SiC power DMOSFET," in *Proc. IEEE Int. Symp. Power Semiconductor Devices IC's*, Naples, Italy, Jun. 2006, pp. 1–4, doi: [10.1109/ISPSD.2006.1666122](https://doi.org/10.1109/ISPSD.2006.1666122).
- [11] A. Kadavelugu *et al.*, "Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, Sep. 2013, pp. 2528–2535, doi: [10.1109/ECCE.2013.6647027](https://doi.org/10.1109/ECCE.2013.6647027).
- [12] H. Niwa, J. Suda, and T. Kimoto, "21.7 kV 4H-SiC PiN diode with a space-modulated junction termination extension," *Appl. Phys. Exp.*, vol. 5, no. 6, Jun. 2012, Art. no. 064001, doi: [10.1143/APEX.5.064001](https://doi.org/10.1143/APEX.5.064001).
- [13] W. Sung and B. J. Baliga, "A comparative study 4500-V edge termination techniques for SiC devices," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1647–1652, Apr. 2017, doi: [10.1109/TED.2017.2664051](https://doi.org/10.1109/TED.2017.2664051).
- [14] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. Hoboken, NJ, USA: Wiley, 2014, p. 432, doi: [10.1002/9781118313534](https://doi.org/10.1002/9781118313534).