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Simulation of the Thermal Performance of HTS Coated Conductors for HVDC SFCL

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Abstract. Within the EU-funded project FastGrid a resistive superconducting fault current limiter for DC-application is actually under development. To reduce substantially the amount of deployed superconducting tape an increase of voltage per length in the limitation case is needed. Moreover, the resistive transition (quench) should be fast and uniform. In the present work, the thermal behavior of three different architectures of coated conductors are investigated by means of transient simulations. The first architecture is composed by an additional Hastelloy shunt layer, which is supposed to avoid overheating of the conductor during fault limitation. The other architectures include layers of silver and copper as stabilizers. Our parameter study including the geometries of the different layers and the inhomogeneity of the critical current density of the superconducting tape shall lead to an optimized tape layout. First comparisons with experiment indicate, that, with the first architecture, electric field strength up to 100 V/m should be within reach.

1. Introduction

In the forthcoming years the goal of European energy policy is to provide a secure, sustainable and competitive energy supply [1]. Electricity is a key point to this goal because it can be generated from a variety of sources (including renewable sources). To ensure that electricity supply is maintained, the European Union wants to hasten the integration of dozens of electrical connections across the continent and establish a competitive, secure, transparent and completely harmonized Europe-wide internal electrical energy market [2].

High voltage direct current transmission (HVDC) technology plays a great role on large capacity transmission systems [3, 4]. Therefore, the protection for the HVDC transmission line becomes particularly important, because the impact of DC faults is wider and damage is more serious. One of the barriers for the development of HVDC systems is the lack of technologies which enable fault protection [5–7].

Resistive superconducting fault current limiters (R-SFCL) have been proposed in order to mitigate the effects of fault currents in DC grids and to improve the system stability during fault conditions [7–11]. The FastGrid project was launched in 2017, aims to develop "low cost" robust HTS conductors for HVDC SFCL [12, 13] and gathers 12 academic or industrial partners: CNRS Grenoble (coordinator), CSIC/ICMAB, EPM, EPFL, IEE, KIT, Oxolutia,

RSE, SuperGrid Institute, STU, TAU and THEVA. The effectiveness of the solutions will be tested on a 50 kV – 1.5 kA demonstrator (designed as a scalable solution for a HV device) [14].

In this work we investigate the thermal performance of the HTS conductor design proposed within the FastGrid project by comparing it with HTS tapes frequently described in the literature. Our goal is, by means of numerical simulation, to determine the temperature distribution $T(x, y, t)$ after the fault period for each tape architecture and evaluate if such distribution can lead to permanent damages on the tape. Critical current inhomogeneity has been taken into account in this study. The simulation model is based on the finite difference method (FDM), which is solved using the alternating direction implicit routine (ADI) [15–17].

2. HTS Coated Conductors

The architecture of HTS conductors is a result of the manufacturing process and the need for electrical, thermal and mechanical stabilization. In general, it consists of stacked layers of different materials. Figure 1 illustrates the three tapes designs considered in this manuscript whereas table 1 lists the thickness values of the layers. The design *Tape 01* is that one proposed in the FastGrid project and is manufactured by THEVA Dünnschichttechnik GmbH. It uses a REBCO tape with an additional soldered layer of Hastelloy® which serves as shunt and increases the thermal heat capacity of the tape. Such conductor is designed to withstand an electric field higher that 130 V/m for a clearing time of 50 ms
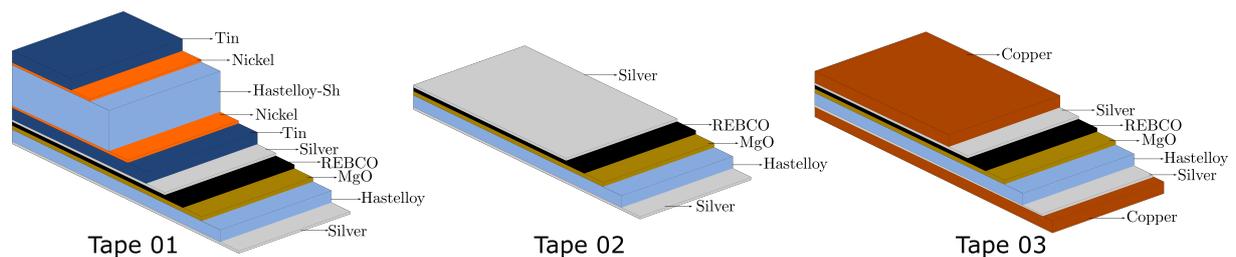
Figure 1. Tape designs considered for comparisons in this work. All the designs are manufactured by THEVA Dünnschichttechnik GmbH.

Table 1. Thickness of each layer for all considered tape designs.

| | Design | | |
	Tape 01	Tape 02	Tape 03
Length	34 cm	34 cm	34 cm
Tin	10 μm	-x-	-x-
Nickel	1.0 μm	-x-	-x-
Hastelloy Shunt	500 μm	-x-	-x-
Silver	2.0 μm	2.0 μm	2.0 μm
REBCO	3.1 μm	3.1 μm	3.1 μm
MgO	3.5 μm	3.5 μm	3.5 μm
Hastelloy Substrate	100 μm	100 μm	100 μm
Copper	-x-	-x-	20 μm

Designs *Tape 02* and *Tape 03* corresponds to the products TPL1100 and TPL4100 series, likewise manufactured by THEVA. These both designs are considered for comparisons aiming to determine the better tape architecture to support thermal stresses.

2.1. Critical Current Inhomogeneity

Since one deals with thermal performance in this work, it is meaningful to consider the variation of critical current along the length of the tape $I_c(x)$, i.e., the critical current inhomogeneity. We have imported in the simulation algorithm measured data provided by THEVA. Measurements were carried out using the TapeStar inductive measurement technique [18]. Precisely the same tape is later used for experiments (see section 4.1).
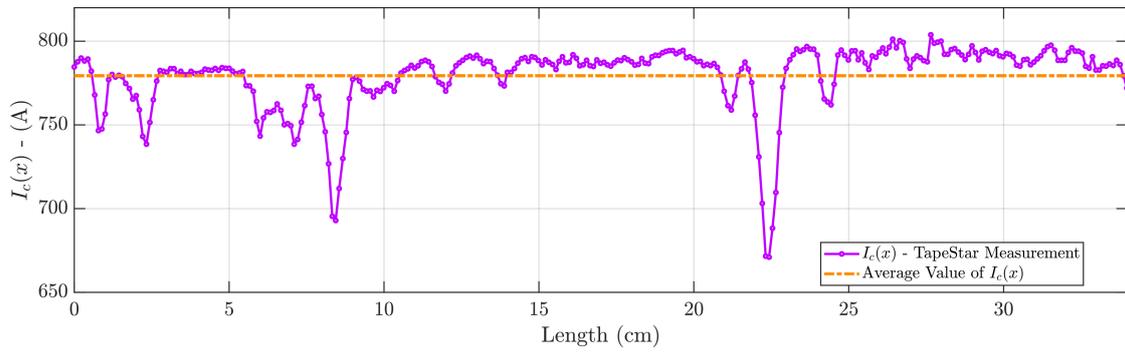
**Figure 2.** Data of the critical current distribution along the length provided by THEVA.

The critical current distribution shown in figure 2 was considered for all the three designs (average $I_{c,av}$ equals to 780 A). In such a way we can obtain a meaningful comparison of the thermal behavior of the different stabilized tapes. The I_c values shown in figure 2 were measured at 77 K. In the simulations, each point follows a linear decrease with the temperature:

$$I_c(x, T) = I_c(x, 77) \left[\frac{T_c - T}{T_c - 77} \right] \tag{1}$$

From figure 2, it is to expect that points near to $\ell = 8.5$ cm and $\ell = 22.5$ cm should obtain highest local temperature values, since at these positions the lowest I_c values are found.

3. Simulation Model

For the simulations we assume that the HTS conductors are in series with a R-L load and a DC voltage source, as shown in figure 3. A DC electrical current i begins to flow in the system when the switch S is closed. The magnitude of the electrical current is defined by the value of the R-L load. Several simulations were performed (considering an applied voltage of 51 V = 34 cm × 1.5 V/cm) to find out the dependence of the maximal temperature with the value of the fault current i.
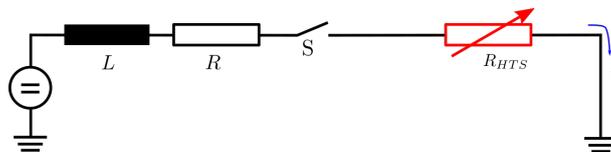
Figure 3. Electrical circuit for the simulation of the thermal behavior.

In order to calculate the temperature $T(x, y, t)$ of the HTS tapes, the heat conduction equation must be taken into account. The y-direction is perpendicular to the tape surface. The temperature along the width of the tape is assumed to be constant. This is justified since in all cases the thickness of the tape is small compared to its width. The simulations are thus made in two dimensions and the Fourier-equation for heat conduction has the form

$$dc\frac{\partial T(x, y, t)}{\partial t} = k\left[\frac{\partial^2 T(x, y, t)}{\partial x^2} + \frac{\partial^2 T(x, y, t)}{\partial y^2}\right] + \dot{g} \tag{2}$$

where d, c, k, and $\dot{g}$ denote the specific mass, the specific heat, the thermal conductivity, and the internal heat generation (per unit volume) for each, respectively. As a boundary condition for equation 2, we have assumed a convective heat transfer between the tapes and the cooling bath (LN$_2$ at 77 K). The heat transfer coefficient $h(\Delta T)$ is not constant and depends on the temperature difference between the surface of the tape and LN$_2$. For the forthcoming simulations, the $h(\Delta T)$ curve presented in [19, 20] have been implemented.

The internal heat generation $\dot{g}$ is defined, for each layer, as:

$$\dot{g} = \rho \times J^2 \tag{3}$$

being ρ the resistivity and J the current density. For the HTS layer, the resistance depends on the so-called E-J curve [21, 22] and has been also implemented in the current work. Because of the high nonlinear resistivity of the superconducting material the aforementioned boundary and initial value problem becomes highly nonlinear and its coupling to the differential equation of the electrical circuit precludes a purely analytical solution.

The development of a numerical method for transient thermal analysis of HTS tapes for SFCL have been widely developed in the literature [23]. The use of the FDM based on the ADI routine was introduced in [15–17]. Basically, it consists on dividing each time step Δt of the simulation process in two parts: in the first half-timestep, equation 2 is solved implicitly in the x-direction, whereas the y-direction is solved explicitly. In the second half-timestep, the process is inverse. Hence, for the first half-timestep, the discretization of equation 2 is:

$$dc\frac{T_{i,j}^{t+\frac{\Delta t}{2}} - T_{i,j}^t}{\Delta t/2} = k\left[\frac{T_{i,j-1}^{t+\frac{\Delta t}{2}} - 2T_{i,j}^{t+\frac{\Delta t}{2}} + T_{i,j+1}^{t+\frac{\Delta t}{2}}}{\Delta x^2} + \frac{T_{i-1,j}^t - 2T_{i,j}^t + T_{i+i,j}^t}{\Delta y^2}\right] + \dot{g} \tag{4}$$

For the second half-timestep the process is inverse, i.e., the y-direction is solved implicitly, whereas the x-direction is solved explicitly:

$$dc\frac{T_{i,j}^{t+1} - T_{i,j}^{t+\frac{\Delta t}{2}}}{\Delta t/2} = k\left[\frac{T_{i,j-1}^{t+\frac{\Delta t}{2}} - 2T_{i,j}^{t+\frac{\Delta t}{2}} + T_{i,j+1}^{t+\frac{\Delta t}{2}}}{\Delta x^2} + \frac{T_{i-1,j}^{t+1} - 2T_{i,j}^{t+1} + T_{i+i,j}^{t+1}}{\Delta y^2}\right] + \dot{g} \tag{5}$$

Further details about the simulation routine, as well as its effectiveness and stability for simulations of SFCL devices are presented in [24–26].


4. Results

Figure 4 shows the simulated results considering that the DC voltage source is set at 51 V, which corresponds to 150 V/m (tape total length is $\ell = 34$ cm). The R-L load was configured to produce a prospective fault current of about 2.5 kA.

As shown in figure 4a, the limitation is higher for *Tape 02* and *Tape 03*. Because of the additional layers (Hastelloy shunt, nickel and tin) the equivalent resistance of *Tape 01* is at the lowest (figure 4c), therefore, leads to a lower limitation factor. The voltage drop over the tape
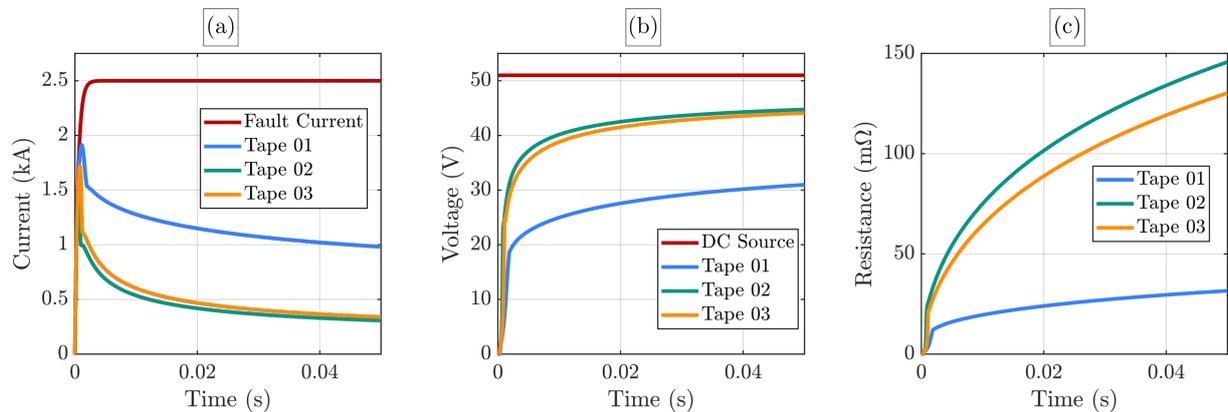
Figure 4. Comparisons of the simulated results for each tape design. (a) Limited current in relation to the prospective fault current, (b) voltage drop over the tape in comparison with the DC voltage source and (c) resistance development during the fault period.
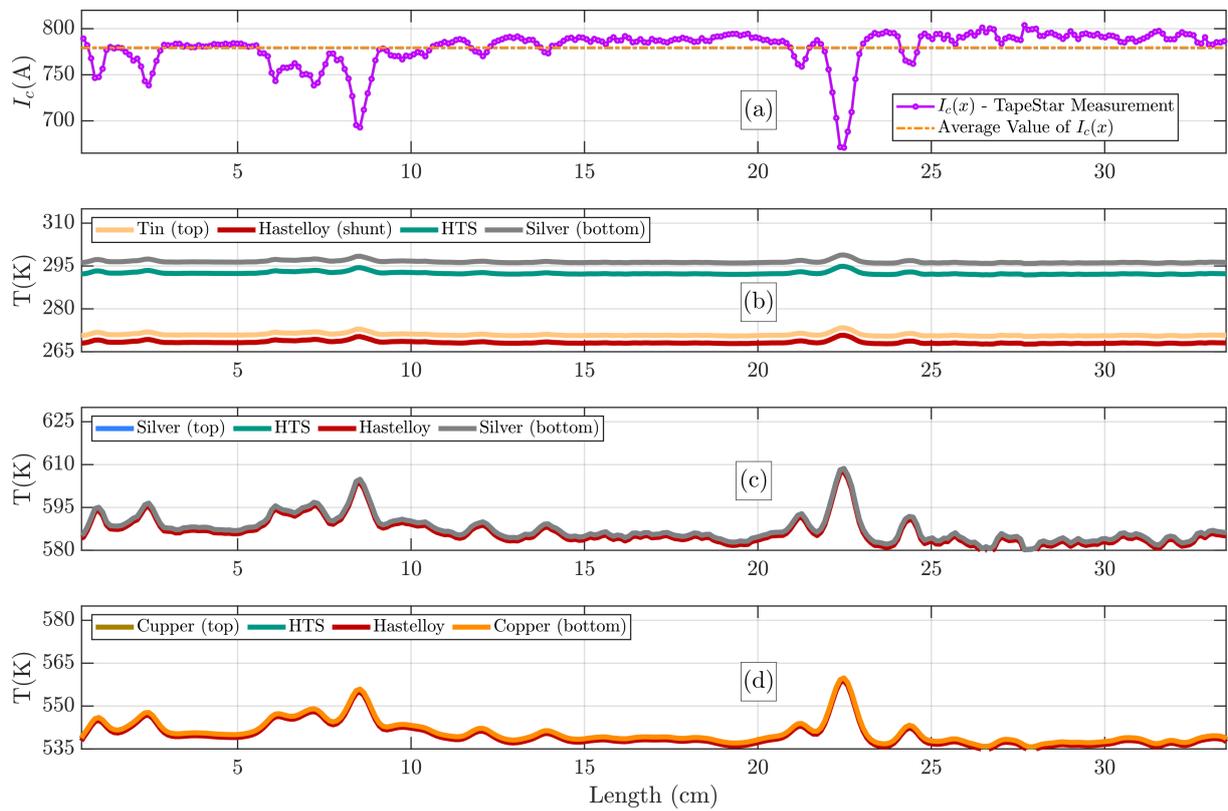
Figure 5. (a) Critical current inhomogeneity $I_c(x, 77)$ and temperature along the length at the end of the fault period for (b) *Tape 01*, (c) *Tape 02* and (d) *Tape 03*.

terminals is shown in figure 4b and is at highest for *Tape 02*, since this one presents the highest resistance value.

For sake of clarity we have plotted the critical current inhomogeneity considered in this work in figure 5a again, to show the corresponding position of hots-pots. It allows us to recognize that, for all considered tape designs, the highest temperature values occurs invariably at the

points where $I_c(x, T)$ is the lowest. As expected, near $\ell = 8.5$ cm and $\ell = 22.5$ cm, are the hot-spot and at those points we observe higher temperature values, regardless of the tape design.

The tape design, however, is very important regarding the magnitude of the achieved temperature value. Such values occur at the defect point, near $\ell = 22.5$ cm. It is clear that, at the end of the fault period, the temperature values of *Tape 01* (figure 5b) are at the lowest in comparison with those show by *Tape 02* and *Tape 03* (figures 5c and 5d respectively). Because of the additional layers (i.e., hastelloy shunt, nickel and tin) the heat capacity of *Tape 01* drastically increases and consequently slows down the heating during the fault period. Based on the same argument, we can state that *Tape 02* shows highest temperature values because of its low thermal capacity.

An interesting feature to be observed in the results presented in figure 5 is the temperature gradient along the thickness (figure 5b) which occurs in *Tape 01*. That is a consequence of the thick hastelloy shunt layer soldered on the top of the conductor. Since Hastelloy has a low thermal conductivity as well as an elevated specific heat, the heat generated at the bottom part of the conductor can be barely transferred to the layers at the upper section. Such temperature gradient does not develop in case of thinner tapes, how is the case of *Tape 02* and *Tape 03*. Both develop nearly no temperature gradient along the thickness.

Several simulations were performed in order to investigate the thermal response of each tape architecture. Graphs shown in figures 4 and 5 presents only results of a same prospective fault current ($I_{fault} = 2.5$ kA). Nevertheless, figure 6 shows the maximum temperatures obtained from the simulations for different values of prospective fault current ranging from 0.5 kA to 3.5 kA (i.e. from $0.64 \cdot I_{c,av}$ to $4.5 \cdot I_{c,av}$). In this plot we can identify that the highest temperature values occur between $1.0 \cdot I_{c,av}$ to $1.5 \cdot I_{c,av}$. In [14] such range was named as hot-spot regime.
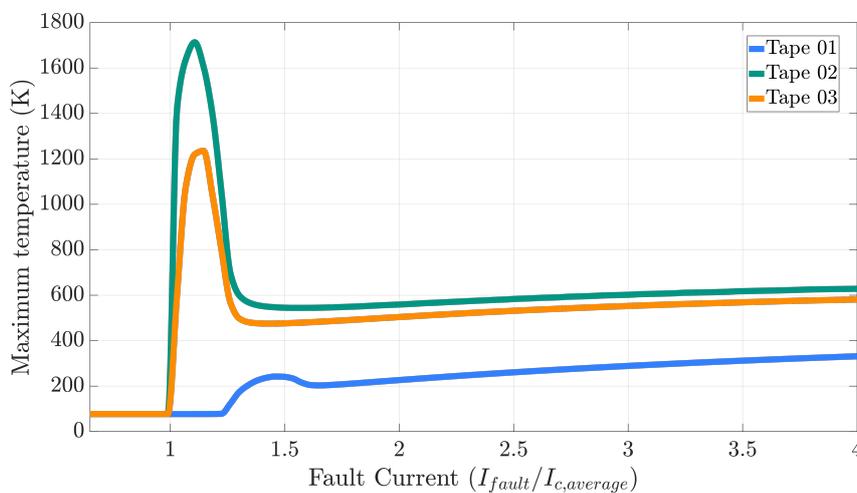
Figure 6. Calculated maximum temperature values at the end of the fault period (50 ms) versus applied prospective fault current (in relation to $I_{c,av} = 780$ A).

In the hot-spot regime the quench begins earlier in the defect position and if the generated heat is not removed (or propagated) effectively, the temperature at these positions will reach huge values, which may lead to the complete destruction of the conductor. That is exactly what happens for the designs *Tape 02* and *Tape 03*: the heat capacity in these tapes architecture is to small and there is a large amount of heat generated in the hot-spots. Since the produced heat is neither removed neither propagated efficaciously, one observes very high temperature values in this range of prospective fault current ($1.0 \cdot I_{c,av}$ to $1.5 \cdot I_{c,av}$). It should be mentioned, that in the real life application, all values of prospective currents may occur.

In the case of design *Tape 01*, temperature values are lower since this tape has a higher thermal heat capacity. Thus, we can conclude that the additional layers soldered on the upper side enhance the heat propagation along the length of the tape.

For all observed cases in figure 6, the weak zone plays no role if the fault currents are high compared to $I_{c,av}$ since the full length quenches.

4.1. Comparison with Experiments

The simulation results shown in the last section indicate the design *Tape 01* is the most suitable to withstand DC fault currents under the 150 V/m condition. In order to validate the simulations, we have performed fault current experiments with several samples provided by THEVA (see figure 7a).
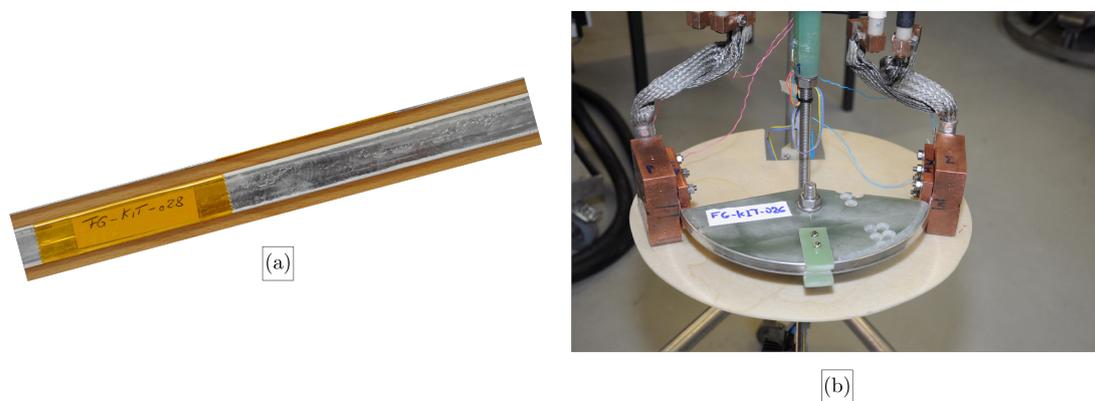
Figure 7. (a) Sample of the HTS conductor (design *Tape 01*) manufactured by THEVA for the FastGrid Project, and (b) experimental setup for fault current experiments at KIT.

The samples were tested at the Institute for Technical Physics (ITEP) of the Karlsruhe Institute of Technology (KIT), as shown in figure 7b. Although the goal is the development of an optimal conductor for DC systems, the experiments tests were carried out in AC regime for technical reasons. This is not a problem, since our target was to validate the simulation model.

Two different tests were carried out: in the first fault current limitation test (duration of 50 ms) a AC voltage of 28.9 V was applied to a sample of 34 cm (which corresponds to 85 V/m). In the second test (duration of 20 ms), a AC voltage of 51 V (150 V/m) was applied to the same sample. The critical current inhomogeneity for the tested tape is that one shown in figure 2.

Figure 8 presents a comparison of experiments and simulations for precisely the sample for which the inhomogeneity is depicted in figure 2. We show the results for both applied voltages. As can be seen, a very good agreement between the results was achieved. Differences between simulations and experiments are below 3 %. Therefore, we can state the developed simulation model is suitable to evaluate the thermal behavior of HTS conductors for fault current limitation.

5. Conclusions

In this work we have presented a simulation model based on the FDM-ADI solution developed to simulate the thermal behavior of HTS conductors for fault current limitation. Since a good agreement between experiments and numerical simulation has been found, it is fair to assume that the simulation model can be considered reliable and credible to be used in this kind of study, such us to optimize the architecture of HTS for an application case.

According to the results given by the simulation, we can conclude that the design *Tape 01* is more indicated to withstand DC voltages of 150 V/m, since its thermal behavior can be considered more effective when compared to the designs of *Tape 02* and *Tape 03*.
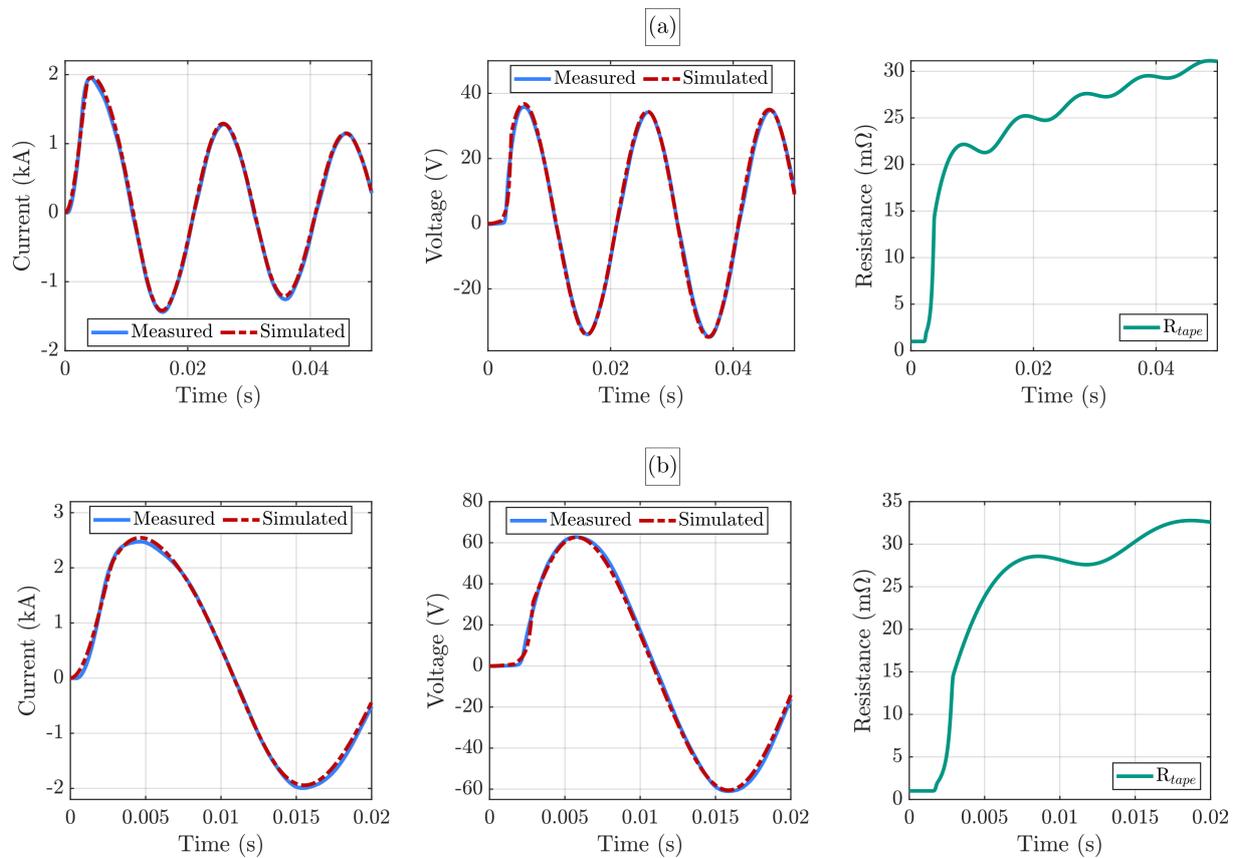
Figure 8. Comparison between experiments and simulations for (a) 85 V/m and (b) 150 V/m.

By means of the simulation model, we could observe that, although *Tape 02* and *Tape 03* yield to a better limitation factor, such designs may fail if the fault current lies between $1.0 \cdot I_{c,av}$ to $1.5 \cdot I_{c,av}$. In this range, the observed temperature values would certainly lead to a complete destruction of the HTS conductor.

It is important, however, to mention that the design *Tape 01* contains soldering between the ordinary tape architecture and the additional layers. It means, if the additional shunt layers are not properly soldered to the tape, high temperature values will be observed in the defect solder point what may also lead to the destruction of the tape. In fact, this has been already observed in some experiments carried out at KIT/ITEP. At present, a good soldering process is under investigation, in order to guarantee an optimal limitation factor and thermal properties of the proposed tape design.

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