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Back-Gate Bias Dependence of the Statistical Variability of FDSOI MOSFETs With Thin BOX

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***Abstract*—The impact of back-gate bias on the statistical variability (SV) of FDSOI MOSFETs with thin buried oxide (BOX) is studied via 3-D "atomistic" drift-diffusion simulation. The impact of the principal sources of SV, i.e., random dopant fluctuations, line edge roughness, and metal gate granularity, on threshold voltage, drain-induced barrier lowering, and drive current is studied in detail. It is shown that reverse back-bias is beneficial in terms of reducing the dispersion of the OFF-current and the corresponding standby leakage power, whereas forward back-bias reduces the ON-current variability. The correlation coefficients between relevant figures of merit and their trends against back-bias are also studied in detail, providing guidelines for the development of statistical compact models of thin-BOX FDSOI MOSFETs for low-standby-power circuit applications.**

***Index Terms*—Back-gate bias, line edge roughness (LER), metal gate granularity (MGG), random dopant fluctuation (RDF), statistical variability (SV), thin buried oxide (BOX).**

I. Introduction

STATISTICAL variability (SV) has become one of the major challenges to CMOS device scaling and integration beyond the 45-nm technology node [1]–[3]. Arising from the discreteness of charge and granularity of matter, the impact of SV adversely affects supply voltage scaling and is difficult to eliminate by simply tuning the fabrication process [4], [5]. This forces the industry to adopt novel device architectures and to advance the traditional deterministic design flow of circuits and systems by adopting statistical circuit simulation and verification technology with the support of the corresponding statistical compact models [5], [6]. Statistical 3-D TCAD simulations greatly facilitate this process in terms of 1) understanding the role and importance of the different sources of SV and 2) making the right technology and device choices and advancing the development of statistical compact models.

Conventional bulk MOSFETs require very high channel doping in order to suppress short-channel effects (SCEs). As a result, it greatly suffers from random dopant fluctuation (RDF) [6], [7]. Planar fully depleted (FD) silicon-on-insulator (SOI) MOSFETs with superior electrostatic integrity can tolerate very low channel doping and, in this way, can greatly suppress the impact of RDF-induced SV. Such devices have demonstrated record low threshold voltage $(V_{\rm TH})$ fluctuations, with an experimentally reported mismatch coefficient on the order of 1–1.3 mV $\cdot$ μm [8], [9]. However, RDF in the source and drain access region that is adjacent to channel—termed SD-RDF—leads to small residual fluctuations and has a pronounced impact on the ON-current variability via fluctuations in the source/drain resistance [10], [11]. Line edge roughness (LER) and metal gate granularity (MGG) remain important sources of SV for FD-SOI technology [8], [10]. The latter can be technologically improved, e.g., by adopting a gate-last process, whereas the former improves with the reduction in the silicon body thickness.

The introduction of devices with ultrathin body and BOX (UTBB) somewhat relaxes the demand for $T_{\rm Si}$ scaling by providing a background plane, which reduces the drain field penetration in the channel region. It also helps to establish a large on/off drain current ratio by back-gate bias (V_b) control [12], [13]. This is essential for low-standby-power (LSTP) devices, where reverse back-gate bias is applied to reduce the power dissipation in a standby mode, whereas forward bias is used to boost the performance in active state. However, the only few available reports about the influence of back-bias on the SV in UTBB devices are with limited scope and focus mainly on threshold voltage variability [9], [12], [14].

In this paper, we present a comprehensive simulation study of the impact of back-gate biasing on the SV of 22-nm UTBB SOI MOSFETs. In addition to the back-gate bias dependence in threshold voltage variability, we analyze the variability in drain-induced barrier lowering (DIBL) and in the effective drive current [15], given their paramount importance in the design and optimization of LSTP circuits [13]. The study is performed at two substrate concentrations, in order to establish if a tradeoff is necessary between the level of back-bias control over threshold voltage and current, and the level of SV. Further, we discuss the correlation between the important electrical figures of merit, in view of their importance for the development of statistical compact models and circuit simulations.

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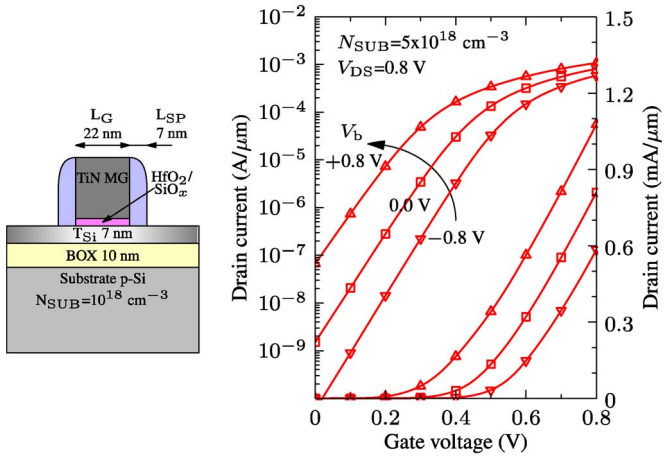

Fig. 1. Schematic and transfer characteristics of the template FD-SOI transistor in saturation, showing more than seven decades on/off ratio achievable with the help of back-bias (V_b) modulation.

II. Methodology

A. Simulations Approach

The study employs the commercial statistical 3-D drift-diffusion simulator Garand, which seamlessly handles all major sources of SV and permits efficient automated simulations of very large statistical ensembles of devices in cluster computing environment [16]. The simulations in this study involve the three principal sources of SV in planar FD-SOI MOSFETs, i.e., RDF, LER, and MGG. Previous studies revealed that atomic scale interface roughness and corresponding statistical body thickness variations play negligible role in FDSOI MOSFETs with dimensions considered in this study [17]–[19]. Since MGG is technology dependent, we present in parallel results with and without MGG throughout our study. The resolution of the individual discrete dopants in the RDF simulations employs fine meshing in conjunction with density gradient quantum corrections. This prevents artificial charge trapping in the sharply resolved Coulomb wells of the ionized dopants and avoids acute mesh-spacing sensitivity [20]. LER is modeled with the assumption that it follows a Gaussian autocorrelation function with three times root-mean-square deviation of the gate edge position of 2.1 nm (approximately 10% of L_G) and a correlation length of 25 nm [21]. The modeling of MGG assumes a TiN gate with two grain orientations differing in workfunction (WF) by 0.2 V, with a probability of 0.4/0.6 for the lower/higher WF, respectively, and an average grain diameter of 5 nm [22].

B. Template Transistor

The statistical ensembles are composed of 1000 microscopically different renditions of a template UTBB FD-SOI n-channel MOSFET, schematically illustrated in Fig. 1, with a 22-nm physical gate length, designed on the basis of the ITRS (2009) guidelines for LSTP applications. The simulations are carried out assuming a supply voltage (V_{DD}) of 0.8 V [23]. The template transistor features (TiN/HfO2/SiO_x) high-k metal gate stack with a SiO_x interfacial layer and an effective oxide thickness of 0.9 nm. The buried oxide (BOX) and Si-body thickness (T_{Si}) are 10 and 7 nm, respectively. The body acceptor doping concentration is 1.2×10^{15} cm^{-3}, while two levels of acceptor doping in the substrate (N_{SUB}) are considered—1.0×10^{18} and 5.0×10^{18} cm^{-3}. Donor concentration in the source and drain extensions is 2.0×10^{20} cm^{-3}, with a 2-nm/dec rolloff under the spacer. Table I summarizes the nominal figures of merit of the template transistor at zero back-gate bias for two substrate concentrations. The saturation threshold voltage Vt_{SAT} reported in Table I is defined as the gate voltage corresponding to a current of 1×10^{-6} A/μm when the drain bias equals V_{DD}.

TABLE I
Electrical Parameters of the Simulated UTBB SOI Device Template at Zero Back-Bias

Parameter	Value	
Substr.Conc. (N_{SUB}), cm^{-3}	1x10^{18}	5x10^{18}
Vt_{SAT}, mV	213	252
SS, mV/dec	88.3	87.9
DIBL, mV/V	106	92
$I_{ON,SAT}$, μA/μm	900	810
I_{OFF}, nA/μm	4.1	1.5

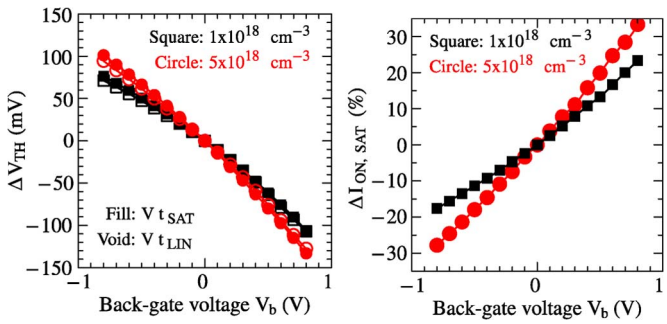

Fig. 2. Back-gate bias (V_b) dependence of (a) ΔVt_{LIN} and ΔVt_{SAT}, and (b) $\Delta I_{ON,SAT}$, showing adequate back-gate control for the nominal device, for both substrate concentrations used (denoted by the symbol shape).

The nominal transfer characteristics of the 22-nm FDSOI transistor with a substrate concentration of 5×10^{18} cm^{-3} in saturation regime at three different back-gate bias conditions are shown in Fig. 1(b). It is clear from the figure that the back-gate is an effective handle to control the power dissipation or to boost the performance. Fig. 2(a) reports the sensitivity of the linear and saturation threshold voltages, i.e., ΔVt_{LIN} and ΔVt_{SAT}, on the back-gate bias. V_T sensitivity of 85 mV/V at $N_{SUB} = 1 \times 10^{18}$ cm^{-3} and of 118 mV/V at $N_{SUB} = 5 \times 10^{18}$ cm^{-3} is observed. Fig. 2(b) reports the back-bias sensitivity of the drive current $\Delta I_{ON,SAT}$, which can be enhanced by 20%–30% with a forward back-gate bias of 0.8 V. Therefore, the data in Fig. 2 show adequate back-gate control and agree well with experimentally observed modulation of 120 mV/V for UTBB devices with a 10-nm BOX [24].

III. Results and Discussion

A. Threshold Voltage Variability

Since there are two widely used definitions of threshold voltage—1) obtained through a constant current criterion, i.e., $Vt_{LIN/SAT}$, and 2) extrapolated from maximum transconductance, i.e., $Vt_{ExL/S}$—it is important to establish which one

TABLE II
NEGATIVE OF THE CORRELATION COEFFICIENT BETWEEN DRAIN CURRENT AND THRESHOLD VOLTAGE. ($N_{SUB} = 1 \times 10^{18}$ cm^{-3})[1]

V_{DS}		$V_b = -V_{DD}$[2]	$V_b = 0$	$V_b = +V_{DD}$
50 mV	I_{OFF}[3], Vt_{ExL}	**0.82/0.89** [4]	**0.87/0.90**	**0.78/0.89**
	I_{ON}, Vt_{LIN}	**0.87/0.85**	**0.82/0.79**	**0.73/0.70**
	I_{ON}, Vt_{ExL}	**0.52/0.77**	**0.51/0.69**	**0.23/0.55**
V_{DD}	I_{OFF}[2], Vt_{ExS}	**0.78/0.86**	**0.66/0.84**	**0.45/0.82**
	I_{ON}, Vt_{SAT}	**0.82/0.93**	**0.76/0.91**	**0.68/0.88**
	I_{ON}, Vt_{ExS}	**0.76/0.85**	**0.65/0.80**	**0.44/0.73**

[1] Correlation I_{OFF}, $Vt_{LIN/SAT}$ ~ 0.98 in all cases and omitted for clarity;
[2] V_{DD}=0.8V; [3] Log(I_{OFF}); [4] without MGG/with MGG.

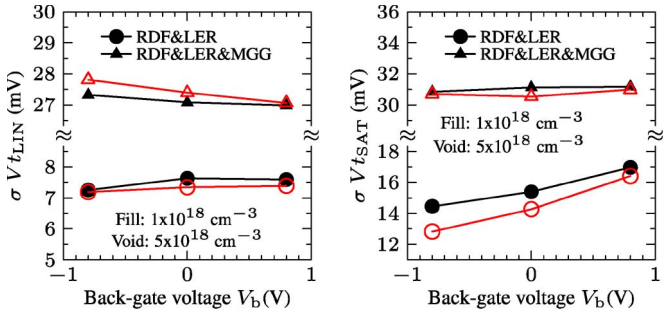

Fig. 3. Variability in the (a) linear and (b) saturation threshold voltage Vt versus back-gate bias (V_b), showing negligible dependence in the linear case, but ~10% modulation of the standard deviation in saturation, if MGG is absent. Fill/void denotes substrate concentration N_{SUB}.

represents a better figure of merit with respect to device variability. Threshold voltage is commonly perceived as an indicator of the magnitude of the ON- and OFF-current in a particular technology. Therefore, a useful definition of the threshold voltage should, from the variability point of view, lead to a higher correlation between threshold voltage and ON/OFF current. Table II reports the correlation coefficients between ON/OFF current and the two definitions of threshold voltage. Several important conclusions stem from the results in Table II. First, the threshold definition based on constant current criterion leads to a higher correlation in all cases. Notably in the linear regime, in the absence of MGG, the correlation between Vt_{ExL} and I_{ON} can be as low as 0.23, whereas Vt_{LIN} and I_{ON} remain well correlated to 0.73. Second, the application of forward/reverse bias appreciably decreases/increases the correlation between threshold voltage and ON/OFF current. Third, the presence of MGG always enhances the correlation between threshold voltage and current, as explained in [10]. Therefore, the constant current criterion offers a more appropriate definition of threshold voltage ($Vt_{LIN/SAT}$), in view of SV, and is used in the rest of the exposition, including the calculation of DIBL.

Fig. 3 shows the back-gate bias dependence of the standard deviation of linear and saturation threshold voltage, with and without MGG, for two levels of substrate doping. It is clear that Vt variability is practically independent of the back-gate bias under linear source–drain bias. The same is true for the variability in the saturation threshold voltage, in the presence of MGG, as shown in Fig. 3(b), due to the dominant character of MGG for planar devices [25], [26]. However, in the absence of MGG, there is a positive back-bias dependence of σVt_{SAT}, leading to more than 10% modulation of the standard

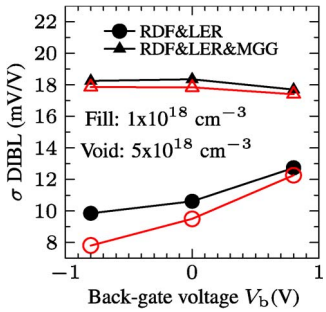

Fig. 4. Back-bias dependence of DIBL variability due to RDF and LER in the presence/absence of MGG, showing strong positive dependence in the absence of MGG. Fill/void denotes substrate concentration N_{SUB}.

deviation. Therefore, in the limiting case of an amorphous metal gate, reverse back-biasing a thin-BOX FDSOI transistor yields the additional advantage of reducing the dispersion of V_T, hence I_{OFF}, and the associated circuit standby leakage power. Fig. 3(b) also shows that a higher substrate concentration tends to suppress the V_T variability while the device transits from linear to saturation region. Both dependence values of σVt (on V_b and on N_{SUB}) are attributed to the reduction in the LER-induced fluctuations, owing to the suppression of SCE and consistent with the DIBL variability discussed next.

B. DIBL Variability

The dependence of the standard deviation of DIBL on the back-gate bias under the influence of RDF and LER, with and without MGG, is plotted in Fig. 4 for two substrate concentrations. In the absence of MGG, σDIBL decreases at negative back-gate bias and high substrate concentration due to the suppressed SCEs but increases with the application of a positive back-bias. This is easily understood if we consider the thin-BOX FDSOI transistor as composed of two single-gated devices in parallel: One is the upper device with good electrostatic integrity, as a result of having a very thin EOT, as defined by the top-gate dielectric, whereas the other is the lower device with bad electrostatic integrity, as a result of having a thick EOT, as defined by the BOX. Under zero or negative back-bias condition, the lower device is well suppressed. However, the relative importance of the lower device increases with the application of positive back-bias, since the peak of the inversion charge centroid shifts away from the top-gate toward the BOX, as shown in Fig. 5, which, in turn, degrades DIBL and makes the device more vulnerable to LER.

The broader dispersion of DIBL under positive back-bias can be a significant issue for power budget control of LSTP circuits, and particularly in SRAM. Moreover, the magnitude of DIBL directly impacts performance through the effective current [13]. Therefore, positive back-bias may increase the absolute magnitude of effective drive current variation.

Fig. 4 also shows that the higher substrate concentration reduces σDIBL, by suppressing the fringing field from the drain to the channel, but increases the corresponding sensitivity.

Finally, in the presence of MGG, σDIBL is doubled. We considered σDIBL in ensembles subjected to the individual influence of RDF, LER, and MGG. The results indicate that the three

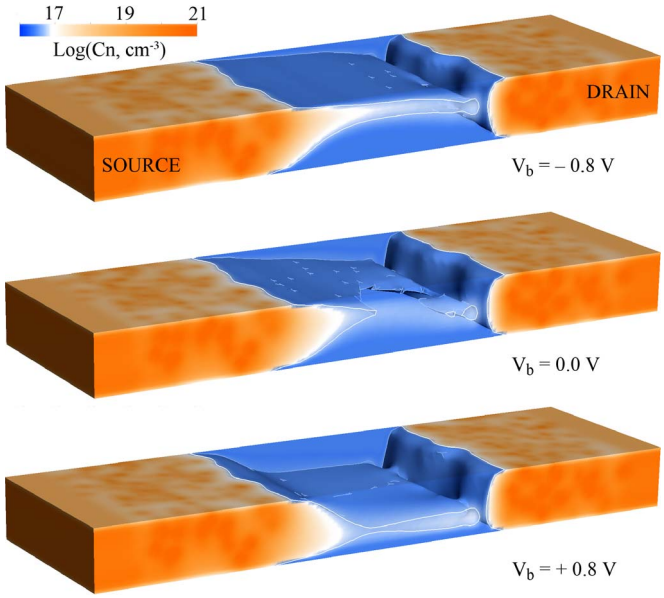

Fig. 5. Impact of back-bias on the current path, illustrated by the electron concentration in the Si-body of a device with RDF and LER, for three back-bias voltages V_b, at $V_{DS} = V_{DD}$, $V_{GS} = Vt_{\rm SAT}$. Gradual transparency below 10^{17} cm^{-3} reveals an iso-concentration surface at 5×10^{16} cm^{-3}, delineating the inversion-charge centroid. Changing V_b from negative to positive shifts the centroid from the top-gate toward the BOX, degrading SCEs and increasing σDIBL.

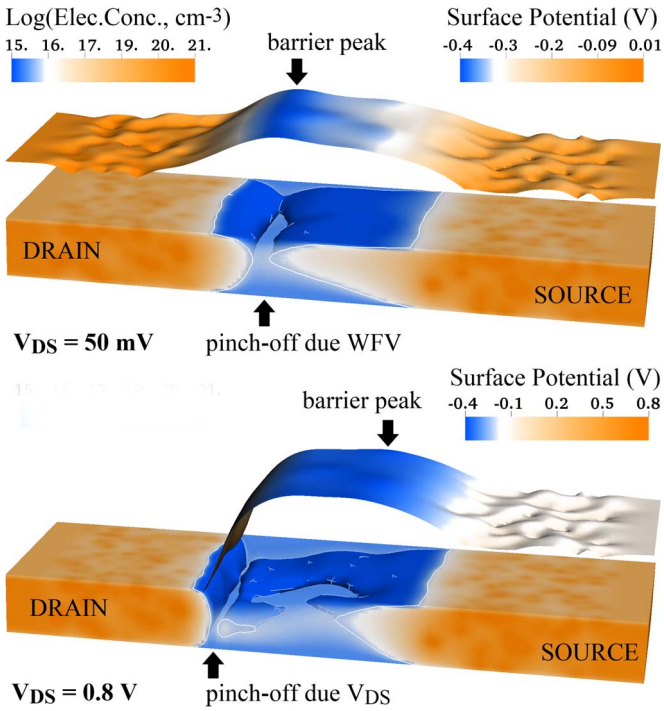

Fig. 6. Surface potential (2-D elevated plot) and electron distribution (3-D plot) with semitransparency revealing an iso-electron surface at 10^{16} cm^3) in the body of a UTBB device subject to RDF, LER, and MGG, at linear and saturation drain–source biases, explaining the pronounced effect of WFV on σDIBL.

sources act in a statistically uncorrelated manner (confirmed by a zero covariance), with MGG being dominant. Further, MGG implicates surface-potential fluctuations, the magnitude of which depends on the ratio between the gate area and the average grain size. This leads to a slightly larger $\sigma Vt_{\rm SAT}$ (31 mV) than $\sigma Vt_{\rm LIN}$ (25 mV), since the channel pinchoff at high drain effectively reduces the area for self-averaging of the potential fluctuations incurred by WF variability (WFV). In turn, there is a slight reduction in the correlation between $Vt_{\rm SAT}$ and $Vt_{\rm LIN}$, i.e., from 0.99 to 0.8, which enhances σDIBL. Fig. 6 provides further insight by comparing the surface potential and the electron distribution in the body of an FDSOI transistor subjected to RDF, LER, and MGG. For the given grain pattern of the metal gate, grains with higher WF appear at the drain side. These grains dictate a high $Vt_{\rm LIN}$ as determined by the peak of the potential barrier, which is nearer to the drain end. Under saturation, however, the peak of the potential barrier is nearer to the source end, where a much lower $Vt_{\rm SAT}$ is dictated by a grain with a smaller WF. The difference in WF of the grains controlling the peak of the potential barrier leads to large DIBL not due to SCE but due to WFV, which increases σDIBL.

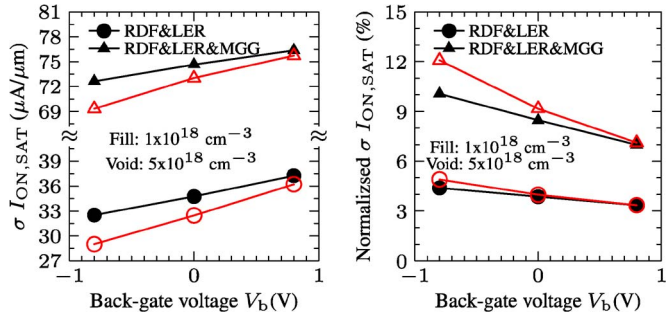

Fig. 7. Back-gate bias dependence of the ON-current variability in saturation: (a) absolute value of the standard deviation, (b) standard deviation normalized to the mean value. Fill/void denotes substrate concentration.

Interestingly, the application of positive back-bias reduces σDIBL in the presence of MGG. This could be understood again in view of the top and bottom gate actions. Since MGG predominantly affects the potential fluctuations at the top interface, the application of positive back-bias reduces its impact by moving the channel closer to the back interface.

C. on-*Current and Effective Current Variability*

The dependence of the standard deviation of the saturation ON-current $\sigma I_{\rm ON,SAT}$ (defined as the drain current when $V_{GS} = V_{DS} = V_{DD}$) on back-gate bias is shown in Fig. 7(a). For both cases, with and without MGG, higher back-gate bias increases the value of $\sigma I_{\rm ON,SAT}$. The underlying cause could not be related to the dependence of $\sigma Vt_{\rm SAT}$ on the back-bias, since, at least in the presence of MGG, $\sigma Vt_{\rm SAT}$ is practically independent of the back-bias (cf. Fig. 3). However, it is known that RDF in the source/drain (SD-RDF) has strong impact on $\sigma I_{\rm ON}$ through fluctuations of the source/drain access resistance σR_{SD} [10], [11], [25]. We attribute the $\sigma I_{\rm ON,SAT}$ dependence on back-gate bias to the RDF-induced fluctuations in the source access resistance, with the following explanation. The drain current in saturation can be expressed as $I_{DS} = \vartheta_S C_{\rm OX} W(V_{GS} - V_T - I_{DS}R_S)$, where ϑ_S is the injection velocity at the source, $C_{\rm OX}$ is the sheet capacitance of the gate oxide, W is the width of the channel, and R_S is the access resistance of the source. The effect of positive/negative back-bias

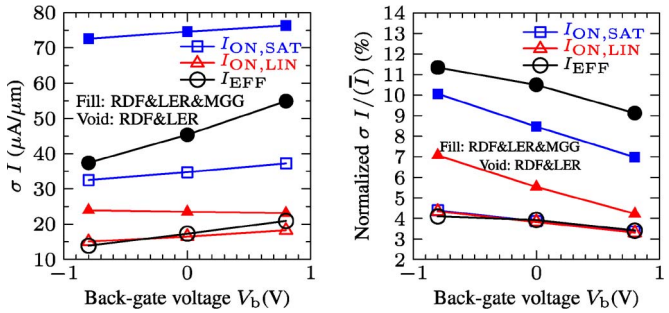

Fig. 8. Comparison of the trends in the variability of $I_{\mathrm{ON,SAT/LIN}}$ and I_{EFF} with the back-gate bias: (a) absolute standard deviation, (b) normalized (by the mean) standard deviation.

is to increase/decrease I_{DS}, hence to amplify/attenuate the fluctuations of the gate overdrive through the $I_{DS}R_S$ term. The relative significance of this term diminishes with the increase in Vt, which can explain the lowering of $\sigma I_{\mathrm{ON,SAT}}$ for higher substrate concentration.

Fig. 7(b) shows back-gate bias dependence of $I_{\mathrm{ON,SAT}}$ variability when normalized by the mean value, i.e., σ/μ. Here, we observe a negative dependence on back-bias, meaning that the mean of the saturation current is more sensitive to the back-gate than the variability in the current. This should be beneficial from circuit application point of view, yielding a lower dispersion in the intrinsic transistor delay at positive back-bias conditions.

Fig. 8 reports the back-gate bias dependence values of the absolute and normalized standard deviations of the linear and saturation ON-current $\sigma I_{\mathrm{ON,LIN/SAT}}$ and effective drive current σI_{EFF}. $I_{\mathrm{ON,LIN}}$ is obtained at 50-mV drain bias. The effective drive current is defined in [15] as $I_{\mathrm{EFF}} = 0.5(I_L + I_H)$, where $I_L = I_{DS}(V_{GS} = 0.5V_{DD}, V_{DS} = V_{DD})$ and $I_H = I_{DS}(V_{GS} = V_{DD}, V_{DS} = 0.5V_{DD})$. It is clear in Fig. 8(a) that σI_{EFF} has the strongest back-gate bias dependence, regardless of the presence of MGG. When normalized by the mean value, I_{EFF} has the largest relative variability in the presence of MGG, $\sim$11% at zero back-bias, slightly decreasing with positive back-bias, as shown in Fig. 8(b). In the case without WFV, there is little difference between the normalized variability of I_{ON} and I_{EFF}, with very weak dependence on back-gate bias. The dependence on substrate concentration is the same as discussed in Fig. 7; hence, we show only results for $N_{\mathrm{SUB}} = 10^{18}$ cm^{-3}.

D. Correlation Between Figures of Merit

Fig. 9 shows the correlation between DIBL and Vt_{SAT} at different back-gate biases in the presence of combined sources of SV. The correlation coefficients are also indicated in the figure. Not surprisingly, for the case without MGG, DIBL and Vt_{SAT} are highly correlated since both of them are mostly influenced by SD-RDF and LER in terms of SCEs. For the case with MGG, their correlation is dramatically reduced since MGG primarily impacts the surface potential and has little influence over SCE at the drain end of the channel under saturation conditions. Fig. 9 has two very important implications. First, the decorrelation between DIBL and Vt_{SAT} in the presence of WFV implies that it may be improper to use DIBL to predict I_{OFF}. Second,

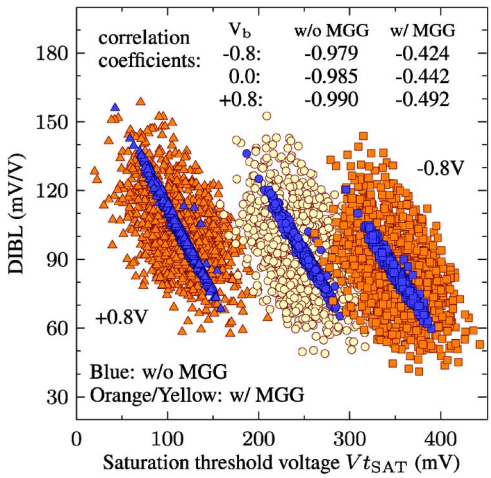

Fig. 9. Back-bias dependence of the correlation between Vt_{SAT} and DIBL due to combined variability sources, with and without MGG.

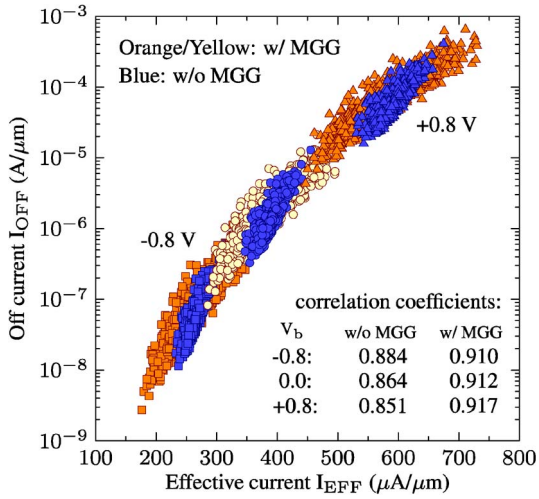

Fig. 10. Dependence of the correlation between effective current and OFF-current (I_{EFF} and I_{OFF}) on back-gate bias, with and without MGG.

the level of correlation between DIBL and Vt_{SAT} may serve as an effective metric for the amount of MGG-induced WFV in a given technology. Note that the correlation coefficients are practically independent of the back-gate bias.

Since DIBL is known to affect the effective current I_{EFF} for high-Vt devices, it is important to note that the scatter plots of DIBL versus I_{EFF} have very similar patterns and trends as illustrated in Fig. 9, although the correlation coefficients are lower in this case (0.85 without MGG and 0.25 with MGG at zero back-bias; plots are not shown for brevity) and somewhat stronger, and opposite back-bias trend exists.

Finally, an important correlation for LSTP applications of thin-BOX FDSOI transistors is the correlation between I_{EFF} and I_{OFF}, shown in Fig. 10. Contrary to the scatter plot of Vt_{SAT} and DIBL, here, there is a stronger correlation in the presence of MGG, which acts as a dominant source of variability for both I_{EFF} and I_{OFF}. For the case without MGG, the correlation is reduced because SD-RDF-induced σR_{SD} acquires a more important role in σI_{EFF}, while $\sigma\mathrm{Log}(I_{\mathrm{OFF}})$ remains determined by σVt_{SAT} (and σSS). The weak dependence of the correlation coefficients is consistent with the trends

in $\sigma I_{\mathrm{ON/EFF}}$, discussed earlier, explained with the growing significance of σR_{SD} as I_{DS} is amplified by a positive back-bias.

IV. Conclusion

The back-gate bias dependence of SV in a 22-nm n-channel thin-BOX FDSOI MOSFETs subject to RDF, LER, and MGG (WFV) is comprehensively studied, including detailed analysis of σV_{TH}, σDIBL, and $\sigma I_{\mathrm{ON/EFF}}$. In the absence of WFV, the application of reverse (negative) back-bias reduces the variability in saturation Vt by more than 10%. However, WFV practically eliminates any dependence of σVt on back-bias, since MGG is a dominant surface source, whereas reverse back-bias improves only SCE and LER sensitivity.

Variability in DIBL and drive current are evaluated under the application of forward (positive) bias on the back-gate. We observe an LER-related increase in σDIBL by more than 20%, in the absence of MGG (WFV). MGG almost doubles σDIBL, as it dominates the fluctuations of Vt_{LIN}, whereas LER has a strong impact on Vt_{SAT}. The competition of MGG and LER reduces the correlation between Vt_{LIN} and Vt_{SAT} and enlarges σDIBL. It is also responsible for the apparent (but weak) reduction in σDIBL when forward bias is applied on the back-gate.

Variability in saturation I_{ON} and I_{EFF} also increases by forward back-biasing the device, which is due to the amplifying of the fluctuations in gate overdrive through the RDF-induced fluctuation in the source access resistance. However, the sensitivity of the current magnitude on back-bias is stronger, and the normalized variability is reduced by over 10% (for I_{EFF} in the presence of MGG), compared with zero back-bias.

Therefore, in view of LSTP application of thin-BOX FDSOI transistors, back-biasing beneficially reduces the dispersion of standby leakage power and of on-demand intrinsic performance, and a higher substrate concentration enhances the above trends.

References

[1] G. Declerck, "A look into the future of nanoelectronics," in *VLSI Tech. Symp.*, 2005, pp. 6–10.

[2] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1837–1852, Sep. 2003.

[3] A. Asenov, "Simulation of Statistical Variability in Nano MOSFETs," in *Proc. IEEE Symp. VLSI Technol.*, 2007, pp. 86–87.

[4] A. Asenov and K. Samsudin, "Variability in nanoscale UTB SOI devices and its impact on circuits and systems," in *Proc. NATO Adv. Res. Workshop Nanoscaled Semicond. Insul. Struct. Devices*, 2007, pp. 259–302.

[5] S. Nassif, K. Bernstein, D. J. Frank, A. Gattiker, W. Haensch, B. L. Ji, E. Nowak, D. Pearson, and N. J. Rohrer, "High performance CMOS variability in the 65nm regime and beyond," in *Proc. IEEE IEDM*, 2007, pp. 569–571.

[6] M. Merrett, P. Asenov, Y. Wang, M. Zwolinski, D. Reid, C. Millar, S. Roy, S. Furber, and A. Asenov, "Modelling circuit performance variations due to statistical variability: MC static timing analysis," in *Proc. DATE*, Grenoble, France, 2011, pp. 1–4.

[7] A. Asenov, S. Roy, R. A. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M. F. Bukhori, X. Wang, and U. Kovac, "Advanced simulation of statistical variability and reliability in nano CMOS transistors," in *Proc. IEEE IEDM*, 2008, p. 1.

[8] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B.-Y. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," in *Proc. IEEE IEDM*, 2008, pp. 1–4.

[9] N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, and S. Kimura, "Local $\mathrm{V_{th}}$ variability and scalability in Silicon-on-Thin-BOX (SOTB) CMOS with small random-dopant fluctuation," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 835–845, Apr. 2010.

[10] S. Markov, B. Cheng, and A. Asenov, "Statistical variability in fully depleted SOI MOSFETs due to random dopant fluctuations in the source and drain extensions," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 315–317, Mar. 2012.

[11] J. Mazurier, O. Weber, F. Andrieu, F. Allain, L. Tosti, L. Brévard, O. Rozeau, M.-A. Jaud, P. Perreau, C. Fenouillet-Beranger, F. A. Khaja, B. Colombeau, G. De Cock, G. Ghibaudo, M. Belleville, O. Faynot, and T. Poiroux, "Drain current variability and MOSFET parameters correlations in planar FDSOI technology," in *Proc. IEEE IEDM*, 2011, pp. 575–578.

[12] Q. Liu, A. Agashita, N. Loubet, A. Khakifirooz, P. Kullarni, T. Yamamoto, K. Cheng, M. Fujiwara, J. Cai, D. Dorman, S. Mehta, P. Khare, K. Yako, Y. Zhu, S. Mignot, S. Kanakasabapathy, S. Monfray, F. Boeuf, C. Koburger, H. Sunamura, S. Ponoth, A. Reznicek, B. Haran, A. Upham, R. Johnson, L. F. Edge, J. Kuss, T. Levin, N. Berliner, E. Leobandung, T. Skotnicki, M. Hane, H. Bu, K. Ishimaru, W. Kleemeier, M. Takayanagi, B. Doris, and R. Sampson, "Ultra-thin-body and box (UTBB) fully depleted device integration for 22nm node and beyond," in *Proc. IEEE Symp. VLSI Technol.*, 2010, pp. 61–62.

[13] T. Skotnicky, "Competitive SoC with UTBB SOI," in *Proc. IEEE SOI Conf.*, Tempe, AZ, Oct. 3–6, 2011, pp. 1–61.

[14] Y. Yang, G. Du, R. Han, and X. Liu, "Simulation study of intrinsic parameter fluctuations in variable-body-factor silicon-on-thin-box metal oxide semiconductor field effect transistors," *Jpn. J. Appl. Phys.*, vol. 50, no. 4, pp. 04DC11-1–04DC11-5, 2011.

[15] M. H. Na, E. J. Nowak, W. Haensch, and J. Cai, "Effective drive current in CMOS inverters," in *Proc. IEEE IEDM*, 2002, pp. 121–124.

[16] Gold Standard Simulations Ltd. [Online]. Available: www.goldstandardsimulations.com/ .

[17] T. B. Hook, M. Vinet, R. Murphy, S. Ponoth, and L. Grenouilet, "Transistor matching and silicon thickness variation in ETSOI technology," in *Proc. IEEE IEDM*, 2011, pp. 115–118.

[18] C. Riddet, A. Brown, C. Alexander, J. Watling, S. Roy, and A. Asenov, "3D Monte Carlo simulation of the impact of quantum confinement scattering on the magnitude of current fluctuations in double gate MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 6, no. 1, pp. 48–55, Jan. 2007.

[19] H. Takeda, K. Takeuchi, and Y. Hayashi, "Scalability study of ultra-thin-body SOI MOSFETs using full-band quantum mechanical based device simulation," in *Proc. IEEE Symp. VLSI Technol.*, 2010, pp. 63–64.

[20] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: A 3-D density-gradient simulation study," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 722–729, Apr. 2001.

[21] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003.

[22] H. Dadgour, De Vivek, and K. Banerjee, "Statistical modeling of metal-gate work-function variability in emerging device technologies and implications for circuit design," in *Proc. IEEE/ACM ICCAD*, 2008, pp. 270–277.

[23] International Technology Roadmap for Semiconductors, 2009. [Online]. Available: http://www.itrs.net/Links/2009ITRS/Home2009.htm

[24] Q. Liu, F. Monsieur, A. Kumar, T. Yamamoto, A. Yagishita, P. Kulkarni, S. Ponoth, N. Loubet, K. Cheng, A. Khakifirooz, B. Haran, M. Vinet, J. Cai, J. Kuss, B. Linder, L. Grenouillet, S. Mehta, P. Khare, N. Berliner, T. Levin, S. Kanakasabapathy, A. Upham, R. Sreenivasan, Y. Le Tiec, N. Posseme, J. Li, J. Demarest, M. Smalley, E. Leobandung, S. Monfray, F. Boeuf, T. Skotnicki, K. Ishimaru, M. Takayanagi, W. Kleemeier, H. Bu, S. Luning, T. Hook, M. Khare, G. Shahidi, B. Doris, and R. Sampson, "Impact of back bias on ultra-thin body and BOX (UTBB) devices," in *Proc. Symp. VLSI Technol.*, 2011, pp. 160–161.

[25] S. Markov, N. M. Idris, and A. Asenov, "Statistical variability in n-channel UTB-FD-SOI MOSFETs under the influence of RDF, LER, MGG and PBTI," in *Proc. IEEE Int. SOI Conf.*, Tempe, AZ, Oct. 3–6, 2011, pp. 1–2.

[26] X. Wang, A. R. Brown, N. Idris, S. Markov, G. Roy, and A. Asenov, "Statistical threshold-voltage variability in scaled decananometer bulk HKMG MOSFETs: A full-scale 3-D simulation scaling study," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2293–2301, Aug. 2011.

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