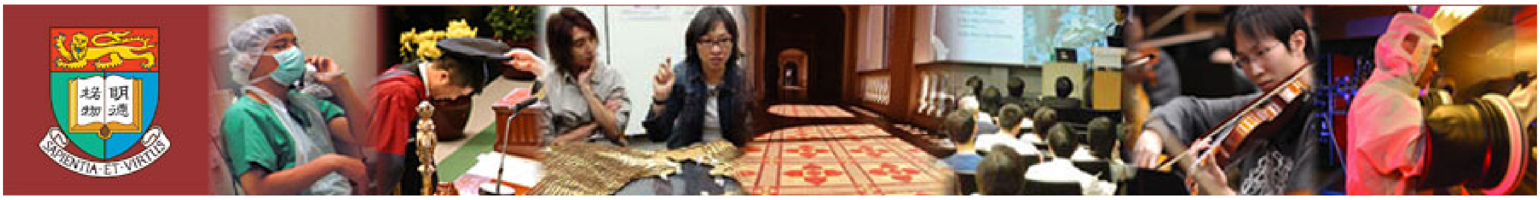

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Author(s)	Chen, MZ
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The Classical n-Port Resistive Synthesis Problem

Michael Z. Q. Chen*

Introduction

An n-port resistive network is an n-port circuit consisting of only passive resistors, which is an important class of passive networks. An n-port resistive network is usually characterized by its *impedance* or *admittance* matrix. Since there are no reactive elements, passivity and reciprocity imply that the impedance and admittance matrices of n-port resistive networks must be nonnegative definite if they exist [21]. Since no transformers are present, there are further constraints. The realizability problem of n-port resistive networks was an active topic and was widely investigated from the 1950s to the 1970s. Recently, the invention of a new mechanical element named inerter [25] has revived research into passive network synthesis. Investigation on n-port resistive network synthesis can be a critical step towards solving transformerless realizations of multi-port passive networks, and its results can be directly applied to minimal realizations of one-port mechanical and electrical networks based on element extraction [11, 12]. Therefore, the significance of this topic has become apparent again.

Problem: What are testable necessary and sufficient conditions for a real symmetric $n \times n$ matrix to be realizable as the admittance (resp. impedance) of an n-port resistive network?

In [24], Tellegen has shown that *paramountcy* is a necessary and sufficient condition for any second-order or third-order real symmetric matrix to be realizable as the impedance (resp. admittance) of a two-port or three-port resistive network. Since Tellegen's proof is in Dutch and there is no English version, [10, Appendix A] presents a full and better structured reworking of Tellegen's discussion.

A question arose whether the condition of paramountcy can be generalized to the case of $n > 3$. Utilizing the graph theory, Cederbaum [8] first showed that if a matrix $Y_n \in \mathbb{S}^n$ (resp. $Z_n \in \mathbb{S}^n$) is the admittance (resp. impedance) of an n-port resistive network, then Y_n (resp. Z_n) must be paramount. In [9], Cederbaum presented a paramount matrix that cannot be realized as either the impedance or the admittance of an n-port resistive network and presented a matrix that is realizable as the impedance but not the admittance of an n-port resistive network. Hence, when $n > 3$, paramountcy is only a necessary but not a sufficient condition for the realization, and realizability conditions of admittances and impedances are not the same.

Investigation on the synthesis of n-port resistive networks when $n > 3$ has primarily focused on the admittance synthesis. For the realizability of admittances as n-port resistive networks, the least number of terminals is $(n + 1)$. Brown *et al.* [5–7, 14] obtained the necessary and sufficient conditions for $Y_n \in \mathbb{S}^n$ to be realizable as admittances of n-port resistive networks with $(n + 1)$ terminals when the port graph $\mathcal{G}_p$ is a *path tree* or a *Lagrangian tree*. Systematic approaches to determine the possible port graphs for realizability are available in [1–4, 14, 16], and the corresponding realizability can be tested by transforming the port graph into a Lagrangian tree based on the discussion in [7]. Unlike the $(n + 1)$-terminal case, the realizability of admittances as n-port resistive networks with more than $(n + 1)$ terminals for $n > 3$ has not

*Department of Mechanical Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong. Email: mzqchen@hku.hk.

been completely solved, although a series of results have been derived [13, 15, 17–20, 22, 23]. Specifically, Chen *et al.* [13] recently derived some new results on the realization problem of n-port resistive networks containing $2n$ terminals, which can be an important step towards solving the realizability with more than $(n+1)$ terminals. However, there are still three challenges in completely solving this problem.

The first challenge of solving this problem is to deal with parameters in realizability conditions with more than $(n+1)$ terminals when $n > 3$. Although some results for the realizability of admittances with $(n+2)$ and $2n$ terminals have been presented in [23] and [13], the conditions are based on the existence of a set of parameters, which are not directly testable. How to eliminate the parameters or to establish a systematic procedure of testing the existence of parameters for $n > 3$ is far from being solved.

The second challenge is the complexity of different cases for the realizability when $n > 3$. The number of possible topological connections becomes increasingly large when n increases. It is difficult to establish a unified framework for the discussion when n is a large number.

The third challenge is the synthesis of impedances when $n > 3$. As shown in [9], the necessary and sufficient conditions for the realizability of impedances and admittances as n-port resistive networks are different when $n > 3$. Therefore, it is necessary to discuss them separately. At present there are few investigations available on realizability of impedances as n-port resistive networks when $n > 3$. It is also difficult to generalize the methodology of investigation on the admittance synthesis to the impedance case.

Conclusion

In summary, the classical n-port resistive synthesis problem is solved in the case of $n \leq 3$, but there exist significant challenges when $n > 3$.

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