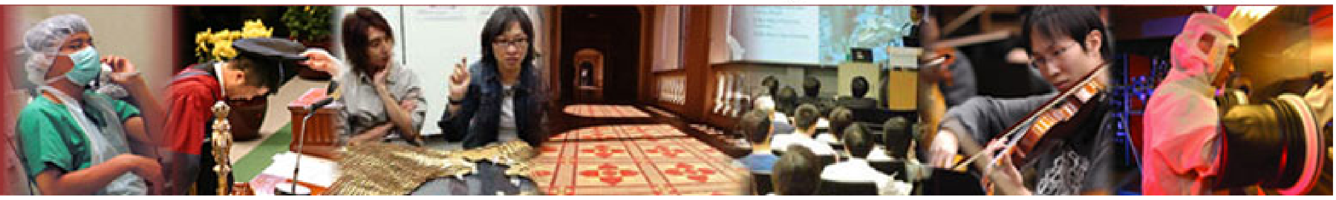

Improved Charge-Trapping Performance of Hf-doped $SrTiO_3$ for Nonvolatile Memory Applications

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The charge-trapping characteristics of Hf-doped $SrTiO_3$ have been studied based on Al/Al_2O_3/Hf-doped $SrTiO_3/SiO_2/Si$ capacitors. The thermodynamic stability of the $SrTiO_3$ film is significantly improved by Hf incorporation, thus resulting in negligible formation of an interlayer at the Hf-doped $SrTiO_3/SiO_2$ interface, as confirmed by X-ray photoelectron spectroscopy and transmission electron microscopy. The memory device with Hf-doped $SrTiO_3$ as charge-trapping layer displays high speed at low operating voltage (a V_{FB} shift of 1.9 V at +6 V, 100 μs) and good data retention (charge loss of 12.7% after 10^4 s). Therefore, the Hf-doped $SrTiO_3$ film is a promising material as charge-trapping layer for high-performance nonvolatile memory applications.

Introduction

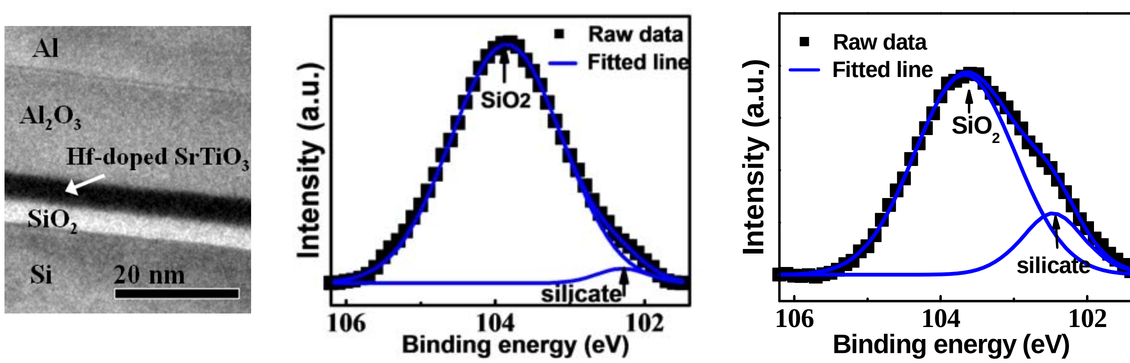
Metal-oxide-nitride-oxide-silicon (MONOS) nonvolatile memories with traps distributed in the dielectrics for charge storage have been considered as a better candidate than their conventional floating-gate counterpart due to their localized charge-storage and coupling-free properties. Intensive researches have been carried out to study high-*k* dielectrics for substituting Si_3N_4 as charge-trapping layer (CTL) mainly due to the stronger scaling ability, lower operating voltage and higher charge-trapping efficiency. In our previous work, $SrTiO_3$ was demonstrated to be a promising CTL for low-voltage MONOS memory applications due to its high-*k* value as well as large band offset with respect to the SiO_2 tunneling oxide (1). However, this memory device with $SrTiO_3$ as CTL displayed severe charge loss mainly due to its poor thermodynamic stability with SiO_2, which resulted in a thick non-stoichiometric interlayer at the $SrTiO_3/SiO_2$ interface. It was also found that this interlayer could be significantly suppressed by inserting HfON between $SrTiO_3$ and SiO_2, leading to better data retention (2). However, the insertion of HfON increases the processing complexity of the memory device. Additionally, the operating speed and operating voltage of the devices mentioned above need to be further improved (1)(2). Therefore, in order to achieve excellent performance for the $SrTiO_3$-based memory device with good retention as well as high speed at low operating voltage, this work aims to investigate the charge-trapping characteristics of Hf-doped $SrTiO_3$ made by co-sputtering technique.

Experiment

MONOS capacitor with an Al/Al_2O_3/Hf-doped $SrTiO_3/SiO_2$/Si structure was fabricated. SiO_2 as tunneling layer (TL) was grown on the p-type Si by thermal oxidation. Then, Hf-doped $SrTiO_3$ film as CTL was prepared by co-sputtering of Hf and $SrTiO_3$ targets in an Ar/O_2 mixed ambient. Following that, Al_2O_3 as blocking layer (BL) was deposited by atomic layer deposition using $Al(CH_3)_3$ and H_2O as precursors at 300 ^oC. Finally Al was evaporated and patterned as gate electrode, followed by forming-gas annealing at 300 ^oC for 20 min. The cross-sectional transmission electron microscopy (TEM) image of the completed MONOS device is shown in Figure 1(a).

Results and Discussion

Figures 1(b) and 1(c) show the Si 2*p* spectrum as well as the curve-fitting lines for Hf-doped $SrTiO_3/SiO_2$ and $SrTiO_3/SiO_2$ on Si substrate by X-ray photoelectron spectroscopy (XPS). Each curve-fitting line is assumed to follow the general shape of Lorentzian–Gaussian function. Both of the Si 2*p* spectra can be decomposed into two components, and correspond to SiO_2 tunneling oxide (103.6 eV) and Ti silicate (102.3 eV) at the CTL/TL interface formed by chemical reaction respectively (3)(4). Note that the area ratio of Si component corresponding to SiO_2 and silicate is 36 for the sample with Hf-doped $SrTiO_3$, which is much larger than that for the sample with pure $SrTiO_3$ (5.0), suggesting a much thinner interlayer at the interface achieved by Hf doping due to the good thermodynamic stability of hafnium oxide contacted with SiO_2 (5). This observation can be further confirmed by the TEM image in Figure 1(a) with no interlayer observed at the CTL/TL interface. Therefore, Hf incorporation can effectively improve the thermodynamic stability of $SrTiO_3$.

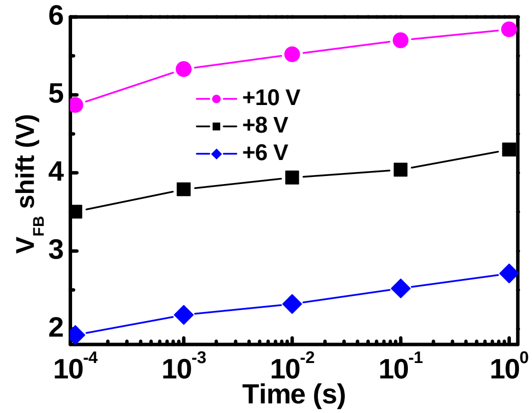


(a) (b) (c)

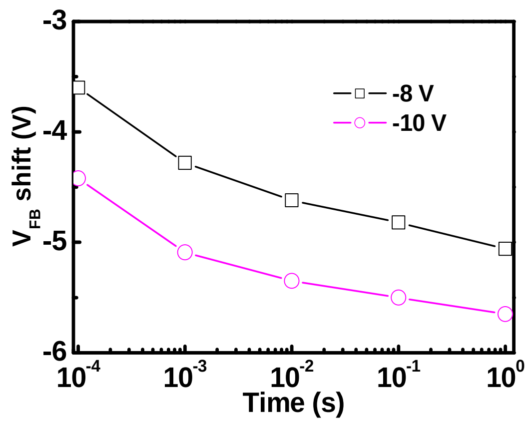
Figure 1. (a) TEM image of the MONOS device, and the thickness of BL/CTL/TL is 15.7 nm/4.3 nm/2.8 nm. (b) Si 2*p* spectrum of the Hf-doped $SrTiO_3/SiO_2$ on the Si substrate. (c) Si 2*p* spectrum of the $SrTiO_3/SiO_2$ on the Si substrate.

Fig. 2 shows the program/erase (P/E) transient characteristics of the MONOS device with Hf-doped $SrTiO_3$ as CTL. As the operating voltage V_G increases from +6 V to +10 V with a pulse width of 1 ms, the V_{FB} shift (ΔV_{FB}) increases from 2.2 V to 5.3 V. The device shows higher ΔV_{FB} (5.3 V at V_G = 10 V, 1 ms) than the device with $SrTiO_3$ (ΔV_{FB}

= 3.2 V at V_G = 10 V, 1 ms) or $SrTiO_3$/HfON (ΔV_{FB} = 2.9 V at V_G = 10 V, 1 ms) as CTL under the same operating conditions, even though the former has a thicker TL (2.8 nm) than the latter (2.0 nm) (2). This should be due to the better interfaces of the dielectric stack and more traps in the CTL induced by Hf incorporation in $SrTiO_3$, thus resulting in higher charge-trapping efficiency for the device with Hf-doped $SrTiO_3$. Moreover, the proposed device presents a high ΔV_{FB} of 1.9 V even at a low V_G of +6 V for 100 µs under program state and a high ΔV_{FB} of 3.6 V at V_G of -8 V for 100 µs under erase state, demonstrating its high P/E speeds with low-voltage operating ability.



(a)



(b)

Figure 2. (a) Program and (b) erase transient characteristics of the memory device with Hf-doped $SrTiO_3$ at various gate voltages.

Figure 3 exhibits the retention characteristics of the device with Hf-doped $SrTiO_3$ as CTL, which shows good data retention with low charge-loss rate (the charge loss rate Q_{loss} after 10^4 s is 12.7%). As shown in the inset of Figure 3, the device with Hf-doped $SrTiO_3$ exhibits similar Q_{loss} as the one with $SrTiO_3$/HfON (Q_{loss} = 12.3 %), and both devices exhibit much better data retention than the one with $SrTiO_3$ (Q_{loss} = 50.2 %) (2). This should be mainly due to the suppressed formation of interlayer at the CTL/TL interface because the interlayer consumes part of the SiO_2 tunneling oxide (thus shortening the leakage path from the CTL to the substrate) and also traps in the non-stoichiometric interlayer usually facilitate charge loss via trap-assisted tunneling.

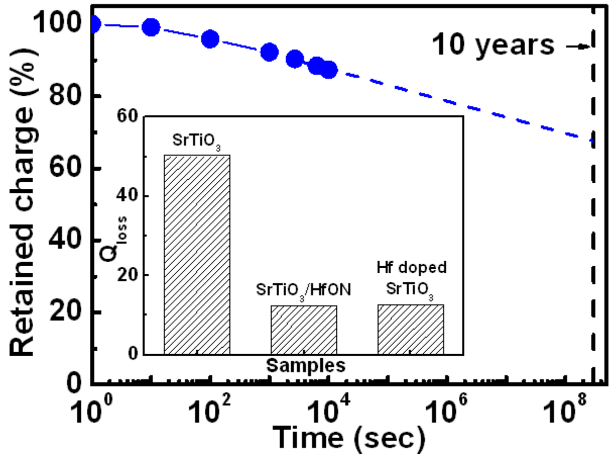


Figure 4. Retention characteristic of the MONOS device with Hf-doped $SrTiO_3$ as CTL measured at room temperature. The inset shows the Q_{loss} of the $SrTiO_3$-based devices.

Conclusion

The charge-trapping characteristics of Hf-doped $SrTiO_3$ have been studied. The thermodynamic stability of the $SrTiO_3$ film can be improved by Hf incorporation. The memory device with Hf-doped $SrTiO_3$ as CTL displays high P/E speeds at low operating voltage and good data retention. Therefore, the Hf-doped $SrTiO_3$ film is a promising material as CTL for MONOS-type memory applications.

Acknowledgments

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