

<b>Title</b>	<b>Plasma-nitrided Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>) as interfacial passivation layer for InGaAs metal-oxide-semiconductor capacitor with HfTiON gate dielectric</b>
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# Plasma-Nitrided $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ as Interfacial Passivation Layer for InGaAs Metal–Oxide–Semiconductor Capacitor With HfTiON Gate Dielectric

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**Abstract**—Plasma nitridation is used for nitrogen incorporation in  $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$  (GGO) as interfacial passivation layer for an InGaAs metal–oxide–semiconductor capacitor with a HfTiON gate dielectric. The nitrided GGO (GGON) on InGaAs can improve the interface quality with a low interface-state density at midgap ( $1.0 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ ), and result in good electrical properties for the device, e.g., low gate leakage current ( $8.5 \times 10^{-6} \text{ A/cm}^2$  at  $V_g = 1 \text{ V}$ ), small capacitance equivalent thickness (1.60 nm), and large equivalent dielectric constant (24.9). The mechanisms involved lie in the fact that the GGON interlayer can effectively suppress the formation of the interfacial In/Ga/As oxides and remove excess As atoms on the InGaAs surface, thus unpinning the Fermi level at the GGON/InGaAs interface and improving the interface quality and electrical properties of the device.

**Index Terms**—HfTiON gate-dielectric, InGaAs metal–oxide–semiconductor (MOS), interface-state, nitrided  $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$  (GGON) interlayer, plasma-nitridation.

## I. INTRODUCTION

RECENTLY, InGaAs MOSFETs with high- $k$  gate dielectric have attracted increasing attention for next-generation low-power and high-speed nanoscale CMOS device applications due to their higher carrier mobility and larger drive current than those of conventional Si devices [1], [2]. Among the high- $k$  materials, Hf-based oxide/silicate/aluminate

have received more attention [3], but their moderate dielectric constant limits further device scaling. Ti-incorporated Hf oxide (HfTiO) can achieve higher  $k$  value [4], and furthermore, nitrogen incorporated in HfTiO can further increase its  $k$  value and reduce its oxide charges and border traps [5]. Therefore, HfTiON is a promising high- $k$  material for InGaAs MOS devices. However, compared with the  $\text{SiO}_2/\text{Si}$  system, the key challenge for InGaAs MOSFETs is the lack of a high-quality and thermodynamically stable insulator that can passivate the interface defects. To improve the interface quality, various surface passivation techniques have been extensively studied, including surface sulfur passivation [6], surface plasma passivation [7]–[9], and Si [10] or Ge [11] as an interfacial passivation layer (IPL). However, Si or Ge can alter the doping concentration or even induce a counter doping in the InGaAs substrate because they are amphoteric dopants for InGaAs [12].  $\text{SiO}_x\text{N}_y$  as an IPL also provides excellent interface quality for InGaAs MOS devices [13], but its  $k$  value is very low ( $\sim 5.5$ ).  $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$  (GGO) has a moderate dielectric constant ( $k = 14\text{--}16$ ), and GGO as a gate dielectric on InGaAs has been proved to unpin the surface Fermi level effectively [14]. However, upon air exposure, GGO has been found to degrade in electrical performance due to moisture absorption [15]. Covering the GGO dielectric film with a high- $k$  dielectric, e.g., HfTiON, not only can effectively protect the GGO from moisture absorption during subsequent processing, but also can increase the  $k$  value of the gate dielectric. Therefore, GGO with a not-so-high dielectric constant is more suitable as an IPL on InGaAs. In addition, it has been demonstrated that incorporation of nitrogen in the IPL on GaAs prevented excessive low- $k$  interfacial layer growth due to the oxidation of GaAs and thus improved the interface quality [16]. Plasma nitridation as one of the nitridation techniques has been shown to be an effective method to improve the thermal and electrical properties of high- $k$  dielectrics on Si and GaAs [17], [18]. However, plasma nitridation of GGO film on InGaAs has not been reported yet. In this paper, to effectively passivate the InGaAs surface,  $\text{NH}_3$ -plasma nitrided GGO (GGON) is adopted as an IPL to improve the interface quality of the InGaAs MOS device, and high- $k$  HfTiON is used as the gate dielectric to increase

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the  $k$  value and also protect the GGO IPL against moisture. As a result, excellent electrical properties have been achieved with small gate leakage current and low interface-state density compared with its counterparts without plasma nitridation and IPL, respectively.

## II. EXPERIMENT

InGaAs MOS capacitors were fabricated on Si-doped  $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}/n^+\text{-InP}$  substrate with a doping concentration of  $2.3 \times 10^{16} \text{ cm}^{-3}$  for  $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ . The wafers were degreased using acetone, ethanol, and isopropanol, and cleaned in diluted HF solution (5%) for 2 min to remove the native oxide, followed by dipping in  $(\text{NH}_4)_2\text{S}$  solution (8%) for 20 min at room temperature for sulfur passivation of the InGaAs surface and then dried by  $\text{N}_2$ . Subsequently, a thin GGO layer of  $\sim 2 \text{ nm}$  was deposited on the InGaAs surface as the IPL by cosputtering of  $\text{Ga}_2\text{O}_3$  and Gd targets in an  $\text{Ar}/\text{O}_2$  (15/3 sccm) ambient. Then some of the wafers were subjected to  $\text{NH}_3$ -plasma nitridation for 5 min at  $300^\circ\text{C}$  in a plasma-enhanced chemical vapor deposition chamber to transform GGO into GGON. Next, an 8-nm HfTiN gate dielectric was deposited on the GGO or GGON by cosputtering of Hf and Ti targets in an  $\text{Ar}/\text{N}_2$  (15/6 sccm) ambient (denoted by GGO and GGON, respectively). For comparison, a control sample with only HfTiN ( $\sim 10 \text{ nm}$ ) as the gate dielectric was also prepared. All the three samples received a postdeposition annealing at  $600^\circ\text{C}$  for 60 s in  $\text{N}_2$  (500 sccm) +  $\text{O}_2$  (50 sccm) to transform HfTiN into HfTiON. Finally, Al was thermally evaporated and patterned as gate electrode and also as back electrode, followed by  $\text{N}_2$  annealing at  $300^\circ\text{C}$  for 20 min to reduce their contact resistance.

High-frequency (HF, 1-MHz) capacitance–voltage ( $C$ – $V$ ) and gate leakage current density versus gate voltage ( $J_g$ – $V_g$ ) curves of the samples were measured using an HP4284A precision LCR meter and an HP4156A semiconductor parameter analyzer, respectively. The physical thickness of the gate dielectric was measured by an ellipsometer. X-ray photoelectron spectroscopy (XPS) was used to examine the chemical states at/near the high- $k$ /InGaAs interface. All electrical measurements were carried out under light-tight and electrically shielded condition at room temperature.

## III. RESULTS AND DISCUSSION

Fig. 1 shows the HF (1-MHz)  $C$ – $V$  curves of all the samples. Obviously, the control sample without an IPL exhibits poor  $C$ – $V$  behavior with the largest stretch out along the voltage axis, indicating high interface-trap density caused by a considerable amount of In–O, Ga–O, As–O, and As–As bonds at the HfTiON/InGaAs interface [6], [19], [20]. However, the stretch out is diminished for the GGO sample, and even disappears for the GGON sample with  $\text{NH}_3$ -plasma nitridation, which should be ascribed to the formation of N-related strong bonds at/near the GGON/InGaAs interface and the blocking role of GGON against oxygen diffusion from HfTiON to the surface of the InGaAs substrate. From Fig. 1, it can also be seen that the accumulation capacitance is larger for the samples with an IPL than the sample without an IPL,

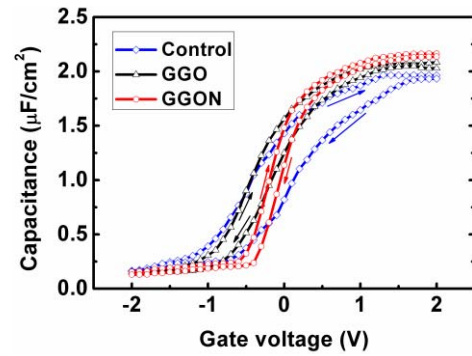


Fig. 1. HF (1-MHz)  $C$ – $V$  curve for the GGON, GGO, and control samples.

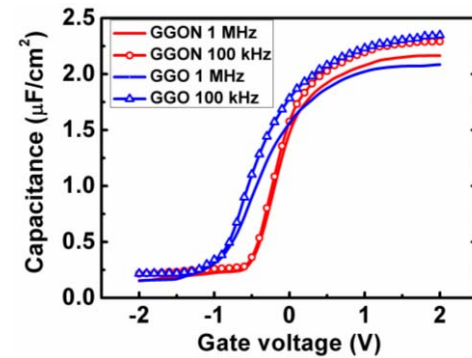


Fig. 2. Frequency dispersion of  $C$ – $V$  curve for the GGON and GGO samples, measured at 1 MHz and 100 kHz.

although the physical thicknesses of their gate dielectrics are approximately equal. This indicates that a low- $k$  interfacial layer (In/Ga/As oxides) is probably grown on the InGaAs surface of the latter without the protection of the IPL. The larger accumulation capacitance for the GGON sample than for the GGO sample is associated with the higher  $k$  value of the gate dielectric in the former due to the incorporation of nitrogen in GGO. Moreover, the GGON sample exhibits the sharpest transition from depletion to accumulation, implying best interface quality. In addition, as shown in Fig. 1, while the hysteresis voltage of the  $C$ – $V$  curve is 540 mV for the control sample and 250 mV for the GGO sample, the smallest hysteresis voltage (150 mV) is obtained for the GGON sample, implying fewest slow states in the HfTiON/GGON stack dielectric and near/at the GGON/InGaAs interface due to the reductions of oxygen defects and In/As out-diffusions induced by the  $\text{NH}_3$ -plasma GGON IPL [21]. Fig. 2 shows the  $C$ – $V$  curves of the GGON and GGO samples measured at 1 MHz and 100 kHz. The frequency dispersion, defined as the percentage of accumulation–capacitance change, is calculated from  $(C_{100 \text{ kHz}} - C_{1 \text{ MHz}})/C_{1 \text{ MHz}}$  at a gate voltage of 2 V. Obviously, the GGON sample exhibits smaller frequency dispersion (5.9%) than the GGO sample (12.7%), indicating less slow states at/near the oxide/InGaAs interface. These indicate that using  $\text{NH}_3$ -plasma GGON as an IPL is an effective way to reduce defective states and unpin the Femi level at the GGON/InGaAs interface.

TABLE I  
PARAMETERS OF THE InGaAs MOS CAPACITORS  
EXTRACTED FROM HF  $C-V$  CURVES

Sample	$V_{fb}$ (V)	$T_{ox}$ (nm)	$Q_{ox}$ ( $\text{cm}^{-2}$ )	$D_{it}$ ( $\text{cm}^{-2}\text{eV}^{-1}$ )	$CET$ (nm)	$K$
GGON	-0.48	10.2	$2.4 \times 10^{12}$	$1.0 \times 10^{12}$	1.60	24.9
GGO	-0.91	10.5	$7.9 \times 10^{12}$	$3.0 \times 10^{12}$	1.66	24.6
Control	-1.09	10.6	$9.6 \times 10^{12}$	$7.5 \times 10^{12}$	1.76	23.5

The capacitance equivalent thickness (CET) and equivalent  $k$  value of the samples can be calculated as  $CET = \epsilon_0 \times k_{\text{SiO}_2} \times A / C_{\text{ox}}$  ( $\epsilon_0$  and  $k_{\text{SiO}_2}$  are the permittivity of free space and dielectric constant of  $\text{SiO}_2$ , respectively;  $A$  is the area of gate electrode;  $C_{\text{ox}}$  is the accumulation capacitance) and  $k = C_{\text{ox}} \times T_{\text{ox}} / (\epsilon_0 \times A)$  ( $T_{\text{ox}}$  is the physical thickness of the gate dielectric determined by multiwavelength ellipsometry), respectively, as listed in Table I. The smallest CET of 1.60 nm and the largest  $k$  value of 24.9 are achieved for the GGON sample, which can be attributed to the fact that the GGON interlayer can effectively suppress the formation of low- $k$  interfacial oxide at the InGaAs surface.

The flatband voltage ( $V_{fb}$ ), equivalent oxide-charge density ( $Q_{ox}$ ) and interface-state density at midgap ( $D_{it}$ ) of the samples are also listed in Table I.  $D_{it}$  ( $=C_{it}/q$ ) is estimated from the 1-MHz  $C-V$  curve by Terman's method [22] based on the formulas:  $C_{it} = C_{\text{ox}}[(d\Psi_s/dV_g)^{-1} - 1] - C_s$ ,  $\Psi_s = \epsilon_s q N / (2C_s^2)$  and  $1/C_s = 1/C - 1/C_{\text{ox}}$  [23], where  $C_{it}$  is the interface-state capacitance;  $q$  is the electron charge;  $\Psi_s$  is the surface potential;  $V_g$  is the gate voltage;  $C$  is total MOS capacitance;  $C_s$  is the depletion-layer capacitance of semiconductor surface;  $\epsilon_s$  and  $N$  are the relative dielectric constant and doping concentration of the substrate, respectively.  $Q_{ox}$  is calculated as  $-C_{\text{ox}} \times (V_{fb} - \phi_{ms}) / q$ , where  $\phi_{ms}$  is the work-function difference between the Al gate and InGaAs substrate. For the three samples, a negative shift of  $V_{fb}$  is observed, implying the presence of positive oxide charges in the dielectric film which should be due to donor-like interface and near-interface traps associated with In/Ga/As diffusions from the substrate to the interlayer and high- $k$  layer [24]. Smaller negative shift of  $V_{fb}$  for the GGON sample (0.48 V) than for the GGO sample (0.91 V) should be attributed to the fact that nitrogen incorporated in the GGO IPL by  $\text{NH}_3$ -plasma nitridation can effectively occupy its oxygen vacancies, resulting in a reduction of defect traps in the GGON IPL and near the GGON/InGaAs interface [17], [25], which is also the main reason why the  $Q_{ox}$  of the GGON sample ( $2.4 \times 10^{12} \text{ cm}^{-2}$ ) is smaller than that of the GGO sample ( $7.9 \times 10^{12} \text{ cm}^{-2}$ ). Moreover, the two samples with an IPL exhibit smaller  $D_{it}$  than their counterpart without an IPL, with the smallest for the GGON sample ( $1.0 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ ) due to the passivation role of H and N atoms dissociated from the  $\text{NH}_3$ -plasma on the dangling bonds near/at the interface [26], [27]. This further indicates that the  $\text{NH}_3$ -plasma GGON as an IPL on the sulfur-passivated InGaAs surface can effectively remove the In/Ga/As oxides, excess As atoms, and relevant defective bonds at/near the GGON/InGaAs interface (as confirmed by the XPS analysis below), thus reducing the defects at/near the interface.

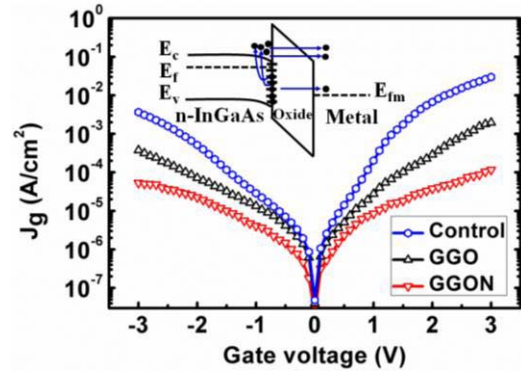


Fig. 3. Gate-leakage current density ( $J_g$ ) versus gate voltage ( $V_g$ ) for the GGON, GGO, and control samples. Inset: schematic of interface-trap-assisted tunneling under positive gate voltage.

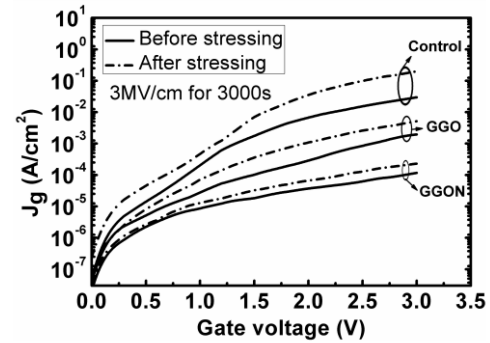


Fig. 4. Gate-leakage current density ( $J_g$ ) of the three samples before and after a high-field stress at 3 MV/cm for 3000 s.

Fig. 3 shows the gate leakage properties of the samples. Large gate leakage current density is observed when positive gate voltage is applied on the sample without an IPL, e.g.,  $2.0 \times 10^{-4} \text{ A/cm}^2$  at  $V_g = 1 \text{ V}$ . This is likely attributed to interface-trap-assisted tunneling caused by a high density of interface states at the HfTiON/InGaAs interface, i.e., most of the trapped electrons are first emitted to the conduction band of InGaAs from the interface traps and then tunnel to the gate electrode, and simultaneously some of the trapped electrons tunnel from the interface traps directly to the gate electrode [28], [29], [30], as shown in the inset of Fig. 3. In addition, the interfacial In/Ga/As-oxide-induced lowering of the conduction-band offset between HfTiON and InGaAs is another possible reason [31]. However, the leakage current density is greatly reduced for the GGO and GGON samples, e.g.,  $2.8 \times 10^{-5} \text{ A/cm}^2$  and  $8.5 \times 10^{-6} \text{ A/cm}^2$  at  $V_g = 1 \text{ V}$ , respectively. The smallest gate leakage current of the GGON sample is closely related to its smallest  $Q_{ox}$  and  $D_{it}$ . To examine the reliability of the samples, a high-field stress at 3 MV/cm [ $=(V_g - V_{fb})/T_{ox}$ ] for 3000 s is performed. The  $J_g-V_g$  properties before and after the stressing are shown in Fig. 4. To analyze the mechanisms involved, the increase in equivalent oxide-charge density ( $\Delta Q_{ox}$ ) extracted from the 1-MHz  $C-V$  curve before and after the stress and the increase in interface-state density at midgap ( $\Delta D_{it}$ ) estimated by the Terman's method are listed in Table II. On one hand,

TABLE II  
 $\Delta Q_{ox}$  AND  $\Delta D_{it}$  OF THE SAMPLES AFTER A HIGH-FIELD  
 STRESS (AT 3 MV/cm FOR 3000 s)

Sample	GGON	GGO	Control
$\Delta Q_{ox} (\times 10^{12} \text{ cm}^{-2})$	1.1	1.9	4.4
$\Delta D_{it} (\times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1})$	0.9	1.6	3.5

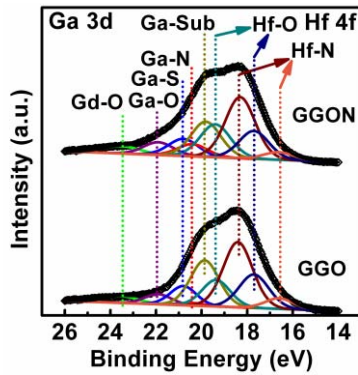


Fig. 5. Ga 3d and Hf 4f XPS spectra of the GGON and GGO samples.

the increased gate leakage current after the stress could come from carrier charging at the original traps of the oxide layer, as confirmed by the  $Q_{ox}$  increase after the stress, and on the other hand, could come from newly created interface and near-interface traps, as proved by the  $D_{it}$  increase after the stress. From Fig. 4, it can be clearly seen that the poststress increase in the leakage current is smallest for the GGON sample, which can be associated with fewer original traps in the GGON interlayer due to: 1) reduction of its oxygen vacancies by nitrogen occupation and 2) less stress-induced generation of interface and near-interface traps as a result of reduction of weak In-/Ga-/As-O bonds and formation of N-related strong bonds at/near the GGON/InGaAs interface during the  $\text{NH}_3$ -plasma nitridation [32].

To determine the chemical composition of the dielectric films and further clarify the mechanisms of the improved GGON/InGaAs interface due to the  $\text{NH}_3$ -plasma nitridation, the HfTiON layer is thinned by an *in situ*  $\text{Ar}^+$  ion beam etching in the XPS chamber, so that the chemical states near/at the high- $k$ /InGaAs interface can be analyzed. As can be seen in Fig. 5 for Ga 3d and Hf 4f XPS spectra of the two samples with an IPL, the two peaks at 17.7 and 19.4 eV are originated from the Hf 4f<sub>7/2</sub> and Hf 4f<sub>5/2</sub> of the Hf-O bonds, respectively. The peaks located at 16.6 and 18.3 eV should be due to Hf-N bonds [33]. In the As 3d, Ti 3p<sub>3/2</sub>, and Hf 5p<sub>3/2</sub> XPS spectra of Fig. 6, the two peaks at 37.4 and 33.8 eV are from the Ti-O and Hf-O bonds, corresponding to Ti 3p<sub>3/2</sub> and Hf 5p<sub>3/2</sub>, respectively. The presence of oxygen can be confirmed by the O 1s spectrum in Fig. 7(a). Also, an N 1s peak is detected, as shown in Fig. 7(b), thus confirming the formation of the HfTiON dielectric. In Fig. 5, the peak at 23.5 eV is attributed to Gd-O bonds, while the two peaks located at 21.9 and 20.4 eV come from the Ga-O and Ga-N bonds respectively. In Fig. 7(b), the Gd-N peak at 394.6 eV can be observed for the GGON sample, while no Gd-N peak

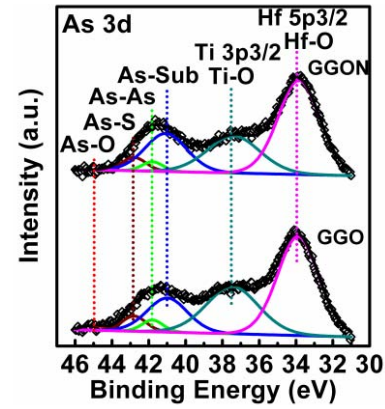


Fig. 6. As 3d, Ti 3p<sub>3/2</sub> and Hf 5p<sub>3/2</sub> XPS spectra of the GGON and GGO samples.

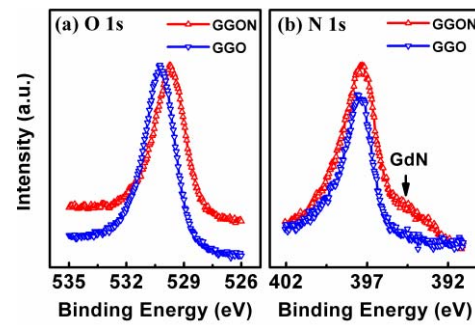


Fig. 7. (a) O 1s and (b) N 1s XPS spectra of the GGON and GGO samples.

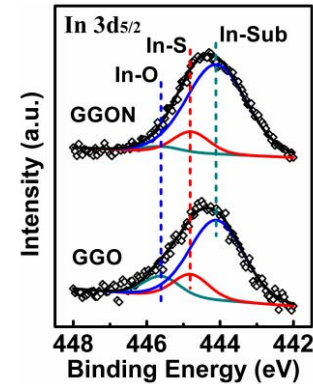


Fig. 8. In 3d<sub>5/2</sub> XPS spectra of the GGON and GGO samples.

appears for the GGO sample. These indicate that a plasma-GGON IPL for the GGON sample has been formed on the surface of the InGaAs substrate.

In Figs. 5, 6, and 8, Ga-S, As-S, and In-S peaks are observed in the Ga 3d, As 3d, and In 3d spectra of the GGON and GGO samples. It is well known that sulfur passivation is beneficial to reducing the formation of In/Ga/As-O bonds on the InGaAs substrate [6], [13], but cannot fully eliminate them. In Fig. 6, As-O bonding only occurs in the GGO sample (its content is 4.9% from the As-O/As<sub>3d</sub> peak-area ratio) but disappears in the GGON sample. Furthermore, as shown in Fig. 8, the intensity of the In-O peak for the GGON sample (a content of 2.8% from the In-O/In3d<sub>5/2</sub> peak-area ratio) is obviously lower than that

for the GGO sample (11.9%). Similarly, from Fig. 7(b), it is also found that the O 1s peak is smaller for the former than the latter. These imply that the GGON IPL can effectively block the diffusion of oxygen to the surface of the InGaAs substrate and protect the surface from oxidation. In addition, it can also be seen in Fig. 6 that the intensity of the As–As peak is lower for the GGON sample (a content of 9.4% from the As–As/As<sub>3d</sub> peak-area ratio) than for the GGO sample (11.8%), which can be attributed to the fact that the reactive species, such as H atoms and NH radicals dissociated from NH<sub>3</sub>, can partially remove the elemental As during the plasma nitridation [34]. All of these indicate that the plasma-GGON as an IPL on sulfur-passivated InGaAs can effectively reduce the formation of weak In/Ga/As–O and As–As bonds, and thus suppress the growth of a low-*k* interfacial layer at the InGaAs surface. This not only leads to large equivalent *k* value and thus large accumulation capacitance, but also effectively reduces the defective states caused by a considerable amount of interfacial In/Ga/As–O bonds and excess As atoms, thus unpinning the Femi level of the InGaAs surface and greatly improving the electrical properties of the devices, as mentioned above.

In addition, the content of Ga–N bond for the GGON sample in Fig. 5 is calculated to be 15.7% based on the Ga–N/Ga<sub>3d</sub> peak-area ratio, which is obviously higher than that of the GGO sample (3.2%). From Fig. 7(b), the intensity of the N 1s peak can also be found to be higher for the GGON sample than the GGO sample. Furthermore, as shown in Fig. 7(a), compared with the GGO sample, the O 1s peak of the GGON sample shifts to lower binding energy by ~0.5 eV mainly due to nitrogen incorporation in the plasma-GGON interlayer. Nitrogen atoms can fill up the oxygen vacancies in the oxynitride [27], resulting in a reduction of defect traps at/near the interface and thus smaller flatband-voltage shift, smaller frequency dispersion, and smaller gate leakage current, as shown in Figs. 1–4.

#### IV. CONCLUSION

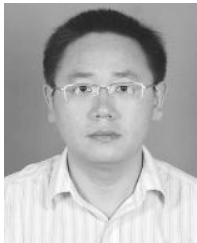
In summary, the effectiveness of NH<sub>3</sub>-plasma GGON as an IPL in improving the quality of the high-*k*/InGaAs interface has been investigated. XPS results show that the plasma-GGON IPL can effectively suppress the formation of the interfacial In/Ga/As oxides and remove excess As atoms at the InGaAs surface due to the incorporation of nitrogen in the interlayer, thus greatly reducing the relevant defects and suppressing the pinning of Femi level at the GGON/InGaAs interface. The improved interface quality with low interface-state and oxide-charge densities, small hysteresis, and low leakage current make the plasma-GGON a promising IPL candidate for InGaAs-based CMOS devices with high-*k* gate dielectric.

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