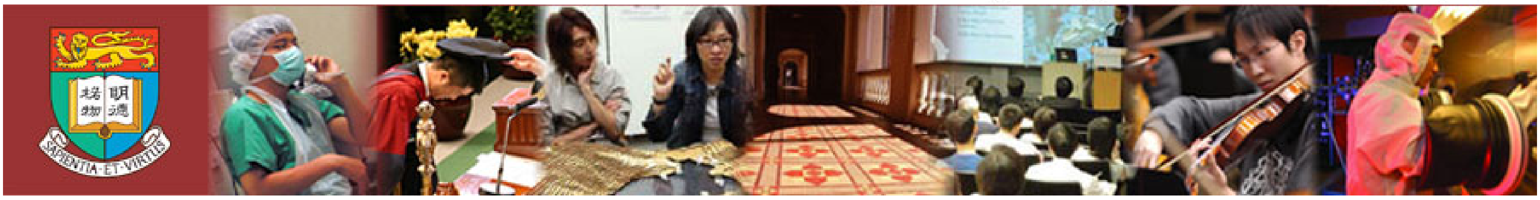

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Improved Performance of Amorphous InGaZnO Thin-Film Transistor With Ta_2O_5 Gate Dielectric by Using La Incorporation

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***Abstract*—In this paper, a comparative study of amorphous InGaZnO thin-film transistors with Ta_2O_5 and TaLaO gate dielectrics has been conducted. It is found that the electrical characteristics of thin-film transistors, including saturation carrier mobility, subthreshold swing, hysteresis, and on-off current ratio, can be effectively improved by the incorporation of La in Ta_2O_5 gate dielectric, which is ascribed to the fact that La incorporation can enlarge the bandgap of Ta oxide and its conduction-band offset with InGaZnO and also reduce the trap densities in the gate dielectric and at the InGaZnO/gate-dielectric interface. As a result, the sample with higher La concentration in the gate dielectric presents superior electrical characteristics, e.g., a high carrier mobility of 30.9 $cm^2/V \cdot s$, a small subthreshold swing of 0.17 V/dec, and slight hysteresis. Moreover, low-frequency noise measurement and X-ray photoelectron spectrum further support that the improvements in electrical properties are due to reduced trap densities induced by the incorporation of La in the Ta_2O_5 gate dielectric.**

***Index Terms*—Amorphous InGaZnO (a-IGZO), thin-film transistor (TFT), Ta_2O_5, TaLaO, high-k, carrier mobility, subthreshold swing.**

I. INTRODUCTION

DURING the past few years, ZnO has attracted much attention as a channel material of thin-film transistors (TFTs) for the application in the field of flat-panel displays (FPDs) due to its superior properties including wide direct bandgap, high carrier mobility and transparency in the visible range [1], [2]. Nevertheless, it is very difficult to form amorphous or single-crystalline ZnO thin films, and in general a polycrystalline structure is obtained, resulting in grain-boundary defects. Accordingly, the uniformity of device performance at different locations across a single FPD can be deteriorated. In addition, the poor chemical durability of pure ZnO against acidic etchants is another drawback of this material, increasing the difficulty in fabrication [2]. Aiming to solve these problems, amorphous InGaZnO (a-IGZO) has been developed to replace ZnO as the channel material in TFTs [3], [4].

Recently, various high-k materials have been adopted as the gate dielectrics of a-IGZO TFTs in order to reduce their operating voltage. Among them, Ta_2O_5 has been regarded as one of the most promising candidates due to its high dielectric constant, large refractive index and excellent step coverage [5]. However, due to narrow band gap (E_G, $\sim$4.4 eV) and correspondingly small conduction-band offset (ΔE_C, $\sim$1 eV on ZnO-based material), Ta_2O_5 gate dielectric has a small electron barrier height, which can induce large leakage current in Metal-Oxide-Semiconductor (MOS) devices [6], [7]. In addition, even though an equilibrium phase of Ta_2O_5 without metastable phases can be obtained, a complicated structure of Ta_2O_5 mixed with distorted TaO_6 octahedral and distorted TaO_7 pentagonal bi-pyramids still can yield many types of oxygen vacancies, resulting in a high density of defect states in the band gap [8]. Such defects in Ta_2O_5 gate dielectric can act as traps to increase the gate leakage current and thus degrade the electrical properties of MOS devices [9], [10].

It was reported that high-k La_2O_3 offers large values of E_G ($\sim$6 eV) and ΔE_C ($\sim$3.1 eV on ZnO-based material), and thus has low leakage current as an insulator [11], [12]. In addition, it was reported the La incorporation could suppress the formation of oxygen vacancies in high-k dielectrics [13]. Accordingly, the effects of La incorporation in Ta_2O_5 gate dielectric on the electrical characteristics of a-IGZO TFTs are studied in this work. For better comparison, TaLaO dielectrics with two different La concentrations have been fabricated in addition to a control sample with pure Ta_2O_5 as gate dielectric.

II. EXPERIMENTAL DETAILS

Each sample was fabricated on a p-type (100) silicon wafer with a resistivity of $0.01 \sim 0.02\ \Omega \cdot cm$ which acts as both the substrate and gate electrode of a-IGZO TFTs. Firstly, the conventional RCA method was used to remove the organic and ionic contaminants on the substrate. Secondly, dielectric films with a thickness of $\sim$40 nm were deposited by means of a sputtering system under a radio-frequency (RF) power supply for a ceramic target of La_2O_3 and a direct-current (DC)

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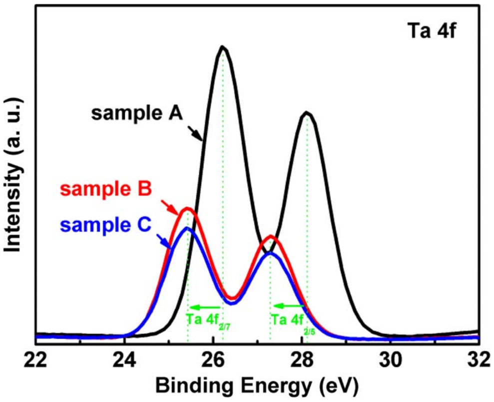

Fig. 1. XPS spectrum of Ta 4f for the gate dielectrics of Ta_2O_5 (in the sample A) and TaLaO (in the samples B, C).

TABLE I
EXTRACTED ELECTRICAL PARAMETERS OF IGZO TFTS

Sample No.	A	B	C
Ta deposition (DC/A)	0.04	0.04	0.04
La deposition (RF/W)	0	40	50
the atomic ratio of La/(Ta+La)	0%	47.8%	55.4%
μ_{sat} (cm^2/V·s)	6.4	24.3	30.9
V_{TH} (V)	1.1	3.4	3.5
SS (V/dec)	0.34	0.20	0.17
N_t (cm^{-2})	8.7×10^{12}	3.4×10^{12}	2.6×10^{12}
ΔV_H (V)	2.9	1.3	0.8
I_{on} (A)	1.6×10^{-4}	4.8×10^{-4}	6.1×10^{-4}
I_{off} (A)	4.9×10^{-9}	8.1×10^{-10}	3.1×10^{-10}
I_{on}/I_{off}	3.2×10^{4}	6.0×10^{5}	2.0×10^{6}
C_{ox} ($\mu F/cm^2$)	0.295	0.231	0.222
t_{ox} (nm)	38	38	37
Dielectric constant	12.7	9.9	9.3

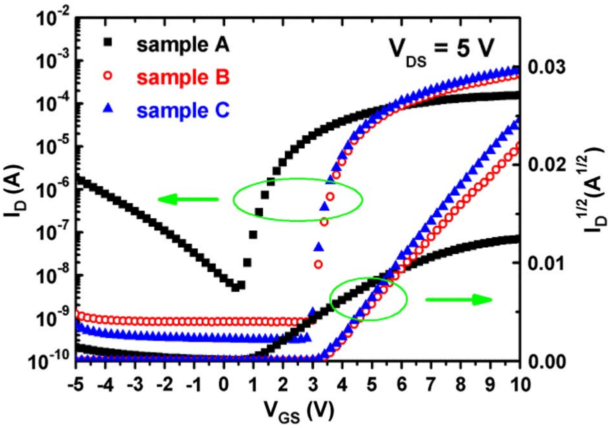

Fig. 2. Transfer characteristics of the a-IGZO TFTs with the gate dielectrics of Ta_2O_5 and TaLaO respectively.

supply for a metal target of Ta in a mixed ambient of Ar and O_2. The RF power was set to be 0 W, 40 W and 50 W for samples A, B and C respectively while the DC supply is fixed at 0.04 A. Thirdly, an annealing treatment at 400 °C in an ambient of N_2 for 10 min with a gas flow rate of 500 ml/min followed in order to improve the quality of the dielectric films. Subsequently, all the samples received a deposition of a 60-nm a-IGZO active layer through RF sputtering from a ceramic target $(Ga_2O_3 : In_2O_3 : ZnO = 1 : 1 : 1)$ in an Ar/O_2 mixed ambient. After that, a lift-off process was utilized to form the source/drain electrodes, which were composed of 20-nm Ti and 80-nm Au deposited by means of electron-beam evaporation. Finally, all the samples were annealed in a forming-gas $(N_2 : H_2 = 95 : 5)$ ambient at 350 °C for 20 min so that the contact resistance of the source/drain electrodes was reduced. In addition, metal-insulator-semiconductor (MIS) capacitor was also prepared beside each sample in order to monitor the gate-oxide capacitance per unit area (C_{ox}). For each TFT device, the channel width (W) and channel length (L) were 100 μm and 20 μm respectively, and all the processing steps except the annealings were conducted at room temperature.

The current-voltage (I–V) curve of the TFTs and the 1-MHz capacitance-voltage (C–V) characteristics of the capacitors were measured by a HP 4145B semiconductor parameter analyzer and a HP 4284A precision LCR meter, respectively. Furthermore, the low-frequency noise (LFN) of the TFTs was monitored by a Berkeley Technology Associates FET Noise Analyzer Model 9603 combined with a HP 35665A Dynamic Signal Analyzer. Besides, the physical thicknesses of Ta_2O_5, TaLaO and IGZO were measured by a multi-wavelength ellipsometer. All the measurements were conducted in a light-tight, electrically-shielded and room-temperature environment.

III. RESULTS AND DISCUSSIONS

Fig. 1 shows the X-ray photoelectron spectrum (XPS) of Ta 4f core level for the gate dielectrics of Ta_2O_5 (in the sample A) and TaLaO (in the samples B, C). All binding energies have been corrected for sample charging effect with reference to the C 1s line at 285.0 eV. As for the sample A, two peaks are located at 26.2 eV and 28.1 eV (for Ta $4f_{2/7}$ and Ta $4f_{2/5}$ respectively) with an energy separation of 1.9 eV, indicating the equilibrium phase of fully oxidized stoichiometric Ta_2O_5 [14]. The shift of Ta 4f double peaks (25.4 eV and 27.3 eV) of the TaLaO gate dielectric in both the samples B and C relative to the Ta_2O_5 reference peaks of the sample A reveals the presence of La atoms in the TaLaO compound structure, with Ta-O bond replaced by Ta-O-La bond. In addition, according to the XPS results, the atomic ratio of $La/(Ta + La)$ is 0%, 47.8% and 55.4% for the samples A, B, and C, respectively. In addition, a continuous reduction of dielectric constant associated with increasing La concentration in the gate dielectric as listed in Table I was observed, which can be explained by the deterioration effect of the hygroscopicity of La-related oxide film on its dielectric constant [15].

Fig. 2 shows the transfer characteristics of the a-IGZO TFTs with the gate dielectric of Ta_2O_5 and TaLaO respectively: drain current (I_D) vs. gate-to-source voltage (V_{GS}) and $I_D^{1/2}$ vs. V_{GS} at a drain-to-source voltage (V_{DS}) of 5 V. The electrical parameters of the devices, including saturation carrier mobility (μ_{sat}), threshold voltage (V_{TH}), subthreshold swing (SS), I_{off} (the smallest I_D), I_{on} ($V_{DS} = 5$ V, $V_{GS} = 10$ V), on-off current ratio (I_{on}/I_{off}), are extracted from Fig. 2 and listed in Table I.

Among them, $\mu_{\rm sat}$ and $\rm V_{TH}$ are calculated from a linear fitting to the plot of $I_{\rm D}^{1/2}$ versus $\rm V_{GS}$, which is based on the I–V equation of field-effect transistor operating in the saturation region

$$I_{\rm D} = \left(\mu_{\rm sat} {\rm C_{ox}} \left(\frac{\rm W}{\rm 2L}\right)\right) ({\rm V_{GS}} - {\rm V_{TH}})^2. \tag{1}$$

As for the sample A, a severe leakage current can be observed under a negative gate bias, and a negative shift of the transfer curve occurs when compared with the samples B and C, indicating the formation of leakage paths. It is believed that the relatively small values of $\rm E_G$ and $\rm \Delta E_C$ (on a-IGZO) of the $\rm Ta_2O_5$ gate dielectric combined with the high trap density within the $\rm Ta_2O_5$ gate dielectric and at the a-IGZO/$\rm Ta_2O_5$ interface contribute to the formation of leakage paths [16]. As a result, the sample A exhibits high values of $I_{\rm off}$ (4.9×10^{-9} A), SS (0.34 V/dec) and low values of $\mu_{\rm sat}$ ($6.4\ {\rm cm^2/V \cdot s}$), $\rm V_{TH}$ (1.1 V), $I_{\rm on}$ (1.6×10^{-4} A), $I_{\rm on}/I_{\rm off}$ (3.1×10^4). On the other hand, the incorporation of La in $\rm Ta_2O_5$ could enlarge the $\rm E_G$ and $\rm \Delta E_C$ (on a-IGZO) of the gate dielectric because $\rm La_2O_3$ has larger values for both parameters than $\rm Ta_2O_5$ [11], [12], thus leading to reduced leakage current ($I_{\rm off} = 8.1 \times 10^{-10}$ A and 3.1×10^{-10} A for the samples B and C respectively). Also, the effect that La incorporation could suppress the formation of oxygen vacancies in high-k dielectrics is supported by the XPS data that the oxygen content of the samples B and C is 1.1% and 1.6% respectively higher than that of the sample A. As a result, the intrinsic traps in the gate dielectric and at the a-IGZO/gate-dielectric interface could be reduced, resulting in smaller SS (0.20 V/dec and 0.17 V/dec for the samples B and C respectively) and less trap-related carrier scattering and thus increased carrier mobility ($\mu_{\rm sat} = 24.3\ {\rm cm^2/V \cdot s}$ and $30.9\ {\rm cm^2/V \cdot s}$ for the samples B and C respectively). As a result, higher $I_{\rm on}$ (4.8×10^{-4} A and 6.1×10^{-4} A for the samples B and C respectively) and larger $I_{\rm on}/I_{\rm off}$ (6.0×10^5 and 2.0×10^6 for the samples B and C respectively) are achieved by the La incorporation compared to those values of the sample A. Moreover, the improvement in electrical characteristics of the sample C is more obvious compared to the sample B, which can be ascribed to more La incorporation in the $\rm Ta_2O_5$ gate dielectric as revealed by the measured atomic ratio of XPS. In addition, the trap density $\rm N_t$ at/near the a-IGZO/gate-dielectric interface can be calculated by the following equation [2], [17]

$$\rm N_t = \left[\frac{SS \log(e)}{\mathit{K}_B \left(\frac{\mathit{T}}{\mathit{q}}\right)} - 1\right] \frac{C_{ox}}{\mathit{q}} \tag{2}$$

where $K_{\rm B}$ is the Boltzmann constant; q is the charge of an electron; and T is the temperature. The extracted $\rm N_t$ value is $8.7 \times 10^{12}\ {\rm cm^{-2}}$, $3.4 \times 10^{12}\ {\rm cm^{-2}}$ and $2.6 \times 10^{12}\ {\rm cm^{-2}}$ for the samples A, B and C, respectively. This result further supports that the trap density at/near the a-IGZO/gate-dielectric interface can be effectively reduced by the incorporation of La in the $\rm Ta_2O_5$ gate dielectric. Fig. 3 displays the output characteristics of the samples. Each sample clearly exhibits the n-type enhancement mode. Moreover, $I_{\rm D}$ increases linearly with $\rm V_{DS}$ in the region of low $\rm V_{DS}$, and current saturation can be observed in the region of high $\rm V_{DS}$. Due to both the increase of carrier mobility and the reduction of leakage current, a significant improvement in output current can be observed with the increase of La concentration in the gate dielectric, which is consistent with the earlier analysis based on the transfer characteristics.

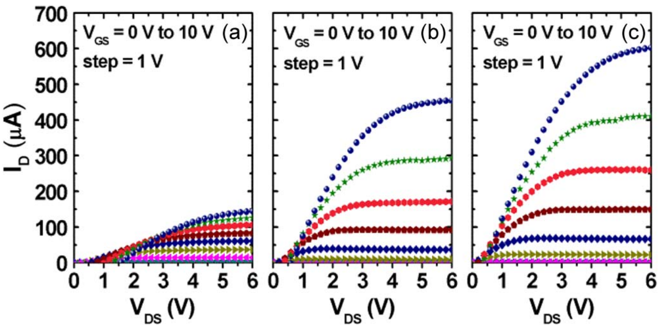

Fig. 3. Output characteristics of the a-IGZO TFTs: (a) Sample A. (b) Sample B. (c) Sample C.

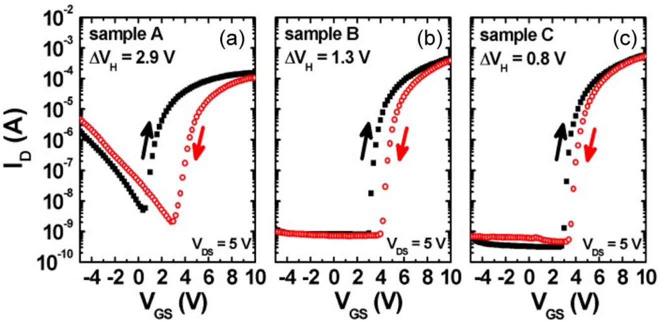

Fig. 4. Transfer characteristics of the a-IGZO TFTs measured under the forward ($\rm V_{GS} = -5$ V to 10 V) and reverse ($\rm V_{GS} = 10$ V to -5 V) sweepings: (a) Sample A. (b) Sample B. (c) Sample C.

As shown in Fig. 4, the hysteresis characteristics of all the samples are investigated accordingly to the transfer characteristics under forward and reverse $\rm V_{GS}$ sweepings successively. $\Delta V_{\rm H}$, defined as the $\rm V_{TH}$ shift in the hysteresis loop, is extracted from Fig. 4 and listed in Table I. It is found that the sample A exhibits an obvious hysteresis with a relatively large $\Delta V_{\rm H}$ (2.9 V), which reflects the existence of a large amount of traps at/near the a-IGZO/$\rm Ta_2O_5$ interface [18]. With the incorporation of La in the $\rm Ta_2O_5$ gate dielectric, the hysteresis can be effectively suppressed as revealed by the smaller $\Delta V_{\rm H}$ of the samples B and C (for the sample B, $\Delta V_{\rm H} = 1.3$ V; for the sample C, $\Delta V_{\rm H} = 0.8$ V), further demonstrating the effective reduction of trap density at/near the a-IGZO/gate-dielectric interface due to the incorporation of La in the $\rm Ta_2O_5$ gate dielectric.

LFN measurement is conducted to study the charge trapping properties of the samples [19]. The normalized noise power spectral density $\rm (S_{iD}/ID_2)$ is measured at a fixed gate overdrive voltage $\rm (V_{GS} - V_{TH})$ of 3.0 V in the linear region $\rm (V_{DS} = 1.0\ V)$ and the frequency range from 3.2 Hz to 1.3×10^4 Hz for each sample as shown in Fig. 5. The LFN of a-IGZO TFTs can be caused by carrier number fluctuation (due to charge trapping

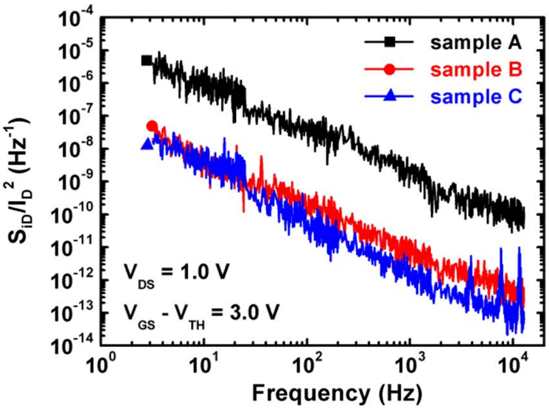

Fig. 5. Low-frequency noise versus frequency of the a-IGZO TFTs with gate dielectric of Ta_2O_5 (sample A) and TaLaO (samples B and C) respectively.

by the traps at/near the a-IGZO/gate-dielectric interface) and/or mobility fluctuation (due to Coulomb scattering by the trapped charge at/near the a-IGZO/gate-dielectric interface) [20], [21]. As shown in Fig. 5, the LFN's of the two samples with TaLaO gate dielectric are over two orders of magnitude smaller than that of the sample A with Ta_2O_5 gate dielectric. Moreover, the sample C, which has the highest La concentration in the gate dielectric among the samples, exhibits the smallest LFN. Hence, the LFN data further supports that the improvement of electrical properties is due to the reduction of traps at/near the a-IGZO/gate-dielectric interface induced by the incorporation of La in the Ta_2O_5 gate dielectric.

IV. CONCLUSION

A comparative study of a-IGZO TFTs with Ta_2O_5 and TaLaO as gate dielectric has been conducted in this work. It is demonstrated that La incorporation in the Ta_2O_5 gate dielectric can effectively improve the electrical characteristics of a-IGZO TFTs by enlarging the E_G and ΔE_C (on a-IGZO) of the gate dielectric and reducing the trap density in the gate dielectric and at the a-IGZO/gate-dielectric interface. As a result, the sample C, which has the highest La concentration in gate dielectric in this work (atomic ratio of $La/(Ta + La) = 55.4\%$), presents superior electrical characteristics, e.g. high μ_{sat} of 30.9 $cm^2/V \cdot s$, small SS of 0.17 V/dec, small ΔV_H of 0.8 V and high I_{on}/I_{off} of 2.0×10^6. In addition, the LFN measurement result further supports the improvement in electrical properties is due to trap reduction in the gate dielectric and at the a-IGZO/gate-dielectric interface achieved by La incorporation in the Ta_2O_5 gate dielectric. In summary, these results demonstrate the potential use of TaLaO gate dielectric for making high-performance a-IGZO TFTs used in the field of high-speed high-resolution FPDs.

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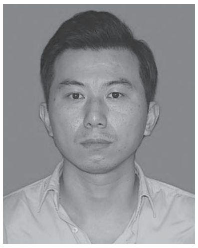

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