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Adaptive Prediction in Digitally Controlled Buck Converter with Fast Load Transient Response

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***Abstract*—An adaptive prediction scheme based on linear extrapolation for digitally controlled voltage-mode buck-type switching converter is presented. A major drawback of conventional digitally controlled switching converters is bandwidth limitation due to the additional phase lag in the digital feedback control loop. By predicting the future error voltage, the ADC sampling time delay is compensated in order to achieve a higher bandwidth even with a modest sampling rate. Both simulation and measurement results show that the output voltage settling time of the digitally controlled buck converter is reduced by as much as 28% with the proposed adaptive prediction. The fastest settling time in response to a 600mA load transient is around 15µs, approaching the transient response of the state-of-the-art analog-based controller.**

Keywords-Adaptive prediction, digital controller, IIR filter, adaptive FIR filter, buck converter.

I. INTRODUCTION

Digital control in switching regulators is gaining popularity because of its inherent benefits such as controller re-configurability without hardware modification, less susceptible to aging, noise and parameter variations, increased robustness of the controller behavior, and the possibility of implementing more advanced control techniques. Despite its many advantages over the analog counterparts, digital control in single sampling suffers a major bandwidth limitation which significantly degrades its dynamic performance. Researchers have previously proposed the multi-sampling approach which reduces the overall phase lag in the digital control loop, hence breaking the bandwidth limitation [1]-[5]. However, the brute-force approach of increasing the sampling rate has several major drawbacks including the injection of high-frequency noise into the feedback loop, the possibility of inducing limit-cycle oscillations, and increased dynamic power consumption. In this paper, an adaptive prediction technique is proposed to provide an early estimation of the error voltage for the next sampling cycle, virtually eliminating the ADC sampling time delay in the digital control loop. Based on the concept of linear extrapolation, the estimation is performed using the two most recent samples of the error voltage. A major benefit is that, unlike the existing prediction schemes [6]-[11], the proposed predictor does not require any prior knowledge of the system. It is basically independent of uncertainties and variations of the system parameters, hence improving the robustness of the digital controller. Section II presents the proposed adaptive prediction scheme and shows how it can reduce the phase lag with a low sampling rate. Section III demonstrates the effectiveness of the proposed digital controller with adaptive prediction in regulating a voltage-mode buck-type switching converter. Simulation and experimental results of the load transient response are presented. Section IV concludes the paper by comparing the proposed digital controller with prior arts.

II. PROPOSED ADAPTIVE PREDICTION SCHEME

In a digitally controlled switching converter using voltage-mode control, the instantaneous feedback voltage V_{fb} is sampled by the ADC and the resulting digitized feedback voltage is compared with the reference voltage $V_{ref.}$ The digital controller is primarily used to ensure that V_{fb} tracks with V_{ref} while achieving the desired closed-loop performance. The Digital Pulse-Width Modulator (DPWM) converts the digital output of the controller into a pulsating waveform to control the power switches. Figure 1 shows a simplified functional block diagram of the proposed digitally controlled buck converter. In a single-sampling scheme, the instantaneous feedback voltage is sampled by the ADC only once per switching cycle. The sample-and-hold process formed by the ADC and Digital Pulse-Width Modulation (DPWM) introduces a phase delay of $2\pi D\frac{f_{UGF}}{f_s}$, where D is the steady-state duty ratio, f_{UGF} is the unity-gain frequency, and f_s is the switching frequency. The phase margin is further reduced

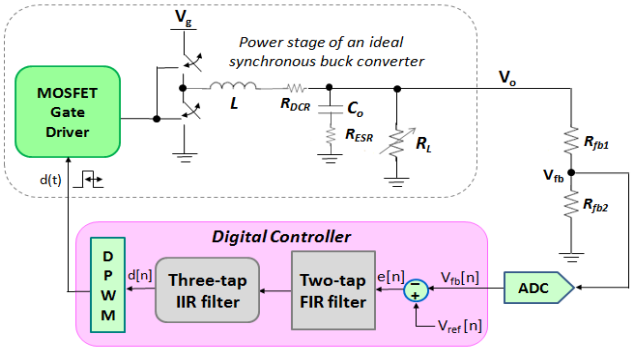

Figure 1. Block diagram of the proposed digitally controlled buck switcher.

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by the total time delay t_d between the ADC sampling instant and the modulation edge of the PWM signal. In general, t_d is a fraction of the switching period T_s given by $t_d = \frac{T_s}{N}$ which accounts for the ADC conversion time and the computational delay across the digital controller. Hence, the total phase lag ϕ due to the digital feedback loop can be expressed as:

$$\phi = \omega D T_s + \omega t_d = 2\pi D \frac{f_{UGF}}{f_s} + 2\pi \frac{f_{UGF}}{N f_s} = 2\pi \frac{f_{UGF}}{f_s}\left(D + \frac{1}{N}\right) \quad (1)$$

As an example, $t_d = \frac{T_s}{2}$, $D = 50\%$, and $\frac{f_{UGF}}{f_s} = \frac{1}{10}$ for a single-sampling digitally-controlled buck converter. Substituting the values into (1), the total phase shift is 36°. This is graphically illustrated in Figure 2 showing the timing diagram of the digital control loop based on the single-sampling scheme. In order to maintain a stable system with sufficient phase margin, the unity-gain frequency f_{UGF} has to be reduced for a given switching frequency, resulting in a smaller bandwidth and slower transient response. Another option is to increase the ADC sampling rate as in the multi-sampling approach [1]-[5].

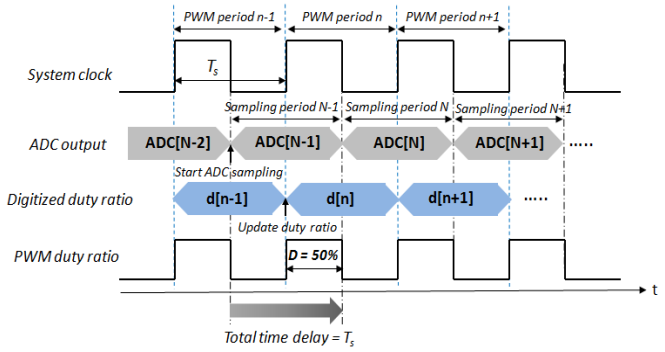


Figure 2. Timing diagram of a single-sampling digital control loop.

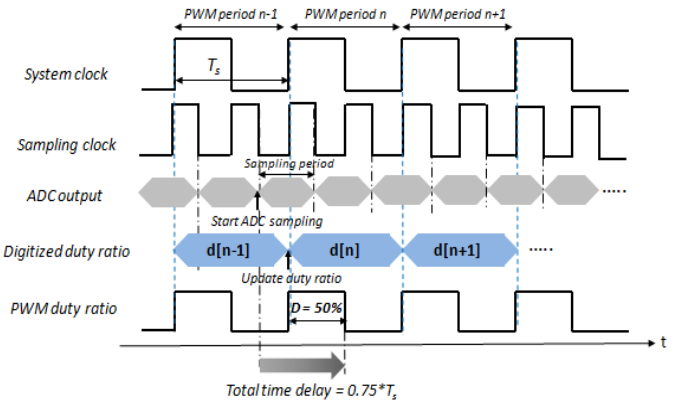


Figure 3. Timing diagram of a double-sampling digital control loop.

By doubling the sampling rate as shown in Figure 3, the total phase lag is reduced from 36° to 27° due to the smaller sampling delay. The challenge is to minimize the phase lag by virtually eliminating the sampling time delay. This leads to the investigation of the proposed adaptive prediction scheme based on a modified form of linear extrapolation. As shown in Figure 1, the error voltage $e[n]$ in the discrete-time domain is given by (2).

$$e[n] = V_{ref}[n] - V_{fb}[n] \quad (2)$$

The primary objective of the proposed adaptive linear predictor is to regulate the buck converter by estimating the error voltage for the next sampling time instant based on the two most recent samples and the last known estimation error. Basically, the underlying prediction function performs self-training by continuously monitoring the last known estimation error. Mathematically, the first-order prediction function is given by (3) and (4).

$$\hat{e}[n+1] = 2e[n] - e[n-1] \pm \frac{1}{2^k}\left|\Delta e_d[n]\right| \quad (3)$$

$$\Delta e_d[n] = e[n] - \hat{e}[n] \quad (4)$$

$\hat{e}[n+1]$ is the future error voltage at the next sampling instant which is extrapolated from the two most recent sampled error values, $e[n]$ and $e[n-1]$, augmented with an error correction term $\frac{1}{2^k}\left|\Delta e_d[n]\right|$. This error term effectively adjusts the slope of the linear extrapolation function, thereby shaping the learning behavior of the predictor. In practice, $\left|\Delta e_d[n]\right|$ is bounded by two pre-defined limits to ensure a conditionally stable closed-loop system. By binning the actual estimation error $\Delta e_d[n]$, appropriate integer values of k can be assigned in order to achieve the desired closed-loop performance of a digitally controlled buck converter. In the event that $\left|\Delta e_d[n]\right|$ becomes smaller than a certain threshold ε indicating a steady-state condition, the error correction term can be zeroed out. Hence, Equation (3) becomes a fixed linear extrapolation function in quiescent operating condition. Given an oversampling ratio of two (i.e. the sampling frequency is twice the switching frequency of the buck converter) and $\frac{f_{UGF}}{f_s} = \frac{1}{10}$, the resulting phase boost provided by the proposed adaptive predictor is approximately 18° relative to the original single-sampling scheme. Consequently, by incorporating the proposed prediction scheme into the digital controller, the unity-gain frequency can be further extended out while maintaining a conditionally stable closed-loop system.

III. BUCK SWITCHING CONVERTER WITH THE PROPOSED DIGITAL CONTROLLER

A. Small-signal Analysis

A small-signal model of the proposed digitally controlled buck converter can be constructed as shown in Figure 4. The sampling process of the ADC is represented by an ideal sampler with a sampling time period T_{sam}. The DPWM is essentially a hold device. Hence, the ADC and DPWM together constitute a sampling and hold device which can be represented by the zero-order hold (ZOH) function. The gain of the ADC and DPWM is jointly represented as K_D and b is the scaling factor given by $R_{fb2}/(R_{fb1}+R_{fb2})$. The total time delay t_d along the digital feedback path is also included in the small-signal analysis. The proposed digital controller is made up of a first-order FIR filter cascaded with a second-order IIR filter.

The Direct Digital Design approach [12] is employed in designing and optimizing the proposed digital controller in the discrete-time domain. The idea is that the controller is a discrete-time system and from the viewpoint of the controller, the power stage also looks discrete. First, the continuous-time power stage model $G_p(s)$ in the s-domain is discretized using the step invariant transformation with zero-hold order (ZOH). Once the discrete-time approximation of the power stage $G_p(z)$ is obtained, the digital controller is designed entirely in the z-domain using the discrete-time frequency response method. The advantage of the direct digital design approach is that the effect of the sampling and hold has already been taken into account by the discrete-time power plant prior to the controller design. In addition, the location of the poles and zeros of the controller can be assigned precisely in the discrete-time domain, resulting in a more predictable and accurate evaluation of dynamic performance.

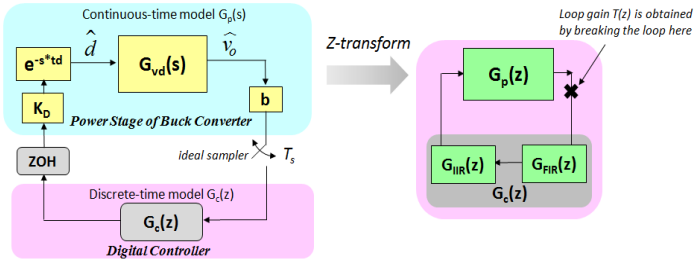


Figure 4. Small-signal block diagram of the proposed buck converter.

Table I lists the system parameters for the proposed voltage-mode buck converter.

Table I. System parameters for the proposed buck converter.

Parameter	Value	Unit
Switching frequency	1	MHz
Sampling frequency	2	MHz
Input voltage	3	V
Maximum output current	600	mA
Inductor	4.7	μH
Output capacitor	4.7	μF

Based on Figure 4, the continuous-time transfer function of the power plant can be expressed as:

$$G_p(s) = bK_D G_{vd}(s) e^{-st_d} \tag{5}$$

where $G_{vd}(s) = \dfrac{\hat{v}_o}{\hat{d}} \approx \dfrac{1+sR_{ESR}C_o}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$.

Based on the system parameters given in Table I, the ZOH equivalent of the continuous-time power plant model in (5) using a sampling period of 0.5μs is given by:

$$G_p(z) = Z\left\{\frac{1-e^{-T_{sam}s}}{s} G_p(s)\right\} = \frac{0.01068\,z^{-1}+0.0002769\,z^{-2}}{1-1.928z^{-1}+0.9395z^{-2}} \tag{6}$$

where Z denotes the z-transform of the function within the parenthesis { }.

From Figure 4, the loop gain function is represented as:

$$T(z) = G_p(z)G_c(z) = G_p(z)G_{FIR}(z)G_{IIR}(z) \tag{7}$$

Due to the complex poles formed by the *L-C* output filter in the power stage of a buck converter, the phase margin drops rapidly at the complex resonant pole frequency ω_{LC0}. To extend the unity-gain frequency beyond ω_{LC0}, a second-order IIR filter is used to generate two compensated zeros $(\omega_{z1}, \omega_{z2})$ to offset the complex poles and provide the necessary phase boost. In addition, the IIR filter generates a dominant pole ω_{p0} at very low frequency and a secondary pole ω_{p1} beyond the unity-gain frequency ω_{UGF}. Unfortunately, this secondary pole increases the phase lag beyond ω_{LC0}, preventing the unity-gain bandwidth to be extended out to higher frequencies. Therefore, a first-order FIR filter is introduced which generates a high-frequency zero ω_{z3} to compensate the secondary pole from the IIR filter. Equation (8) gives the relative location of all the poles and zeros in the loop gain function with respect to the unity-gain frequency.

$$\omega_{p0} < \omega_{z1} < \omega_{LC0} < \omega_{z2} < \omega_{UGF} < \omega_{p1} < \omega_{z3} \tag{8}$$

It is assumed that an output capacitor with a very low ESR is used. Hence, the ESR zero lies beyond the switching frequency and its effect on the loop gain frequency response is minimal.

The open-loop frequency response using the FIR filter with *fixed* linear extrapolation is first investigated. The discrete-time transfer function for this particular FIR filter is given by:

$$G_{FIR}(z) = 2 - z^{-1} \tag{9}$$

Basically, the FIR filter defines the location of the third compensated zero ω_{z3}.

Now, the only unknown is the transfer function of the IIR filter $G_{IIR}(z)$. The loop gain function in (7) is re-expressed as:

$$T(z) = G_p(z)G_{FIR}(z)G_{IIR}(z) = G_{pF}(z)G_{IIR}(z) \qquad (10)$$

Using invertible Bilinear Mapping (Tustin's method), a "pseudo-continuous" transfer function $G_{pF}(w)$ in the w-plane can be written as:

$$G_{pF}(w) = G_{pF}(z)\Big|_{z=\frac{1+(T_{sam}/2)w}{1-(T_{sam}/2)w}} \qquad (11)$$

This effectively maps the unit circuit in the z-plane to the imaginary axis in the w-plane. Basically, it enables the use of conventional frequency response techniques such as Bode plot to design the IIR filter. Using Matlab's *sisotool*, the discrete-time transfer function of the IIR filter is obtained as follows.

$$G_{IIR}(z) = \frac{9.166 - 16.69z^{-1} + 7.582z^{-2}}{1 - 1.516z^{-1} + 0.5156z^{-2}} \qquad (12)$$

The resulting unity-gain bandwidth is 6.82×10^5 rad/sec with a phase margin of 59.8° and gain margin of 17.6 dB as shown in Figure 5. The unity-gain bandwidth is approximately one-ninth of the switching frequency. It is interesting to note that if the FIR filter is removed from the existing digital controller, the phase margin is reduced to 43° at the same unity-gain bandwidth. The degradation in phase margin is mainly due to the absence of the third compensated zero ω_{z3}. This is graphically illustrated in Figure 6.

Consider the case when the proposed adaptive prediction technique is used. The first coefficient of the FIR filter in (9) is being modulated by the error correction term during transient.

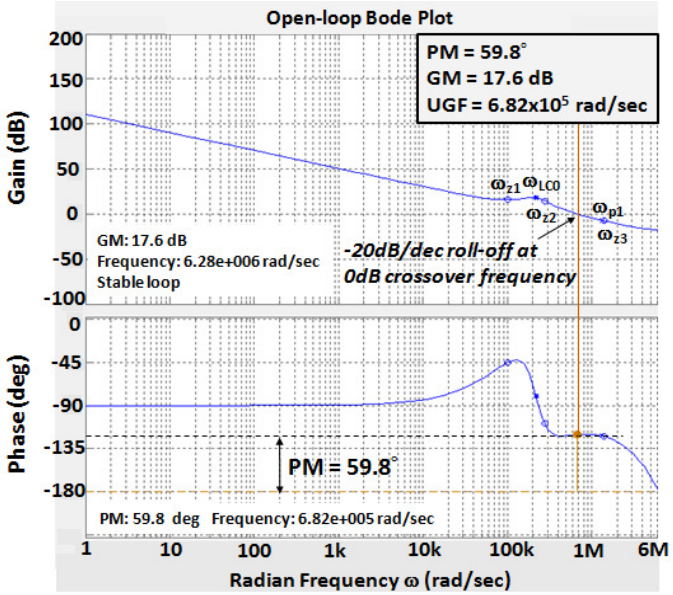


Figure 5. Bode magnitude and phase plots of the open-loop frequency response with fixed linear extrapolation (including pole and zero locations).

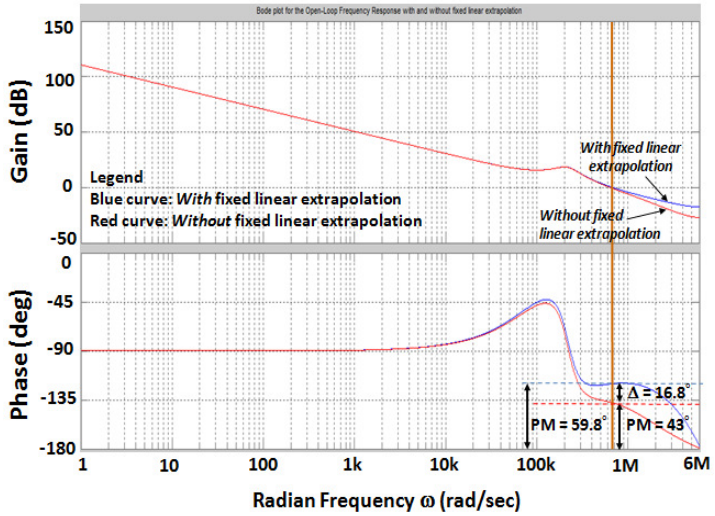


Figure 6. Bode magnitude and phase plots of the open-loop frequency response *with* and *without* fixed linear extrapolation.

Suppose $k = 2$ and $|\Delta e_d[n]| \le e[n]$. The range of $\hat{e}[n+1]$ in (3) is given by:

$$1.75e[n] - e[n-1] \le \hat{e}[n+1] \le 2.25e[n] - e[n-1] \qquad (13)$$

The discrete-time transfer function of the FIR filter is therefore modified as:

$$G_{FIR}(z) = a_0 - z^{-1} \quad \text{for } 1.75 \le a_0 \le 2.25 \qquad (14)$$

It is crucial to ensure that the closed-loop system remains conditionally stable at the two endpoints of a_0. Figure 7 highlights the change in the open-loop frequency response as a_0 varies from 1.75 to 2.25. It shows that the stability of the system is *not* compromised as the unity-gain bandwidth is increased. The stability metrics for $a_0 = 1.75$ and $a_0 = 2.25$ are summarized in Table II. In general, loop stability should be examined for the largest possible gain value applied by the digital controller with the proposed adaptive prediction scheme.

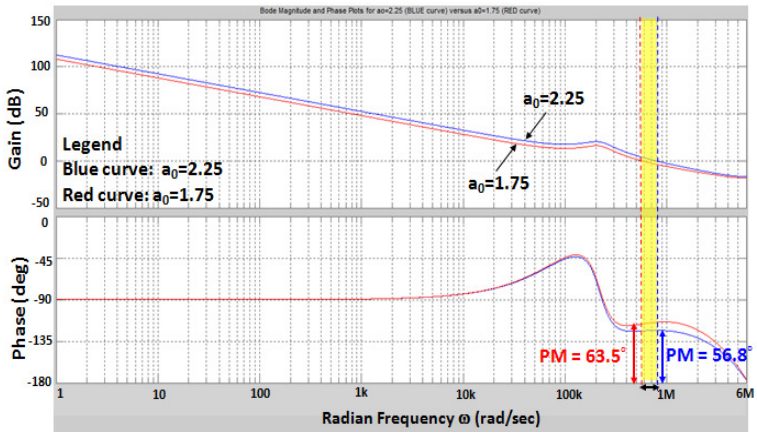


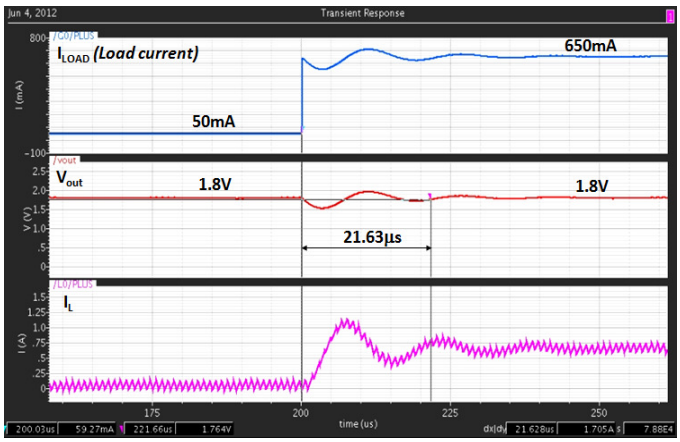
Figure 7. Bode magnitude and phase plots for $a_0 = 1.75$ and $a_0 = 2.25$.

Table II. Stability metrics for the upper and lower bound of a_0.

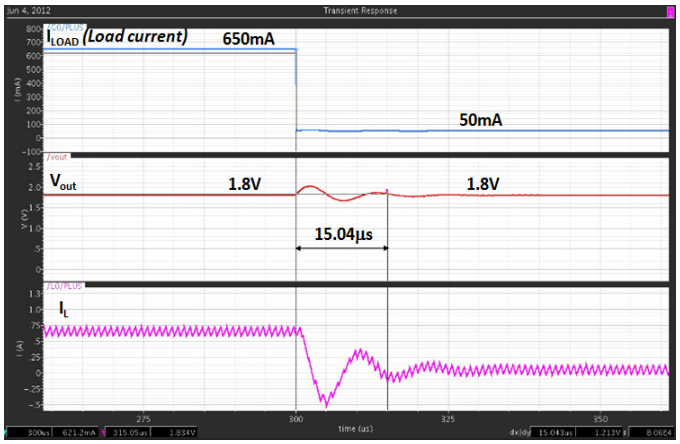
Parameter	a_0=1.75	a_0=2.25
Phase Margin	63.5°	56.8°
Gain Margin	18.1 dB	16.9 dB
Unity-gain frequency	5.71×10^5 rad/sec	7.88×10^5 rad/sec
f_{UGF}/f_s	1/11	1/8

B. Simulation Results

A Cadence Spectre macro model for the closed-loop system of a buck converter compensated by the proposed digital controller was created. Mixed-mode simulations were conducted using Cadence SpectreVerilog simulator in which the digital controller was being modeled in Verilog RTL and the power stage of the buck converter was modeled as ideal circuit components with major parasitics included. Load transient simulations were performed to study the transient behavior of the closed-loop system. For the sake of consistency, both Cadence time-domain models and Matlab small-signal models use the same set of system parameters specified in Table I. The load transient response for a maximum load step of 600mA using the proposed adaptive prediction control scheme was simulated. Figure 8 shows the load step-up and step-down transient, respectively.



(a)



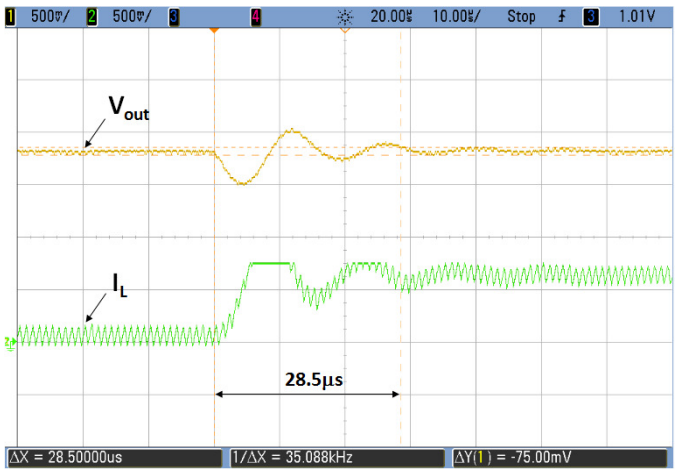
(b)

Figure 8. Simulated load a) step-up and (b) step-down transient response with the proposed adaptive prediction control scheme.

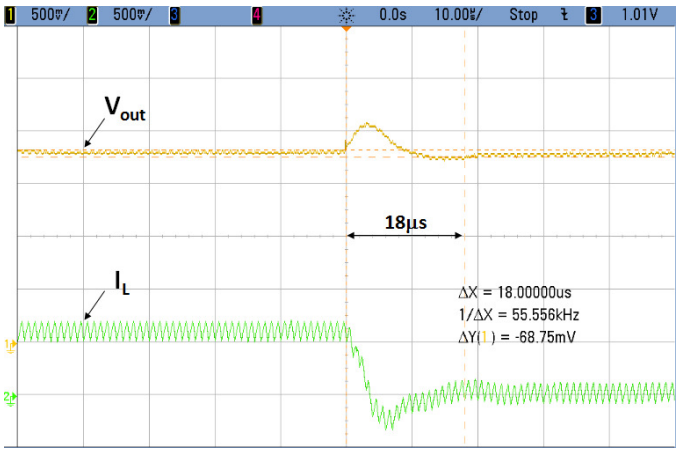
Cadence simulation shows that the output voltage settling times (i.e. the time it takes for the output to settle within 2% of its steady-state value) for step-up and step-down load transient are 21.63µs and 15.04µs, respectively.

C. Experimental Results

An FPGA-based hardware prototype of the proposed digitally controlled buck converter was implemented based on the system specification in Table I. First, a digital controller with *fixed* linear extrapolation was tested. The output settling time in response to a load transient of 600mA was measured. The actual measurement result shows that the output settling times for step-up and step-down load transient are 28.5µs and 18µs, respectively, as shown in Figure 9. Second, the load transient experiment was repeated for the proposed *adaptive* extrapolation scheme. The output settling time for step-up and step-down load transient was measured to be 20.6µs and 15.5µs, respectively, as shown in Figure 10.

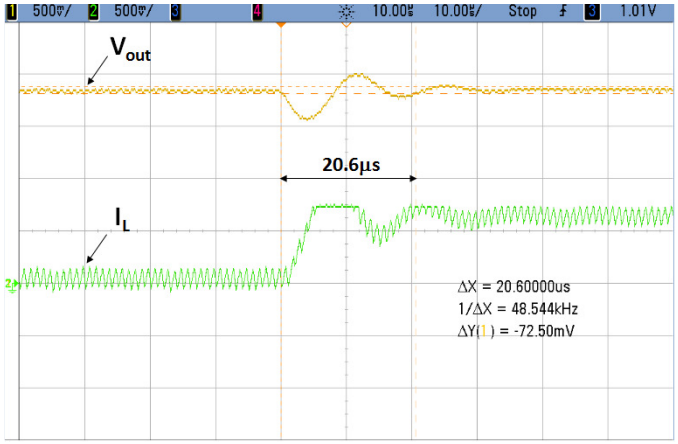


(a)

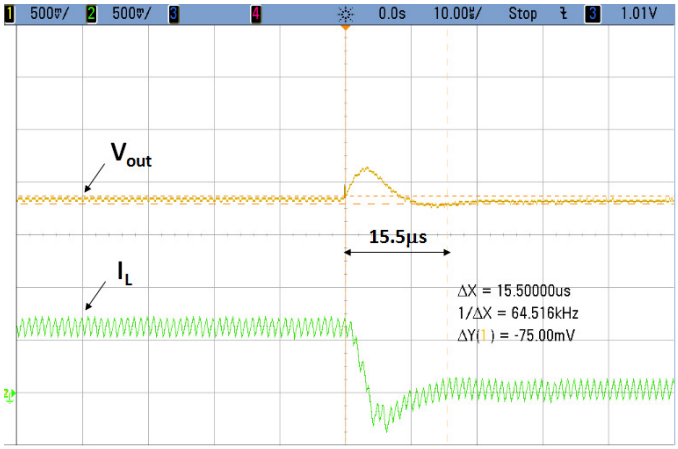


(b)

Figure 9. (a) Step-up (b) Step-down load transient response for fixed linear extrapolation.



(a)



(b)

Figure 10. (a) Step-up (b) Step-down load transient response for the proposed adaptive prediction scheme.

Experimental results show that the proposed adaptive prediction scheme improves the load transient response by as much as 28%. Also, the output settling times from simulation and measurement are within ±5% of each other.

IV. CONCLUSION

This paper presents an adaptive digital prediction control scheme for switch-mode power supplies (SMPS). This scheme is demonstrated to be effective. We have shown that the overall bandwidth is further increased even with a modest oversampling ratio. The proposed digital compensator allows very precise assignment of pole-zero locations which are programmable, depending on the transfer function of the power stage. Table III concludes this paper by comparing the settling time of the output voltage from the proposed digitally controlled switching converter with prior arts. It shows that the proposed digital controller achieves much faster output settling time than existing digital compensators [13]-[16] and its transient response is approaching to that of the analog-based pseudo-type III compensator [17][18].

Table III. Comparison with Prior Arts.

	Compensator Type	Output voltage settling time	Load current step
Patella 2003 [13]	Digital PID	>70µs	500mA
Xiao 2004 [14]	Digital PID	Around 100µs	100mA
Chui 2005 [15]	Digital PID	Around 50µs	100mA
Soenen [16]	First-order Digital Filter	1ms	200mA
Wu 2010 [17]	Analog (Pseudo-Type III)	Within 7µs	500mA
Malcovati [18]	Analog (Type-III Compensation)	<20µs	1.9A
This Work	Proposed Digital Filter with Adaptive Linear Extrapolation	Between 15µs and 21µs	600mA

REFERENCES

[1] L. Corradini, and P. Mattavelli, "Analysis of multiple sampling technique for digitally controlled dc-dc converters", in *Proceedings of the IEEE 37th Annual Power Electronics Specialist Conference, PESC 2006*, pp.1-6, June 18-26 2006.

[2] E. Tedeschi, P. Mattavelli, D. Trevisan, L. Corradini, "Repetitive ripple estimation in multi-sampling digitally controlled dc-dc converters", *32nd Annual Conference of the IEEE Industrial Electronics Society, IECON 2006,* pp.1685-1690, November 7-10 2006.

[3] L. Corradini, P. Mattavelli, S. Saggini, "Elimination of sampling-induced dead bands in multiple-sampled pulse width modulators for dc-dc converters", *33rd Annual Conference of the IEEE Industrial Electronics Society, IECON 2007,* pp.1495-1500, November 5-8 2007.

[4] Luca Corradini, Paolo Mattavelli, Elisabetta Tedeschi, and Daniele Trevisan, "High bandwidth multisampled digitally controlled dc–dc converters using ripple compensation", *IEEE Transactions on Industrial Electronics,* vol. 55, no. 4, pp. 1501-1508, April 2008.

[5] Luca Corradini, and Paolo Mattavelli, "Modeling of multisampled pulse width modulators for digitally controlled dc–dc converters", *IEEE Transactions on Power Electronics.*, Vol. 23, No. 4, pp. 1839-1847, July 2008.

[6] Doug Sprock and Ping Hsu, "Predictive discrete time control of switch-mode applications", *28th Annual IEEE Power Electronics Specialists Conference, PESC 1997,* pp.175-181, 22-27 June 1997.

[7] S. Bibian, H. Jin, "A simple prediction technique for the compensation of digital control time delay in dc switchmode power supplies", *14th Annual Applied Power Electronics Conference and Exposition, APEC 1999,* pp. 994-1000, 14-18 March 1999.

[8] S. Bibian, H. Jin, "Time delay compensation of digital control for dc switchmode power supplies using prediction techniques", *IEEE Transactions on Power Electronics,* Vol. 15, No. 5, pp. 835-842, September 2000.

[9] J. Chen, A. Prodic, R.W. Erickson, and D. Maksimovic, "Predictive digital current programmed control", *IEEE Transactions on Power Electronics*, Vol. 18, No. 1, pp. 411-419, January 2003.

[10] M. Ferdowsi, "An estimative current mode controller for dc-dc converters operating in continuous conduction mode", *21st Annual Applied Power Electronics Conference and Exposition, APEC 2006,* pp.1133-1136, March 19-23, 2006.

[11] Kai Wan and Mehdi Ferdowsi, "Reducing computational time delay in digital current-mode controllers for dc-dc converters", *in IEEE 30th International Telecommunications Energy Conference, INTELEC 2008*, September 14-18 2008.

[12] Y. Duan, H. Jin, "Digital controlled design for switch mode power converters", *14th Annual Applied Power Electronics Conference and Exposition*, *APEC 1999*, Vol. 2, pp 967-973, March 1999.

[13] Benjamin J. Patella, Aleksandar Prodic, Art Zirger, and Dragon Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters", *IEEE Transactions on Power Electronics*, Vol. 18, No. 1, pp. 438-446, January 2003.

[14] Jinwen Xiao, Angel Peterchev, Jianhui Zhang, and Seth Sanders, "An ultra-low-power digitally controlled buck converter IC for cellular phone applications", *19th Annual Applied Power Electronics Conference and Exposition, APEC 2004,* pp.383-391, February 26, 2004.

[15] Martin Yeung-Kei Chui, Wing-Hung Ki, and Chi-Ying Tsui, "A programmable integrated digital controller for switching converters

with dual-band switching and complex pole-zero compensation", *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 3, pp.772-780, March 2005.

[16] Eric G Soenen, Alan Roth, Justin Shi, Martin Kinyua, Justin Gaither, and Elizabeth Ortynska, "A robust digital dc-dc converter with rail-to-rail output range in 40nm CMOS", *2010 IEEE International Solid-State Circuits Conference*, pp. 198-199, February 7-11, 2010.

[17] Patrick Y. Wu, Sam Y. S. Tsui, and Philip K. T. Mok, "Area- and power-efficient monolithic buck converters with pseudo-type III compensation", *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 8, pp.1446-1455, August 2010.

[18] Piero Malcovati, Massimiliano Belloni, Fabio Gozzini, Cristiano Bazzani, Andrea Baschirotto, "A 0.18μm CMOS 91%-Efficiency 0.1-to-2A Scalable Buck-Boost DC-DC Converter for LED Drivers", *2012 IEEE International Solid-State Circuits Conference*, Session 16, No. 4, pp.280-281, February 2012.