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Reset-Sensing Quasi-V^2 Single-Inductor Multiple-Output Buck Converter with Reduced Cross-Regulation

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Abstract—**This paper proposes a reset-sensing quasi-V^2 single-inductor multiple-output (SIMO) converter with minimal cross-regulation. The conventional quasi-V^2 sensing scheme in SIMO converters suffers from serious cross-regulation which is primarily induced by the load differentiation with unbalanced loads. It is shown that the proposed reset-sensing quasi-V^2 control scheme can significantly reduce cross-regulation by completely discharging the feed-forward sensing node to zero volts during the idle phase in Discontinuous Conduction Mode (DCM). The cross-regulation with the conventional quasi-V^2 single-inductor dual-output (SIDO) converter for a load current step of 150 mA is experimentally verified to be more than 1.25 mV/mA. By employing the proposed quasi-V^2 control method, the experimental results demonstrate that the cross-regulation for a load current step of 150 mA is significantly reduced to within 0.087 mV/mA. Hence, with the proposed scheme, a load transient in one output will have a minimal effect on the DC operating point of another output. This enables separate current control at each individually-driven output of a SIMO converter.**

Index Terms—**Reset-Sensing Quasi-V^2 Control, Cross-Regulation, Discontinuous Conduction Mode (DCM), Single-Inductor Multiple-Output (SIMO).**

I. Introduction

Minimizing cross-regulation has always been a major design challenge for single-inductor multiple-output (SIMO) switching converters [1]-[4]. It occurs when a load transition in one output causes unwanted voltage variation at the unchanged outputs. A quasi-V^2 single-output buck converter first appears in the literature in which a low-pass RC filter is inserted across the inductor to monitor the inductor current [5]. This particular type of buck converter can achieve fast load transient response with a recovery time in the order of several micro-seconds [5], [6]. It offers a simple and lossless approach of sensing the inductor current without requiring a highly accurate current-sense resistor and current-sense operational amplifier. The quasi-V^2 control scheme has also been used to regulate a single-inductor multiple-output (SIMO) buck converter [7]. However, the quasi-V^2 SIMO converter suffers from serious cross-regulation with unbalanced loads due to an inherent DC offset in the feed-forward sense voltage. A change in the average load current of one output causes an unwanted change in that of the unchanged output. Therefore, in this paper, a reset-sensing control method is proposed to address the cross-regulation issue in typical quasi-V^2 SIMO converters. The root cause of cross-regulation in conventional quasi-V^2 single-inductor dual-output (SIDO) converters is formally investigated. The operating principle of the proposed reset-sensing quasi-V^2 control scheme is discussed. The experimental results are also provided to validate its effectiveness in minimizing cross-regulation in quasi-V^2 SIDO converters.

II. Cross-Regulation in Conventional Quasi-V^2 SIDO Converter

The system architecture of a conventional quasi-V^2 SIDO buck converter is depicted in Fig. 1. In this section, the cross-regulation of this particular type of SIDO converter is investigated.

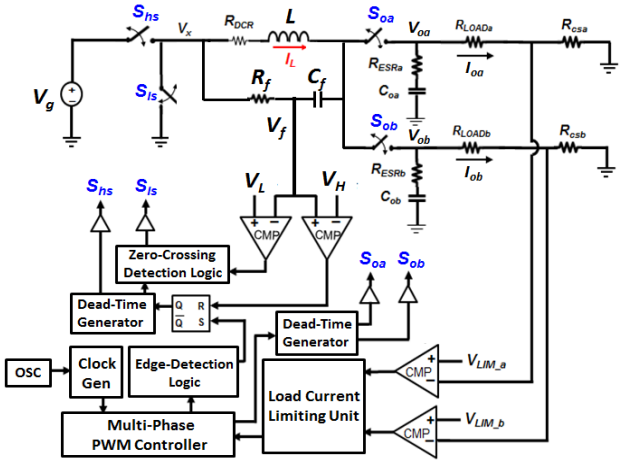

Fig. 1. System architecture of the conventional quasi-V^2 SIDO buck converter.

The two outputs share a single inductor L and the energy stored in L is distributed across the two outputs in a time-multiplexed fashion. Ideally, the voltage ripple at the quasi-V^2

node, ΔV_f, is proportional to the inductor current ripple ΔI_L with zero phase shift [5]-[7]. By comparing the sensed V_f against a pre-determined set of high threshold voltage (V_H) and low threshold voltage (V_L), the peak-crossing and zero-crossing events of I_L can be easily detected. Fig. 2 shows the origin of cross-regulation as the SIDO buck converter transitions from balanced loads to unbalanced loads.

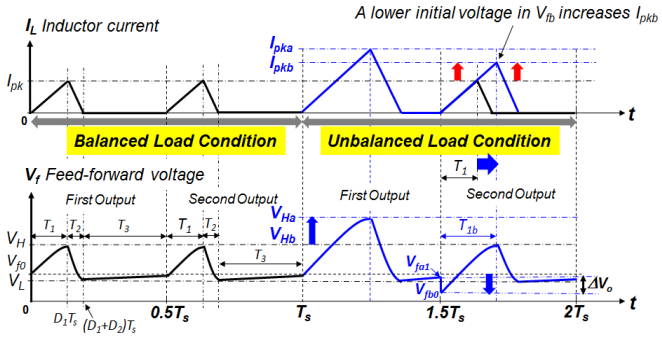

Fig. 2. Cross-regulation occurs when the inductor current for the first string is increased.

In balanced load conditions, the output voltage and the load current are completely identical across the two outputs (i.e. $V_{oa} = V_{ob} = V_o$ and $I_{oa} = I_{ob} = I_o$). Let $T_1 = D_1T_s$ for the first sub-interval, $T_2 = D_2T_s$ for the second sub-interval, $T_3 = D_3T_s$ for the third sub-interval (idle phase), and T_s is the switching period as illustrated in Fig. 2. Since the SIDO buck converter operates in DCM, the duty ratio D_1 in the first sub-interval is given by [8]:

$$D_1 = M\sqrt{\frac{2L}{R_{LOAD}T_s(1-M)}} \tag{1}$$

where $M = V_o/V_g$ (V_g is the input voltage) and $R_{LOAD} = V_o/I_o$ (assuming $R_{LOAD} >> R_{CS}$). Hence, T_1 can be expressed in terms of V_o as:

$$T_1 = \sqrt{\frac{2LV_oI_oT_s}{V_g(V_g-V_o)}} = \sqrt{\frac{2LV_o^2T_s}{V_g(V_g-V_o)R_{LOAD}}} \tag{2}$$

By invoking volt-second balance, T_2 can be obtained as:

$$T_2 = \sqrt{\frac{2L(V_g-V_o)I_oT_s}{V_gV_o}} = \sqrt{\frac{2L(V_g-V_o)T_s}{V_gR_{LOAD}}} \tag{3}$$

To simplify the ensuing analysis, the output voltage V_o is assumed to be ideal with a constant DC value and negligible AC ripple. V_{f0} represents the initial value of V_f at the beginning of every switching phase (i.e. $t = nT_s/2$) as shown in Fig. 2. Under balanced load conditions, V_{f0} has a constant value across every switching phase in steady-state condition. In steady-state DCM, $V_f(t)$ can be expressed in the general form:

$$V_f(t) = V_{f0} + (V_g - V_{f0})(1-e^{-t/(\tau_f)}) \quad 0 \le t < D_1T_s \tag{4a}$$

$$V_f(t) = V_He^{-t/\tau_f} \quad D_1T_s \le t < (D_1+D_2)T_s \tag{4b}$$

$$V_f(t) = V_L + (V_o - V_L)(1-e^{-t/\tau_f}) \quad (D_1+D_2)T_s \le t < T_s \tag{4c}$$

where τ_f denotes the time constant of the low-pass R_fC_f filter. V_g *and* V_o are the input and the output voltage, respectively. D_1 and D_2 are the duty ratios for the first and second sub-interval, respectively. T_s represents the switching period. In particular, at $t = D_1T_s$, $V_f(t) = V_H$, where V_H is the high threshold voltage. Hence, eqn (4a) becomes:

$$V_H = V_{f0} + (V_g - V_{f0})(1-e^{-T_1/\tau_f}) \tag{5a}$$

Likewise, at $t = (D_1+D_2)T_s$, $V_f(t) = V_L$, where V_L is the low threshold voltage. Hence, eqn (4b) becomes:

$$V_L = V_He^{-T_2/\tau_f} = V_{fo}e^{-(T_1+T_2)/\tau_f} + V_ge^{-T_2/\tau_f}\left(1-e^{-T_1/\tau_f}\right) \tag{5b}$$

Finally, at $t = T_s$, $V_f(t) = V_{fo}$. Therefore, V_{fo} can be derived from eqn (4c) as follows.

$$V_{fo} = V_L + (V_o - V_L)(1-e^{-T_s/\tau_f}) = V_o - (V_o - V_L)e^{-T_s/\tau_f} \tag{5c}$$

For a particular output voltage V_o (assuming other circuit parameters are fixed), the values of V_H, V_L and V_{fo} can be obtained by solving the three independent equations, namely eqn (5a), (5b) and (5c). Notice that V_{fo} remains constant at all times with balanced loads. On the other hand, for the general case of unbalanced loads where the output voltage is different between the two outputs, $V_f(t)$ changes abruptly at the phase boundary due to an inherent load-induced coupling via the capacitor C_f. As depicted in Fig. 2, the average inductor current in the first output is increased while that of the second output is assumed to remain unchanged. Hence, the output voltage in the first output is increased with respect to that in the second output (i.e. $V_{oa} > V_{ob}$). The new initial value for the second output V_{fb0} is given by:

$$V_{fb0} = V_{fa1} - \Delta V_o \tag{6}$$

where V_{fa1} represents the final value of V_f at the end of the switching period corresponding to the first output and ΔV_o is the difference between the two output voltages (i.e. $\Delta V_o = V_{oa} - V_{ob}$, where $V_{oa} > V_{ob}$). The feed-forward voltage V_f experiences a voltage drop of ΔV_o at the phase boundary when the SIDO converter switches from the first output to the second one. Based on eqn (5c), V_{fa1} can be written as:

$$V_{fa1} = V_{oa} - (V_{oa} - V_L)e^{-T_s/\tau_f} \tag{7}$$

By substituting (7) into (6), we have

$$V_{fb0} = V_{oa} - (V_{oa} - V_L)e^{-T_s/\tau_f} - \Delta V_o \tag{8}$$

Since $\Delta V_o = V_{oa} - V_{ob}$, V_{fb0} can be re-expressed as:

$$V_{fb0} = V_{ob} - (V_{oa} - V_L)e^{-T_s/\tau_f} \tag{9}$$

By comparing (9) with (5c), it can be seen that $V_{fb0} < V_{f0}$ since $V_{oa} > V_o$ and $V_{ob} \cong V_o$ (assume minimal cross-regulation). It is important to note that V_{fb0} is a function of both V_{oa} and V_{ob}.

Consequently, an increase in the first output voltage will unavoidably affect the second output by reducing its initial voltage V_{fb0}. In addition, it can be shown that a smaller V_{fb0} actually causes the second output voltage to rise. From eqn (5a), the first sub-interval T_{1b} for the second output is given by:

$$T_{1b} = \tau_f \ln\left(\frac{V_g - V_{fb0}}{V_g - V_H}\right) \tag{10}$$

The input voltage V_g, the high threshold voltage V_H and the time constant τ_f remain constant for the second output. The only variable in (10) is V_{fb0}. Hence, a smaller value of V_{fb0} will lead to a larger value of T_{1b}. Further, the first-order derivative of V_o with respect to T_1 (i.e. dV_o/dT_1) can be derived from eqn (2) which is given by:

$$\frac{dV_o}{dT_1} = \frac{2T_1 V_g R_{LOAD}(V_g - V_o)}{4LT_s V_o + T_1^2 V_g R_{LOAD}} \tag{11}$$

Since $(V_g - V_o) > 0$ for a buck converter, $dV_o/dT_1 > 0$ which means that an increasing value of T_{1b} will always result in a higher value of V_{ob}. In other words, an increase in the first output voltage will cause an unwanted increase in the second output voltage. By substituting T_{1b} from (10) into (2) and solving for V_{ob}, a new value of the second output voltage can be estimated. The effect of this cross-regulation can also be visualized by using simple geometry. In Fig. 2, at $t = 1.5T_s$, the load-induced AC coupling reduces the initial voltage for the second output, i.e. $V_{fb0} < V_{f0}$. Given the same high threshold voltage V_H, a smaller initial voltage implies that it will take longer for V_f to reach the high threshold, i.e. $T_{1b} > T_1$. This results in a higher inductor peak current ($I_{pkb} > I_{pk}$) as I_L and V_f are in phase, thereby increasing the average inductor current (or load current) for the second output. For a fixed load resistance, a larger load current causes the output voltage to increase. The cross-regulation phenomenon is also verified experimentally. Fig. 3 shows the measured waveforms for a 150 mA load current increase in the first string.

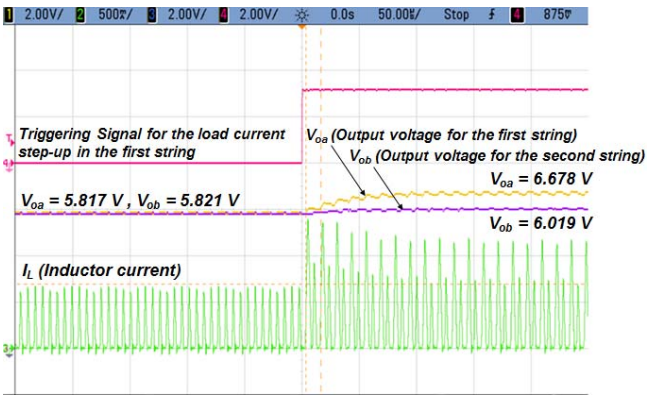

Fig. 3. Measured transient waveforms for a 150 mA load current increase in the first string.

The measured steady-state output voltage of the second (unchanged) string before and after the load transient in the first string are 5.821 V and 6.019 V. The output voltage in the second string changes by 198 mV due to a 150 mA load increase in the first string. Hence, the measured cross-regulation $\Delta V_{ob}/\Delta I_{LEDa}$ is 1.320 mV/mA. Fig. 4 shows the measured waveforms for the opposite case in which the load current in the first string is reduced by 150 mA.

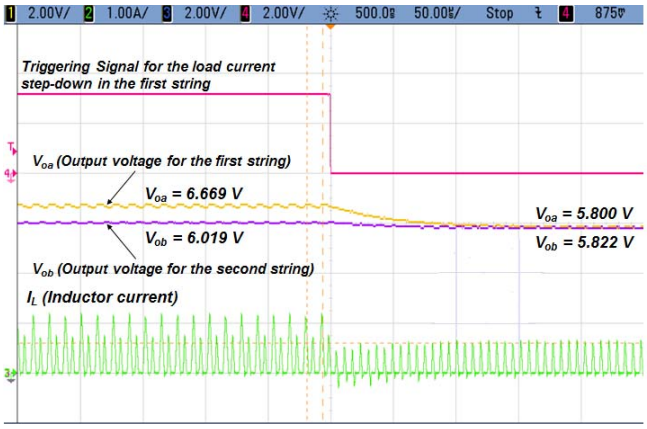

Fig. 4. Measured transient waveforms for a 150 mA load current reduction in the first string.

The output voltage of the second string changes by 197 mV due to the 150 mA load transient in the first string. The measured cross-regulation $\Delta V_{ob}/\Delta I_{LEDa}$ is 1.313 mV/mA. The experimental results confirm that there is serious cross-interference between the two outputs in conventional quasi-V^2 SIDO converter.

III. RESET-SENSING QUASI-V^2 SIDO CONVERTER

To substantially mitigate the cross-regulation, a reset-sensing quasi-V^2 SIDO buck converter for regulating the DC current in each of the two independently-driven outputs is proposed as shown in Fig. 5.

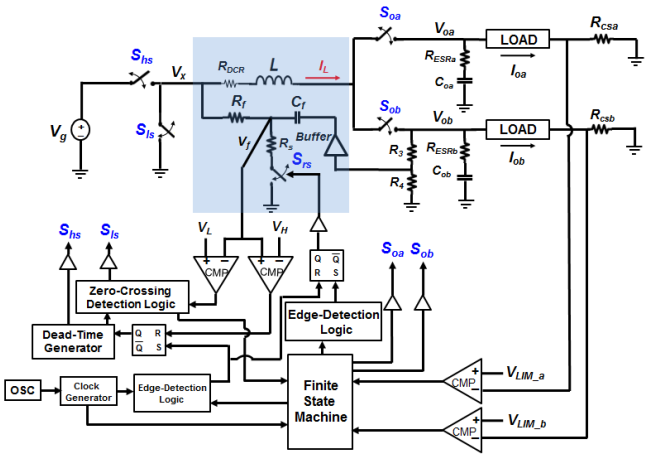

Fig. 5. System architecture for the proposed reset-sensing quasi-V^2 SIDO buck converter.

The output of the low-pass filter V_f is tied to ground via a current-limiting resistor R_s and a reset-sensing MOSFET S_{rs}. This additional MOSFET is ON only during the third sub-interval (idle phase) in DCM which fully discharges the state node V_f to zero volts. A key feature of the proposed circuit is that V_f is periodically reset to zero at the end of every switching phase, so-called "reset-sensing", which provides the necessary isolation between the two neighboring outputs. No residual energy is accumulated in the RC filter at the end of each switching phase. Also, the feedback voltage from either one of the two strings is connected to the negative terminal of C_f. This additional feedback loop eliminates the undesirable load-induced coupling from the changing output to the low-pass RC filter. This ensures that the quasi-V^2 node V_f remains "undisturbed" by any load differentiation across the two strings. Fig. 6 shows the ideal waveforms of the proposed SIDO converter.

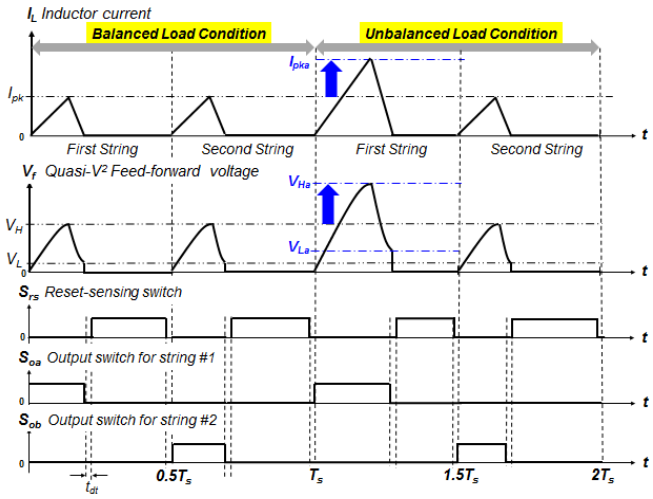

Fig. 6. Ideal waveforms for the proposed reset-sensing quasi-V^2 SIDO buck converter.

Notice that the waveform of V_f closely resembles that of I_L as both of them return to zero during the idle phase in DCM. As soon as V_f hits the low threshold voltage which indicates zero crossing of the inductor current, the output switch (either S_{oa} or S_{ob}) is OFF and after a small dead-time period t_{dt}, the "reset-sensing" switch S_{rs} is ON. Dead-time logic is required between the output switch and the "reset-sensing" switch in order to avoid an accidental short between the output node and ground. Fig. 6 shows that an increase in the inductor current of the first output will *not* affect that of the second unchanged output.

The underlying cause of the cross-regulation problem is that the initial voltage of one output is a function of the output voltage from the neighboring output. Eqn (9) shows that V_{fb0} is a function of V_{oa}. Mathematically, in order to eliminate the cross-regulation, V_{fb0} should be independent of V_{oa}. One simple solution is to reset the initial voltage to zero during the idle phase in DCM (i.e. $V_{fa0} = V_{fb0} = 0$). Therefore, by substituting $V_{fb0} = 0$ into (10), the first sub-interval for the second output T_{1b} is given by:

$$T_{1b} = \tau_f \ln\left(\frac{V_g}{V_g - V_H}\right) \tag{12}$$

Eqn (12) shows that the first sub-interval is independent of the initial voltage and is a function of only the high threshold voltage (assuming the other circuit parameters are kept constant). The proposed "reset-sensing" control scheme also leads to a much simplified analytical expression for either the high or low threshold voltage. By substituting $V_{f0} = 0$ into (5a), the high threshold voltage V_H can be re-expressed as:

$$V_H = V_g(1 - e^{-T_1/\tau_f}) \tag{13}$$

Likewise, the low threshold voltage V_L can be re-expressed as:

$$V_L = V_g e^{-T_2/\tau_f}\left(1 - e^{-T_1/\tau_f}\right) \tag{14}$$

By definition, the hysteretic window ΔV_{hsy} is the difference between the high threshold and low threshold voltage (i.e. $\Delta V_{hsy} = V_H - V_L$) and it must be non-zero [5]. By dividing (13) by (14), the ratio between V_H and V_L can be obtained as:

$$\delta = \frac{V_H}{V_L} = e^{\frac{T_2}{\tau_f}} \tag{15}$$

First, T_2 must be non-zero since $(V_g - V_o) > 0$ for a buck converter and hence, from eqn (3), $T_2 \neq 0$. Second, (T_2/τ_f) must also be non-zero. This implies that T_2 (or the switching period T_s) cannot be too small, compared with the time constant τ_f of the low-pass filter (where $\tau_f = R_f C_f$). This imposes a design constraint for the chosen values of R_f and C_f with respect to the switching frequency. In general, τ_f and T_s should differ by no more than an order of magnitude in order to ensure a finite hysteresis window. Fig. 7 contains a 3-D surface plot showing the relationship between the hysteresis window, the switching period, and the output current.

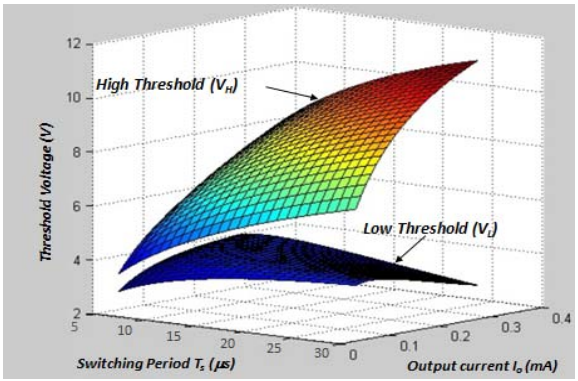

Fig. 7. 3-D plot showing the relationship between the hysteresis window, switching period and output current.

The proposed SIDO buck converter is implemented on an FPGA-based hardware prototype according to the design

specifications given in Table 1. For illustration purpose, it is used to drive two independent LED strings. A photo of the experimental setup with unbalanced LED loads is shown in Fig. 8. The experimental results are presented and discussed in Section IV.

Table 1 Design specifications of the proposed SIDO buck converter in DCM.

Design Parameter	Value	Unit
Input Voltage (V_g)	15	V
Switching Frequency (f_s)	83.33	kHz
Inductor (L)	15	μH
Output Capacitor (C_o)	10	μF
ESR of Output Capacitor (R_{ESR})	100	mΩ
Resistor in the First-Order Filter (R_f)	3	kΩ
Capacitor in the First-Order Filter (C_f)	1	nF
Duty Ratio of Idle Phase (D_3)	≥10	%

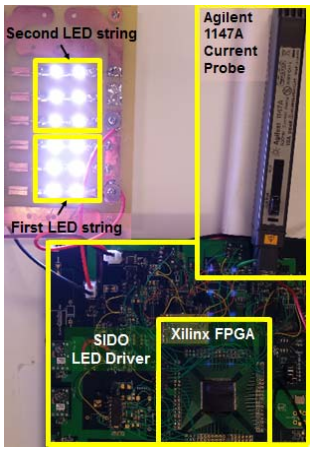

Fig. 8. Experimental setup of the proposed SIDO buck driver with unbalanced loads.

IV. EXPERIMENTAL RESULTS

The cross-regulation with the proposed SIDO driver is experimentally verified by increasing the LED current in the first string from 160 mA to 310 mA while that in the second string is unchanged at 160 mA. Fig. 9 shows the corresponding measured waveforms with a 150 mA load current increase in the first string. It shows that the output voltage in the second string remains largely undisturbed by the load transient in the first string. The steady-state output voltages for the second (unchanged) string V_{ob} before and after the load transient in the first string are measured to be 6.317 V and 6.327 V, respectively. Hence, the measured cross-regulation $\Delta V_{ob}/\Delta I_{LEDa}$ is around 0.067 mV/mA.

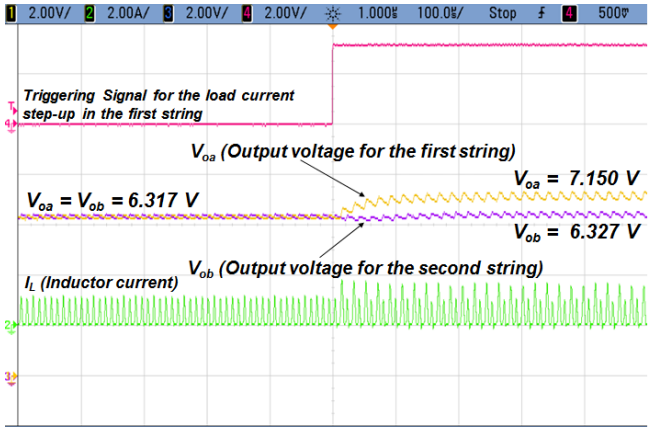

Fig. 9. Measured waveforms when the load current in the first string increases from 160 mA to 310 mA.

Fig. 10 shows the measured waveforms in which the load current in the first string is reduced by 150 mA.

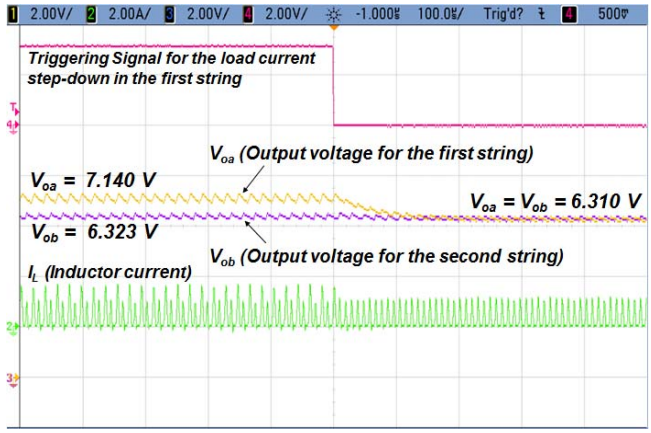

Fig. 10. Measured waveforms when the load current in the first string decreases from 310 mA to 160 mA.

Again, the output voltage in the second string remains largely unaffected by the load transient in the first string. The steady-state output voltages of the second (unchanged) string V_{ob} before and after the load transient in the first string are measured to be 6.323 V and 6.310 V, respectively. Hence, the resulting cross-regulation $\Delta V_{ob}/\Delta I_{LEDa}$ is 0.087 mV/mA. The system is shown to be stable after the load transient.

V. CONCLUSION

Cross-regulation has always been a major design challenge for SIMO converters. To resolve the cross-regulation issue in the original quasi-V^2 SIDO driver, this paper proposes a reset-sensing quasi-V^2 SIDO converter to significantly reduce the cross-regulation across the two outputs. It enables fully-independent current control in each of the two outputs which is especially useful for achieving precise luminous control and flexible color-mixing in a dual-string LED system. The key

features of the proposed SIDO system include the addition of a reset-sensing MOSFET to return the feed-forward sense voltage to zero volts at the end of every switching phase as well as the use of a feedback network to maintain a fixed DC offset for the RC filter regardless of any load changes in either string. The proposed circuit changes are simple to implement and facilitates scalability from SIDO to SIMO easily. It is shown that the proposed reset-sensing architecture gives a much simplified analytical expression for determining the high and low threshold values in a quasi-V^2 SIDO converter. The experimental results confirm the effectiveness of the proposed reset-sensing control scheme in minimizing the cross-regulation in a quasi-V^2 SIDO converter.

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