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Ballistic Transport in Monolayer Black Phosphorus Transistors

Fei Liu, Yijiao Wang, Xiaoyan Liu, Jian Wang, and Hong Guo

***Abstract*— We report a comprehensive theoretical investigation of ballistic quantum transport in monolayer black phosphorus (ML-BP) field-effect transistors (FETs). Our calculation is from tight binding atomistic model based on the nonequilibrium Green's function formalism. Several important device properties, including the drain current, ON–OFF ratio, transfer characteristic, short channel effects, intrinsic delay, and power delay product are determined against the channel length, transport direction, bias, and gate voltages. The atomistic simulation provides microscopic understanding of the device physics. Due to the anisotropic band structure of ML-BP, an orientation-dependent transport characteristic manifests itself in the major transistor properties. Comparing device performance in the zigzag and armchair direction (AD), we predict that transport along the AD has higher ON-state current and faster switching speed due to the lighter carrier effective mass. Comparing with ML MoS_2 FET, ML-BP FET produces higher current density and faster switching speed, but costs more switching energy. Double gated ML-BP FETs show promising device characteristics that fulfill the international technology roadmap for semiconductors requirements in the 10-year horizon.**

***Index Terms*— Ballistic transport, black phosphorus (BP), field-effect transistors (FETs).**

I. Introduction

THE 2-D layered material has been intensively investigated due to potential applications in electronic devices [1]–[3]. For transistor applications, suitable bandgaps and high carrier mobilities are the basic material properties that are required. Graphene has excellent mobility and flexibility but no bandgap, which is a major obstacle for applications in logic circuits [4]. Creating a bandgap in graphene is a challenge and a contemporary research topic. Alternative to graphene, the transition metal dichalcogenides (TMDCs) represent another set of 2-D layered materials; several of them have suitable bandgaps and are hotly perused as the channel material of field-effect transistors (FETs) [3], [5], [6]. So far, the theoretical intrinsic carrier mobility of the highly studied monolayer (ML) TMDC material MoS_2 is $\sim$300–400 $cm^2/V\,s$ at room temperature that is orders of magnitude smaller than that of intrinsic graphene [7], [8]. Experimentally, the measured mobility of TMDC is actually lower [9]–[11] than the theoretical prediction. Nevertheless, with the achievable mobility, TMDC FETs have shown good device performances [9], [12]–[15].

Very recently, a new 2-D material—the ML black phosphorus (BP), is obtained experimentally and applied to FET [16], [17]. Like graphene, BP is made of a single nonmetal element that makes it simpler than TMDC [16]–[19]. In the bulk 3-D crystalline form, BP has a direct bandgap of $\sim$0.3 eV with high mobility approaching 10^5 $cm^2/V\,s$. An ML-BP structure—the phosphorene, can be mechanically exfoliated and is stable at room temperature [17]. The puckered layer structure is formed by sp^3 hybridization of the atomic orbital of the phosphorus atoms. Importantly, ML-BP has a direct bandgap of 1.5–2.0 eV making it suitable for FET application [20]–[23]. Experiments have shown that the mobility of ultrathin BP of 5-nm-thick can reach 1000 $cm^2/V\,s$ [16]. Few layer phosphorene FETs were reported to have high-hole field effect mobility at 286 $cm^2/V\,s$ and an ON/OFF ratio of 10^4 [17].

The FET made of the ML-BP material is so new that many aspects of such devices have not been understood and warrant extensive investigation. More recently, the device performance of ML-BP FET is estimated by the top of barrier model [24]. In this paper, we report a comprehensive theoretical analysis of its ballistic quantum transport property. Our theory is based on self-consistently solution the Poisson equation and Schrödinger equation within the nonequilibrium Green's function (NEGF) formalism, using a tight binding Hamiltonian to describe the material property. The tight binding Hamiltonian reproduces accurately the correct band structure of the material in the low-energy regime that allows us to extract the effective masses in different directions. Several major device merits are determined against the channel length, transport direction, bias, and gate voltages, including the drain current, ON–OFF ratio, transfer characteristic, short channel effects, intrinsic delay, and power delay product (PDP). Due to the anisotropic band structure, device performance of ML-BP FETs in the armchair direction (AD) and zigzag direction (ZD) are found

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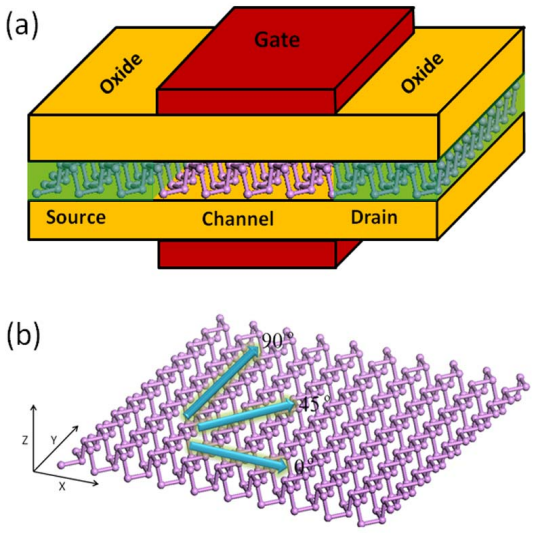

Fig. 1. (a) Device structure of the double gated ML-BP FET with HfO_2 as the gate insulator. FET is composed of the source, the intrinsic channel, and the drain, all of that are made of ML-BP. (b) Atomistic structure of ML-BP.

to be quite different in the ballistic limit. We also report the calculated scaling behavior of the ML-BP FET that can be compared with that of the MoS_2 FET. Our result indicates that ML-BP FETs fabricated along the AD provide a very interesting device having very competitive transistor characteristics. Comparing with the device performance of ML-BP FET with the requirements of ITRS 2013 for the 2024 horizon, we conclude that ML-BP FET is a good candidate in terms of the ON-state current, intrinsic delay, and PDP.

II. Device Model and Theoretical Method

We consider a double gated ML-BP FET shown in Fig. 1(a). A 2-nm-thick HfO_2 material with dielectric constant $\kappa \approx 25$ is used as the gate insulator. The FET is composed of n-type doped source and drain with a density of 7.0×10^{13} cm^{-2}, and an intrinsic channel under the gate. In the atomistic calculations (see below), the length of source or drain that is included in the simulation box is 10 nm; the channel length ranges from 5 to 15 nm. Outside the simulation box, the source/drain extends to infinity where bias voltage is applied and current is collected. Fig. 1(b) shows atomic structure of ML-BP. Due to its anisotropic band structure, anisotropic transport is expected. In particular, the transport direction can be along the x-axis which is the AD, or along the y-axis which is the ZD, as shown in Fig. 1(b). We apply the NEGF formalism to simulate the ballistic quantum transport properties of the FET [25], [26]. To account for the bias and gate potentials along the device channel, the Schrödinger equation and Poisson equation are solved self-consistently within NEGF. A 4-band tight-binding Hamiltonian is used to describe the ML-BP material [23], which can fit the low-energy band structures obtained by the highly accurate GW approximation. The 4-band tight binding Hamiltonian of ML-BP is given by

$$H = \sum_{\langle i,j \rangle} t_{i,j} a_i^\dagger a_j - q \sum_i V_i a_i^\dagger a_i \qquad (1)$$

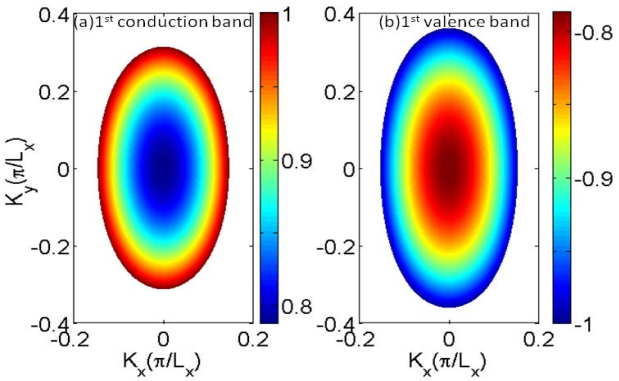

Fig. 2. (a) and (b) Contour maps of the conduction band and valence band around the Γ point with energy up to $|E| = 1.0$ eV, respectively.

where $a_i^\dagger (a_i)$ is the creation (annihilation) operator of electrons at site i, t_{ij} is the hopping parameter between the ith and jth sites including the third nearest neighbor, and V_i is the electrostatic potential at the ith site obtained by solving the Poisson equation. The Green's function of the system is computed by inverting the Hamiltonian matrix

$$G(E) = \left[(E + i0^+)I - H(k_t) - \Sigma_S(E, k_t) - \Sigma_D(E, k_t)\right]^{-1} \qquad (2)$$

where I is the identity matrix, Σ_S and Σ_D are the self-energies due to interactions between the scattering region and the source or drain electrodes, and k_t is the wave vector perpendicular to the transport direction. The transmission coefficient is given by

$$T(E) = \text{trace}\left[\Gamma_S(E, k_t) G(E, k_t) \Gamma_D(E, k_t) G^+(E, k_t)\right] \qquad (3)$$

where $\Gamma_{S,D} = i(\Sigma_{S,D} - \Sigma_{S,D}^+)$ is the line width functions of the source or drain electrode. The ballistic source-to-drain current is then obtained

$$I_D = \frac{G_0}{qW} \int dE \sum_{k_t} T(E, k_t)[f_S(E) - f_D(E)] \qquad (4)$$

where $G_0 = 2q^2/h$ is the conductance quanta where the factor 2 accounts for spin degeneracy, and W is the channel width. For comparison purpose, we have also applied a 3-band tight binding Hamiltonian [27] to simulate the device performance of MoS_2 FET.

III. Results and Discussion

Bulk BP has a layered structure in which the phosphorus layers are stacked together by van der Waals forces. Each puckered ML is formed by sp^3 hybridization. Band structures of various BP structures have been calculated by the density functional theory (DFT) and the GW method [20]–[23]. It has been found that ML-BP has a large direct bandgap in the range of 1.5–2.0 eV, and few-layer BP has anisotropic band structures. Fig. 2(a) and (b) shows our calculated contour maps of the conduction band and valence band around the Γ point with energy up to $|E| = 1$ eV, using the 4-band tight binding model [23] (1). From this result, we observe a clear anisotropic property and electron-hole asymmetry of ML-BP that is also observed in both DFT [20], [21] and

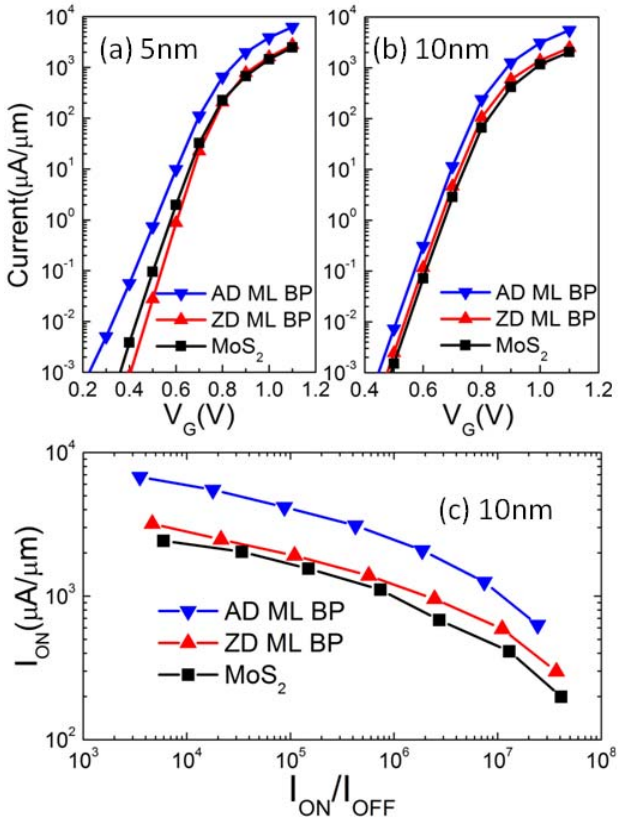

Fig. 3. (a) and (b) Drain current I_D versus gate voltage V_G for 5- and 10-nm n-type ML-BP FETs, respectively, in comparison with the ML MoS_2 FETs. (c) I_{ON} versus I_{ON}/I_{OFF} ratio for the 10-nm ML-BP FETs and MoS_2 FETs at drian bias $V_D = 0.5$ V.

GW [22], [23] calculations. We should notice that the tight binding model can fit the band structure well in a limited energy region, which is ~0.35 eV above the conduction band minimum (CBM) and ~0.25 eV below the valence band maximum. In our simulation of n-type ML-FETs, the Fermi level is ~0.14 eV above the CBM, therefore, the calculation can capture the main contribution of the first conduction band. The effective mass of electron and hole can be extracted from the calculated band structure and, going from the AD (x-axis) to the ZD (y-axis), the effective mass increases monotonously. Along the AD, the effective mass is smaller than that along the ZD, and we found $m_e = 0.17\ m_0$ and $m_h = 0.19\ m_0$ in AD; $m_e = 0.87\ m_0$ and $m_h = 1.17\ m_0$ in ZD, where m_0 is the bare mass.

Fig. 3(a) and (b) shows the calculated drain current I_D versus gate voltage V_G for ML-BP n-type FETs having 5- and 10-nm channels in comparison with that of ML MoS_2 FETs. Here, we chose MoS_2 FETs in the ZD that has promising performance for a fair comparison. Due to the anisotropic electronic structure of ML-BP, transport along AD has larger current than along ZD for the same V_G, especially for short channel 5-nm ML-BP FET shown in Fig. 3(a). Quantitatively, the 5-nm ZD transistor reaches only 41.2% of the current of AD transistor at $V_G = 1.0$ V. As a comparison, we studied the transport properties of MoS_2 FETs. At the gate voltage region $V_G < 0.9$ V the current of MoS_2 FETs sits

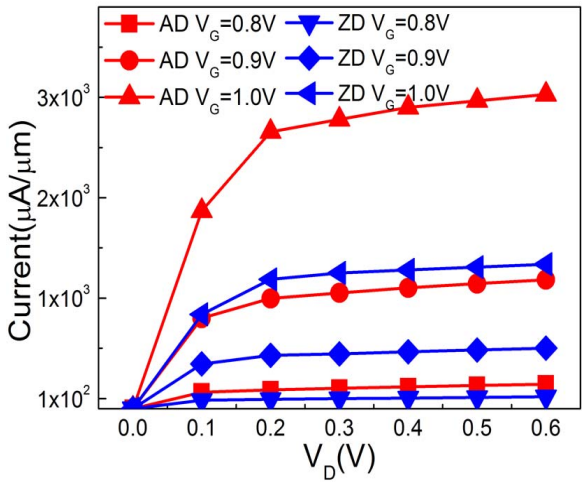

Fig. 4. Drain current I_D as a function of drain voltage V_D for 10-nm channel ML-BP FETs in AD and ZD at different gate voltages.

in between the AD and ZD ML-BP FETs. When the gate voltage reach $V_G = 1$ V the current of 5-nm MoS_2 transistor is roughly 91.0% of that in ZD ML-BP FETs. For 10-nm FETs, the current of MoS_2 FETs is always smaller than that of ML-BP FETs. The anisotropic transport property of the ML-BP device mainly comes from different effective masses of the first conduction band; electrons have smaller effective mass in AD that increases the direct source-to-drain tunneling. To further evaluate device performance, the I_{ON} versus I_{ON}/I_{OFF} characteristics is extracted and shown in Fig. 3(c) with bias window set at the supply voltage V_D; this result is helpful for selecting desirable devices for a particular I_{ON}. For I_{ON}/I_{OFF} ratio from three orders to eight orders, ML-BP FETs in AD can provide larger ON-state current compared with ML-BP FETs in ZD and the MoS_2 FETs.

Fig. 4 is the calculated source-to-drain current I_D versus the drain voltage V_D for different gate voltages of a 10-nm channel ML-BP FETs, showing a good device performance. The drain current density in AD can reach $3.1 \times 10^3 \mu A/\mu m$ at $V_G = 1.0$ V. The current in ZD, on the other hand, is lower by about $1.4 \times 10^3 \mu A/\mu m$, i.e., ~45.2% of that in AD. The ON-current of AD transistor at $V_G = 1.0$ V is also found to be larger than that of MoS_2 FETs. As the ON-state current of MoS_2 FET meets ITRS requirements for high-performance logic devices in the 10-year horizon [15], [28], the ML-BP FET is therefore likewise.

In the nanometer scale, short channel effects, such as drain-induced barrier lowering (DIBL) and high leakage current greatly degrade device performance. To investigate DIBL, in the OFF-state we set the drain current at 100 nA/μm according to the requirement of ITRS [28] 2013. Fig. 5 shows the calculated band profiles along the channel in the OFF-state of ML-BP FETs. We note that the effective barrier heights of ML-BP FETs along AD and ZD are different due to different effective masses. Since AD has smaller effective mass than ZD, it is easier for electron in AD to tunnel through the barrier, hence to obtain the same OFF-state current the barrier hight must be higher in AD than that in ZD, as shown Fig. 5(a). From this result, we observe a clear DIBL effect

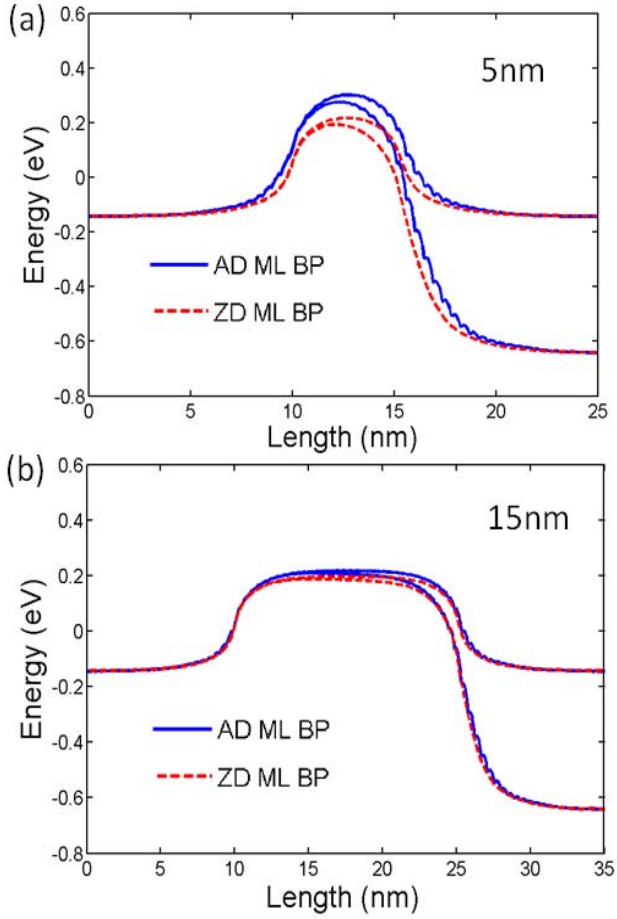

Fig. 5. Band profiles of ML-BP FETs in the OFF-state at drain voltage $V_D = 0$ and 0.5 V. (a) For 5-nm channel. (b) For 15-nm channel.

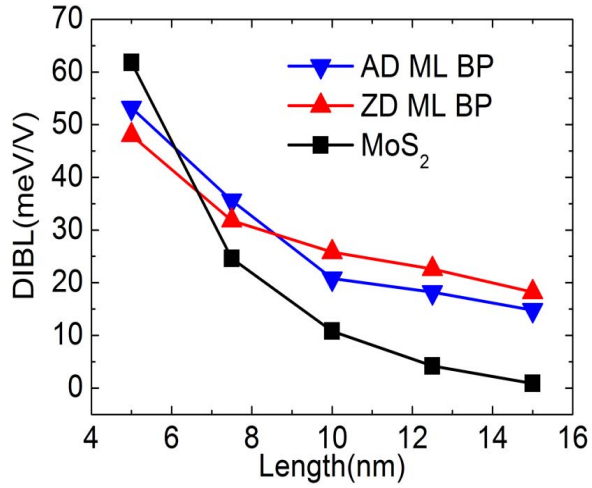

Fig. 6. Drain-induced barrier lowering effect as a function of channel length of ML-BP FETs and MoS_2 FETs.

when the drain voltage is increased from 0 to 0.5 V. The barrier drop is 26.6 and 24.0 meV in 5-nm channel transistor in AD and ZD, respectively. When the channel length is increased to 15 nm, the DIBL effect becomes insignificant, as shown in Fig. 5(b). In addition, the barrier drop in the 15-nm channel device in AD is 7.4 meV that is smaller than the 9.1 meV obtained for the ZD transistor. Fig. 6 compares DIBL

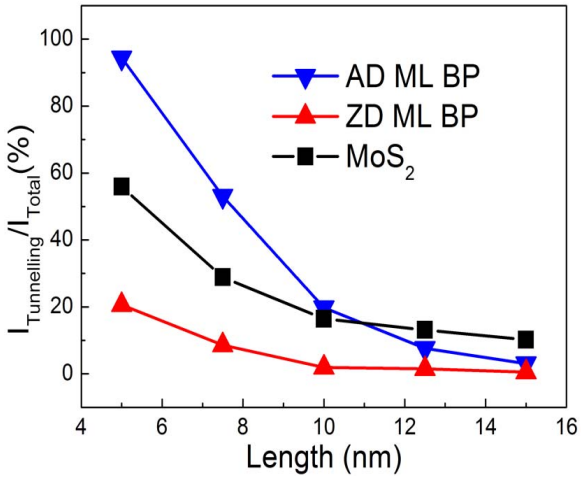

Fig. 7. Percentage of direct source-to-drain tunneling current of ML-BP FETs and MoS_2 FETs with different channel length in the OFF-state.

in ML-BP FETs having different channel lengths; DIBL effect is more pronounced for 5- and 7.5-nm devices in AD. When the channel length reaches 10 nm, the drain drop in AD becomes smaller than that in ZD. As far as the DIBL effect is concerned, we found MoS_2 FETs to have a much better characteristic as its DIBL decreases more quickly with the increasing of channel length. For instance, we found that for the 15-nm channel MoS_2 FETs the barrier drop is only 0.4 meV.

In nanotransistors, the direct tunneling current increases dramatically with decrease of the channel length that degrades device performance. Here, we compare this short channel effect between ML-BP and MoS_2 FETs by calculating the OFF-state tunneling. In the OFF-state, the total current is comprised of two contributions, e.g., by direct quantum tunneling and by thermionic transport. They are obtained from the following formula [29]:

$$G = G_0 \int dE\beta T(E) e^{\beta(E-E_f)} f^2(E-E_f), \quad \beta = (k_B T)^{-1}. \tag{5}$$

Thermionic and tunneling currents are separated by the top of the barrier. For a 5-nm ML-BP channel in AD, we found that the total current is mainly contributed by direct quantum tunneling, at about 94.4%. On the other hand for the same channel length in ZD, the direct tunneling current contributes only 20.6% to the total. The difference can be attributed, again, to the different effective mass along the two directions. As mentioned above, the effective mass in AD is only 19.5% of that in ZD, hence quantum tunneling is much easier in AD. With the increase of channel length, the direct quantum tunneling deceases rapidly, as shown in Fig. 7. The percentage of direct tunneling current is 5% and 0.5% of the total for ML-BP FETs in AD and ZD at 15 nm, respectively. In comparison, the quantum tunneling of 5-nm MoS_2 FET accounts for 56.0% of the total OFF-state current that lies between the AD and ZD BP transistors; this is expected since the electron effective mass of MoS_2 is in between that of AD and ZD ML-BP. It is interesting to note that when channel

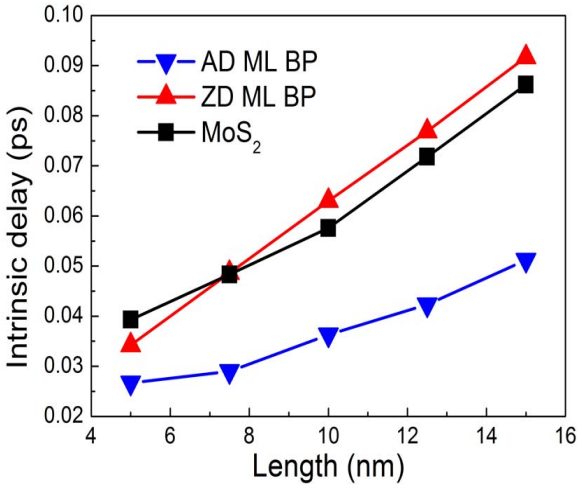

Fig. 8. Intrinsic delay as a function channel length of ML-BP FETs and MoS_2 FETs.

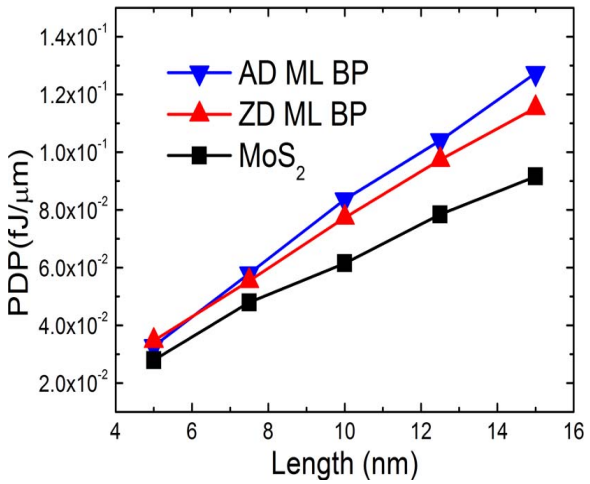

Fig. 9. Power delay as a function channel length of ML-BP FETs and MoS_2 FETs.

length reaches 12.5 nm, the percentage of direct tunneling in MoS_2 FET is actually larger than both AD and ZD ML-BP.

For transistor technology, intrinsic delay is an important device parameter. Fig. 8 shows the estimated intrinsic delay of ML-BP FETs in AD and ZD compared with the MoS_2 FET. The intrinsic delay is estimated [15] by $\tau = (Q_{\rm ON} - Q_{\rm OFF})/I_{\rm ON}$, where $Q_{\rm ON}/Q_{\rm OFF}$ is the charge in the channel at the ON/OFF-state, and $I_{\rm ON}$ is ON-state current. Again, the OFF-state is chosen at $I_{\rm OFF} = 100$ nA/μm. As shown in Fig. 8, ML-BP FETs in AD shows the smallest delay that means the fastest switching speed, in comparison with ZD transistors and MoS_2 FETs. Increasing the channel length makes the difference of the intrinsic delay even larger. For FETs with 5-nm channel, we estimate a switching speed of ZD transistor to be 78.1% of the AD transistor. Increasing to 15 nm, the switching speed of ZD is only 55.8% of AD. This difference is again due to the difference of the effective masses. To obtain the same OFF-state current, a larger gate voltage must be applied in ZD that gives rise to more carriers accumulated in the channel. At the same time, the ON-state current of ZD is smaller than that in AD. Hence, it is natural to expect a larger time scale for turning ON/OFF the ZD transistors that is what we have obtained in Fig. 8.

Power dissipation is a major concern for high performance logic applications. To this end, we have estimated the PDP per device width of ML-BP FETs and MoS_2 FETs. This quantity is determined by PDP $= (Q_{\rm ON} - Q_{\rm OFF})V_D$ and results are shown in Fig. 9. We found that even though the switching speed of AD transistor is faster, it costs more switching energy when the channel length is beyond 7.5 nm. There are fewer carriers in AD transistors, but the unit cell width in AD is 3.27 Å—smaller than the 4.43 Å of ZD, hence the electron density per width in AD is larger that costs more switching energy per width. As compared with MoS_2 FETs, ML-BP FETs are found to cost more switching energy in all channel lengths we investigated, as shown in Fig. 9. Hence, MoS_2 FETs have better PDP merit.

Finally, in Table I, we compare device performance of 7.3-nm ML-BP FETs with the ITRS requirements for high performance logic devices in the 2024 horizon, and we conclude that they have promising characteristics. $I_{\rm ON}$, the intrinsic switching delay and PDP of ML-BP FETs can fulfill the ITRS requirements for the 2024 horizon, for both ADs and ZDs. In AD, the switch speed is 21 times faster and the PDP is only 27.2% of the ITRS requirement for the 2024 horizon.

TABLE I
PERFORMANCE METRICS OF ML-BP FETS AND THE ITRS REQUIREMENTS FOR HIGH PERFORMANCE LOGIC DEVICES IN THE 2024 HORIZON

	Node 2024	AD	ZD
L_G(nm)	7.3	7.3	7.3
V_D(V)	0.69	0.69	0.69
EOT(nm)	0.49	0.49	0.49
$I_{OFF}(\mu$ A/μ m)	0.1	0.1	0.1
$I_{ON}(\mu$ A/μ m)	1170	6343	3800
τ(ps)	0.451	0.022	0.037
PDP(fJ/μ m)	0.36	0.098	0.097

IV. CONCLUSION

In this paper, we have made a comprehensive investigation of ML-BP FET within the ballistic quantum transport model, and compared the results with those of the TMDC-based MoS_2 FETs that have received extensive study in the literature. Our calculation is from tight binding atomistic models using NEGF where the material Hamiltonian is obtained by fitting to the local energy electronic structure of the material calculated from first principles. Several major device merits were calculated against the channel length, transport directions, bias, and gate voltages, including the drain current, ON–OFF ratio, transfer characteristics, short channel effects, intrinsic delay, and power delay.

The NEGF atomistic calculation allows us to understand the properties in the quantum ballistic transport regime at the microscopic level. Due to the anisotropy of the electronic structure of ML-BP, the device performance of ML-BP FETs substantially depends on the transport direction. A smaller carrier effective mass in AD leads to faster switching speed and better ballistic $I_{\rm ON}$ performance than transport in the ZD.

Compared with MoS_2 FET, the advantage of ML-BP is the higher ON-current and faster switching speed. On the other hand, for channel lengths longer than 7.5 nm, drain-induced barrier lowering effect is more significant in ML-BP FETs than in MoS_2 FET; it will also cost more energy to switch ML-BP FET than that needed for MoS_2 FETs. As compared with the requirements of ITRS, ML-BP FETs show promising device characteristics for high performance logic application in the 10-year horizon. Finally, we should mention that our simulated ML-BP FETs have well doped source and drain, while existing experimental devices were of Schottky barrier type. To realize the high performance limit of the theoretical simulation, an important task is to develop Ohmic metal-BP contacts. Further, atomistic simulation should assist this research direction.

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