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Author(s)	Chen, J; Xu, J; Liu, L; Lai, PT
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Improved performances of metal-oxide-nitride-oxide-silicon memory with HfTiON as charge-trapping layer

J. X. Chen,[1] J. P. Xu,[1,a)] L. Liu,[1] and P. T. Lai[2,a)]
[1]*School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, People's Republic of China*
[2]*Department of Electrical and Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong*

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The properties of HfTiON as charge-trapping layer of metal-oxide-nitride-oxide-silicon memory are investigated, and effects of different Hf/Ti ratios in HfTiON films on the physical and electrical characteristics are analyzed. It is found that the higher the Ti content, the higher is the charge-trapping efficiency, thus, larger memory window and higher program/erase speeds. However, excessive Ti can diffuse to the HfTiON/SiO_2 interface and cause the formation of a Ti-silicate interlayer, which deteriorates the retention of data. Experimental results indicate that the device with a Hf/Ti ratio of ~1:1 can give a good trade-off between performance and reliability. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4829880]

Recently, metal-oxide-nitride-oxide-silicon (MONOS) charge-trapping flash memory has attracted much concern for the next-generation nonvolatile memory application due to its advantages of low operating voltage, feasibility of scaling, and simple fabrication process.[1–3] Various high-κ dielectrics, e.g., HfO_2,[4,5] Ta_2O_5,[6] ZrON,[7] LaON,[8] and HfGdO,[9] have been investigated as the charge trapping layer (CTL) to improve the performance and reliability. Among these high-κ materials, HfON, due to its high k value (~22), good thermal stability with SiO_2, deep conduction-band edge relative to SiO_2 (~1.5 eV), and deep trap energy (~1 eV),[10–12] was listed in the ITRS [The International Technology Roadmap for Semiconductors, 2009, www.itrs.net.] to replace the conventional Si_3N_4 for further down-scaling. The main problem of HfON is its inferior trapping efficiency as compared to Si_3N_4.[13,14] Several approaches, including band engineering[15] and implant of dopants into HfON,[16] have been proposed to obtain a larger memory window. On the other hand, TiO_2 is a high-κ material ($\kappa > 80$),[17] which is very beneficial for further down-scaling. Also, it has been reported that incorporation of Ti atoms into the rare earth dielectric films as CTL, e.g., $HfTiO_4$,[18] $YbTiO_5$,[19] and Dy_2TiO_5,[20] can improve the physical and electrical properties of memory devices. In view of the above points, we investigated the physical and electrical properties of HfTiON as the CTL of MONOS flash memory. Furthermore, the Hf/Ti ratio in the HfTiON film was optimized by considering a trade-off between memory performance and reliability.

Both metal-nitride-oxide-silicon (MNOS) and MONOS capacitor memories were fabricated on p-silicon wafers with a resistivity of 1–10 Ω·cm. After the standard Ratio Corporation of America cleaning, a 3.1-nm SiO_2 film was thermally grown at 900 °C in dry O_2. Next, a high-κ HfTiON film was deposited as CTL by reactive co-sputtering method using Denton Vacuum Discovery Deposition System at room temperature (RT). In order to investigate the effects of Ti content on the charge-trapping properties of HfTiON, different Ti contents were incorporated into HfON by co-sputtering of Hf and Ti targets in a mixed ambient of $Ar/N_2/O_2 = 12/15/3$ at a fixed Hf-target RF power of 28 W and different Ti-target DC powers (6.7 W, 14.9 W, and 29.6 W, respectively), and the corresponding samples were denoted as HTON1, HTON2, and HTON3 with an atomic Hf/Ti ratio of 3.31:1, 1:1.07, and 1:2.97, respectively, determined by normal x-ray photoelectron spectroscopy (XPS) analysis. All the HfTiON films had roughly the same thickness of 6.8 nm. Rapid thermal annealing was performed at 500 °C for 1 min in N_2 ambient to improve the quality of the high-κ dielectric film. Subsequently, a 13.2-nm Al_2O_3 as blocking layer was deposited by atomic layer deposition using $Al(CH_3)_3$ as precursor and H_2O as oxidant at 300 °C in an Oxford OpAL System. The corresponding MNOS capacitors without Al_2O_3 were also prepared for constant-current stress (CCS) measurements. Finally, Al was thermally evaporated and patterned as gate electrode and also as back electrode, followed by a forming-gas annealing in H_2/N_2 (5% H_2) at 300 °C for 20 min.

The physical and electrical characteristics of the HfTiON CTL were thoroughly investigated. The film thickness was measured by multi-wavelength ellipsometry and confirmed by transmission electron microscopy (TEM) images. The elemental composition and chemical bonding were analyzed by XPS using a monochromatic Al K_α (1486.7 eV) source. Capacitance-voltage (C-V) and CCS measurements were carried out using HP4284A precision LCR meter and HP4156A precision semiconductor parameter analyzer, respectively. The flat-band voltage (V_{FB}) of the samples was extracted by assuming $C_{FB}/C_{OX} = 0.5$ (C_{FB} and C_{OX} are the flat-band and oxide capacitances, respectively, determined from 1-MHz high-frequency C-V curve).

Fig. 1 shows the cross-sectional TEM images of the MONOS capacitors after annealing the stacked gate dielectrics. The thickness of the HfTiON films is evaluated to be 6.8 nm, 6.7 nm, and 6.9 nm for the HTON1, HTON2, and

a)Authors to whom correspondence should be addressed. Electronic addresses: jpxu@mail.hust.edu.cn and laip@eee.hku.hk.

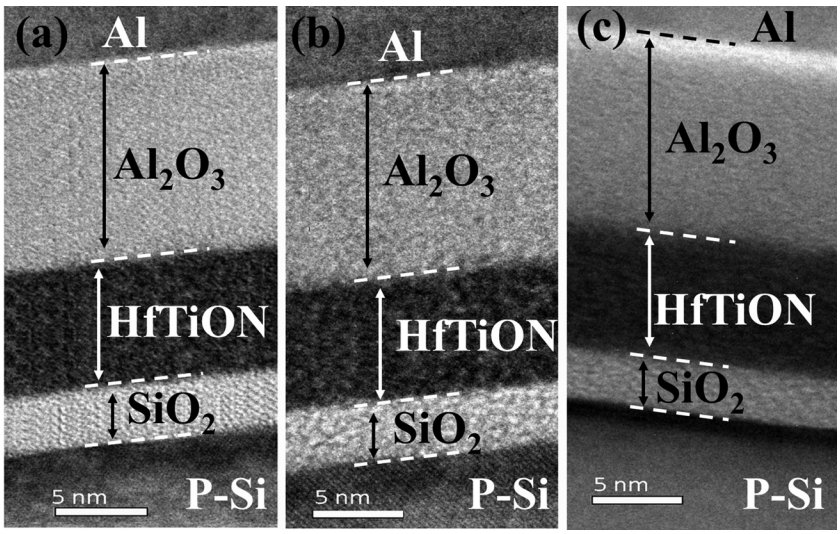

FIG. 1. Cross-sectional TEM image of $Al/Al_2O_3/HfTiON/SiO_2/Si$ structure. (a) HTON1 sample, (b) HTON2 sample, and (c) HTON3 sample.

HTON3 samples, respectively. It can be observed that the $HfTiON/SiO_2$ interface is clearer and sharper for the HTON1 sample than the HTON2 and HTON3 samples, indicating better interface quality for the HTON1 sample. Moreover, no evidence of structural phase transformation can be found as the Ti content increases, i.e., all the HfTiON films should be amorphous. The XPS spectra of Hf 4*f*, Ti 2*p*, and O 1*s* are shown in Fig. 2. It can be seen that the chemical bonding of the three samples is almost the same, independent of the Ti-target sputtering power. Using Gaussian fitting, the Hf 4*f* and Ti 2*p* spectra can be decomposed into two and three sub-peaks, respectively. As shown in Fig. 2, the peak binding energies located at around 18.3/16.6 eV for Hf $4f_{5/2}$/Hf $4f_{7/2}$ and 464.0/458.3 eV for Ti $2p_{1/2}$/Ti $2p_{3/2}$ are assigned to be HfON[21] and TiON, respectively. This is fully in agreement with our previous investigation.[22] Moreover, Ti 2*p* shows a peak binding energy at 460.0 eV, which should be attributed to Ti silicate.[23] In fact, as shown in Fig. 2(c), for TiON films deposited on SiO_2 with the same Ti-target DC power and deposition ambient as the HfTiON films, the same peak at 460.0 eV is also observed, which should correspond to Ti-Si bonds and is the precursor of the Ti silicate formed during the subsequent post-deposition annealing.

To further confirm the composition of the HfTiON films with different Ti contents, the O 1*s* spectrum which can be decomposed into three sub-peaks is examined, as shown in Fig. 2(d). The three peaks appeared at 530.0 eV, 529.5 eV, and 531.6 eV correspond to HfON, TiON, and Ti silicate, respectively. The peak binding energy for Ti silicate agrees with that reported by Sarkar *et al.*[24] From Figs. 2(b) and 2(d), it can be seen that the peak intensity corresponding to Ti silicate increases as Ti content increases, suggesting that more Ti incorporation in the HfTiON film leads to thicker interfacial layer.

The difference in charge-trapping characteristics of the HfTiON films with different Hf/Ti ratios is examined by the CCS method. A constant current of 10 $\mu A/cm^2$ or 20 $\mu A/cm^2$ is applied to the gate electrode of the MNOS capacitors for 1 s, respectively. The trapped charge centroid (X_t) and the trapped charge (Q_{trap}) extracted from the CCS measurement are given as[25]

$$X_t = t_{stack}\left(1 - \frac{\Delta V_{-g}}{\Delta V_{+g}}\right)^{-1}, \tag{1}$$

$$Q_{trap} = \frac{\varepsilon_0 \varepsilon_{stack}}{t_{stack}}\left(1 - \frac{\Delta V_{-g}}{\Delta V_{+g}}\right), \tag{2}$$

where X_t is measured from the Al/HfTiON interface to the $HfTiON/SiO_2$ interface; ΔV_{-g} and ΔV_{+g} are the negative and positive gate-voltage shifts; t_{stack} and ε_{stack} are the physical thickness and equivalent dielectric constant of the $HfTiON/SiO_2$ stack, respectively. The extracted X_t and

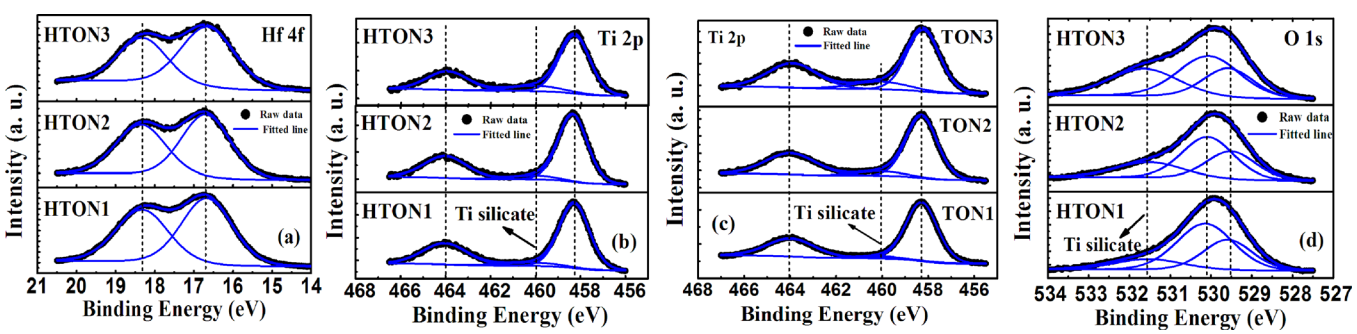

FIG. 2. Hf 4*f* (a), Ti 2*p* (b), and O 1*s* (c) core level XPS spectrum of HfTiON films with different Ti contents; Ti 2*p* (c) core level XPS spectrum of the as-deposited TiON film under the same Ti-target DC power and deposition ambient as HfTiON deposition. The TON1, TON2, and TON3 are corresponding to HTON1, HTON2, and HTON3, respectively.

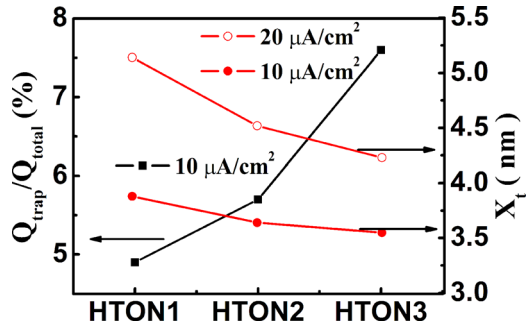

FIG. 3. X_t and Q_{trap}/Q_{total} under the constant-current stress for HfTiON MNOS capacitors with different Ti contents.

Q_{trap}/Q_{total} for the HfTiON films with various Ti contents are shown in Fig. 3. The charge-trapping efficiency (defined as Q_{trap}/Q_{total}) is increased as the incorporated Ti increases, indicating that adding Ti atoms into the HfON film can effectively improve the charge-trapping efficiency. Also as shown in Fig. 3, the X_t moves toward the HfTiON/SiO_2 interface as the constant-current stress increases, suggesting that the injected electrons tend to fill the traps near the Al/HfTiON interface first, which is beneficial for the retention characteristics by suppressing electrons tunneling back to the silicon substrate.[12]

Fig. 4(a) is the memory window of the samples when HfTiON with different Ti contents is used as CTL. The largest window of 4.8 V is achieved for the HTON3 sample, as compared to 3.5 V and 4.3 V for the HTON1 and HTON2 samples, respectively, under program/erase (P/E) voltages of +/−13 V for 1 s. Obviously, the more the Ti incorporation, the larger is the memory window, further confirming the higher charge-trapping efficiency can be achieved for higher Ti content. In addition, the dielectric constant extracted from the accumulation capacitance (C_{OX}) of C–V curve (not shown here) is 18.6, 22.2, and 24.8 for the HTON1, HTON2, and HTON3 samples, respectively, indicating that the dielectric constant of the HfTiON film increases with the Ti content.[26] As a result, the voltage drop across the tunnel oxide is larger for the HTON3 sample than the other two samples, inducing a higher electric field across the tunnel layer, and thus more electrons injected to the HfTiON CTL. Thus, a reasonably high Ti content in the HfTiON CTL can improve the storage capability and injection efficiency of charges.

Fig. 4(b) is the transient P/E characteristic of the samples as a function of pulse width varying from 0.1 ms to 1 s. Under a P/E voltage of ±12 V for 1 ms, the HTON3 sample shows a V_{FB} shift of 2.73/−2.58 V, which is larger than 1.96/−1.82 V for the HTON1 sample and 2.32/−2.18 V for the HTON2 sample, i.e., highest P/E speed obtained for the HTON3 sample with the highest Ti content. This is attributed to higher charge-trapping efficiency and higher charge-injection efficiency. Moreover, no significant over-erase phenomenon is observed for all the devices, implying negligible hole trapping in the CSL.[27]

Fig. 5 is the retention characteristics of the samples under programming state (12 V for 1 s), measured at RT and 85 °C, respectively. The charge retention rate after 10^4 s is 89.0%, 85.8%, and 79.3% at RT, and drops to 69.4%, 64.2%, and 48.1% at 85 °C for the HTON1, HTON2, and HTON3

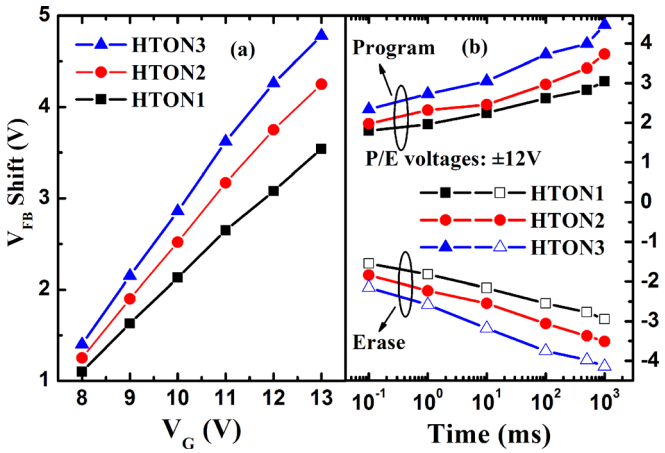

FIG. 4. Memory window of the MONOS capacitors under various gate biases (a) and transient P/E characteristics of the MONOS capacitors as a function of time (b).

samples, respectively. Apparently, charge loss rate is increased as the Ti content in the HfTiON CTL increases. From the results of the trapped charge centroid in Fig. 3, the memory device with higher Ti content should have better data retention because the trapped charge centroid is farther away from the HfTiON/SiO_2 interface. However, excessive Ti in the HfTiON film can diffuse to the HfTiON/SiO_2 interface,[23] leading to the formation of Ti silicate at the interface, and thus interfacial traps, which can increase the discharge of electrons through the trap-assisted tunneling mechanism. Moreover, the conduction-band offset relative to the silicon substrate decreases to less than 1 eV for the HfTiON film with a Hf/Ti ratio of 1:2,[28] and so the trapped electrons in the CTL can tunnel back to the silicon substrate more easily, causing the degradation of the retention characteristics. Further deterioration in the data retention at 85 °C indicates that more electrons in the HfTiON CTL can obtain sufficient thermal energy to go through the tunnel oxide to the Si substrate. Therefore, the Ti content in the HfTiON film should be carefully chosen to obtain a good trade-off between memory performance and reliability. For example, the HTON2 sample with a Hf/Ti ratio of 1:1.07 has a large memory window of 4.25 V at ± 13 V, high P/E speed with 2.32/−2.18 V at +/−12 V for 1 ms, and good data retention of 85.8% at room temperature and 64.2% at 85 °C.

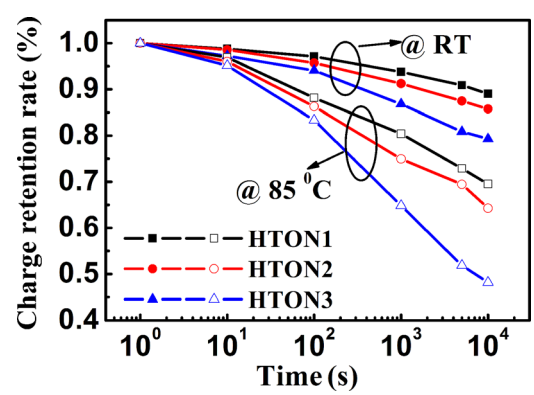

FIG. 5. Retention characteristics of HfTiON memory devices measured at RT and 85 °C.

TABLE I. Comparison of memory performances between the HfTiON CTL in this work and other HfXON CTL (X denotes other metal).

Stacked gate structure	Dielectric constant	Memory window (V)	Program/erase V_{FB} shift (V)	Retained charge after 10 yr (%)
$Al/Al_2O_3/HfTiON/SiO_2/Si$ (HTON2) (13.2/6.8/3.1 nm)	22.2	3.75 V@ ± 12 V, 1 s	2.32 V@ + 12 V, 1 ms −2.18 V@ − 12 V, 1 ms	85.8% @RT 64.2% @85 °C
$Al/Al_2O_3/HfYON/SiO_2/Si$ (Ref. 12) (20/12/3 nm)	NA	6.0 V@ ± 14 V, 1 s	2.9 V@ + 12 V, 1 ms NA	79%@RT
Al/ HfLaON/SiO_2/Si (Ref. 29) (15/3 nm)	17.6	3.25 V@ ± 12 V, 1 s	1.5 V@ + 10 V, 1 ms −1.1 V@ − 10 V, 1 ms	66%@RT

To demonstrate the potential of Ti incorporation into HfON, a comparison of memory performances between the HfTiON CTL in this work and other HfXON CTL[12,29] (X denotes other metal) is given in Table I. It can be seen that based on a comprehensive evaluation, the HfTiON CTL exhibits good memory performances and thus has promising application for nonvolatile memory devices.

The effects of Ti incorporation in HfON on the physical and electrical properties of MONOS capacitor memory with HfTiON as CTL are investigated. It is found that increasing the Ti content will induce higher charge-trapping efficiency, thus improving the memory window and P/E speeds. However, the data retention characteristics are degraded. Therefore, the Ti content in the HfTiON film needs to be optimized to achieve a good trade-off between performance and reliability. In this work, the MONOS memory with a Hf/Ti ratio of ∼1:1 in the HfTiON CTL exhibits a large memory window, high P/E speed, and good data retention. In summary, high-κ HfTiON with an optimal Ti content has high potential as the CTL of the MONOS memory device.

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