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Light programmable organic transistor memory device based on hybrid dielectric

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ABSTRACT

We have fabricated the transistor memory devices based on SiO₂ and polystyrene (PS) hybrid dielectric. The trap states densities with different semiconductors have been investigated and a maximum 160V memory window between programming and erasing is realized. For DNNT based transistor, the trapped electron density is limited by the number of mobile electrons in semiconductor. The charge transport mechanism is verified by light induced V_{th} shift effect. Furthermore, in order to meet the low operating power requirement of portable electronic devices, we fabricated the organic memory transistor based on AlO_x/self-assembly monolayer (SAM)/PS hybrid dielectric, the effective capacitance of hybrid dielectric is 210 nF cm⁻² and the transistor can reach saturation state at -3V gate bias. The memory window in transfer I-V curve is around 1V under +/-5V programming and erasing bias.

Keywords: organic transistor memory device, hybrid dielectric, light programmable

1. INTRODUCTION

Organic memory devices are known as the promising data storage devices for future electronic market since their flexibility and simplified fabrication process. There are various kinds of device structure have been demonstrated to realized memory function for transistor based device structure, including burring the floating gate into dielectric layer, using polymer electrets as charge trapping media^[1] and inserting metal nanoparticles into dielectric^[2] or semiconductor^[3]. In these device structures, polymer electrets is desirable to realize high performance memory devices due to its fast programming/erasing speed and good charge retention property^[4]. Baeg *et al.* has reported the pentacene transistor memory devices with different type of polymer electrets and most of the devices can be programmed within few ms and maintaining the programming states over 10000 s, in which the retention time of device based on PS could be close to 10⁸ s. Furthermore, Baeg *et al.* also investigated the relationship between charge retention properties and electrets band gap^[5]. Indicated that the charge injection efficiency is related to the band gap of electrets, the polymer that has larger band gap may need stronger voltage bias to fulfill trap states and at the same time has longer retention time due to the deeper charge trapping state for p-type OTFT. However rather than the polymer electrets materials, only little effort has been focused on the charge transport process correlated to the semiconductor. In order to further improve the device performance, detailed investigations are needed including the understanding of charge transfer and injection process, and comparing the device performance using various kinds of semiconductors. Furthermore, the operating voltage of transistor memory device is high because of relatively low permittivity of SiO₂, in order to reduce the power consumption of organic devices, the operating voltage of transistor memory devices should be largely reduced.

Most of reported polymer electrets devices are using pentacene as p-type semiconductor which has been well studied^[6]. Compare to pentacene, transistors made by dinaphtho-[2,3-b:2',3'-f]-thieno[3,2-b]thiophene (DNNT) has higher field-effect mobility that allows the device operating at higher frequency^[7]. More importantly, most of organic devices degraded fast in ambient condition that limits their commercial applications. One of the advantages of DNNT based devices is the stable electrical performance under ambient air^[8] or extreme high temperature condition^[9]. Someya *et al.* demonstrated that the mobility of DNNT transistor only degraded around 25% after 8 months stored in ambient air^[8]. However to our knowledge there is limited result reported about DNNT used for organic transistor memory devices.

In this work we fabricated the organic memory transistors based on PS electrets and using pentacene/DNNT as semiconductor. Pentacene based memory transistor shows threshold voltage shift in both positive and negative directions after programming/erasing bias. However, the DNNT devices can only be programmed by electrical bias while exposing to the external light source; otherwise the large band gap of DNNT prohibits the electrical bias induced electron

injection. This finding reveals that the charge injection efficiency in memory devices is dominated by the band gap of semiconductor. Finally a low voltage transistor memory device with high-k dielectric (aluminum oxide) is demonstrated and the programming voltage could be reduced for about 30 times.

2. EXPERIMENT

Heavily doped Si wafer with thermally growth 300 nm oxide layer is used as substrate, prior to deposition, the substrate was cleaned by DI water with soap, DI water, acetone and ISO propanol in sequence and dried with N₂ flow. PS (M_W=200,000) purchased from Sigma-Aldrich without further purification is dissolved into toluene solvent with 0.5 % weight ratio and then spun coated onto SiO₂ substrate with 6000 rpm for 1 min, then dried in N₂ atmosphere for 1 hour at 90 °C. 40 nm DNTT or pentacene were thermally evaporated after spin coating of PS in vacuum chamber with base pressure 5 × 10⁻⁷ torr, followed by 50 nm Ag top electrode defined by shadow mask with channel width 2 mm and channel length 0.1 mm. All the electrical measurements are carried out by two Labview controlled Keithley 2400 sourcemeters in oxygen and water free environment. The blue and red high power LED were purchased from Luxeon Star and calibrated by Newport power meter.

3. RESULT AND DISCUSSION

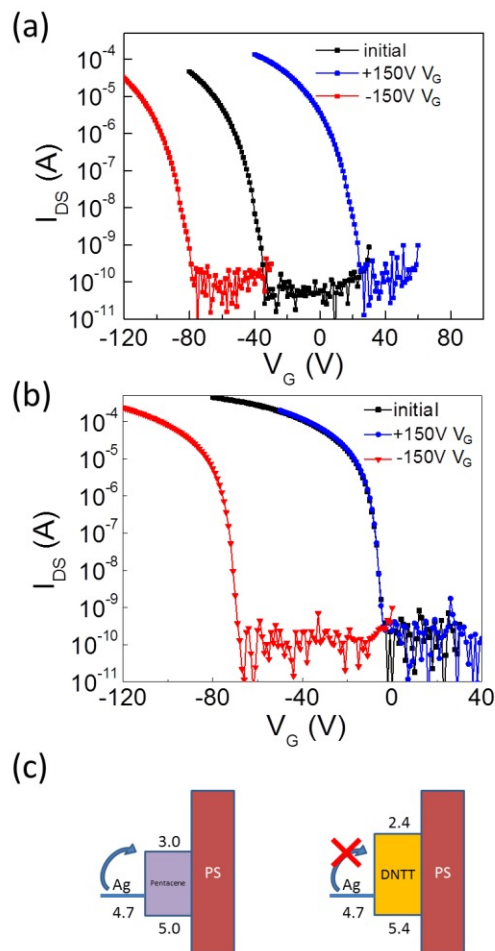


Figure 1. a, the transfer I-V of pentacene based PS electret memory transistor; b, the transfer I-V of DNTT based PS electret memory transistor programmed under dark; c, schematic diagram of band structure for pentacene and DNTT based PS electret memory device.

The memory transistor based on PS electrets with two different organic semiconductors, pentacene and DNTT are fabricated on SiO₂ substrates. On top of SiO₂, a spun coated PS is deposited with the thickness calculated about 30nm based on the solution concentration, spin speed and molecular weight of PS^[10]. For pentacene based transistor, the black curve in Fig. 1a is the transfer I-V without any previous bias condition. The field-effect mobility at saturation state is 0.35 cm² V⁻¹ s⁻¹ and the sub-threshold swing is 5 V decade⁻¹. Here the positive gate bias is defined as programming bias, and negative gate bias is erasing bias. The biasing period of programming and erasing are both 10 s. The blue and red curves in Fig.1a represent the device under +150 V programming or -150 V erasing gate bias, respectively. Due to the trapped charges stored in the PS layer, the threshold voltage of transistor can be largely shift to both directions while maintaining relative same device mobility and sub-threshold swing as summarized in table 1. The bidirectional shift of V_{th} on the basis of initial V_{th} value indicated that both holes and electrons can be trapped in the PS as one sign of traps can only shift the V_{th} in one direction by balancing the channel electrical field^[11]. And the traps charge injection efficiency is related to the band structure of device. In pentacene based transistor, holes can be trapped in PS because they are transport through the HOMO of pentacene and there is no injection barrier from drain-source Ag electrode to semiconductor. The trapped holes at PS/pentacene interface or in bulk PS prohibit the formation of channel that the transistor needs larger gate bias to balance the traps in order to reach accumulation state therefore the V_{th} left shift and the value of shift is proportional to number of traps^[1]. For electrons, it is more difficult to induce electrons in pentacene because the energy barrier between Fermi level of Ag electrode and LUMO of pentacene that requires a large gate voltage to overcome. Therefore a critical programming voltage exists for polymer electret devices that below that voltage, there is no obvious V_{th} change observed^[1].

Table 1

pentacene				DNTT			
	μ_{FET} (cm ² V ⁻¹ s ⁻¹)	V _{th} (V)	SS (V decade ⁻¹)		μ_{FET} (cm ² V ⁻¹ s ⁻¹)	V _{th} (V)	SS (V decade ⁻¹)
initial	0.352	-49	5	initial	0.972	-7.5	1.5
programming	0.536	45	5	programming	0.981	-7.4	1.5
erasing	0.559	-101	5	erasing	0.961	-73.2	1.6

On the other hand, In DNTT based transistor as shown in Fig. 1b, the device can only be erased by applying a negative gate bias but no positive V_{th} shift even under +150V gate bias. Similar as pentacene, holes can be easily induced from electrode through HOMO of DNTT and then being trapped at PS interface or in bulk PS. However as shown in Fig. 1c, the larger band energy difference between LUMO of DNTT and Ag electrode requires stronger electrical bias to overcome the barrier so that the electrons can be induced into DNTT. As a result, the density of the trapped electrons could be several orders lower than holes since mobile electrons are minority carriers in p-type DNTT semiconductor. In table 1, the +150V programming bias which is large for SiO₂ dielectric can only leads to negligible positive V_{th} shift of DNTT transistor. This result indicated that the current electrical bias is inadequate to overcome the charge injection barrier shown in Fig. 1c and no traps is being filled in PS electrets due to the lack of electron supply from the DNTT. Furthermore, once the DNTT transistor is being erased, the recovery is also difficult because the device needs electron to balance the hole traps that return neutral state, as a result the DNTT memory transistor become non-programmable.

In order to induce electrons into DNTT semiconductor, the device can be optically programmed rather than applying electrical bias. We firstly exam the absorption spectrum of DNTT thin film, 40 nm DNTT is thermally growth on a quartz glass and the absorbance is in Fig. 2a. The major absorption peak is located at 443 nm due to the large band gap of DNTT. Based on the result we choose wavelength peak at 447 nm with FWHM around 20 nm blue LED (shown in Fig. 2a) as light source to optically program the transistor. Fig. 2b shows programming/erasing sequence of the same DNTT memory transistor described above. Initially the device appears a typical p-type transfer I-V and the V_{th} is close to zero. Then a -150 V erasing bias is applied under dark so the V_{th} negatively shift due to the injection of hole traps in PS. After that the device is programmed at +150 V gate bias at the same time exposed under blue LED. Unlike Fig. 1b, a large number of positive V_{th} shift is observed under the programing bias and blue light illumination. The device can be erased to negative state after -150 V gate bias under dark and has very similar V_{th} value as the first time erasing. DNTT transistor behaves completely different from it being programed under dark that having large number of positive V_{th} shift after programed under light. The possible mechanism of this light programming effect can be explained as follow. The

incident photon from light source were absorbed by DNTT and generate excitons inside, and those excitons will dissociate into electrons and holes soon due to the applied gate bias^[12]. Holes will be collected by electrode and contribute to the drain-source current. Because the transistor is under positive gate bias, electrons generated by light are trend to accumulate at DNTT/PS interface and being trapped at PS interface or in bulk PS. With the aid of incident light, the DNTT based transistor memory device can be programmed since electrons are able to induce into DNTT. On the contrary, erasing process does not need assistance of light since there are plenty of holes in DNTT when applying a negative gate bias. As indicated in Fig. 2b, the bidirectional V_{th} shift is reversible and each of state can maintain for long time. Fig. 2c shows the charge retention performance of DNTT transistor memory device. We firstly applied a programming/erasing gate bias then measure the drain-source current at zero gate bias. The measurement was performed under dark and the on/off ratio after 10^4 s was maintaining almost the same as beginning.

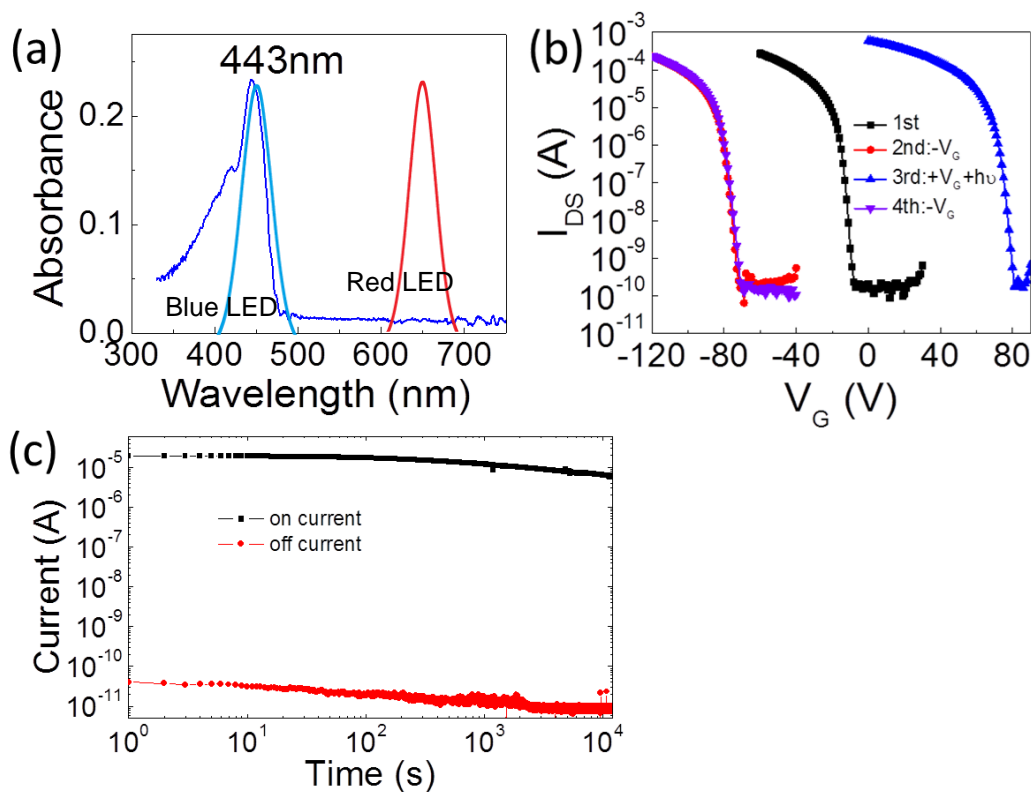


Figure 2. a, absorbance of DNTT thin film on quartz glass, and the emission spectrum of blue and red LED; b, transfer I-V of DNTT based memory transistor programmed with light and erased under dark; c, charge retention performance measured under dark.

In order to distinguish the light effect and bias effect on the V_{th} shift of transistor, two experiments are carried out in the following. Based on the absorption spectrum from Fig. 2a, we choose blue and red LED as light source to test the wavelength effect of light programmable V_{th} shift of transistor. The wavelength spectrum of commercial LED can be found in Fig. 2a. The absorbance of DNTT is mostly overlapped with blue LED emitting spectrum but shows almost zero absorbance for red LED. Fig. 3a exhibits the transistor response for different light source after programming. The DNTT/PS transistor was erased by -150 V gate bias before test. After that, the device was programmed at the same gate bias but simultaneously exposed under red or blue LED light source with intensity about 3.79 mW cm^{-2} . For red light irradiation, similar to the dark situation, only negligible V_{th} shift happened but for blue light, the shift of V_{th} is around 150 V. This result indicated that photon absorption of DNTT is the source of electron traps so that red light leads to no V_{th} shift. However only light irradiation cannot help to trap charges. When the device exposed under blue light but without applying gate bias, the transfer I-V did not shift (not shown). It proves that the light programmable V_{th} effect was the result of both light and electrical bias, light is able to generate free charges in semiconductor, but those charges cannot be trapped without gate bias. The observed transistor behavior under light and bias can be explained by the band structure shown in Fig. 3b. When a positive gate bias was applied on the transistor, because of the band bending of

DNTT, hole concentration is largely decreased, at the same time due to the charge injection barrier between Ag electrode and LUMO of DNTT, no electron accumulated in the dark either, therefore no positive V_{th} shift under dark. Once the channel region was exposed under blue light, the light generated excitons in DNTT was eventually dissociate to holes and electrons. Holes were contributed to the drain-source current in p-type channel, but electrons can be captured by trapping media such as PS under a positive gate bias^[13]. As a result, the V_{th} shows a large value of positive shift after device was programmed under light.

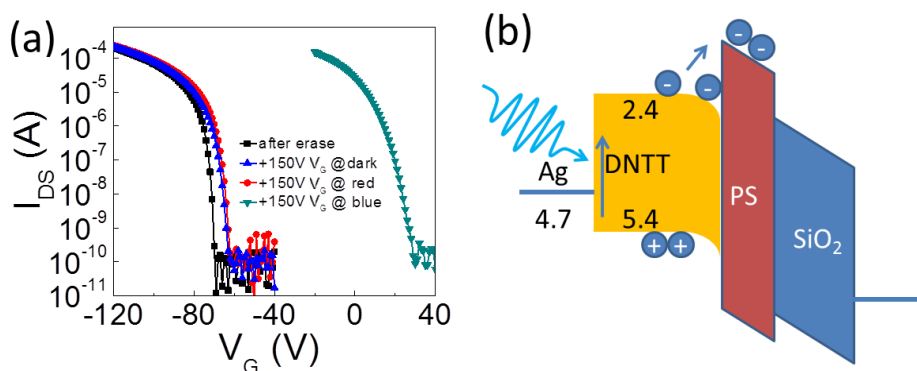


Figure 3. a, transfer I-V of DNTT memory transistor under different light source; b, schematic band structure of DNTT based memory transistor under positive gate bias and light irradiation

In addition to the light assisted programming transistor memory device, most of the hybrid dielectric of polymer electret devices is using SiO_2 as dielectric. The relatively low permittivity of SiO_2 makes the operating voltage greater than 100V which is not suitable for portable electronic applications. Instead of SiO_2 , we also demonstrated the hybrid dielectric transistor memory device that using UV-Ozone growth aluminum oxide as dielectric and then spin coated PS as electret. A thermal evaporated 100 nm Al was deposited on glass substrate and then was put into UV-Ozone chamber to form a thin layer of oxide. The aluminum oxide was immersed into ODP solution to allow SAM growth and finally covered by PS electret. Fig. 4a shows the schematic diagram of device and Fig. 4b shows the transfer I-V and V_{th} shift after programming/erasing. The measured effective capacitance of hybrid dielectric is 210 nF cm^{-2} , due to the higher effective capacitance of aluminum oxide hybrid dielectric, the operating voltage of transistor is largely reduced to 3 V and the programming/erasing bias is also as small as 5 V. Other than trapping charges, PS also enhance the electrical strength of hybrid dielectric. Because UV-Ozone growth aluminum oxide is not dense as oxygen plasma treated oxide film^{[14][15]}, the large leakage current becomes critical issue that affecting the transistor performance. The leakage current can be suppressed if aluminum oxide was covered by a protective layer such as parylene-C^[15]. In this work PS is used to replace parylene-C because rather than blocking the leakage current, PS simultaneously serves as charge trapping media. The 30 times reduce of programming/erasing voltage that from 150 V to 5 V makes the device suitable for portable electronic applications.

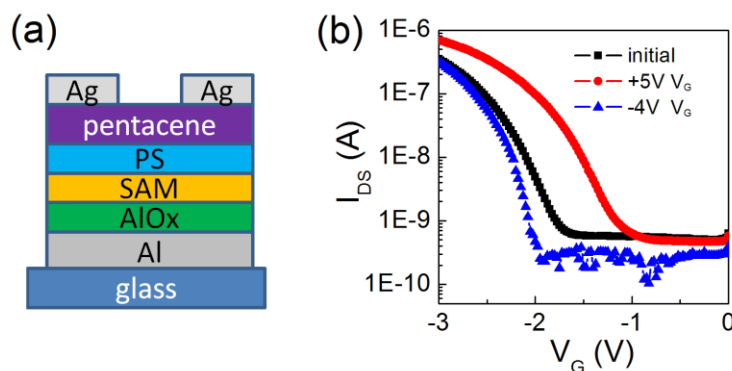


Figure 4. a, schematic diagram of aluminum oxide and PS hybrid dielectric; b, transfer I-V of low voltage transistor memory device, the programming and erasing gate bias are 5V and -4V respectively.

4. CONCLUSION

In conclusion, we have fabricated the DNTT based PS electrets memory transistor. Both holes and electrons can be trapped at PS electrets surface. The mobility of memory device is around $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and can achieve large memory window over 160 V and good retention time. This large memory window is potentially used for multiple state memory applications. The optical programmable property of DNTT has been studied and explained, it is conclude that most of electron traps in DNTT transistor are coming from photon excited charges. The electrical bias can only induce hole traps due to the charge injection barrier of electrode. UV-Ozone growth aluminum oxide was used to replace SiO_2 in order to reduce the operating voltage, the device with aluminum oxide and PS as hybrid dielectric can be programmed/erased at $\pm 5 \text{ V}$ gate bias.

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