Transient Mitigation of DC–DC Converters for High Output Current Slew Rate Applications

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***Abstract*—This paper presents a method of mitigating the transient overshoots of dc–dc converters undergoing large load disturbances. The method involves a small power auxiliary circuit which exists as an energy buffer to provide a smooth absorption and release of excess energy from and to the main dc–dc converter during transients. In the method, the regulation of the current magnitude of the converter and energy storage of the auxiliary circuit are guaranteed by the relevant control schemes. The cost and size of the auxiliary circuit will be relatively small as it only operates intermittently. In this paper, the voltage deviation analysis and the auxiliary circuit design guideline are provided. Experimental results validating the approach are presented.**

***Index Terms*—Auxiliary circuit, dc–dc converters, fast transients, large transients, slew rate.**

I. Introduction

THERE is a growing demand for ultrafast-response dc–dc converters [1]. Many interesting control solutions such as the one-cycle control [2], sliding mode control [3], minimum-time geometric control [4], time-optimal control [5], boundary control [6], and nonlinear control [7]–[9], etc., have been applied to converters to meet such an objective. However, for a general-purpose converter operating with a large step load change (hundreds of A per microsecond), there is no control scheme that can prevent voltage deviations from not appearing at the output [10]. For most critical applications, a very large electrolytic capacitor is typically required to achieve a satisfactory suppression of the overshoots. This may significantly increase the cost and the size of the converter, while reducing its lifetime and reliability.

Different approaches of dealing with such kinds of load disturbance for the converters have been presented in [11]–[30]. One interesting approach is to instantaneously change the inductance value corresponding to a load change to achieve the necessary load delivery with a large slew rate [11]–[13]. By varying the inductance, the output voltage overshoot can be alleviated when load disturbances appear. While a high efficiency is achievable with the proposed method, the complicated transformer or tapped inductor design is the drawback of using this method [26].

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Another approach of handling large transients is to parallel a linear controllable current source to the output port to compensate the transient current [14]–[16]. The transient overshoot is largely suppressed at the expense of a lower efficiency attributed by the linear current source.

The third possible approach is through circuit augmentation [17]–[20], which provides an effective means of achieving ultrafast dc–dc converters. With this scheme, an extra energy path is directly added to the converter without altering the slew rate of the inductor. The combined use of geometric digital control and circuit augmentation enhances the converter response to cater for very fast load steps. But to deal with load step changes, resistors of small value and high power rating are needed, resulting in inevitable energy losses.

The fourth approach is to use a specialized control strategy which includes a switching auxiliary circuit [21]–[25], of which energy can be flexibly transferred between the filter capacitor and the power line to regulate the output voltage. This is an effect way of dealing with both positive and negative load disturbances. Moreover, the energy loss of the relevant circuit can be decreased to a very low level. In particular, for the application of converters with a low duty cycle, where the overshoot caused by a positive current step is insignificant, this approach which focuses on handling unloading transient is preferred for its high efficiency and low cost [26]–[28].

In this paper, a different active solution for suppressing transient overshoots for both positive and negative step changes in the load current, via the use of a small low-cost auxiliary power circuit and a complementary control scheme, is proposed. With the auxiliary circuit operating as an energy buffer, a much improved transient response is achievable through the transfer of energy between its capacitor and the main dc–dc converter in the event of large load variations. Furthermore, comparing with previous methods, the features of the proposed method are as follows:

1) The auxiliary circuit is decoupled from the input and will not transfer energy from the load to the power line.
2) There is no recirculation of the transient energy. Excess energy from the main converter is absorbed by the auxiliary circuit and stored in the capacitor. The energy is utilized in the positive disturbance. This is unlike previous methods which transfer the excess energy from the output back into the input port causing a recirculation of energy between the input and the output.
3) The proposed method is generally applicable to all dc–dc converters because the topology is independent of the main converter. Moreover, it can be modified and applied to inverter systems.

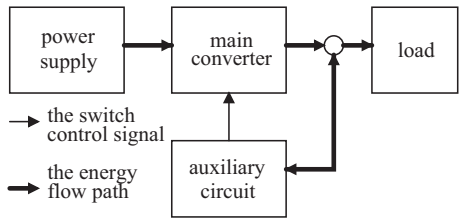

Fig. 1. Converter with an auxiliary circuit.

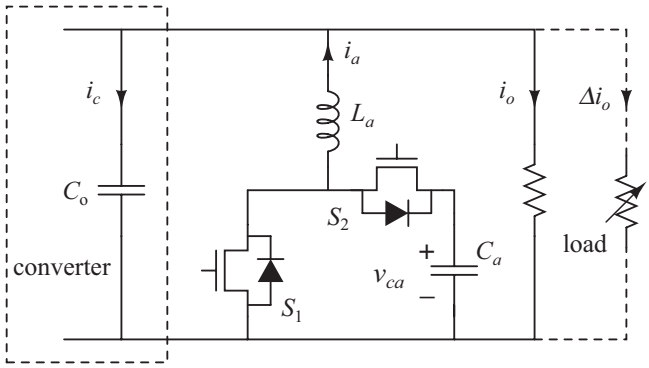

Fig. 2. Schematic diagram of an auxiliary circuit.

II. Fast Transient Using an Auxiliary Circuit

An essential idea of the proposed method of tackling fast load transients is the use of an auxiliary circuit. It includes an energy storage element which can provide bidirectional current flow to and from the load. Fig. 1 shows an overview of the concept. Here, the auxiliary circuit operates only when it is required and it is fully decoupled from the input terminal.

To achieve bidirectional energy buffering of the converter that can deal with both positive and negative transients, a bidirectional buck/boost converter [31] is adopted as the auxiliary circuit. It comprises two MOSFET switches, one inductor and one capacitor, as shown in Fig. 2. The mean power of all the components is dependent on the load-step value and the frequency of the step changes since the circuit only operates following a load step. Generally speaking, the current rating of the components is much lower than that of the main converter [32]. Therefore, low-power, low-cost components can be used for the implementation of the auxiliary circuit.

When S_1 and S_2 are turned OFF, the auxiliary circuit has no effect on the converter. When S_1 is turned ON and OFF alternately, the polarity of i_a will be negative and current will be pumped from the output port of the main converter into C_a, thereby increasing its stored charges. Conversely, when S_2 is activated, i_a will be positive which will release the charges from C_a to the load, thereby decreasing the energy storage level. Essentially, the auxiliary circuit will operate only in the following two conditions:

1) When there is a difference between the load and the inductor current of the main converter during load transients, the auxiliary circuit will operate to control the output current i_a to provide/absorb the current deficit.

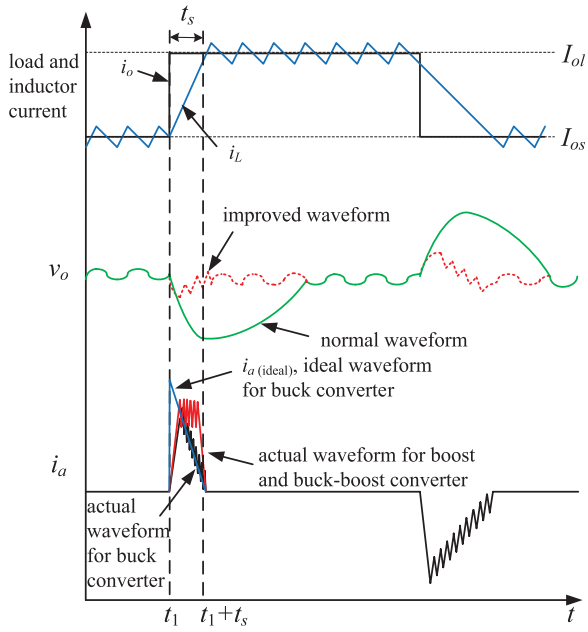

Fig. 3. Normalized waveforms of key variables.

2) After each load disturbance, the auxiliary circuit needs to regulate the energy stored in its capacitor C_a to deal with all possible transients in future. In this case, the voltage of C_a will become the reference of the auxiliary circuit operation. The duty cycle of two switches will be set very small to generate a small i_a so that there is minimum interference on the converter's steady-state operation. Note that the the main energy dissipation in the switches only occurs during transients.

III. Operating Mechanism of the Auxiliary Circuit

The proposed control method involves the control of the output current of the auxiliary circuit i_a and its reservoir capacitor voltage v_{ca} which represents the energy storage level. The first aspect of the control is to ensure that voltage overshoot of the main converter is minimized and constant output voltage regulation is achieved. The second aspect is to ensure that the reservoir capacitor of the auxiliary circuit has sufficient storage energy as well as storage space for any predictable load disturbances.

A. Output Current Control

Fig. 3 shows a set of normalized waveforms illustrating the key variables of the main converter and its auxiliary circuit. In the figure, I_{os} and I_{ol} represent the desired steady-state levels of the load transients, with I_{os} being the lower level and I_{ol} the higher current level. When the load experiences a sudden step change from I_{os} to I_{ol} at time t_1, the fastest response is to lock the duty cycle at "1" making the inductor current rise to the new operating point in the time duration t_s. Conversely, when load drops, the duty cycle is locked at "0." Clearly, the change of inductor current is much slower than the change of load current. Hence, there is a momentary shortage of energy that can be delivered from the inductor to the load. The proposed

TABLE I
IDEAL CALCULATION OF i_a FOR STEP-UP LOAD ($i_o = I_{os} \rightarrow I_{ol}$) AND STEP-DOWN LOAD ($i_o = I_{ol} \rightarrow I_{os}$)

Variable		Buck	Boost	Buck-boost
i_L	step-up load	$I_{os} \rightarrow I_{ol}$	$I_{os} \cdot \frac{1}{1-D} \rightarrow I_{ol} \cdot \frac{1}{1-D}$	$I_{os} \cdot \frac{1}{1-D} \rightarrow I_{ol} \cdot \frac{1}{1-D}$
	step-down load	$I_{ol} \rightarrow I_{os}$	$I_{ol} \cdot \frac{1}{1-D} \rightarrow I_{os} \cdot \frac{1}{1-D}$	$I_{ol} \cdot \frac{1}{1-D} \rightarrow I_{os} \cdot \frac{1}{1-D}$
k_L	step-up load	$\frac{V_i - V_o}{L}$	$\frac{V_i}{L}$	$\frac{V_i}{L}$
	step-down load	$\frac{-V_o}{L}$	$\frac{V_i - V_o}{L}$	$\frac{-V_o}{L}$
$i_{a(ideal)}$	step-up load	$I_{ol} - [I_{os} + k_L(t - t_1)]$	I_{ol}	I_{ol}
	step-down load	$I_{os} - [I_{ol} + k_L(t - t_1)]$	$I_{os} - \left[I_{ol} \cdot \frac{1}{1-D} + k_L(t - t_1)\right]$	$I_{os} - \left[I_{ol} \cdot \frac{1}{1-D} + k_L(t - t_1)\right]$

TABLE II
DECREMENTAL/INCREMENTAL ENERGY STORED IN THE CAPACITOR OF THE AUXILIARY CIRCUIT FOR A STEP LOAD CHANGE

	ΔE_1 (Step up)	ΔE_2 (Step down)
Buck	$\frac{1}{2}\left(\frac{I_{ol}}{I_{os}} - 1\right)^2 I_{os}^2 \frac{LD}{1-D}$	$\frac{1}{2}\left(\frac{I_{ol}}{I_{os}} - 1\right)^2 I_{os}^2 L$
Boost	$\frac{I_{ol}}{I_{os}}\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 L}{(1-D)^2}$	$\frac{1}{2}\left[\left(\frac{I_{ol}}{I_{os}} + 1\right)\frac{1}{1-D} - 2\right]\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 L}{D(1-D)}$
Buck-boost	$\frac{I_{ol}}{I_{os}}\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 DL}{(1-D)^2}$	$\frac{1}{2}\left[\left(\frac{I_{ol}}{I_{os}} + 1\right)\frac{1}{1-D} - 2\right]\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 L}{1-D}$

strategy is to supply this transient shortage using energy from the reservoir capacitor of the auxiliary circuit in real time during t_s. Specifically, a very small inductor and a high-speed switch are used to trace an "ideal" transient output current, denoted as $i_a(t)$, which is varying with time, according to the circuit parameters and transient specifications.

For example, when a load connecting to the buck converter increases from I_{os} to I_{ol} instantly at t_1, as shown in Fig. 3, the inductor current rises with a slew rate of $(V_i - V_o)/L$. In this time period, the inductor is unable to deliver current to the load at the required level. Hence, to eliminate the large voltage dip at v_o, an extra current denoted conceptually as $i_{a(\text{ideal})}$ as shown in Fig. 3 is needed. The expression of this current related to time is $i_{a(\text{ideal})} = I_{ol} - [I_{os} + (t - t_1)(V_i - V_o)/L]$. Here, the actual current i_a is controlled by S_2 and it will track closely the ideal current $i_{a(\text{ideal})}$. A smaller L_a or a higher switching frequency can reduce the overshoot ripple of the output voltage.

For different converters undergoing step-up and step-down loads, respectively, i_a is given in Table I, under the condition that a step load appears at t_1. Here, i_a is only defined for the time duration $[t_1, t_1 + t_s]$, where t_s represents the transition time duration and it can be obtained from

$$t_s = \frac{(I_{ol} - I_{os})}{k_L} \tag{1}$$

where k_L represents the current slew rate of the inductor and it can be found in Table I. To produce the expected i_a, the following variables t_1, t_s, and $i_{a(\text{ideal})}$ must be known. t_1 is detectable from the circuit and t_s is proportional to the step change of I_{ol} to I_{os}. If i_a is precisely equal to its ideal value, the current of the filter capacitor of the main converter, denoted as i_c, will be equal to zero. This means that i_c can be used as the error signal of i_a related to its ideal value for control.

B. Reservoir Capacitor Voltage Control

When the auxiliary circuit operates to deal with the load disturbances, the energy of C_a changes in a passive and uncontrollable way. Over time, the energy released from or absorbed by the reservoir capacitor may not be equivalent. It is necessary that the auxiliary circuit operates actively to regulate the reservoir capacitor voltage after handling each load disturbance. Otherwise, the storage energy and storage space of the capacitor may not be sufficient to sustainably handle future disturbances.

In other words, it must be ensured that the capacitor is always capable of satisfying the energy diverting requirement for all possible load disturbances. For any step load disturbance occurring at t_1, the energy change in C_a during t_s can be calculated as

$$\Delta E = \int_{t_1}^{t_1 + t_s} V_o |i_a(t)| dt. \tag{2}$$

Correspondingly, ΔE_1 and ΔE_2 are used to represent the value of ΔE, when the auxiliary circuit is operating for a step-up (I_{os} to I_{ol}) or step-down (I_{ol} to I_{os}) load disturbance. After expanding (2) with the expression of $i_{a(\text{ideal})}$ given in Table I, ΔE_1 and ΔE_2 can be derived and are given in Table II.

For any converter, there is a specified range of output current, e.g., from $I_{o\min}$ to $I_{o\max}$. The converter can operate anywhere within these levels and it is possible to shift from the current level I_o to a new point within $[I_{o\min}, I_{o\max}]$ anytime. Therefore, it is reasonable to assume that the maximal ΔE_1 or ΔE_2 will appear when the load current I_o steps to $I_{o\max}$ or $I_{o\min}$ and they

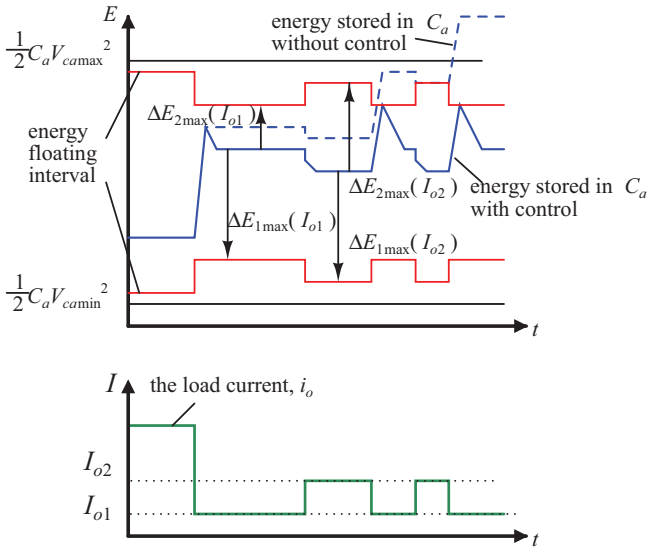

Fig. 4. Reservoir capacitor voltage and the energy balance waveforms.

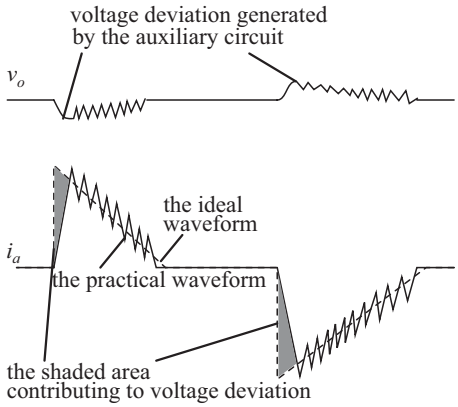

Fig. 5. Current and voltage waveforms during load changes.

can be defined as $\Delta E_{1\max}$ and $\Delta E_{2\max}$. Furthermore, the range of operating voltage for the reservoir capacitor can be specified as a lower boundary, $V_{ca\min}$, which must not be less than v_o of the main converter, and an upper boundary, $V_{ca\max}$, which must not exceed the voltage rating of the capacitor.

Hence, for every I_o, a suitable V_{ca} can be found. The energy released by the capacitor due to the change of V_{ca} to $V_{ca\min}$ will be able to facilitate the load transient of I_o stepping to $I_{o\max}$. Similarly, the energy storage space gained by the capacitor from V_{ca} changing to $V_{ca\max}$ will be able to serve the load steps of I_o changing to $I_{o\min}$. Hence, v_{ca} can be written as a function of i_o, i.e., (3), as shown at the bottom of the page.

Details of the mathematical derivations can be found in Appendix A.

IV. Performance Analysis and Design Guidelines

Due to the finite slew rate of i_a, it is not possible to achieve a perfect current step. This produces a small voltage deviation right after the onset of the load disturbance, before the auxiliary current reaches the required level, as illustrated in Fig. 5. In this section, the characteristic of voltage deviation with respect to the reference $v_{t\mathrm{aux}}$ will be first analyzed. Then, an analysis on the switching frequency f_{as}, ripple current $I_{r\mathrm{aux}}$, and voltage ($v_{r\mathrm{aux}}$) of the auxiliary circuit will be presented. The guideline to choosing the circuit components will be provided.

A. Possible Voltage Deviation

A practical auxiliary circuit cannot provide a current shaped like the ideal waveform. By assuming that k_c is the slew rate of the inductor when it is de-energizing and k_{aux} represents the slew rate of i_a, the time period taken for the auxiliary circuit current to catch up with the load step is $\frac{I_{ol}-I_{os}}{k_c+k_{\mathrm{aux}}}$. The shaded area in Fig. 5, which represents $v_{t\mathrm{aux}}$, can be expressed as

$$v_{t\mathrm{aux}} = \frac{1}{C_o}\int_{t_1}^{t_1+\frac{I_{ol}-I_{os}}{k_c+k_{\mathrm{aux}}}} |(k_c+k_{\mathrm{aux}})(t-t_1)-i_a|dt = \frac{1}{2C_o(k_c+k_{\mathrm{aux}})}(I_{ol}-I_{os})^2 \quad (4)$$

where for a boost or buck–boost converter, when the load is undertaking a step-up change, the current flowing to the load from the inductor will be always zero. Hence, k_c is equal to 0. Otherwise, $k_c = k_L$, which is found in Table I. Here, $k_{\mathrm{aux}} = (v_{ca}-V_o)/L_a$ or $k_{\mathrm{aux}} = -V_o/L_a$ are true in a step-up or step-down load operations. The inductance L_a affects the voltage deviation and could be determined from the overshoot limit, $v_{t\mathrm{auxmax}}$.

Since the auxiliary circuit is a switching circuit, the maximum value of the switching frequency, $f_{as\max}$, is limited by the specification and also the size of the inductor as

$$f_{as} \approx \left[I_{r\mathrm{aux}}L_a\left(\frac{1}{V_{ca}-V_o}+\frac{1}{V_o}\right)\right]^{-1} = \frac{V_o(V_{ca}-V_o)}{I_{r\mathrm{aux}}L_aV_{ca}} \quad (5)$$

where $I_{r\mathrm{aux}}$ is the ripple band selected by the designer. $I_{r\mathrm{aux}}$ induces a voltage ripple at the output port directly and the voltage ripple can be expressed as

$$v_{r\mathrm{aux}} = \frac{I_{r\mathrm{aux}}}{8C_of_{as}}. \quad (6)$$

$$v_{ca}(i_o) = \sqrt{\frac{1}{2}(V_{ca\min}^2+V_{ca\max}^2)+\frac{1}{C_a}\left(\frac{1}{2}\left(\frac{I_{o\max}}{I_o}-1\right)^2 I_o^2\frac{LD}{1-D}-\frac{1}{2}\left(\frac{I_o}{I_{o\min}}-1\right)^2 I_{o\min}^2 L\right)} \quad (3)$$

TABLE III
DESIGN SPECIFICATIONS OF A SYNCHRONOUS BUCK CONVERTER

Description	Parameter
Input voltage	12 V
Output voltage	5 V
Inductor value	10 μH
Capacitor value	47 μF
Switching frequency	200 kHz
Output current	1 A — 10 A
Controller chip	IRU3037 (voltage mode)

B. Components Value and Guidelines

With the chosen $v_{t\text{auxmax}}$, $I_{r\text{aux}}$, and $f_{as\max}$, from (4) and (5), we can derive the design conditions of the inductor as

$$\begin{cases} L_a \le \min\left\{ \dfrac{V_{ca\min}-V_o}{\frac{\Delta I_{o\max}^2}{2C_o v_{t\text{auxmax}}}-k_c}, \dfrac{V_o}{\frac{\Delta I_{o\max}^2}{2C_o v_{t\text{auxmax}}}+k_c} \right\} \\ L_a \ge \dfrac{V_o(V_{ca\max}-V_o)}{I_{r\text{aux}} f_{as\max} V_{ca\max}}. \end{cases} \tag{7}$$

Note that a larger inductance relates to a lower switching frequency, but a larger voltage deviation. If the design specifications are strict on power dissipation, the inductance should be as high as possible but within the upper limit.

The capacitance of the auxiliary circuit is governed by the required size of the energy storage and its voltage range. As presented previously, the energy floating interval is a variable with $i_o \in [I_{o\min}, I_{o\max}]$. It must always be within the energy boundary of the capacitor, i.e., $\le \frac{1}{2}C_a(V_{ca\max}^2 - V_{ca\min}^2)$. The capacitor requirement is given as

$$C_a \ge \max_{i_o \in [I_{o\min}, I_{o\max}]} \left\{ \frac{\Delta E_{1\max} + \Delta E_{2\max}}{\frac{1}{2}\left(V_{ca\max}^2 - V_{ca\min}^2\right)} \right\} \tag{8}$$

of which it can be observed that there is a tradeoff between the level of the capacitor voltage and its size. If a smaller capacitor is expected, V_{ca} must be sufficiently high, which will increase the leakage current and the voltage rating of the relevant components. Conversely, the choice of a lower voltage rating will require the use of a larger capacitor.

V. SIMULATION AND EXPERIMENTAL VERIFICATIONS

The proposed scheme is validated through simulations and experiments on a synchronous buck converter. In this section, the experimental setup is described and the relevant results are reported.

A. Simulation Results

The specifications of the buck converter for simulation and the experimental prototype is shown in Table III. The switching frequency and the inductor are chosen based on the current ripple. The capacitor value is selected based on the ripple requirement of 50 mV. A type-III compensator with voltage control is utilized in this converter. With the maximum converter's voltage deviation of 0.15 V, the maximum auxiliary circuit's switching frequency of 1.5 MHz, and the maximum auxiliary circuit's current ripple of 4 A, the parameters of the auxiliary circuit can be calculated from the design procedure as $v_{ca} \in [8.5\text{ V}, 10\text{ V}]$, $L_a = 0.42\ \mu$H, $C_a = 40\ \mu$F, and the regulation formula as $v_{ca} = 0.19\sqrt{(i_o + 81.58)(32.74 - i_o)}$ by using (3). Using a load-step interval of 10 ms, the permitted voltage ripple during v_{ca} regulation is 10 mV. So, t_{w} is set as 0.12 μs and the operation interval is set as 16 μs.

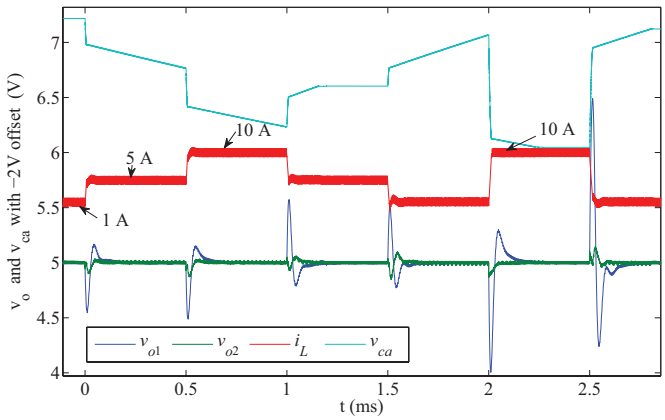

Fig. 6. Simulated waveforms of the synchronous buck converter operating with and without the auxiliary circuit.

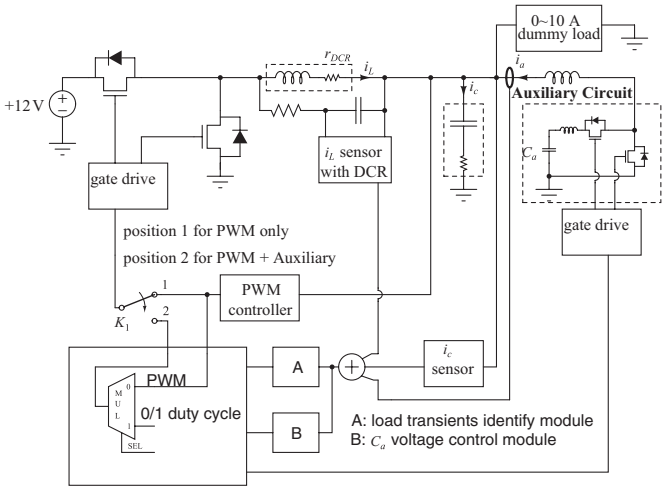

Fig. 7. Block diagram of the whole prototype.

To validate the effect of the proposed auxiliary circuit, two simulations (one with auxiliary circuit and the other without auxiliary circuit) have been conducted and the results are given in Fig. 6 for comparison. In the diagram, v_{o1} is the output voltage of the converter without the auxiliary circuit and v_{o2} is that with the auxiliary circuit. The simulated waveforms illustrate that when load disturbances appear at 0, 0.5, 1.0 ms, etc., the transient voltage is greatly reduced (having a maximum reduction of 90%) with the use of the auxiliary circuit.

B. Experimental Prototype

The experimental prototype is constructed using the same converter and auxiliary circuit design adopted in the simulation. The block diagram of the prototype is given in Fig. 7. The detailed schematic diagram is given in Appendix B. In Fig. 7, it

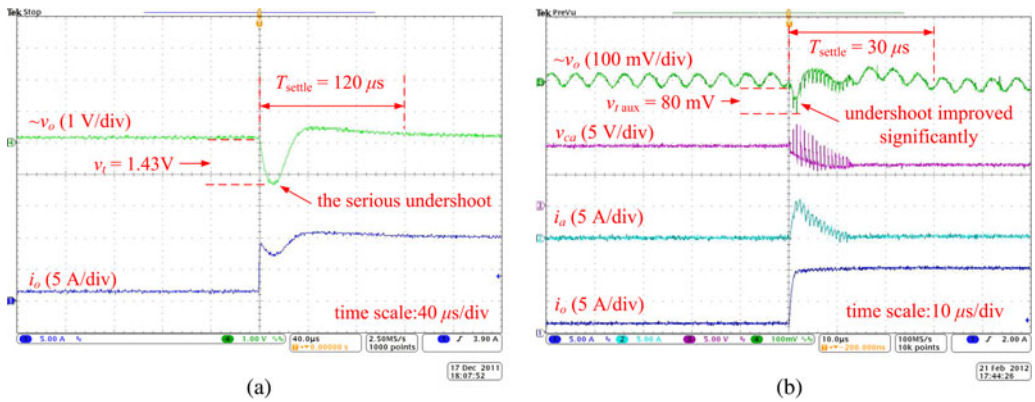

Fig. 8. Waveforms of the buck converter using a 47 μF filter capacitor under a step-up change from 1 to 10 A (a) without the auxiliary circuit and (b) with the auxiliary circuit.

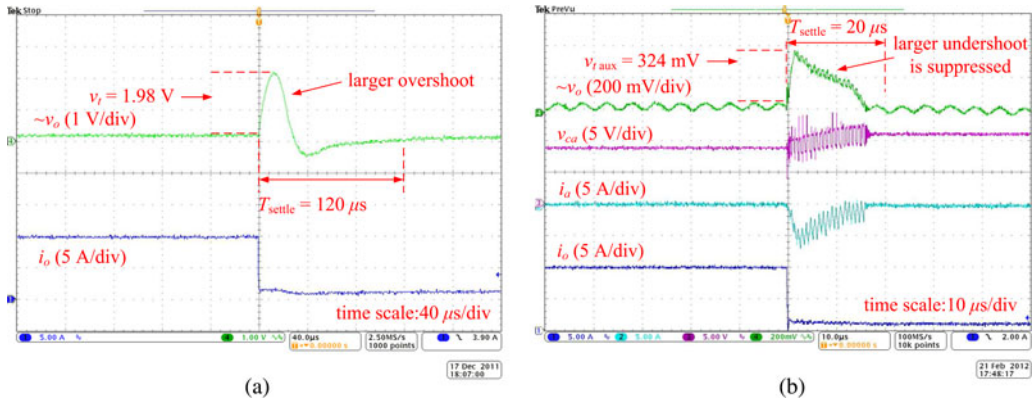

Fig. 9. Waveforms of the buck converter using a 47 μF filter capacitor under a step-down change from 10 A to 1 A (a) without the auxiliary circuit and (b) with the auxiliary circuit.

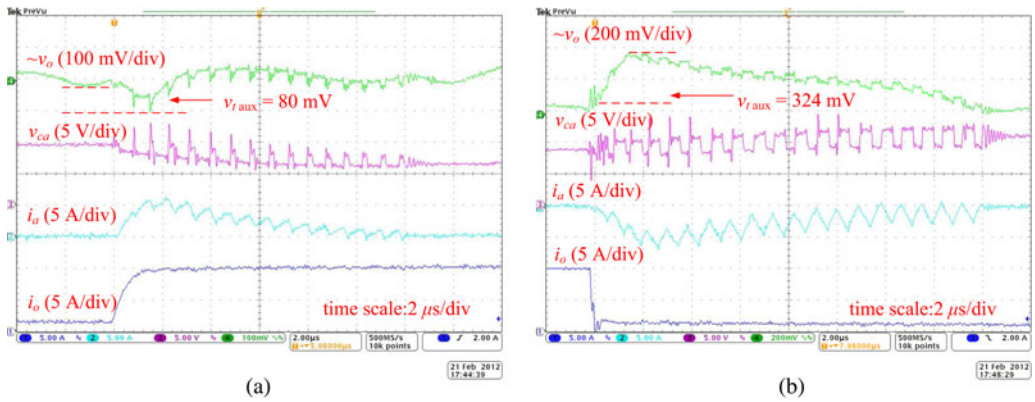

Fig. 10. Enlarged waveforms of the buck converter (using a 47 μF filter capacitor) for a step load change between 1 and 10 A with the auxiliary circuit in the case of (a) step-up load and (b) step-down load.

can be seen that a switch K_1 has been included to switch between the choice of using or not using the auxiliary circuit. To validate the effectiveness of the proposed scheme, different values of filter capacitance are utilized and the relevant compensation network parameters are optimally adjusted.

C. Experimental Results

To validate the proposed solution, the synchronous buck converter is tested with different filter capacitance values of which for each capacitance, the compensation network is optimally tuned for the best transient performance.

Figs. 8–10 show the voltage and current waveforms of the buck converter with and without the auxiliary circuit for a step load change between 1 and 10 A. In Figs. 8(a) and 9(a), a large voltage overshoots of 1.4 and 2.0 V, respectively, and a long settling time of 120 μs can be seen. Comparably, waveforms in Figs. 8(b) and 9(b) present the improved response of the synchronous buck converter with the auxiliary circuit. The

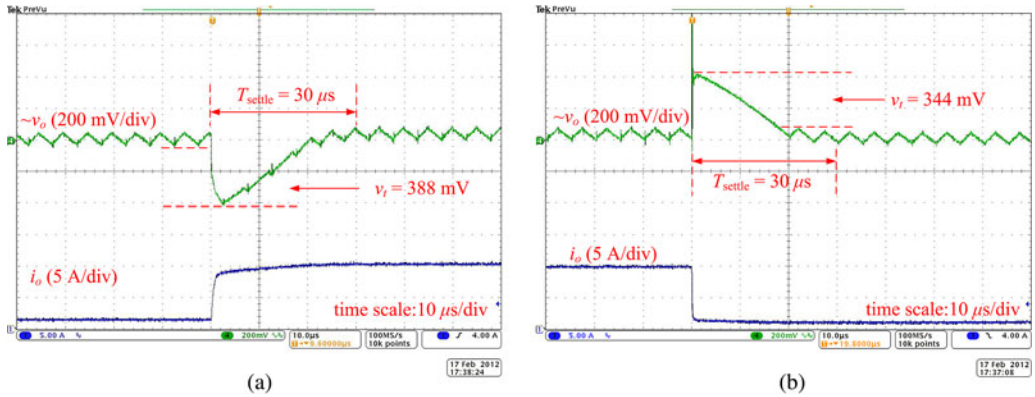

Fig. 11. Waveforms of the buck converter using a 1000 μF filter capacitor for a step load change between 1 and 10 A in the case of (a) step-up load and (b) step-down load.

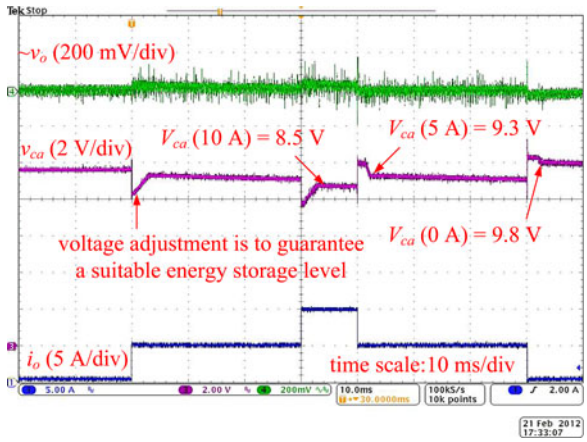

Fig. 12. Waveform showing the effectiveness of the capacitor voltage regulation mechanism of the auxiliary circuit in maintaining energy balance of the capacitor and handling load transients.

TABLE IV
PERFORMANCE COMPARISON BETWEEN CONVERTERS WITH AND WITHOUT THE AUXILIARY CIRCUIT FOR DIFFERENT FILTER CAPACITANCE

Prototype	Disturbance Polarity	Performance	
		Voltage Overshoot (V)	Settling Time (μs)
without auxiliary circuit	load step up	1.43	120
47 μF filter capacitor	load step down	1.98	120
with auxiliary circuit	load step up	0.080	30
47 μF filter capacitor	load step down	0.324	20
without auxiliary circuit	load step up	0.420	30
470 μF filter capacitor	load step down	0.492	30
without auxiliary circuit	load step up	0.388	30
1000 μF filter capacitor	load step down	0.344	30
without auxiliary circuit	load step up	0.214	30
1500 μF filter capacitor	load step down	0.226	32
without auxiliary circuit	load step up	0.208	32
3300 μF filter capacitor	load step down	0.240	30

voltage overshoot for the step-up change is reduced to 80 mV and for the step-down change to 324 mV. The settling times are 30 and 20 μs, respectively. The reservoir capacitor voltage changes (between 7 and 11 V) while the auxiliary circuit handles the transients. In Fig. 10, the enlarged waveforms of Figs. 8(b) and 9(b) are shown. In both cases, the switching frequency is around 1.25 MHz, which is kept within the maximum switching frequency design limit of 1.5 MHz. The current ripple at i_a is about 3 A, which is less than the specification of 4 A. The voltage overshoot is larger than the designed requirement of 0.15 V. This discrepancy is attributable to the detection time delay (about 0.5 μs) of the load current step.

To validate the effectiveness of the reservoir capacitor voltage control, a large-time-scale waveform of various transient operations is given in Fig. 12. In this test, the load is stepped up from 0 to 5 A and then 10 A, and then stepped down to 5 A and back to 0 A. The process of regulating the reservoir capacitor energy can be found after the operation for each step load. The reservoir capacitor voltage is regulated to the expected value after each load changing cycle.

Waveforms of the converter without the auxiliary circuit but with a 1000 μF filter capacitor are shown in Fig. 11. The voltage overshoots are larger and the settling time are longer than that of the converter using 47 μF capacitor with the auxiliary circuit. The experimental results of the transient voltage overshoot and settling time for all cases of capacitance are tabulated in Table IV. From the table, it can be seen that for both step-up and step-down load change, the dynamic responses are improved with the auxiliary circuit. The transient overshoot has been suppressed by at least 85% and the settling time shortened by 80%. In practice, a converter with a large voltage overshoot is not allowed. The typical practice is to increase the size of the capacitance to the point where the transient response is satisfactory. From the experimental results, it can be seen that even with an output filter capacitor of 3300 μF, the step-up overshoot is still much larger than the case of 47 μF with the auxiliary circuit. With an output filter capacitor of 1000 μF, the response of load step down is comparable to the proposed method. However, the total capacitance used with the auxiliary circuit is no more than 1/10 of 1000 μF. In the proposed method, only ceramic capacitors are used, which have a longer lifespan.

Furthermore, the auxiliary circuit only operates intermittently as and when required. Hence, only the peak current value is considered for the design of the auxiliary circuit. If the load-step intervals are relatively long, thermal factors need not be considered.

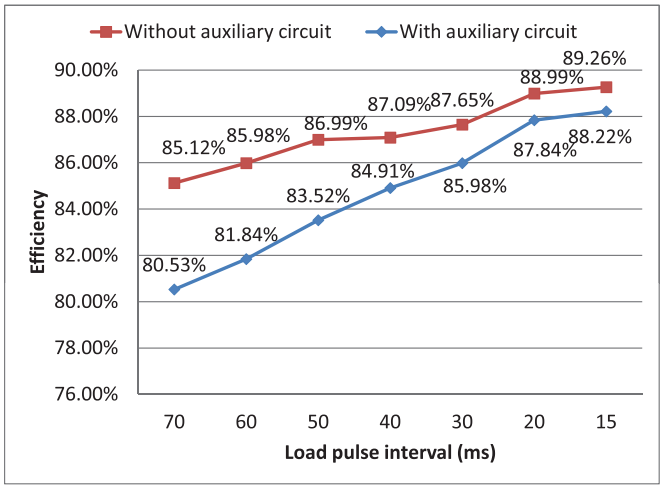

Fig. 13. Plots of the data collected from the efficiency tests.

Finally, an experiment on the power efficiency has been conducted with the following testing conditions:

1) load steps changing between 0 and 10 A;
2) pulsewidth duration of the 10 A load is 10 ms;
3) pulse interval of the 10 A load is a variable between 15 and 70 ms;
4) filter capacitor of a prototype converter is fixed at 47 μF.

Two series of data have been collected and plotted as given in Fig. 13. It can be observed that with the auxiliary circuit, the efficiency is few percent lower. This is the price to pay for an improved transient performance. It can also be observed that with a shorter pulse interval, the efficiency between the converter with and without the auxiliary circuit is closer (about 1% decline). This means that the amount of energy losses is approximately constant. The reservoir capacitor leakage current and the driving circuits may be the main contribution to the energy losses. Hence, it will become insignificant when the output power of the system is higher. Therefore, in applications where there is frequent load transients the auxiliary circuit can be applied practically, since the frequent energy exchange between the circuit and the main converter will not lead to an increase in energy cost.

VI. Conclusion and Final Remark

This paper proposes a method of incorporating an auxiliary switching circuit and a complementary control scheme in dc–dc converters to cope with very fast load disturbances. Large filter capacitors are no longer needed for suppressing excessive overshoots. Longer lifetime ceramic capacitors can be used instead of electrolytic capacitors as the filter capacitors. The auxiliary circuit operates as an energy buffer that will decouple itself from the power line. The presented scheme of active energy storage adjustment guarantees that the energy storage level and storage space of the capacitor can always undertake any predictable step load change. It is validated experimentally for a synchronous buck converter and the idea is generally applicable to other power converters.

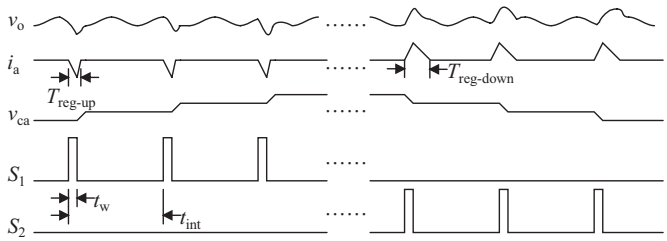

Fig. 14. Key waveforms of reservoir capacitor voltage regulation.

Recently, the performance gain in dynamic response resulting from microprocessors providing information of the load dynamics to their power supplies has been discussed [33]. This is a new design direction to cope with very fast transient requirement through communication between the actual load and the power supply. For the case of microprocessor loads, a signal containing information of the occurrence of load transient can be communicated to the power supply so as to allow fast transient control to be applied almost synchronously without the need for sensing the onset of the load transient. Thus, very fast transients can be achieved in dc–dc converters if information of the load dynamics is available and an appropriate fast transient control method is used.

Appendix A
Derivation Details of Reservoir Capacitor Voltage Control

Mathematically, the limitation of v_{ca} is

$$\begin{cases} \frac{1}{2}C_a v_{ca}^2 - \Delta E_{1\max} \geq \frac{1}{2}C_a V_{ca\min}^2 \\ \frac{1}{2}C_a v_{ca}^2 + \Delta E_{2\max} \leq \frac{1}{2}C_a V_{ca\max}^2 \end{cases} \tag{9}$$

which can be combined as

$$\frac{1}{2}C_a V_{ca\min}^2 + \Delta E_{1\max} \leq \frac{1}{2}C_a v_{ca}^2 \leq \frac{1}{2}C_a V_{ca\max}^2 - \Delta E_{2\max} \tag{10}$$

e.g., for a buck converter, where $\Delta E_{1\max} = \frac{1}{2}(\frac{I_{o\max}}{I_o} - 1)^2 I_o^2 \frac{LD}{1-D}$ and $\Delta E_{2\max} = \frac{1}{2}(\frac{I_o}{I_{o\min}} - 1)^2 I_{o\min}^2 L$. $\Delta E_{1\max} + \Delta E_{2\max}$ is defined as the energy floating interval. For a given i_o, if $\frac{1}{2}C_a v_{ca}^2$ does not fall within the inequalities given in (10), the auxiliary circuit may exceed the operating boundary in the next operation. To prevent this from happening, the auxiliary circuit can be operated to charge or discharge some of its energy such that v_{ca} falls within the inequality in (10) before the occurrence of the next disturbance. This method of capacitor voltage control is illustrated in Fig. 4, where the normal energy ranges are depicted in black solid lines while the energy floating intervals are depicted in red lines. The dashed line in Fig. 4 corresponds to the case of v_{ca} exceeding the upper limit without the reservoir capacitor voltage control.

Practically, the midpoint of the interval defined by inequality (10) can be chosen as the optimal regulation reference for v_{ca}. This means that the energy floating interval will always be located at the center of the normal energy range of C_a. This can

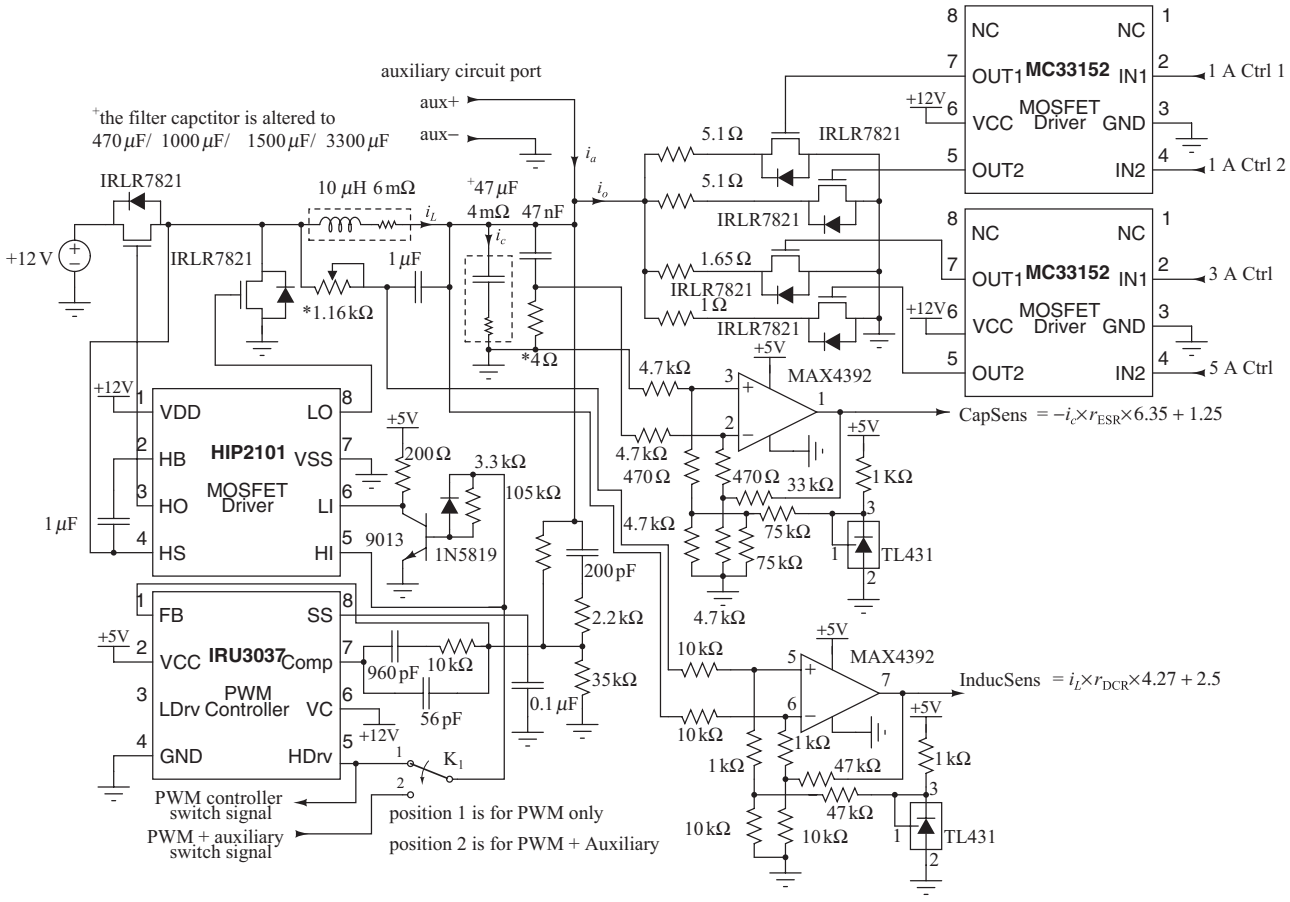

Fig. 15. Schematic diagram of the synchronous buck converter.

be mathematically expressed as

$$\frac{1}{2}C_a v_{ca}^2 = \frac{1}{2}\left[\frac{1}{2}C_a(V_{ca\min}^2 + V_{ca\max}^2) + (\Delta E_{1\max} - \Delta E_{2\max})\right] \tag{11}$$

and after simplification as

$$v_{ca}(i_o) = \sqrt{\frac{1}{2}(V_{ca\min}^2 + V_{ca\max}^2) + \frac{\Delta E_{1\max} - \Delta E_{2\max}}{C_a}}. \tag{12}$$

By substituting $\Delta E_{1\max}$ and $\Delta E_{2\max}$ into the buck column of Table II, (3) is generated.

With knowledge of the output current i_o, the relevant reference of v_{ca} can be calculated using (12). If the actual v_{ca} is larger than the reference value, S_2 is driven by a series of short-pulse signal (at a small duty ratio) to release some energy from the capacitor to the load at a relatively low speed. Through this process, excessive energy from the capacitor is released to the load. If v_{ca} is lower than the reference, S_1 is driven by a small duty ratio such that v_{ca} increases slowly until it reaches the reference value.

The turn-on time of switches $t_{\rm w}$ and the turn-on interval $t_{\rm int}$ should be chosen following this principle. First, as such operations will induce a small voltage ripple at v_o, $t_{\rm w}$ should be sufficiently small to ensure the voltage ripple to be within the converters ripple band. On the other hand, $t_{\rm int}$ affects the response time of the voltage regulation and the stability of the converter. A shorter $t_{\rm int}$ gives a faster voltage regulation but induces a larger current flow in the main converter. Therefore, $t_{\rm int}$ should be as large as possible but is limited by the required response time of v_{ca}. The waveforms corresponding the reservoir capacitor voltage regulation process are shown in Fig. 14.

When S_1 is operated to increase the value of v_{ca}, the ripple voltage at the converter's output will be

$$\begin{aligned} v_{r\rm reg} &= \frac{1}{C_o}\int_{<T_{\text{reg-up}}>} |i_a|dt \\ &= \frac{1}{2}\frac{V_o t_{\rm w}}{L_a}\left[t_{\rm w} + \frac{V_o t_{\rm w}}{C_o L_a}\left(\frac{V_{ca}-V_o}{L_a}\right)^{-1}\right] \\ &= \frac{1}{2}\frac{V_o t_{\rm w}^2}{C_o L_a}\frac{V_{ca}}{V_{ca}-V_o} \end{aligned} \tag{13}$$

where v_o and v_{ca} become approximately constant. A maximum value of $v_{r\rm reg}$ will appear when $v_{ca} = V_{ca\min}$, i.e.,

$$v_{r\rm regmax} = \frac{1}{2}\frac{V_o t_{\rm w}^2}{C_o L_a}\frac{V_{ca\min}}{V_{ca\min}-V_o}. \tag{14}$$

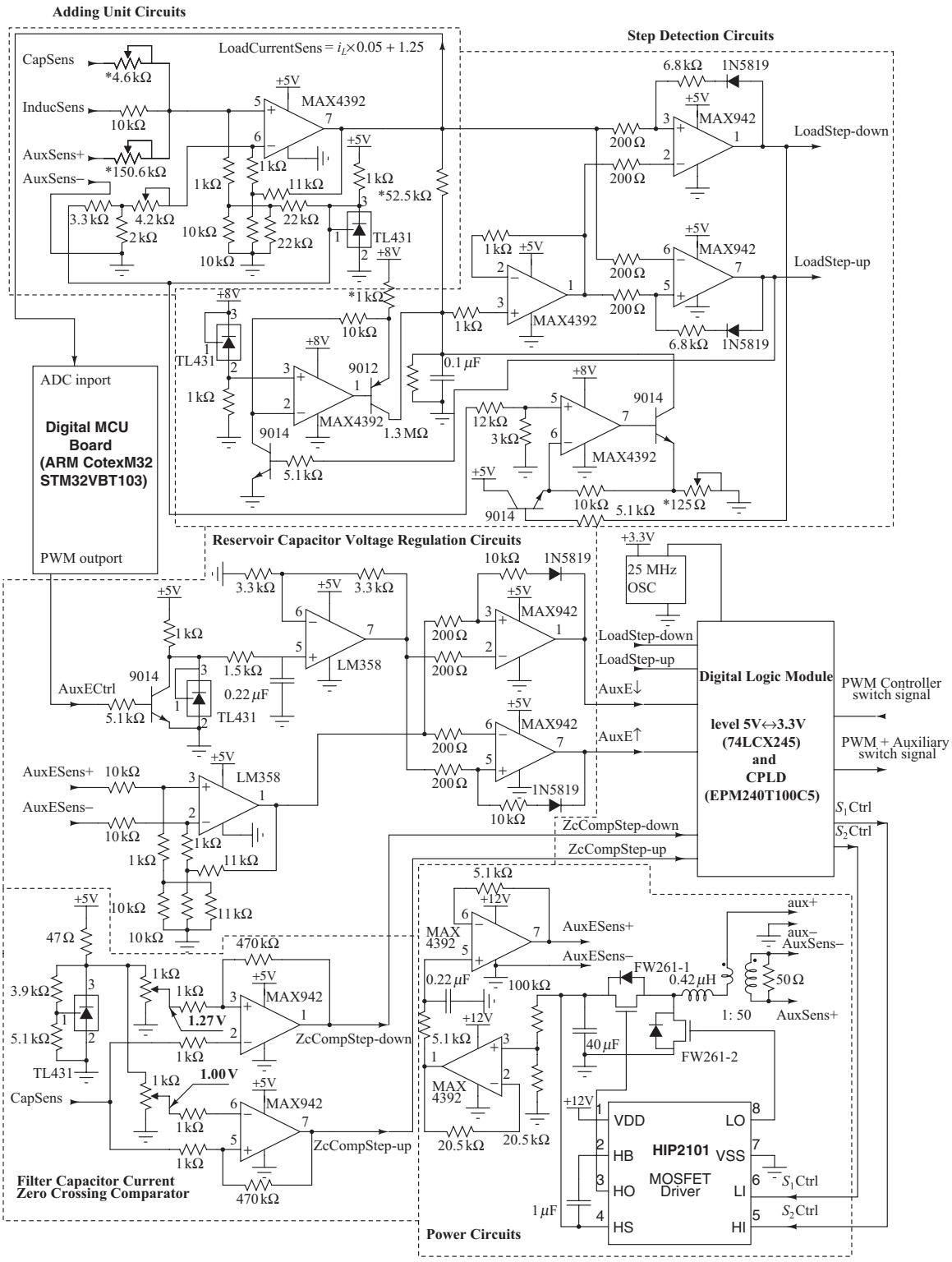

Fig. 16. Schematic diagram of the auxiliary circuit and its control.

Similarly, when S_2 is operated to decrease the value of v_{ca}, the ripple voltage can be derived as

$$v_{\mathrm{rreg}} = \frac{1}{C_o}\int_{<T_{\text{reg-down}}>} |i_a|dt = \frac{1}{2}\frac{(V_{ca}-V_o)t_{\mathrm{w}}^2}{C_o L_a}\frac{V_{ca}}{V_o} \quad (15)$$

and its maximum as

$$v_{\mathrm{rregmax}} = \frac{1}{2}\frac{(V_{ca\max}-V_o)t_{\mathrm{w}}^2}{C_o L_a}\frac{V_{ca\max}}{V_o}. \quad (16)$$

If the specified ripple band is v_{rregmax}, to satisfy the specification, t_{w} is limited to

$$t_{\rm w} \le \min\left\{\sqrt{\frac{2v_{r\rm regmax}C_oL_a(V_{ca\min}-V_o)}{V_oV_{ca\min}}}\right.$$
$$\left.\sqrt{\frac{2v_{r\rm regmax}C_oL_aV_o}{(V_{ca\max}-V_o)V_{ca\max}}}\right\}. \quad (17)$$

The energy change of C_a for a complete switching action of S_1 or S_2 is

$$\Delta E_{\rm S1/S2} = \int_{<T_{\rm reg\text{-}up}/T_{\rm reg\text{-}down}>} V_o|i_a|dt. \quad (18)$$

Under a reasonable approximation that v_{ca} is a constant, the approximate energy changes of C_a for S_1 and S_2 are, respectively,

$$\Delta E_{\rm S1} > \frac{1}{2}\frac{V_o^2t_{\rm w}^2}{L_a(V_{ca\max}-V_o)}V_{ca\max} \quad (19)$$

and

$$\Delta E_{\rm S2} > \frac{1}{2}\frac{(V_{ca\min}-V_o)t_{\rm w}^2}{L_a}V_{ca\min}. \quad (20)$$

Assuming the voltage regulation range of v_{ca} is from $V_{ca\min}$ to $V_{ca\max}$, the maximum number of switching cycles needed for the completion of the voltage adjustment process is

$$N_{\rm switchmax} = \max\left\{\frac{\frac{1}{2}C_a(V_{ca\max}^2-V_{ca\min}^2)}{\Delta E_{\rm S1}}\right.$$
$$\left.\frac{\frac{1}{2}C_a(V_{ca\max}^2-V_{ca\min}^2)}{\Delta E_{\rm S2}}\right\}. \quad (21)$$

If the smallest load-step interval is $t_{\rm loadmin}$, then $N_{\rm switchmax}$ times of cycles of S_1 or S_2 must be completed during $t_{\rm loadmin}$. The switching interval can be derived as

$$t_{\rm int} = \frac{t_{\rm loadmin}}{N_{\rm switchmax}}. \quad (22)$$

APPENDIX 2
DETAILS OF EXPERIMENTAL SETUP

The schematics diagrams of the converter and the auxiliary circuit are given in Figs. 15 and 16, respectively. The mechanism of the auxiliary circuit and control is as follows. The top left corner of Fig. 16 shows the adding unit circuit for the capacitor current, the inductor current, and the auxiliary current. The signal representing the load current step ("LoadStep-down" and "LoadStep-up") is generated by the step detection circuit at the top-right corner. Once a load step appears, this circuit will generate a negative pulse with duration t_s. The sensed filter capacitor current signal (bottom left of the figure) is fed into two zero-crossing comparators to generate two different signals ("ZcCompStep-down" and "ZcCompStep-up") for a step-down load or a step-up load, respectively. Switch S_1 or S_2 will be turned "OFF" when the negative pulse appears and "ON" when the zero crossing signal returns to "1."

The energy regulation signals "AuxE↑" and "AuxE↓" (middle right) provide the direction as to whether the auxiliary circuit should increase or decrease v_{ca} with respect to the reference. The reference signal is generated by the external MCU controller board using the sampled output current and an i_o-to-v_{ca} software algorithm.

The control signals for S_1, S_2 and the main converter switch are generated by the "digital logic module." The principle of the control has been presented in Section III. When the load is constant and the main converter is operating at steady state, the control signal of the main converter switch will be equal to the PWM controller output. However, when a load step is detected, the control signal will be locked at "ON" or "OFF" depending on the polarity of the load step.

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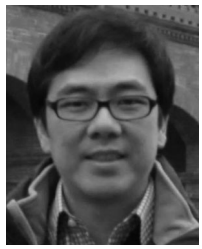

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