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Phase-Shift Interleaving Control of Variable-Phase Switched-Capacitor Converters

Sitthisak Kiratipongvoot, Siew-Chong Tan, *Senior Member, IEEE*, and Adrian Ioinovici, *Fellow, IEEE*

***Abstract*—This paper proposes a phase-shift interleaving control method for variable-phase switched-capacitor (SC) converters that can perform voltage conversions with little electromagnetic interference over a wide range of operating condition. This is achieved by having multiple units of SC converter connected in parallel and an N-state hysteresis unit selection control scheme which works along the interleaving control to vary the number of converters in operation. By having the capacitors of inactive units connected to the output and the converters operating with output interleaving operation, the output capacitor that is typically required in SC converters for maintaining a small voltage ripple is made redundant in this configuration. A three-unit SC converter of the proposed configuration is described in this paper. Experimental results show that the proposed solution works satisfactorily with good regulation, input and output interleaving operations, and dynamic response for a wide operating range.**

***Index Terms*—Interleaving, parallel, phase-shift control, power converters, switched-capacitor (SC) converters.**

I. Introduction

A TYPICAL switched-capacitor (SC) converter is a standalone converter made up of one or more circuit phases of capacitors and switches that are controlled by pulsewidth-modulation (PWM) control [1]–[23]. An SC converter with PWM control, however, inherits the problem of having a large pulsating input current, which leads to electromagnetic interference (EMI) problems [21].

A possible method of alleviating the EMI issue in SC converters is to reconfigure multiple units of SC converters as a parallel converter (instead of a single standalone SC converter) and to operate the units in interleaving operations applied at both the input and output terminals [23]–[27]. This method has the additional advantage of increasing the power rating of the converter. However, they work perfectly in a steady-state operation but fail to give the expected results from interleaving when a variation appears in the input voltage or load.

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An adaptive solution combining the on-time control and the switching frequency control, which ensures the output regulation and the proper input/output interleaving of the SC converter under a varying load and input voltage, is proposed in [28]. **However, the method is only valid for a limited range of load and input voltage conditions**. For [28], the load range of the converter is limited to 75%–100% of the full-load power.

In this paper, we propose a phase-shift interleaving control method that incorporates an N-state hysteresis unit selection scheme which varies the number of active SC converter units in operation based on the level of the operating load and, at the same time, adopts a variable frequency control to maintain the input and output interleaving operations and voltage regulation. **The proposed method adopts a fundamentally different control architecture from that of** [28]. **Additionally, it allows the SC converter to be optimally configured such that all the capacitors are always in a charging or discharging process and never in a holding or idling state. This ensures the maximum transfer of energy from the input source to the load by the SC converter using the least required capacitance. Hence, the usage of capacitors in the SC converter will be optimized with this control approach, thereby optimizing the power density of the SC converter which is previously not possible with the control method proposed in** [28].

II. Proposed Phase-Shift Interleaving Control

A. Topology

The variable-phase SC converter is made up of N number of SC converter units (depending upon the load) connected in parallel. As an illustration, a three-unit configuration is chosen (see Fig. 1). Each unit comprises two phases of SC circuit as discussed in [28]. The converter is designed for three ranges of load, which can be classified as light, medium, and heavy load.

B. Operating States and Timing Diagrams

1) Light Load: Unit 1 is active and is operated to perform both the charging and discharging operations. The remaining two units are inactive and are switched for discharging operation with their flying capacitors connected to the output load throughout the light-load condition. Fig. 2(a) shows the timing diagram. There are two states. In State 1 $(0 < t \leq T_S/2)$, C_{11} is operated in charging phase, and the remaining capacitors C_{12}, C_{21}, C_{22}, C_{31}, and C_{32} are operated in discharging phase [see Fig. 2(c)]. Here, $r_{\rm ch}$ and $r_{\rm eq}$ are equivalent resistances of the circuit. Stray inductance is neglected since they are relatively

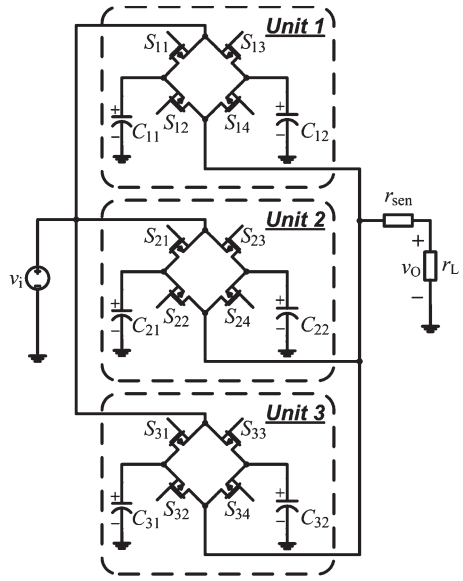

Fig. 1. Three-unit configuration of the proposed SC converter.

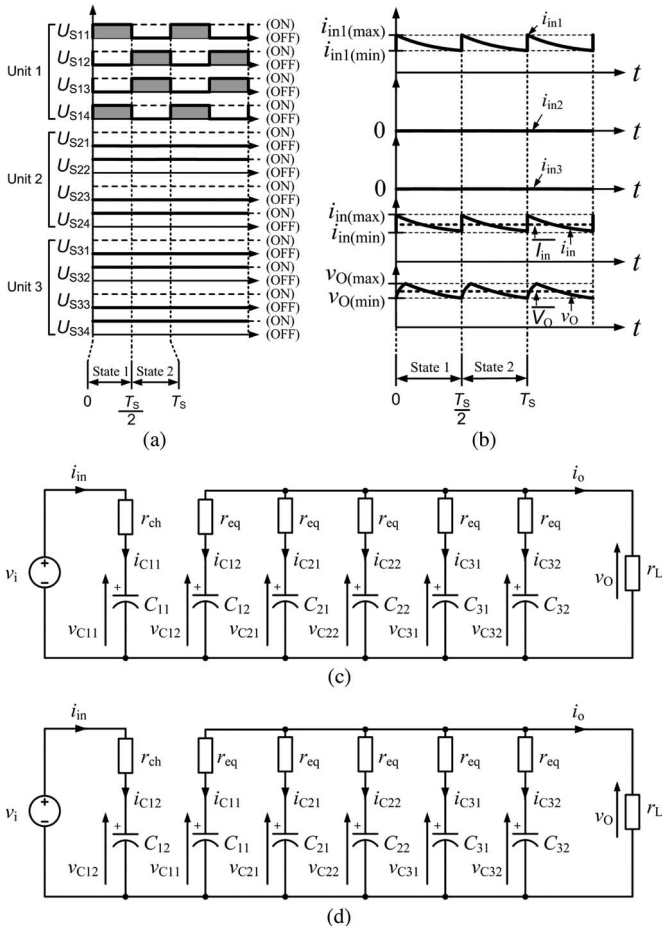

Fig. 2. Operation at light-load condition. (a) Timing diagram. (b) Current and voltage waveforms. (c) State 1. (d) State 2.

small. In State 2 ($T_S/2 < t \leq T_S$), C_{12} is operated in charging phase, and all other capacitors are operated in discharging phase [see Fig. 2(d)]. The unit current, overall converter input current, and output voltage are shown in Fig. 2(b), of which $i_{\rm in}$ is the total input current and $i_{{\rm in}x}$, where $x = 1$, 2, *and* 3, is the input

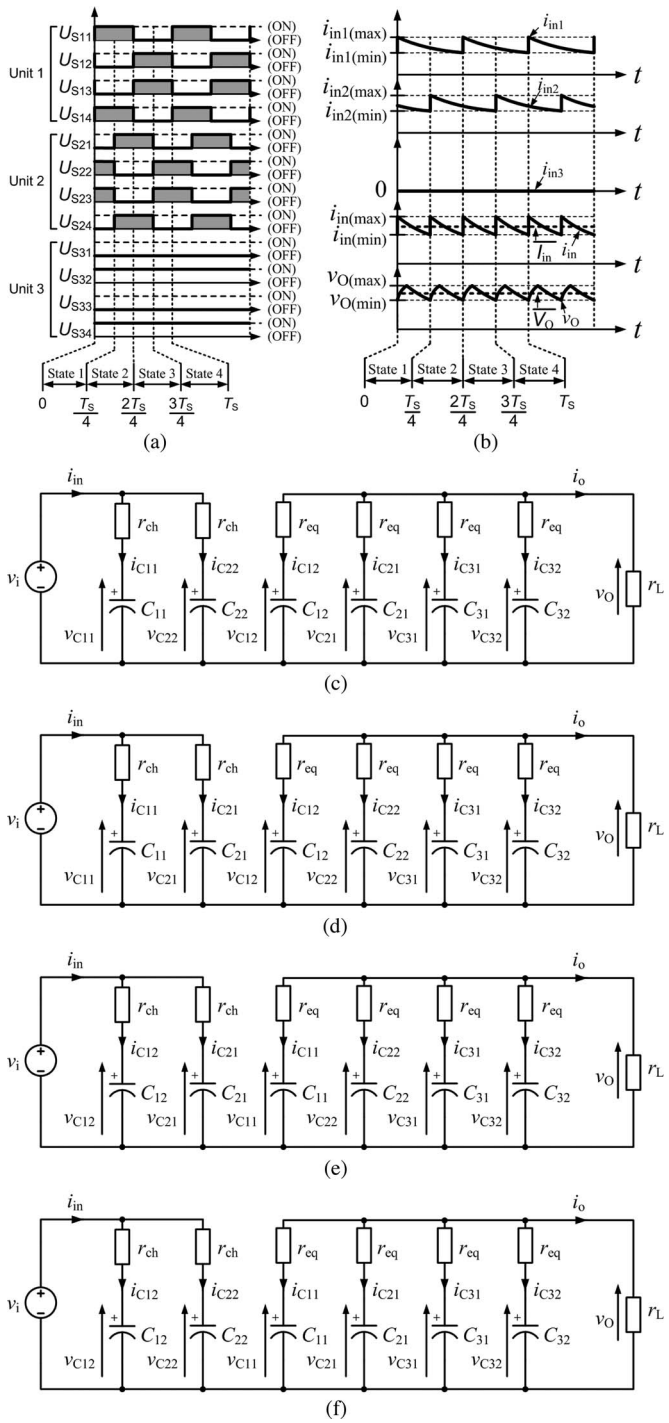

Fig. 3. Operation at medium-load condition. (a) Timing diagram. (b) Current and voltage waveforms. (c) State 1. (d) State 2. (e) State 3. (f) State 4.

current of each SC unit. Here, the frequency of the input current and the output voltage is two times the switching frequency of each converter unit. Without output interleaving, the output voltage ripple is minimized by the flying capacitors of the inactive units.

2) Medium Load: There are two active units operated with interleaving charging and discharging operations with a time delay of $T_S/4$. The other unit is inactive and is operated in the discharging operation. Fig. 3(a) shows the timing diagram, and Fig. 3(b) shows the unit current, input current, and output

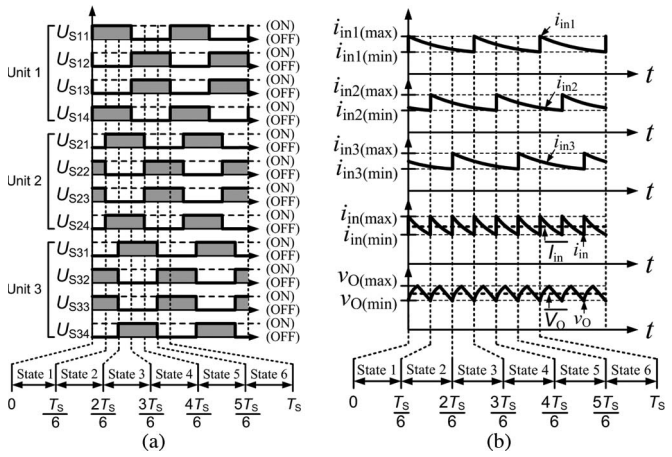

Fig. 4. Operation at heavy-load condition. (a) Timing diagram. (b) Current and voltage waveforms.

voltage waveforms. There are four operating states. In State 1 $(0 < t \leq T_S/4)$, C_{11} and C_{22} are in the charging phase, and the remaining flying capacitors are in the discharging phase [see Fig. 3(c)]. In State 2 $(T_S/4 < t \leq 2T_S/4)$, C_{11} and C_{21} are in the charging phase, and all other flying capacitors are in the discharging phase. In State 3 $(2T_S/4 < t \leq 3T_S/4)$, only C_{12} and C_{21} are in the charging phase [see Fig. 3(e)]. In State 4 $(3T_S/4 < t \leq T_S)$, only C_{12} and C_{22} are in the charging phase. The input current is the summation of the currents of Units 1 and 2. The frequency of the input current and output voltage is four times the switching frequency of each SC converter unit. Here, the output ripple is minimized by the output interleaving operation of the two active units and also the flying capacitors of the remaining inactive unit.

3) Heavy Load: All three converter units are actively operated with interleaved charging and discharging operations with a time delay $T_S/6$. The timing diagram is shown in Fig. 4(a). Fig. 4(b) shows the unit current, input current, and output voltage waveforms. The frequency of the input current and output voltage is six times the switching frequency of each SC converter unit. Here, the output ripple is minimized solely by the output interleaving operation.

C. Control Methodology

1) Hysteresis Unit Selection Scheme: The state selection diagram is shown in Fig. 5(a). There are three modes and four transition points. The unit selection scheme is shown in Fig. 5(b). When the output current of the converter operating with one active unit is increased $(A_{1U(\text{increase})})$ to $i_{\text{ac},12}$, the operating mode switches to two active units. When the output current of the converter operating with two active units is increased $(A_{2U(\text{increase})})$ to $i_{\text{ac},23}$, the operating mode is changed to three active units. Now, when the output current of the converter operating with three active units is reduced $(A_{3U(\text{reduced})})$ to $i_{\text{ac},32}$, the operating mode is changed back to two active units and so on.

2) Feedback Control: Fig. 6 shows an overview of the proposed control. There are two feedback signals, namely, the output voltage and the output current. The proportional–integral

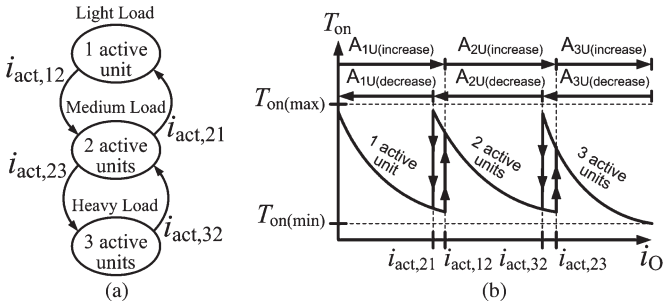

Fig. 5. Unit selection scheme of the proposed control. (a) State diagram. (b) Unit selection scheme.

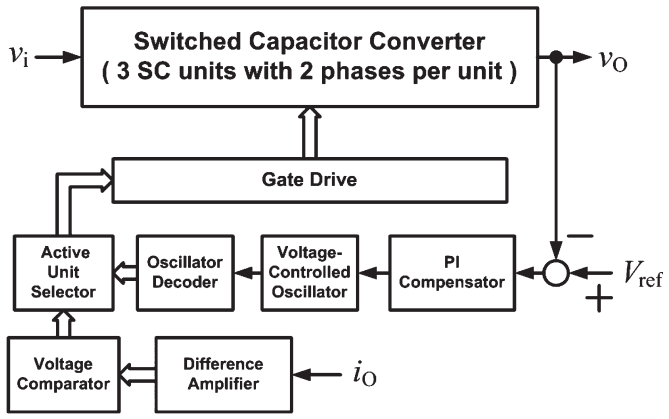

Fig. 6. Closed-loop control block diagram.

compensator amplifies the difference between the output and the reference voltages, which is fed into the voltage-controlled oscillator to generate a frequency f_{VCO}. This is decoded into four signals by the oscillator decoder. The charging signals have a switching frequency $f_S = f_{\text{VCO}}/12$, a duty ratio $D_{\text{on}} = 0.5$, and an interleaving time delay $T_D = 1/(2nf_S)$ for the case of having more than one active unit. The sensed output current signal is required for unit selection. It is fed into the low-pass filter with gain compensation and is compared with the current reference of the voltage comparator. These output signals are fed into the gate drives. Discharging signals are inverse of the charging signals.

III. Theoretical Proofs

As discharging time constant τ_{dis} is much larger than the discharging time duration $T_{\text{dis}} = T_{\text{on}}/n$, the relationship of each capacitor with its ripple voltage can be approximated as

$$v_{C(\max)} - v_{C(\min)} = \frac{T_{\text{on}}\overline{V_O}}{nr_L C} \tag{1}$$

where $C = C_{11} = C_{12} = C_{21} = \ldots = C_{32}$; $v_{C(\max)}$ and $v_{C(\min)}$ are the maximum and minimum voltages of C, respectively; n is the number of active units; T_{on} is the charging time of one active unit of the converter; $\overline{V_O}$ is the average output voltage; and r_L is the load.

Fig. 7(a) shows the discharging circuit of one active-unit mode, and Fig. 7(b) shows its equivalent circuit. The minimum voltage of the equivalent discharging capacitor $v_{\text{Cdis}(\min)}$ is simply the minimum voltage of capacitor $v_{C(\min)}$.

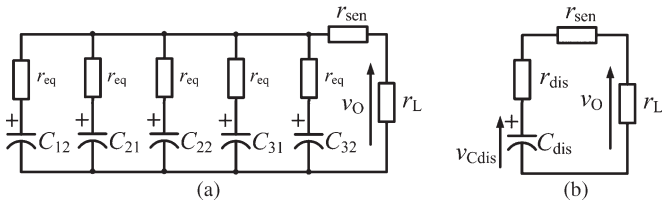

Fig. 7. (a) Discharging circuit of one active-unit mode and (b) its equivalent circuit.

The maximum voltage of $C_{\rm dis}$ in terms of $v_{C(\max)}$ and $v_{C(\min)}$ after the energy redistribution process between parallel capacitors is

$$v_{\rm Cdis(max)} = \frac{v_{C(\max)}}{(2N-n)} + \frac{(2N-n-1)v_{C(\min)}}{(2N-n)}. \quad (2)$$

Equation (2) can be derived by considering (1) as

$$v_{\rm Cdis(max)} = \frac{T_{\rm on}\overline{V_O}}{(2N-n)nr_LC} + v_{C(\min)}. \quad (3)$$

Additionally, the average voltage of $C_{\rm dis}$ is

$$\frac{v_{\rm Cdis(max)} + v_{\rm Cdis(min)}}{2} = \frac{r_{\rm eq}\overline{V_O}}{(2N-n)r_L} + \frac{(r_{\rm sen}+r_L)\overline{V_O}}{r_L} \quad (4)$$

where $r_{\rm sen}$ is the output current sensing resistance. Substituting (3) into (4), we have

$$v_{C(\min)} = \frac{r_{\rm eq}\overline{V_O}}{(2N-n)r_L} + \frac{(r_{\rm sen}+r_L)\overline{V_O}}{r_L} - \frac{T_{\rm on}\overline{V_O}}{2(2N-n)nr_LC}. \quad (5)$$

Finally, the dc conversion ratio of the variable-phase SC converter can be derived as

$$\frac{\overline{V_O}}{v_i} = \frac{2nr_LC}{\alpha_1+\alpha_2} \quad (6)$$

where $\alpha_1 = T_{\rm on}[\coth(T_{\rm on}/2r_{\rm ch}C) + 1 - (1/(2N-n))]$ and $\alpha_2 = [(2nrC/(2N-n))] + 2(r_{\rm sen}+r_L)C$. The derivation is given in Appendix A.

A. Output Ripple

As given in Appendix B, the output ripple can be derived from the discharging characteristic as

$$V_{\rm O(rip)} = \frac{T_{\rm on}\overline{V_O}}{[r_{\rm eq}+(2N-n)(r_{\rm sen}+r_L)]\,nC}. \quad (7)$$

B. Boundary Condition of the Proposed Control Solution

The range of the input voltage that can sustain the interleaving condition can be found by solving (6) for $0 \le T_{\rm on} \le 4\tau_{\rm ch}$ (refer to Appendix C) as

$$\begin{cases} v_i \ge \frac{[r_{\rm eq}+(2N-n)(r_{\rm sen}+r_L)]\overline{V_O}}{(2N-n)r_L} + \frac{r_{\rm ch}\overline{V_O}}{nr_L} \\ v_i \le \frac{\left[r_{\rm eq}+(2N-n)(r_{\rm sen}+r_L)-\left(\frac{2}{n}\right)r_{\rm ch}\right]\overline{V_O}}{(2N-n)r_L} + \frac{4.0746r_{\rm ch}\overline{V_O}}{nr_L}. \end{cases} \quad (8)$$

IV. Experimental Results and Discussions

A. Prototype

The schematic and a photograph of the experimental prototype of the proposed control and the variable-phase SC converter are shown in Figs. 8 and 9, respectively. Table I gives the specifications of the converter. The values of the transition points $i_{\rm act21}$, $i_{\rm act12}$, $i_{\rm act32}$, and $i_{\rm act23}$ are found by first obtaining the output current I_O range of the SC converter for different n values under open-loop control. With these ranges found, their overlapped regions between different n values can be determined. The transition points are arbitrarily chosen within the overlapped regions such that, for the specified operating mode, the voltage ripple of the converter is always within its specified value.

B. Closed-Loop Performance

Fig. 10(a)–(c) shows the total input current of the SC converter and the current of each unit when it operates with an output current at 4 A (light-load mode with one active unit), at 7.3 A (medium-load mode with two active units), and at 10.1 A (heavy-load mode with three active units), respectively. The switching frequency of each unit is 75.3 kHz ($T_{\rm on} = 6.64\ \mu$s).

Fig. 11(a)–(c) shows the total input current, phase current, capacitor voltage, and output voltage ripple when $T_{\rm on}$ is 3.98 μs. This demonstrates that, regardless of the turn-on time [as compared to Fig. 10(a)–(c)], perfect interleaving at different loads and active modes is always achieved. The maximum output voltage ripple is within 10% of nominal voltage for the entire load range, which is within the predesigned specification. The ripple can be reduced by a larger flying capacitance value.

Fig. 12(a) shows the plots of the measured output voltage versus the output current of this prototype and that presented in [28]. With the proposed control, the converter has a much wider load range and a better load regulation of around 1% over the entire range. From Fig. 12(b), the power efficiency, however, is lower with this control as compared to that in [28] since the latter utilizes all four units in parallel in the power conversion which leads to a lower equivalent resistance and hence less losses.

C. Dynamic Performance

Fig. 13(a)–(c) shows the transient response of the prototype. For step-load change between 2.5 and 6.0 A [Fig. 13(a)], the settling time is around 500 μs for both step-up and step-down conditions. For step-load change between 2.5 and 10.0 A [Fig. 13(b)], the settling time is around 500 μs (step down) and 4 ms (step up). For change between 6.0 and 10.0 A [Fig. 13(c)], the settling time is around 1 (step down) and 4 ms (step up). Notice that, during the load disturbance, the SC converter still operates in perfect interleaving condition.

V. Further Discussion: Generic Application

The discussion by far is based on a unity transformation gain dual-phase SC converter in which the voltage conversion

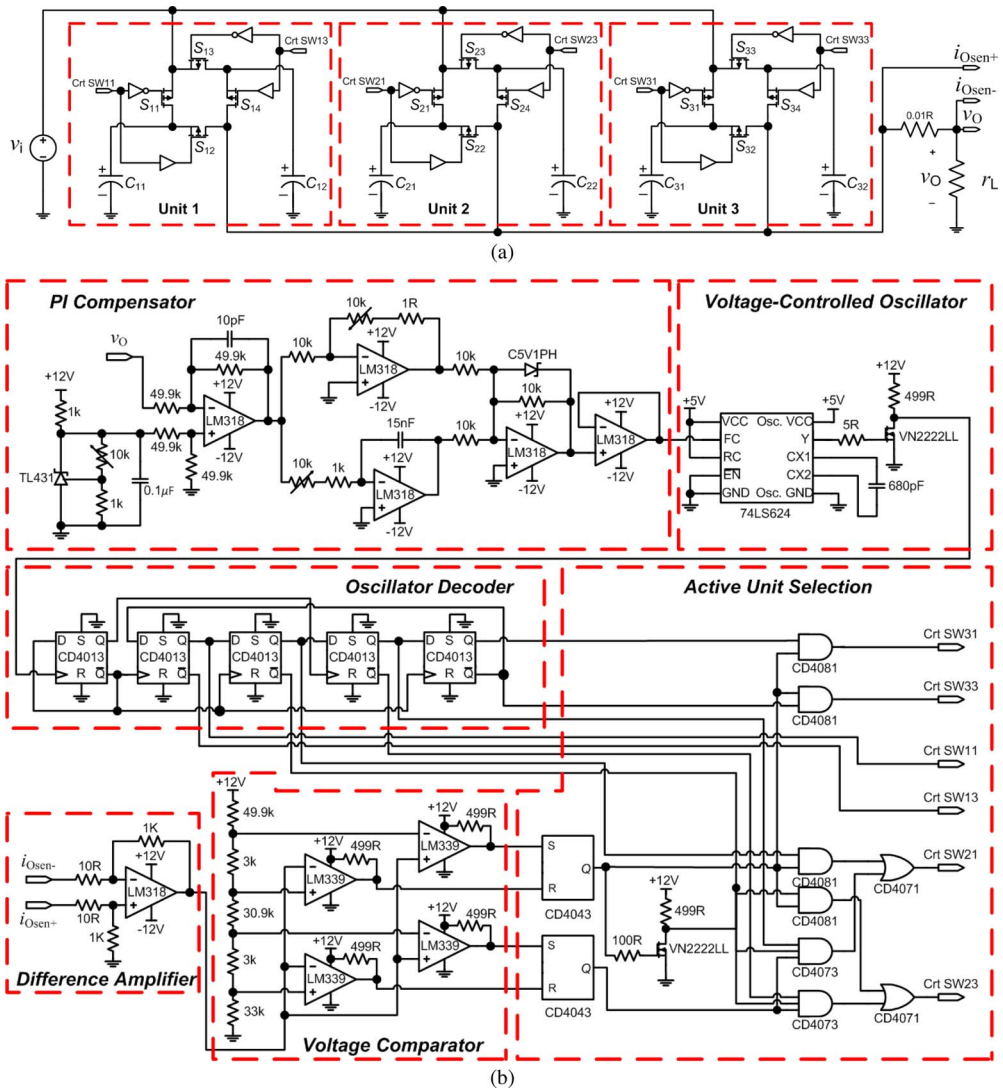

Fig. 8. Schematic of the experimental prototype. (a) Multiphase SC converter with driving circuit. (b) Control circuit.

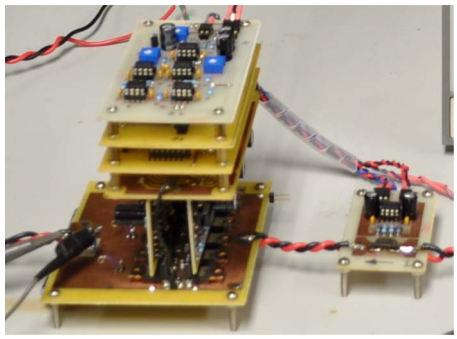

Fig. 9. Photograph of the experimental prototype.

TABLE I
SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE

v_{i}	12 V
V_{O}	9 V
P_{O}	18–99 W
$i_{\mathrm{act},21}$	4.11 A
$i_{\mathrm{act},12}$	4.48 A
$i_{\mathrm{act},32}$	8.33 A
$i_{\mathrm{act},23}$	8.70 A
S_{11}, S_{13}, S_{21} S_{23}, S_{31}, S_{33}	IRF9520: $I_{\mathrm{d}} = -6.8$ A $V_{\mathrm{ds}} = -100$ V, $R_{\mathrm{ds(on)}} = 0.48\ \Omega$
S_{12}, S_{14}, S_{22} S_{24}, S_{32}, S_{34}	IRF5305: $I_{\mathrm{d}} = -31$ A $V_{\mathrm{ds}} = -55$ V, $R_{\mathrm{ds(on)}} = 0.065\ \Omega$
Gate drivers	MC33151 (charging), MC33152 (discharging)
C_{11}, C_{12}, C_{21} C_{22}, C_{31}, C_{32}	Multi-layer ceramic capacitors EMK325BJ476MM: 47 μF, ESR = 10 mΩ)
Voltage control	$G_{\mathrm{PI}}(s) = 0.284 + \frac{6060}{s}$ (by trial-and-error tuning)
Dead time	Inserted by oscillator detector & active unit selection

gain is ideally $\overline{V_O}/v_i = G$. Here, the proposed idea is extended to the more "practical" types of an N-SC converter that has an M step-down (i.e., $M < 1$) or step-up (i.e., $M > 1$) conversion gain. The overall voltage conversion gain of these SC converters is $\overline{V_O}/v_i = G \cdot M$. Readers are referred to [28] for the step-up/step-down SC converter topology, interleaving configuration, and parameter conversion table. Fig. 14(a) and (b) shows the equivalent circuit of a general SC converter after the application of the proposed control.

Here, the general steady-state charging equation is

$$v_{\mathrm{Cch(max)}} - v_{\mathrm{Cch(min)}} = v_i \varepsilon - v_{\mathrm{Cch(min)}} \varepsilon \tag{9}$$

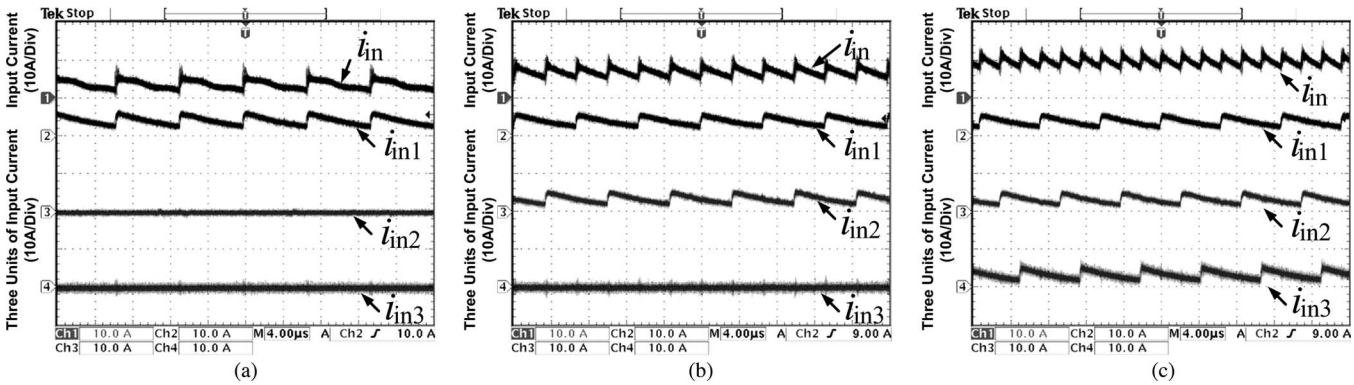

Fig. 10. Waveforms of the input current and per-unit currents of the prototype. (a) At $i_o = 4$ A (one active unit). (b) At $i_o = 7.3$ A (two active units). (c) At $i_o = 10.1$ A (three active units).

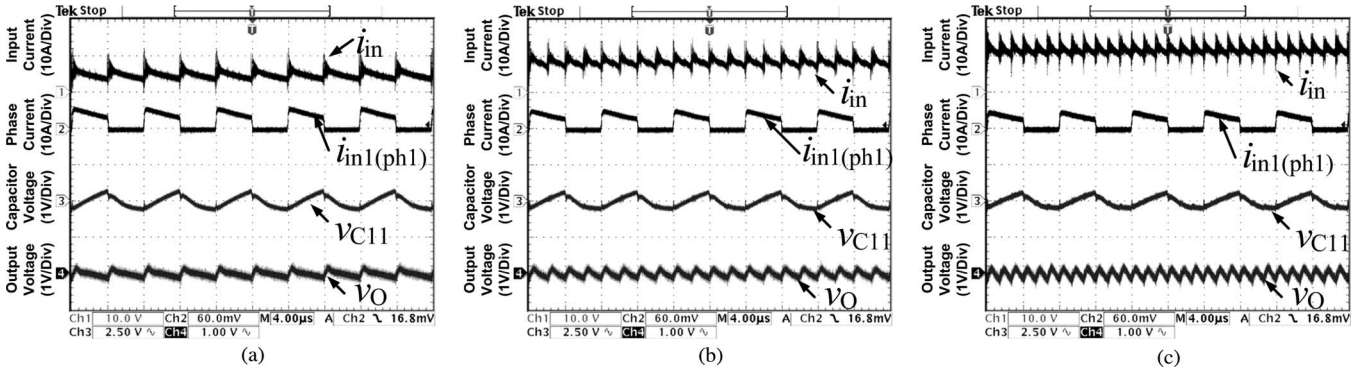

Fig. 11. Waveforms of the total input current, phase current, capacitor voltage, and output voltage of the prototype. (a) At $i_o = 4.60$ A (one active unit). (b) At $i_o = 8.27$ A (two active units). (c) At $i_o = 11.38$ A (three active units).

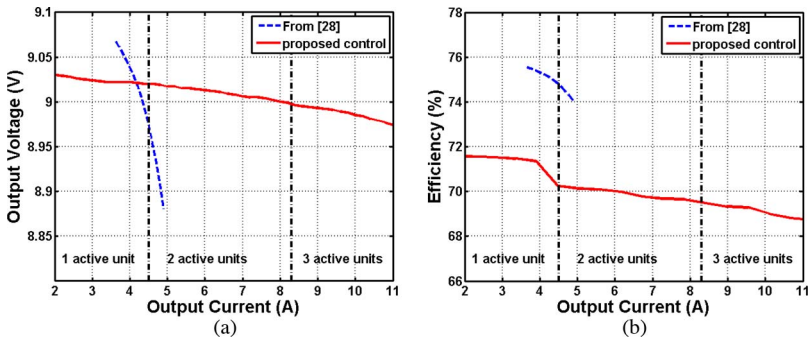

Fig. 12. Plots of (a) the load regulation and (b) the power efficiency of this prototype and that presented in [28]. (a) Load regulation. (b) Power efficiency.

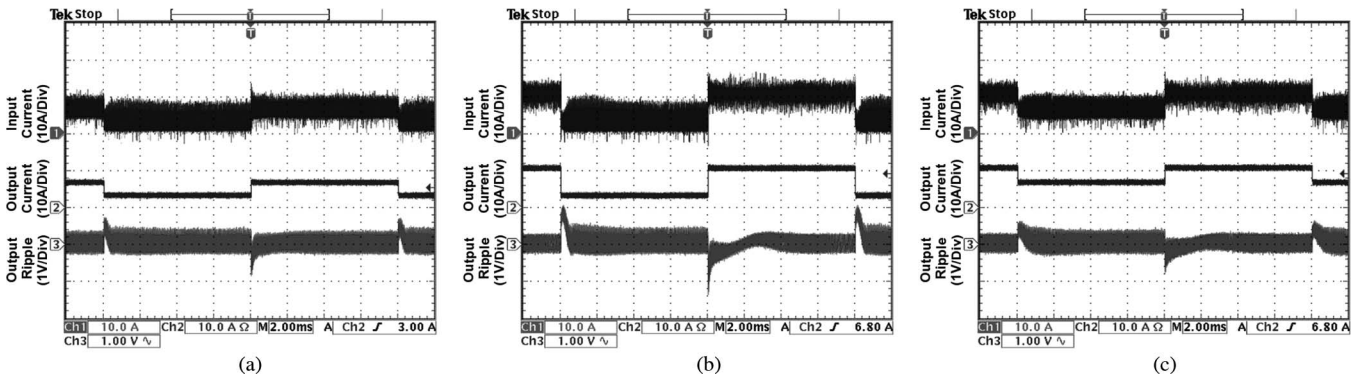

Fig. 13. Waveforms of total input current, output current, and output voltage with step-load change. (a) Load change between 2.5 and 6.0 A. (b) Load change between 2.5 and 10.0 A. (c) Load change between 6.0 and 10.0 A.

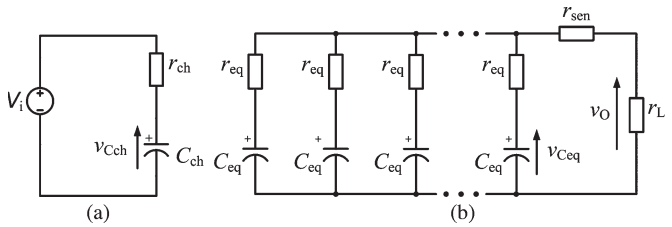

Fig. 14. (a) Equivalent charging circuit and (b) equivalent discharging circuit of a general SC converter with the proposed control.

where $\varepsilon = 1 - e^{[-T_{\rm on}/r_{\rm ch}C_{\rm ch}]}$. The ripple voltage of $C_{\rm ch}$ is

$$v_{\rm Cch(max)} - v_{\rm Cch(min)} = \frac{1}{M}\left[\frac{T_{\rm on}\overline{V_O}}{nr_L C_{\rm eq}}\right]. \tag{10}$$

The minimum voltage of $C_{\rm ch}$ can be derived in terms of the discharging circuit parameters as

$$v_{\rm Cch(min)} = \frac{[r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L)]\,\overline{V_O}}{M(2N-n)r_L} - \frac{T_{\rm on}\overline{V_O}}{2M(2N-n)nr_L C_{\rm eq}}. \tag{11}$$

Using the approach described in Appendix A, the dc conversion ratio can be derived as

$$\frac{\overline{V_O}}{v_i} = \frac{2Mnr_L C_{\rm eq}}{T_{\rm on}\gamma + \frac{2nr_{\rm eq}C_{\rm eq}}{(2N-n)} + 2(r_{\rm sen}+r_L)nC_{\rm eq}} \tag{12}$$

where $\gamma = \coth(T_{\rm on}/2r_{\rm ch}C_{\rm ch}) + 1 - (1/(2N-n))$. Following Appendix B, the output ripple is derived as

$$V_{\rm O(rip)} = \frac{T_{\rm on}\overline{V_O}}{[r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L]\,nC_{\rm eq}}. \tag{13}$$

VI. Design Procedure

A. Design Specifications

Define v_i, $\overline{V_O}$, maximum output current $\overline{I_O}$, and maximum switching frequency $f_{S(\max)}$.

B. Find Transformation Gain M of Converter

The overall input-to-output voltage conversion gain is

$$Y = G \cdot M = \left|\frac{\overline{V_O}}{v_i}\right| \tag{14}$$

and the type of the SC converter units and the transformation gain M is found from

$$M = \begin{cases} \frac{1}{\lfloor \frac{1}{Y} \rfloor}, & \text{if } Y \le 0.5 \text{ (step-down converter)} \\ 1 \quad , & \text{if } 0.5 < Y <; 1 \text{ (unity-gain converter)} \\ \lceil Y \rceil, & \text{if } Y \ge 1 \text{ (step-up converter).} \end{cases} \tag{15}$$

C. Determine $r_{\rm ch}$

With appropriate switches selected based on power rating and converter type, $r_{\rm ds(on)}$ is known. Since capacitor equivalent series resistance is much smaller than $r_{\rm ds(on)}$, the charging resistance of each unit is mainly dependent on $r_{\rm ds(on)}$. The charging resistance is

$$r_{\rm ch} = \begin{cases} \left(1 + \frac{1}{M}\right) r_{\rm ds(on)} & \text{for step-down converter} \\ r_{\rm ds(on)} & \text{for unity-gain converter} \\ \frac{2r_{\rm ds(on)}}{M} & \text{for step-up converter.} \end{cases} \tag{16}$$

D. Find Total Number of SC Units N

The total number of units is calculated from

$$N = \left\lceil \frac{M^2 r_{\rm ch}\overline{I_O}}{Mv_i - \overline{V_O}} \right\rceil. \tag{17}$$

E. Find Load Range for Different n Values

From (8), the output current range is

$$\frac{(Mv_i - \overline{V_O})}{\frac{2r_{\rm ch}M^2}{n}(\coth(2) + \lambda_1) + \beta_1} \le \overline{I_O} \le \frac{(Mv_i - \overline{V_O})}{\frac{r_{\rm ch}M^2}{n} + \beta_1} \tag{18}$$

where

$$r_{\rm eq} = \begin{cases} 2Mr_{\rm ds(on)} & \text{for step-down converter} \\ r_{\rm ds(on)} & \text{for unity-gain converter} \\ (1+M)r_{\rm ds(on)} & \text{for step-up converter} \end{cases} \tag{19}$$

$\lambda_1 = (2N-n-1)/(2N-n)$, and $\beta_1 = r_{\rm eq}/(2N-n)$. For $n = 1, 2, \ldots, N$, find the ranges.

F. Choose Capacitor Value

Equation (13) can be modified as

$$Cf_{S(\min)} \ge \frac{50M}{\left[r_{\rm eq} + \frac{(2N-1)\overline{V_O}}{\overline{I_{\rm O(min),1}}}\right]\%V_{\rm O(rip)}} \tag{20}$$

where $f_{S(\min)}$ is the minimum frequency for ensuring that output voltage ripple is within a desired percentage $\%V_{\rm O(rip)}$. Here, $\overline{I_{\rm O(min),1}}$ is the lower value of inequality (18) for $n = 1$. With a selected minimum switching frequency, C can be chosen.

G. Define Transition Points

The transition points must be designed within the overlapped region of the output currents of incremental n units. For example, if the output current at $n = 1$ is in the range of $\overline{I_{\rm O(min),1}} \le I_O \le \overline{I_{\rm O(max),1}}$ and that at $n = 2$ is in the range of $\overline{I_{\rm O(min),2}} \le I_O \le \overline{I_{\rm O(max),2}}$, where $\overline{I_{\rm O(max),1}} > \overline{I_{\rm O(min),2}}$, the overlapped region will be $\Delta I_{12} = \overline{I_{\rm O(max),1}} - \overline{I_{\rm O(min),2}}$. The transition point for switching from $n = 1$ to $n = 2$ can be derived as

$$i_{\rm act,12} = \overline{I_{\rm O(max),1}} - \Psi\Delta I_{12} \tag{21}$$

and the transition point for switching from $n = 2$ to $n = 1$ can be derived as

$$i_{\rm act,21} = \Psi\Delta I_{12} + \overline{I_{\rm O(min),2}} \tag{22}$$

where Ψ is a scaling factor in the range of $0 < \Psi < 0.5$.

VII. Conclusion

A phase-shift interleaving control with N-state hysteresis unit selection scheme has been proposed to widen the range of operating condition of variable-phase SC converters while maintaining a continuous input current. In the proposed configuration, a relatively low output voltage ripple is achieved regardless of the frequency, by using a high equivalent output capacitance ($C_{\rm out} = (2N-1)C$) when the load is light and by using a smaller equivalent output capacitance ($C_{\rm out} = NC$) when the load is heavy, along with the output interleaving operation. The experimental results confirm the theoretical proof: The proposed control gives good regulation, nonpulsatory input current, small output voltage ripple, and good dynamic response for a wide operating range.

Appendix A
Derivation of DC Conversion Ratio

According to the charging condition, the steady-state ripple equation of the flying capacitor is

$$v_{C(\max)} - v_{C(\min)} = \left(v_i - v_{C(\min)}\right)\left[1 - e^{\frac{-T_{\rm on}}{r_{\rm ch}C}}\right]. \quad (23)$$

Substituting (1) and (5) into (23) gives

$$2(2N-n)nr_LC\frac{v_i}{\overline{V_O}} = T_{\rm on}\left[\frac{2(2N-n)}{1-e^{\frac{-T_{\rm on}}{r_{\rm ch}C}}} - 1\right] + \left(2\left[r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L)\right]nC\right). \quad (24)$$

The term $2(2N-n)/(1-e^{-T_{\rm on}/r_{\rm ch}C})$ can be derived as

$$\frac{2(2N-n)}{1-e^{\frac{-T_{\rm on}}{r_{\rm ch}C}}} = (2N-n)\left[\coth\left(\frac{T_{\rm on}}{2r_{\rm ch}C}\right)+1\right]. \quad (25)$$

Substituting (25) into (24) and dividing it by $2N-n$ gives

$$\frac{\overline{V_O}}{v_i} = \frac{2nr_LC}{\alpha_1+\alpha_2} \quad (26)$$

where $\alpha_1 = T_{\rm on}[\coth(T_{\rm on}/2r_{\rm ch}C) + 1 - (1/(2N-n))]$ and $\alpha_2 = [2nrC/(2N-n)] + 2(r_{\rm sen}+r_L)C$.

Appendix B
Derivation of Output Voltage Ripple

The equation describing the output charge of $C_{\rm dis}$ flowing to the load is

$$C_{\rm dis}\left(v_{\rm Cdis(max)} - v_{\rm Cdis(min)}\right) = \frac{T_{\rm dis}\overline{V_O}}{r_L}. \quad (27)$$

Since $C_{\rm dis} = (2N-n)C$, $v_{\rm Cdis(max)} - v_{\rm Cdis(min)} = \lambda_6(v_{\rm Omax} - v_{\rm Omin})$ (by voltage divider law) where $\lambda_6 = (r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L))/(2N-n)r_L$, and by substituting $T_{\rm dis} = T_{\rm on}/n$ into (27), we have

$$(2N-n)C\lambda_6(v_{\rm Omax} - v_{\rm Omin}) = \frac{T_{\rm on}\overline{V_O}}{nr_L}. \quad (28)$$

The output voltage ripple $V_{\rm O(rip)} = v_{\rm Omax} - v_{\rm Omin}$ is

$$V_{\rm O(rip)} = \frac{T_{\rm on}\overline{V_O}}{\left[r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L)\right]nC}. \quad (29)$$

Appendix C
Derivation of Boundary Condition

Equation (6) can be rewritten as

$$v_i = \frac{T_{\rm on}}{2nr_LC}\left[\coth\left(\frac{T_{\rm on}}{2r_{\rm ch}C}\right) + 1 - \frac{1}{2N-n}\right]\overline{V_O} + \frac{r_{\rm eq} + (2N-n)(r_L+r_{\rm sen})}{(2N-n)r_L}\overline{V_O}. \quad (30)$$

A. Lower Boundary Limit

Substituting $T_{\rm on} = 0$ into (30) gives

$$v_i \geq \lim_{T_{\rm on}\to 0}\left[\frac{T_{\rm on}}{2nr_LC}\coth\left(\frac{T_{\rm on}}{2r_{\rm ch}C}\right)\right]\overline{V_O} + \frac{r_{\rm eq} + (2N-n)(r_L+r_{\rm sen})}{(2N-n)r_L}\overline{V_O}. \quad (31)$$

The term $\lim_{T_{\rm on}\to 0}[(T_{\rm on}/2nr_LC)\coth(T_{\rm on}/2r_{\rm ch}C)]$ can be solved using L'Hôpital's rule as

$$\begin{aligned}\lim_{T_{\rm on}\to 0}\left[\frac{T_{\rm on}}{2nr_LC}\coth\left(\frac{T_{\rm on}}{2r_{\rm ch}C}\right)\right] &= \lim_{T_{\rm on}\to 0}\left[\frac{\frac{d}{dT_{\rm on}}\left(\frac{T_{\rm on}}{2nr_LC}\right)}{\frac{d}{dT_{\rm on}}\left(\tanh\left(\frac{T_{\rm on}}{2r_{\rm ch}C}\right)\right)}\right] \\ &= \frac{r_{\rm ch}}{nr_L}. \end{aligned} \quad (32)$$

The substitution of (32) into (31) gives

$$v_i \geq \frac{\left[r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L)\right]\overline{V_O}}{(2N-n)r_L} + \frac{r_{\rm ch}\overline{V_O}}{nr_L} \quad (33)$$

which describes the lower limit of the input voltage.

B. Upper Boundary Limit

The substitution of $T_{\rm on} = 4r_{\rm ch}C$ into (30) gives the upper limit of the input voltage as

$$v_i \leq \frac{\left[r_{\rm eq} + (2N-n)(r_{\rm sen}+r_L) - \left(\frac{2}{n}\right)r_{\rm ch}\right]\overline{V_O}}{(2N-n)r_L} + \frac{4.0746r_{\rm ch}\overline{V_O}}{nr_L}. \quad (34)$$

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