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Citation	IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2014, v. 61 n. 3, p. 930-942
Issued Date	2014
URL	http://hdl.handle.net/10722/196276
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Classification of Auxiliary Circuit Schemes for Feeding Fast Load Transients in Switching Power Supplies

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Abstract—This paper presents a systematic classification of auxiliary circuit schemes for feeding fast load transients in switching power converters. The classification is based on the types of the implementation methods, practical constraints and performance. In particular, auxiliary circuits are classified according to the ways in which they are connected with the power supplies and loads, as well as the choice of control methods. Designed as a shunt output, the “intruding” type of auxiliary circuits is effective and less dissipative. Moreover, to reduce complexity, auxiliary circuits may be designed in the form of a bridge output, and employs a “non-intruding” type of control scheme. Furthermore, provision of pre-informed loading condition leads to further simplification of auxiliary circuitry and improvement of efficiency. Experimental measurements are provided to support the analysis of the properties of various types of circuits.

Index Terms—Auxiliary circuit, classification, dc-dc converter, fast transient.

I. INTRODUCTION

MODERN digital loads, such as microprocessors or digital signal processors (DSPs), impose challenging requirement for power supplies to feed high slew-rate transients [1], [2]. The main challenge in the power supply design is that after the occurrence of a transient, the power supply should keep its output voltage fluctuation within a short transition period and recover itself to a new operation point. If the converter can always keep its output voltage within a specified range around the reference point, e.g., $\pm 2\%$ of the reference value, the response of the power converter is said to produce a null-response to large-signal transients. The fundamental limitation for achieving null-response to large-signal transients is the size of the filter capacitor [3]–[5]. Many nonlinear control schemes, e.g., time optimal control [6]–[9], sliding-mode control [10], boundary control [11], [12], etc., have pushed the dy-

Manuscript received May 30, 2013; revised July 19, 2013; accepted August 20, 2013. Date of publication October 16, 2013; date of current version February 21, 2014. This work was supported by Hong Kong Polytechnic University Research Committee Projects G-U866 and G-YJ32. This paper was recommended by Associate Editor F. M. Neri.

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Digital Object Identifier 10.1109/TCSI.2013.2284174

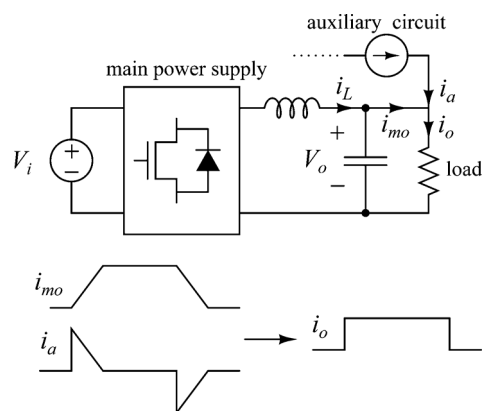


Fig. 1. Equivalent model of auxiliary circuit for fast load transients.

amic performance of a converter near to its physical limit. To achieve further breakthrough without efficiency degradation, a number of methods utilizing auxiliary circuits have been proposed [3]–[5], [13]–[31]. Such auxiliary circuits operate as add-on current sources which will feed current with identical magnitude but in reverse direction to the transient to counteract the fast load change. An equivalent model of the auxiliary circuit is given in Fig. 1.

The use of auxiliary circuits has been proven effective for improving the dynamic response of the original converter. The increased complexity and efficiency reduction due to the use of the auxiliary circuit have been discussed for different practical situations. Specifically, the efficiency reduction has been studied previously in [5], [19], [25]. The problem of efficiency reduction in these schemes becomes significant because high-performance microprocessors operate with transients of huge magnitude and high repeating rate. To achieve optimal performance for specific applications, it is necessary to derive a common set of design principles for the application of auxiliary circuits. In this paper, we propose a way to classify the existing schemes of auxiliary circuits. Through the process of classification study, we hope to provide a systematic exposition of the design considerations of auxiliary circuits and to offer insights into the construction of suitable auxiliary circuits to satisfy specific requirements.

II. OVERVIEW OF CLASSIFICATION

The earliest auxiliary circuits are achieved by linear circuits that may be a linear voltage regulator or power transistor pair [13]–[16]. Resistance branches are added to create auxiliary cur-

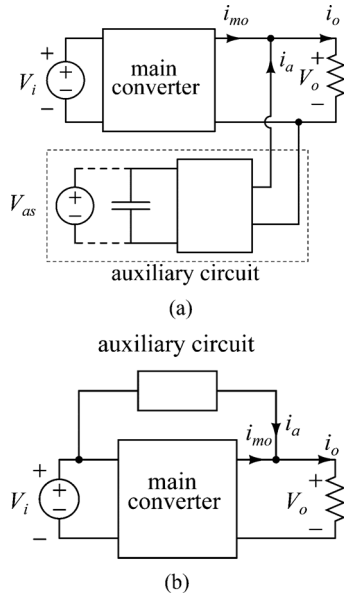


Fig. 2. Classification of auxiliary circuits according to connection style. (a) Shunt-output style; (b) bridge-connection style.

rent paths [3]–[5], [29], [31]. Such auxiliary circuits can be regarded as the *linear current-source style*, because the output current of the auxiliary circuit is provided by a linear regulator, i.e., the transistor is operating in the active region or the current-limiting resistors are in series with the output circuit. This type of auxiliary circuits gives an adequately fast transient but incurs significant power loss, especially when load transients occur more frequently. Moreover, the *linear current-source style* scheme uses no reactive components, and hence can be integrated on-chip. Therefore, in some low-power applications, this linear circuit scheme can be adopted to establish an on-chip solution of the power management [15], [29]. On the other hand, the use of *switching current-source style* constitutes a different type of auxiliary circuits in which the output current of the auxiliary circuit is controlled by regulating the duty cycle of a switching power circuit [17]–[28], [32] or the charge level of a switching capacitor [30], [33]. Since the switching power circuit achieves a much higher efficiency than the linear voltage regulator, *switching current-source* based schemes are expected to enjoy a higher popularity.

In terms of connection style, auxiliary circuits can be classified into two categories, namely, the *shunt-output style* (or simply called *shunt style*) [13]–[20], [30], [33] and the *bridge-connection style* (or simply called *bridge style*) [3]–[5], [21]–[29], [31], [32], [34], [35], as shown in Fig. 2. For the shunt style, the auxiliary circuit is plugged on to the output port of the power supply and hence can be used in isolated power supplies. Moreover, the auxiliary circuit must include sufficient capacity of energy storage elements or independent power source. For the bridge style, the auxiliary circuit is connected across the input and output ports of the power supply.

In terms of interaction style of control loops, classification can be performed according to the way in which the control loop of the auxiliary circuit interacts with that of the main

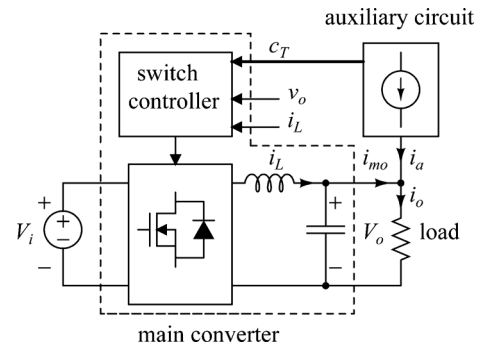


Fig. 3. Classification of auxiliary circuits according to control loop interaction. Presence and absence of c_T signal defines an *intruding* scheme and *non-intruding* scheme, respectively.

power converter. Specifically, we can classify auxiliary circuits as *intruding style* [3]–[5], [16], [17], [19], [20], [22]–[28], [30]–[32], [34], [35] or *non-intruding style* [13]–[15], [18], [21], [29], [33], depending on whether the control loop of the main converter would be interrupted or affected during the transient operation. In the *intruding style*, the auxiliary circuit control loop will affect the switching actions of the main converter, as shown in Fig. 3. Such auxiliary circuits can achieve the fastest change of the inductor current. On the other hand, in the *non-intruding style*, the auxiliary circuit does not interact with the main converter whose dynamics will be solely determined by its own feedback loop at all times. The auxiliary circuit effectively makes the original fast load transient appear as a slowly changing current slope that can be treated as a small-signal interference.

Recently, there has been rapid development in the availability of computer load information, resulting in a likely trend that the load profile including transient magnitude and time of occurrence can be accurately provided. Specifically, microprocessors, loads with fast transients, can predict the energy requirement and time of code executions quite accurately [36]–[41]. A paradigm shift in power supply design may therefore be conceived that the design of power converters may make use of the advance information about load changes [30], [31]. The impact of this paradigm shift on the design of auxiliary circuits is that communication is possible between the load and the auxiliary circuit, and hence load changes are no longer necessarily regarded as random or unpredictable processes. Thus, the load may pre-inform the auxiliary circuit before it steps up or down such that the switching frequency of the auxiliary circuit can be changed to avoid unwanted delays in transient detections. We refer to this type of auxiliary circuits as *load-informed style* as given in Fig. 4 and to others as *non-load-informed style*.

In the next section, we make a comparison of the *shunt-output* and the *bridge-connection* schemes. In Section IV, the development trend and implementations of the *intruding* scheme are discussed. In Section V, the pros and cons of the *load-informed* auxiliary circuit schemes are discussed. Finally, in Section VI, we present some experimental measurements based on a buck converter to validate the various comparative properties under the proposed classification schemes.

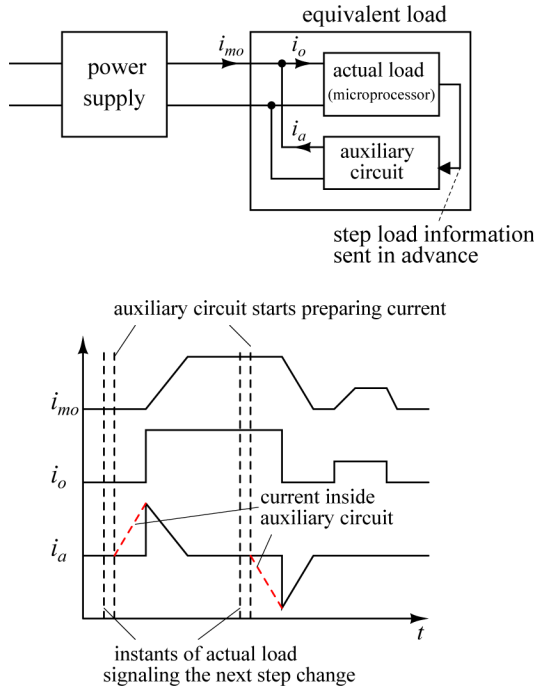


Fig. 4. Illustration of i_a supplied by the auxiliary circuit to the converter with advance load information.

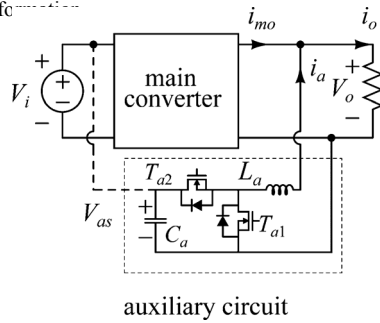


Fig. 5. Auxiliary circuit scheme using a buck-boost converter.

III. SHUNT-OUTPUT AND BRIDGE-CONNECTION AUXILIARY CIRCUITS

A. Power Loss

For the sake of comparison, we employ the bi-directional buck-boost converter as the auxiliary circuit for both shunt and bridge styles, as given in Fig. 5. Without the connection to V_i , the auxiliary circuit belongs to the shunt style. Here, V_{as} varies according to the choice of circuit parameters and the operation of the circuit [19]. Moreover, with the connection to V_i , the circuit assumes the bridge style and V_{as} becomes a constant.

The conduction power loss, switching loss and driver loss [27], [42] in the auxiliary circuit can be expressed mathematically as respectively

$$P_{\text{con_loss}} = \left(\frac{I_{\text{step}}^2}{3} + \frac{I_{pv}^2}{12} \right) (R_{\text{on}} + R_l), \quad (1)$$

$$\begin{aligned} P_{\text{sw_loss}} &= P_{\text{sw_on}} + P_{\text{sw_off}} \\ P_{\text{sw_on}} &= \frac{2}{3} C_{\text{oss}} V_{as}^2 f_s \\ P_{\text{sw_off}} &= \frac{1}{4} V_{as} I_{\text{step}} t_f f_s \end{aligned} \quad (2)$$

TABLE I
VARIABLE MEANING OF POWER LOSS ESTIMATIONS

Variables	Meanings
I_{step}	Magnitude of load transients
I_{pv}	Peak-valley value of deviation referring to mean i_a in one switching cycle
R_{on}	On resistance of MOSFETs*
R_l	Winding resistance of the inductor
C_{oss}	Output capacitance of MOSFETs
C_{iss}	Input capacitance of MOSFETs
V_{gs}	Driver voltage of MOSFETs
V_{as}	Source voltage of the auxiliary circuit
f_s	Switching frequency
t_f	Turn off time of MOSFETs

*assuming that characteristics of the MOSFETs are identical

and

$$P_{\text{gd_loss}} = C_{\text{iss}} V_{gs}^2 f_s. \quad (3)$$

The meaning of the variables are explained in Table I. Here, (1) indicates that the conduction loss is independent of V_{as} . From (2) and (3), it can be observed that for the required I_{step} and the given components, the switching and driving losses mainly depend on V_{as} and f_s .

When the auxiliary circuit is operating for a negative transient (i.e., step-down load current), T_{a1} is operating as an active switch, as shown in Fig. 6. Usually, m_1 (the slope of the falling edge), m_3 (the slope of mean i_a) and I_{pv} are specified by the application. It can be observed that f_s depends on V_{as} , i.e.,

$$\begin{aligned} m_3 &= \frac{I_{\text{step}}}{T_{\text{tran}}} = m_2(1 - D_1) - m_1 D_1 \\ &= V_{as} m_1 \frac{D_1}{V_o} - \frac{(V_{as} - V_o)}{V_o m_1}, \end{aligned} \quad (4)$$

$$\begin{aligned} D_1 &= \frac{m_1 (V_{as} - V_o)}{\frac{m_1 V_{as}}{V_o} - m_3} \\ &\approx 1 - \frac{V_o}{V_{as}} (m_1 \gg m_3) \end{aligned} \quad (5)$$

and

$$f_s = \frac{D_1}{T_{\text{on}}} \approx \frac{1}{T_{\text{on}}} \left(1 - \frac{V_o}{V_{as}} \right) \quad (6)$$

where T_{on} is a function of m_1 , m_3 and I_{pv} . Substituting f_s in (2) and (3) by (6), the sum of switching power loss and driver loss can be found as

$$\begin{aligned} P_{\text{sw_loss}} + P_{\text{gd_loss}} &= \frac{2}{3} \frac{C_{\text{oss}}}{T_{\text{on}}} V_{as} (V_{as} - V_o) \\ &\quad + \frac{1}{4} I_{\text{step}} t_f \frac{V_{as} - V_o}{T_{\text{on}}} \\ &\quad + C_{\text{iss}} V_{gs}^2 \left(1 - \frac{V_o}{V_{as}} \right) \frac{1}{T_{\text{on}}}. \end{aligned} \quad (7)$$

From the above equations, we clearly see that decreasing V_{as} will substantially reduce power loss.

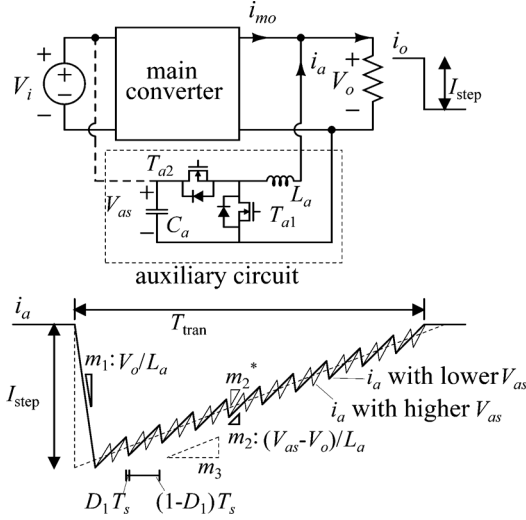


Fig. 6. Operation under negative load transient, i.e., step-down load current.

The scenario of positive transient, i.e., step-up load current, is shown in Fig. 7. The power loss can be calculated in a likewise manner as for the case of negative transient above, i.e.,

$$m_3 = \frac{I_{\text{step}}}{T_{\text{tran}}} = m_1 D_1 - m_2 (1 - D_1) \quad (8)$$

$$D_1 = \frac{\frac{m_1 V_o}{(V_{as} - V_o)} - m_3}{\frac{m_1 V_{as}}{(V_{as} - V_o)}} \approx \frac{V_o}{V_{as}} (m_1 \gg m_3), \quad (9)$$

$$f_s = \frac{D_1}{T_{\text{on}}} \approx \frac{V_o}{T_{\text{on}} V_{as}}. \quad (10)$$

And finally, we get

$$P_{\text{sw_loss}} + P_{\text{gd_loss}} = \frac{2 C_{\text{oss}}}{3 T_{\text{on}}} V_{as} V_o + \frac{1}{4} I_{\text{step}} t_f \frac{V_o}{T_{\text{on}}} + C_{\text{iss}} V_{gs}^2 \frac{V_o}{T_{\text{on}} V_{as}}. \quad (11)$$

In this case, the minimal value of $P_{\text{sw_loss}} + P_{\text{gd_loss}}$ exists while $V_{as} = \sqrt{3 C_{\text{iss}} / 2 C_{\text{oss}}} V_{gs}$. Since C_{iss} is usually a few times of C_{oss} and V_{gs} is 8 to 12 V for low V_o applications, variation in V_{as} will not quite affect (11), as compared to (7). Fig. 8 shows a plot of the total power loss versus V_{as} .

B. Choice of Applications

When the converter is operating at a high input-to-output ratio, e.g., $V_i/V_o = 12/2.5\text{V/V}$. The auxiliary circuit only need to work for negative transients [25]. When the bridge-connection scheme is chosen, the auxiliary circuit will incur a high dissipation. This is because V_{as} is fixed and has the same voltage as V_i . However, when the shunt scheme is applied, V_{as} will be provided by C_a and controlled by configuring the capacitance. In this case, a strategy for energy balance is necessary, and can be achieved by reservoir capacitor voltage control, which will

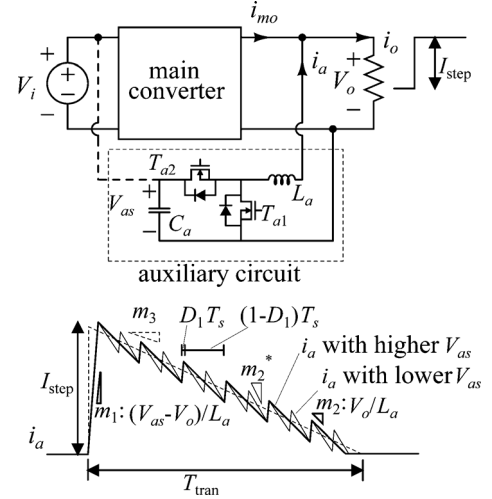
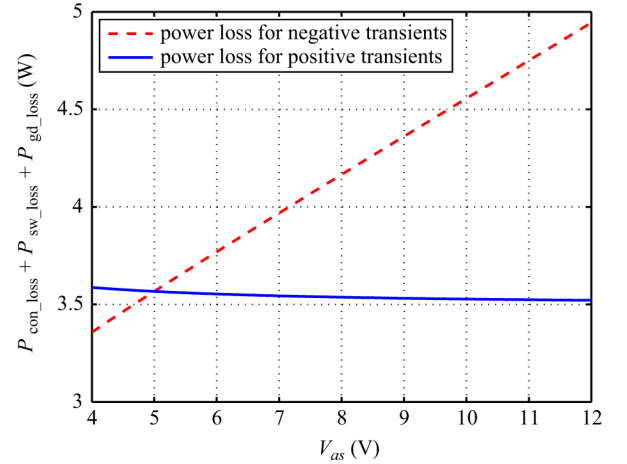


Fig. 7. Operation under positive load transient, i.e., step-up load current.

Fig. 8. Power loss versus V_{as} during auxiliary circuit operation ($V_i = 12\text{ V}$, $V_o = 2.5\text{ V}$, $C_{\text{iss}} = 460\text{ pF}$, $C_{\text{oss}} = 95\text{ pF}$, $t_f = 20\text{ ns}$, $V_{gs} = 12\text{ V}$, $I_{\text{step}} = 15\text{ A}$, $I_{pv} = 2\text{ A}$, $m_1 = 5\text{ A}/\mu\text{s}$, $T_{\text{on}} = 0.4\text{ }\mu\text{s}$, $R_{\text{on}} = 35\text{ m}\Omega$).

incur power loss [19]. If this power loss is sufficiently small, the shunt scheme will still be more desirable.

On the other hand, when the converter is operating at a low input-to-output ratio, e.g., $V_i/V_o = 5/2\text{V/V}$. The power loss of the circuit in the bridge-connection scheme will be naturally reduced. Thus, the simpler bridge scheme is preferred.

Moreover, when isolation is required between the input and output, the shunt scheme will be the only choice.

IV. NON-INTRUDING AND INTRUDING AUXILIARY CIRCUIT SCHEMES

The purpose of using an auxiliary circuit is to make a large load fast transient “appear” as a slow transient load current so that any ordinary power supply would be able to handle the load change. Effectively, the auxiliary circuit and the load together present themselves as a composite smart load (whose transients are always slow) to the power supply. When the resulting slope of the transiting current is relatively high, the operation time required of the auxiliary circuit is relatively short, as shown in Fig. 9. The intruding scheme provides the shortest operation

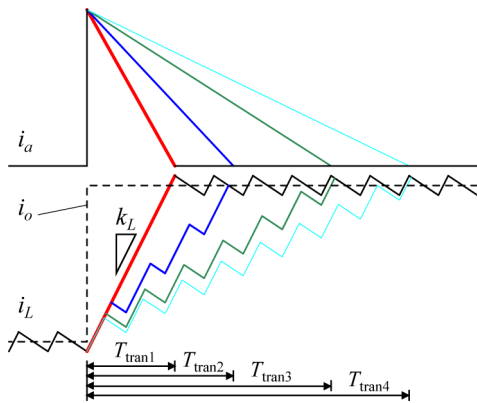


Fig. 9. Operation time of the auxiliary circuit depends on the current slope of i_a but is limited by k_L .

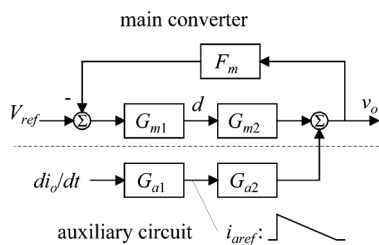


Fig. 10. Non-intruding auxiliary circuit schemes are achieved by a closed-loop main converter and an open-loop auxiliary circuit.

time of the auxiliary circuit thus incurring less power loss, while the non-intruding scheme offers the advantage of design simplicity.

A. Non-Intruding Schemes

Suppose the application of the auxiliary circuit makes the resulting load current change slowly, i.e., a relatively long T_{tran} . The resulting current thus becomes a small perturbation having most frequency components lying within the bandwidth of the control loop of the main converter. In this case, v_o can be tightly regulated. In this operation, the programmed i_a is well tracked by the main converter, as illustrated in Fig. 10.

The auxiliary circuit does not interact with the control loop of the main converter, and is referred to as a *non-intruding* auxiliary circuit scheme. The advantage is that two parts (main converter and auxiliary circuit) are almost operating independently. Using this scheme, an existing main converter might be enhanced in dynamic performance without modifications on its original circuit design to cater the scheme.

The simulation result is given in Fig. 11, where the main converter takes $500 \mu\text{s}$ (100 switching cycles) to relocate its operation point. The application of non-intruding schemes obviously have their drawback as they may incur a higher power loss due to the prolonged active period T_{tran} . Components with larger current and heat rating are thus needed. Hence, trade-off between size, efficiency and overshoot on v_o would need to be considered.

B. Intruding Schemes

To overcome the inherent deficiency of the non-intruding scheme, we need to shorten the active time, for example, by

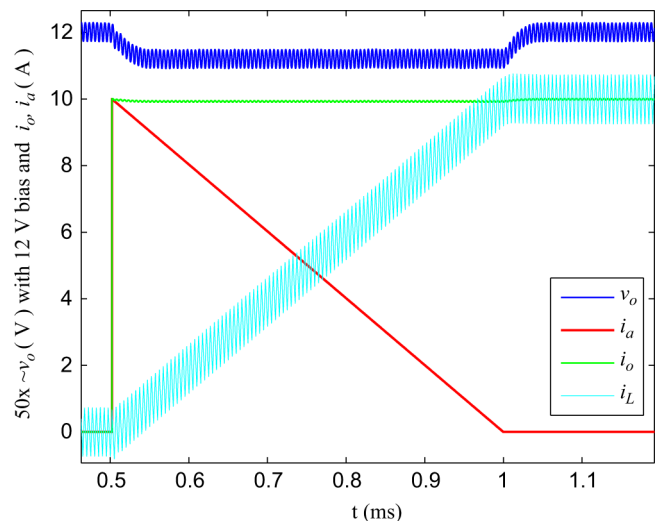


Fig. 11. Simulation waveforms of non-intruding scheme for a 10 A positive transient, with $V_i/V_o = 12/2.5\text{V/V}$, and switching frequency of main converter at 200-kHz. The auxiliary circuit provides a ripple-free i_a .

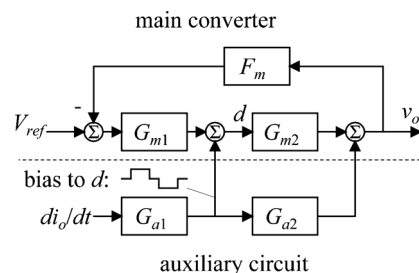


Fig. 12. Intruding auxiliary circuit model.

speeding up the rate of decline of i_a . The shortest possible active time of i_a is T_{tran1} , as shown in Fig. 9. However, the main converter may fail to follow i_a for such a fast trajectory, as controllers cannot have infinite control bandwidth [43]. The solution is to let the auxiliary circuit interact with the control loop of the main converter to achieve the fastest transition while the auxiliary circuit is following the state of i_L to provide the required current. Auxiliary circuits that interact with the main control loop are referred to as *intruding* auxiliary circuits.

In the mechanism described in Fig. 12, there is a circuit block to identify the transient at i_o , intruding a biasing signal to change the duty cycle of the main converter. This obviously will increase the complexity of the control system. Only a few additional low power components need to be included in the existing PWM controller ICs. In practice, there are two ways to achieve the intruding function in PWM controllers.

1) *Brute-Force Switching of the Switch Signal*: A multiplexer can be added to the switch controller of the main converter, as explained in Fig. 13. Normally, c_1 from the original feedback controller is enabled, while the auxiliary circuit is suspended. When an i_o transient is detected, c_2 from the auxiliary circuit is enabled to enforce a “100%” duty cycle for a positive transient or “0%” duty cycle for a negative transient. This method has been adopted in most auxiliary circuit schemes [17], [19], [20], [22], [24]–[27], [30].

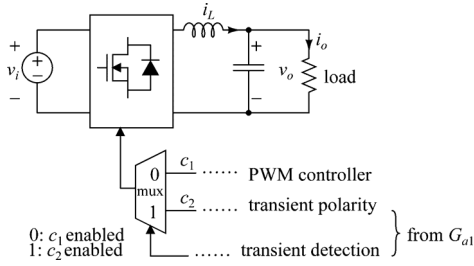


Fig. 13. Schematics of the brute-force switch-signal switching in the intruding scheme.

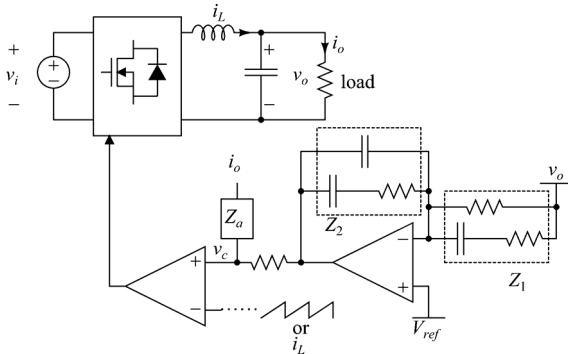


Fig. 14. Schematics of the feedforward-signal injecting in the intruding scheme, where a signal corresponding to i_o is injected into feedback controller.

2) *Injecting a Feedforward Signal*: Another way to achieve intruding is shown in Fig. 14, where a feedforward signal dependent on i_o is injected to the feedback control through the network Z_a [3]–[5], [23], [32], [34], [35]. In a conventional linear controller, the control signal v_c derived from v_o cannot follow i_o in the large-signal sense. When the feedforward signal is added to the feedback network, a fast transient at i_o will lead to a large increment or decrement in v_c , which can achieve a “100%” or “0%” duty cycle instantly.

Injecting a feedforward signal has an extra merit. When the auxiliary circuit is active, the operating point is allowed to shift at a large scale in a short time. However, under a linear feedback controller, the operating point can only move slowly at small-signal scale. Thus, the feedback controller cannot take v_c to the new steady-state point quickly enough following a rapid change in i_L . The feedforward signal not only switches the duty cycle to 1 or 0, but also pushes v_c to the new operating point without any overshoot in v_o . Fig. 15 shows the comparison of the brute-force switch-signal switching and the use of feedforward signal. It is noted that at instants of 1.0 ms and 1.5 ms, the load transients and voltage deviations have been addressed by the auxiliary circuit.

In Fig. 15(b), the duty cycle is switched to “0” or “1” by brute-force switching. It is clear that i_L initially is not tracked to v_c as the control loop is temporarily suspended, and after the transition (active period of the auxiliary circuit), i_L is re-tracked to v_c . In this process, a voltage deviation occurs. Moreover, in Fig. 15(c), v_c is influenced by the feedforward signal, causing i_L to react spontaneously during the transition.

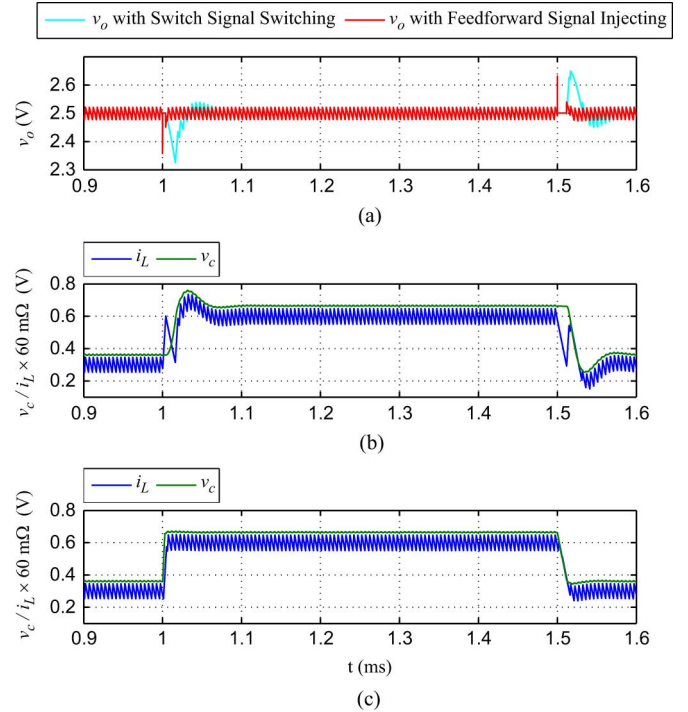


Fig. 15. (a) Comparison of waveforms of output voltage. Waveforms of inductor current (i_L) and current reference (v_c) of the controller intruded by (b) brute-force switching of the switch-signal; (c) injecting a feedforward signal.

V. LOAD-INFORMED AUXILIARY CIRCUITS

As explained in Section II, computer loads are capable of providing accurate load profile information, including the magnitudes and times of occurrence of load transients. Auxiliary circuits can thus be designed with the assumption of the availability of load information. Essentially, the load communicates with the auxiliary circuit about a future occurrence of a load transient, allowing the auxiliary circuit to pre-charge its storage element appropriately and provide the necessary fast transient current at the time it occurs. This eliminates the limitation caused by sensing delays when the load transients occur at random times.

A. Benefits of Load-Informed Schemes

The first obvious advantage of the load-informed scheme is the elimination of transient sensing circuits [30], [31]. Voltage deviations due to the sensing delays can thus be avoided.

In the previously described non-load-informed auxiliary circuit using a switching power circuit, the design involves trade-off consideration between efficiency and output voltage deviation. In the scenario of Figs. 6 and 7, to provide faster i_a to meet the high slew rate requirement, a small inductor should be employed, necessitating the use of a high switching frequency and incurring a high power dissipation.

With the load-informed auxiliary circuit, the load information including step time, magnitude and direction are known in advance. Thus, the auxiliary circuit can pre-energize its storage elements and to address the transient at the right synchronized

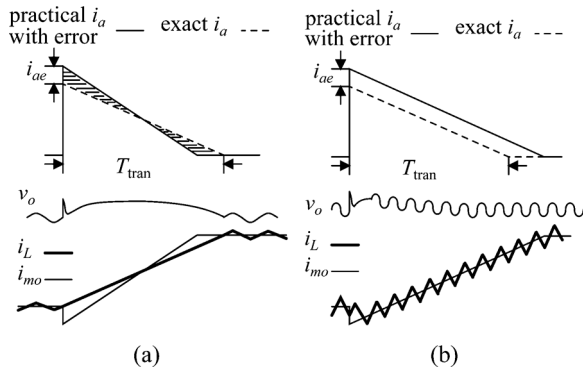


Fig. 16. Prediction inaccuracy in the magnitude of transient for (a) intruding and (b) non-intruding schemes.

time [30]. The auxiliary circuit can thus be designed to achieve a higher current slew rate at a lower switching frequency.

B. Limitations of Load-Informed Schemes

The effectiveness of the load-informed scheme depends on the precision of loading prediction, and the effect of inaccurate load profile information remains fundamental. Since the loading prediction method of microprocessor or computer loads is based on execution models of the given codes, errors may be inevitable due to some unexpected events such as interrupts.

When the predicted magnitude of I_{step} has an error of i_{ae} , i_a may be adaptively regulated, as depicted in Fig. 16(a) for the intruding scheme, to make sure the two hatched triangles have identical area. In this case, a current sensor will indicate the real value of I_{step} . Hence, i_L will not run beyond the needed scale. It is noted that this sensor does not require a wide bandwidth, while the active time of the auxiliary circuit is controlled by load information instead of transient detection. The voltage overshoot due to the inaccuracy of magnitude prediction can be estimated as

$$\Delta v_{oe} < \frac{T_{\text{tran}} i_{ae}}{4C_o}. \quad (12)$$

For the non-intruding scheme, as shown in Fig. 16(b), i_a can track the scheduled trajectory and the converter is able to follow i_{mo} . The voltage overshoot is caused by the main converter feeding a transient of i_{ae} . As long as the main converter can feed a small transient, i.e., i_{ae} , the scheme will allow a maximum prediction error of i_{ae} .

Furthermore, a sync signal indicating the time instant of a transient occurrence may be introduced to guarantee the synchronization of the action of the auxiliary circuit with the transient. Essentially, the auxiliary circuit may prepare itself with the received information, and the action of delivering i_a can be induced by the sync signal, as illustrated in Fig. 17. Therefore, an inaccurate prediction in the time of transient occurrence may be lumped on the magnitude error which can be handled readily.

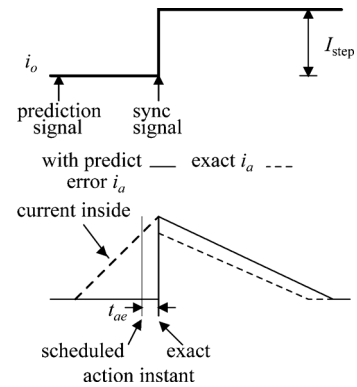


Fig. 17. Prediction inaccuracy in the time of transient occurrence for non-intruding schemes.

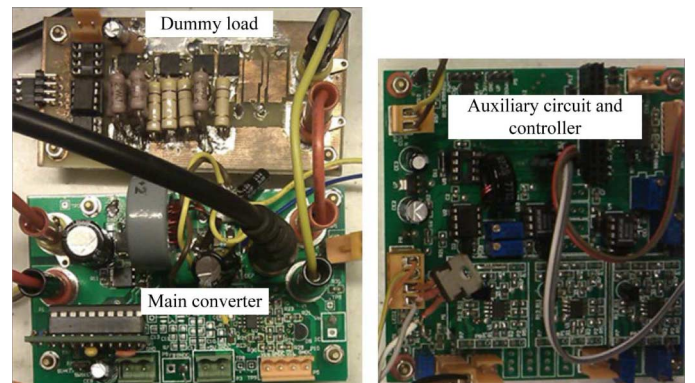


Fig. 18. Photo of the experimental circuit which can be configured in either brute-force switching mode or feedforward mode.

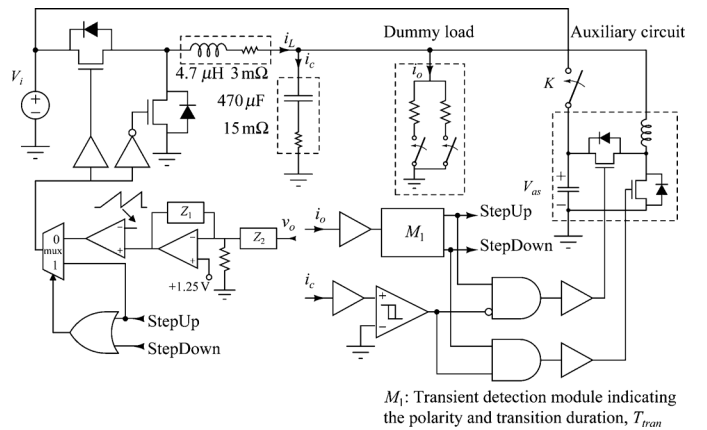


Fig. 19. Schematic of the experimental circuit for comparing bridge-connection and shunt-output schemes.

VI. EXPERIMENTAL VALIDATION

A. Experimental Circuits

To validate the above analysis, two sets of experimental circuits are constructed. Fig. 18 shows the experimental circuit. A buck converter (parameters given in Table II) with an auxiliary circuit (parameters given in Table III) operating in a shunt-output style or bridge-connection style is implemented. The schematic diagram is given in Fig. 19.

TABLE II
PARAMETERS OF THE BUCK CONVERTER FOR COMPARISON OF
BRIDGE-CONNECTION AND SHUNT-OUTPUT SCHEMES

Parameter	Value
V_i	12 V–5 V
V_o	2.5 V
Controller	IRU3037
Control mode	voltage mode
f_s	200 kHz
L	4.7 μ H, 3 m Ω
C	470 μ F, 15 m Ω
MOSFETs	IRL3715
Load	1 A–15 A
V_o deviation	≤ 80 mV

TABLE III
PARAMETERS OF AUXILIARY CIRCUITS.

Parameter	Value
V_{as}	equal to V_i (bridge-connection) 4 V to 6 V (shunt-output)
T_{on}	0.3 μ s
I_{pv}	2 A
m_1	≥ 5 A/ μ s
Inductor	0.47 μ H, 5 m Ω FW261
MOSFETs	$R_{on} = 35$ m Ω $C_{oss} = 95$ pF $C_{iss} = 460$ pF $V_{gs} = 12$ V $t_f = 20$ ns
C_a	33 μ F

The switch K is for selecting the operation mode between the *shunt-output style* and the *bridge-connection style*. When K is on, V_{as} is duplicated from V_i , establishing a *bridge-connection* scheme. Conversely, when K is off, a *shunt-output* scheme is established. Here, V_{as} is controlled by the reservoir capacitor voltage [19]. For brevity, the function mode of the reservoir capacitor voltage control is not shown in Fig. 19. The dummy load is able to generate transients from 5 A to 10 A. The module M_1 is used to detect the transient at the load side and generate an indication pulse (“StepUp” and “StepDown”), whose pulse width is proportional to the amplitude of the transient. Also, i_c is measured from the value of dv_o/dt by a differential circuit, and i_o is measured by a current sensor with current sensor amplifier ADM4073T.

Another buck converter (parameters given in Table IV) with an auxiliary circuit (parameters are same with Table III) operating in the *intruding style* under the two implementation strategies described earlier is implemented. The schematic diagram is shown in Fig. 20. The transient detection and the control circuits are the same as the first prototype constructed for the shunt-output scheme.

In the control circuit of the main converter, two functional blocks are employed to achieve the “intruding” scheme, which will facilitate generation of a fastest response under the two implementation approaches, namely, brute-force switching of the switch-signal and feedforwarding. The circuit serving the former is a multiplexer. When no transients occur, the channel 0 is selected and hence the traditional peak current control loop is formed. Either “StepUp” or “StepDown” signal is enabled, and the high-side switch is set as “1” or “0”. The circuit serving

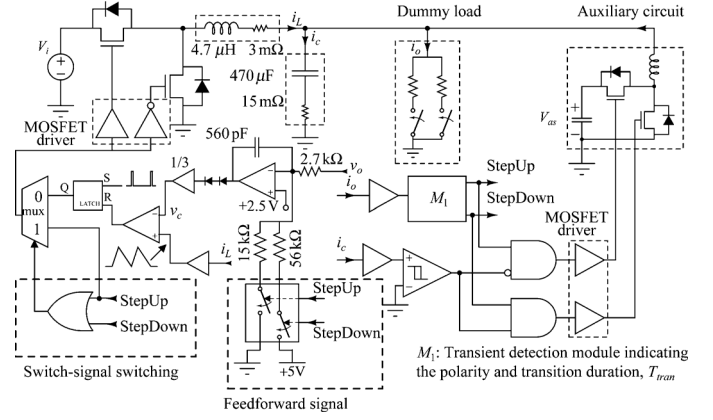


Fig. 20. Schematic of the prototype demonstrating the effectiveness of two intruding schemes, namely switching of switch-signal and feedforwarding.

TABLE IV
PARAMETERS OF THE BUCK CONVERTER FOR STUDYING
THE INTRUDING SCHEME

Parameter	Value
V_i	12 V
V_o	2.5 V
Controller	UC3843
Control mode	current mode
Current sensor	3 m Ω (with 20 V/V amplifier, ADM4073T)
Bilateral switch	CD4066
f_s	200 kHz
L	4.7 μ H, 3 m Ω
C	470 μ F, 15 m Ω
MOSFETs	IRL3715
Load	5 A–15 A
V_o deviation	≤ 80 mV

for the latter is a bilateral switching resistors group, where bilateral switches are implemented by CD4066. When “StepUp” or “StepDown” is enabled, the corresponding switch will be turned on to vary v_c .

In these prototypes, the buck converter is controlled by a current-mode controller UC3843. A simple RC compensation network ($R = 2.7$ k Ω , $C = 560$ pF) maintains stability in the main converter. To achieve the appropriate feedforwarding in v_c , two 15 k Ω and 56 k Ω resistors are employed. Hence, when the negative terminal of the error amplifier is connected to 0 V through the 15 k Ω resistor, a $360\text{mV}/\mu\text{s}v_c$ ramp-up is achieved. On the other case, when 5 V is connected through the 56 k Ω resistor, a $96\text{mV}/\mu\text{s}v_c$ ramp-down is achieved. The two implementations of the intruding scheme will be enabled separately.

B. Power Loss Comparison of Shunt-Output and Bridge-Connection Schemes

When the load is undertaking a 5 A transient, the auxiliary circuit operates separately in the two schemes for different V_i . Power loss in these two cases are compared and given in Fig. 21. All measured values in the plots represent power loss of the auxiliary circuit during its normalized active period, i.e., 9.4 μ s which is the active time of the auxiliary circuit for 5 A step-down transients. For the *shunt-output* scheme, the energy loss in the reservoir capacitor voltage regulation is also included in

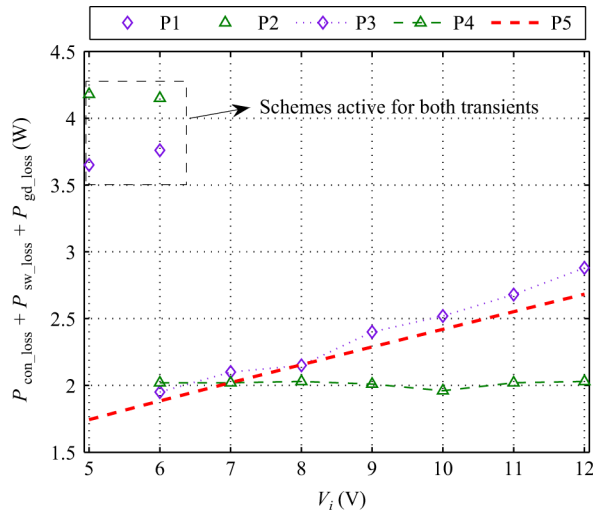


Fig. 21. Power loss measurement comparison of the auxiliary circuit assisting a buck converter in various schemes with varying V_i . Lines P1 and P2 correspond, respectively, to bridge-connection scheme and shunt-output scheme for either step-up and step-down transients, Lines P3 and P4 correspond to step-down transients for the bridge-connection scheme and shunt-output scheme, respectively. Line P5 is ideal power loss for step-down transients in the bridge-connection scheme or the shunt-output scheme with $V_{a,s}$ chosen in the range of 5 to 12 V.

the total energy loss. Note that when V_i is high, the auxiliary circuit is only active for step-down transients.

For the *bridge-connection* scheme, $V_{a,s}$ is equal to V_i . Referring to Fig. 21, the loss in the bridge-connection scheme for step-down transients (line P3 in the figure) is close to the ideal loss (line P5), which displays a rising trend as V_i increases. Furthermore, for the *shunt-output* scheme, with a fixed range of $V_{a,s}$ (4 V to 6 V), the auxiliary circuit is always pumping around 2 W power. The ideal power loss can be estimated as around 1.75 W, as labeled as dotted line P5 in Fig. 21. The absorbed energy will be discharged to the output slowly with dissipation. Thus, the real current power loss is higher than the ideal value.

From Fig. 21, we see that when V_i is around 6 V to 8 V, the power loss of the two schemes are very close. However, when V_i is higher, the power loss of *bridge-connection* style becomes significantly larger than that of the *shunt-output* style. This result verifies the analysis presented in Section III-B.

When V_i drops to 6~V, the auxiliary circuit should be made to work to handle a step-up transient. Operating for a step-up transient incurs a higher power loss in the *shunt-output* scheme than the *bridge-connection* scheme. The reason is two-fold. First, the requirement of balanced bidirectional charging of the reservoir capacitor (only for *shunt-output* scheme) will incur more energy loss. Second, in the *bridge-connection* scheme, a lower V_i will reduce the energy loss in the auxiliary circuit for negative transients while the *shunt-output* scheme is still applying 4 to 6 V in $V_{a,s}$, incurring a constant energy loss. In this case, when V_i is lower than 6 V, the *bridge-connection* scheme is preferred.

The overall efficiency comparison of the two auxiliary circuit schemes with the conventional buck converter without the schemes is presented in Fig. 22. A load transient of 5 A to 10 A is repeated every 100 μ s. The mean load current is 7.5 A. Compared to the shunt-connection scheme, the converter

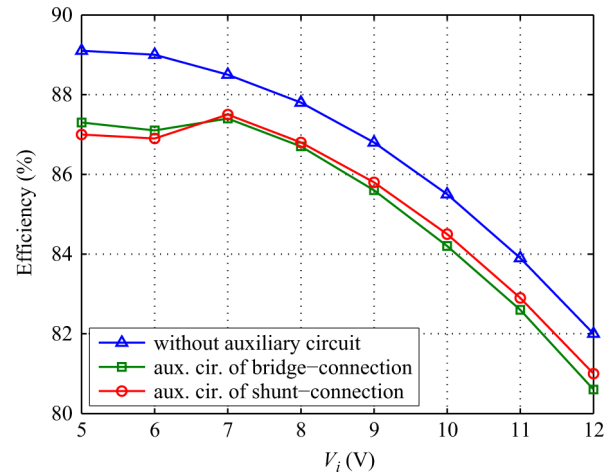


Fig. 22. Overall efficiency of the conventional buck converter, the converter with auxiliary circuit of bridge-connection, and that of shunt-connection.

with the bridge-connection scheme achieves a higher efficiency when V_i/V_o is larger. As we can see, the efficiency difference is 0.5% between the two schemes when $V_i = 12$ V. The efficiency degradation incurred by the scheme is around 1% when V_i is from 7 V to 12 V.

C. Comparison of Intruding Auxiliary Circuits

For the purpose of testing, we apply step-up and step-down load transients of 5 A to a standard buck converter under current-mode control with and without an *intruding* auxiliary circuit. The transient waveforms of v_o and i_L of the regulated buck converter are shown in Fig. 23(a). A 160 mV fluctuation in v_o has been observed at the instant of application of a 5 A step-down transient. Auxiliary circuits using the two mentioned *intruding* schemes (as given in Section IV-B) are implemented, and the measured waveforms are given in Fig. 23(c) to Fig. 23(f). A reduced voltage fluctuation in v_o has been observed for these cases.

Moreover, when the intruding scheme is implemented by brute-force switching of the switch-signal, voltage overshoot can be suppressed only during the active period of the auxiliary circuit, but the switch control signal of the main PWM controller is still in the transition stage. Hence, a secondary transient occurs and is marked in Fig. 23(e), where the control signal v_c and the current signal v_{iL} are highlighted to illustrate this mechanism.

On the other hand, for the implementation using the feedforward scheme, we observe from Fig. 23(f) that v_c has been appropriately changed by the feedforward signal which results in i_L moving to the new operation point with an expected amount of voltage fluctuation. Hence, the feedforward scheme is suitable for tackling fast load transients in converters under current-mode control.

We omit the experimental validation of the load-informed schemes in this paper, as a more detailed exposition will be provided in a separate future publication [44] and the experimental prototype would involve a substantially different setup in order to illustrate the advance provision of load information in such schemes.

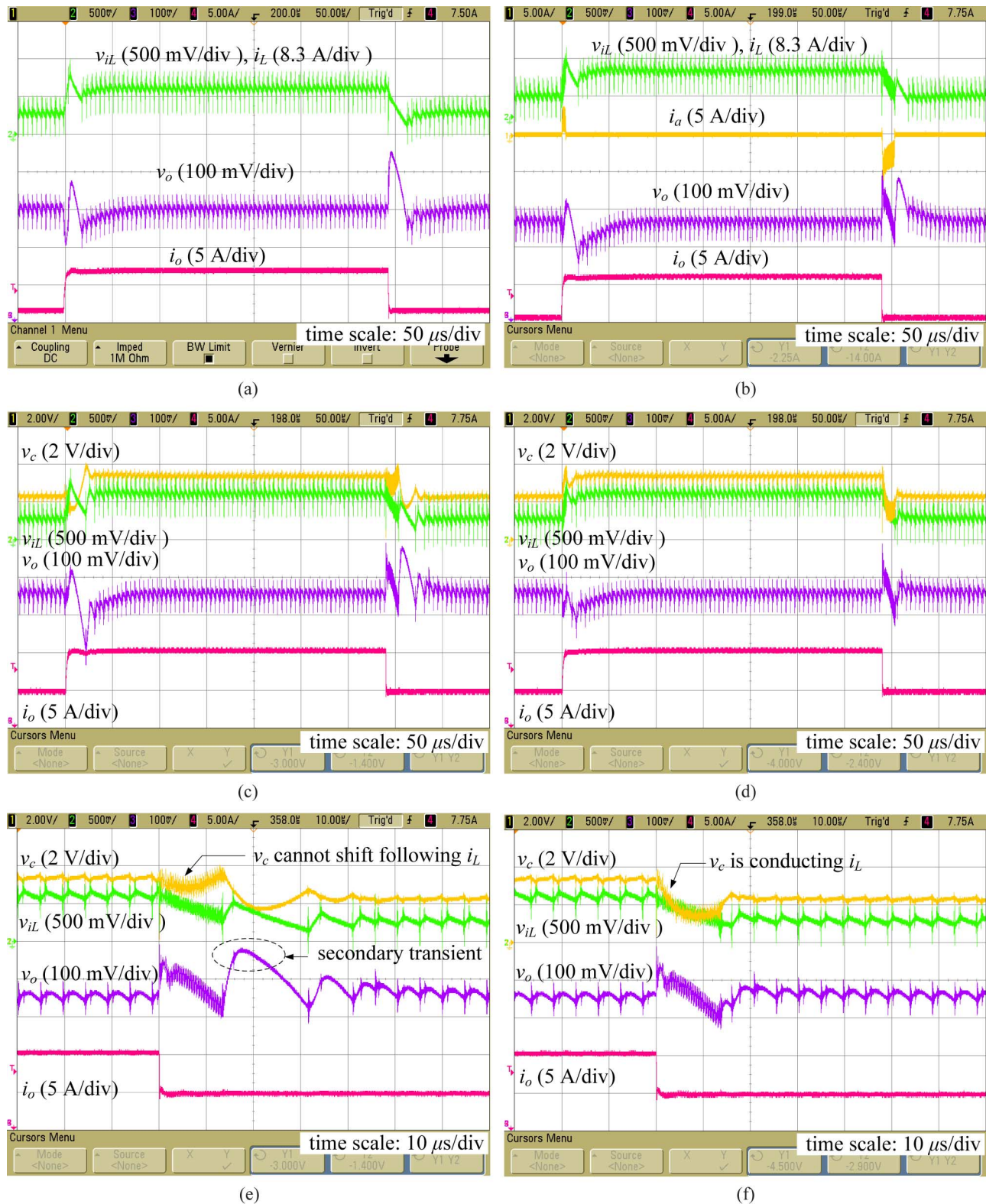


Fig. 23. Waveforms under application of 5 A load transients for buck converter (a) without the auxiliary circuit, (b) with the auxiliary circuit. Comparisons between two intruding schemes: (c) switching of switch-signal and (d) feedforwarding. Enlarged waveforms of (c) and (d) are given in (e) and (f).

VII. EXISTING CIRCUITS UNDER THE PROPOSED CLASSIFICATION

The systematic classification of auxiliary circuits presented above provides a convenient framework for comparison of various types of auxiliary circuits. Specifically, it would be useful

for circuit designers in deciding on the use of a specific circuit style or control method if the various auxiliary circuits can be compared in terms of their efficiency, circuit and control complexity, possible applications, along with some existing implementations.

TABLE V
COMPARISON OF AUXILIARY CIRCUITS FOR PRACTICAL DESIGN APPLICATIONS

Classification	Types	Power loss	Complexity	Applications (load conditions)	Existing implementations (references)	
Power devices used	linear current source	relatively high, as given by $P_{\text{loss}} = (V_i - V_o)\overline{i_a}$ or $P_{\text{loss}} = V_o\overline{i_a}$	consists of transistors and resistors only	<ul style="list-style-type: none"> low transient current low transient repetition rate integrated on-chip 	[3]–[5], [13]–[16], [29], [34], [35]	
	switching current source	low, as given by Eqs. (11) and (7)	uses reactive elements	<ul style="list-style-type: none"> high transient current high transient repetition rate based on discrete parts 	[17]–[28], [30], [32], [33]	
Connection styles with the power supply and load	bridge connection	$P_{\text{loss}} \propto V_i$ (step-down transients) depending on V_i	no energy storage elements needed	<ul style="list-style-type: none"> non-isolation applications low V_i/V_o ratio 	[13]–[20], [29], [30], [32], [34], [35]	
	shunt connection	$P_{\text{loss}} \propto V_{a.s}$ (step-down transients) depending on $V_{a.s}$	uses energy storage elements or extra power supply	<ul style="list-style-type: none"> isolation or non-isolation high V_i/V_o ratio 	[3]–[5], [21]–[28], [33]	
Control methods	non-intruding	$E_{\text{loss}} = P_{\text{loss}}T_{\text{tran4}}$ referred to Fig. 9, high	no interactions between the main converter and the auxiliary circuit	<ul style="list-style-type: none"> existing main power supply not modifiable 	[13]–[15], [18], [21], [29], [33]	
	intruding	brute-force switching of switch signal	$E_{\text{loss}} = P_{\text{loss}}T_{\text{tran1}}$ referred to Fig. 9, low	switches the switch driving signal when the circuit is operating, complex	<ul style="list-style-type: none"> main power supply of voltage mode control with modifiable switch driving 	[17], [19], [20], [30], [22], [24]–[27]
		injecting feedforward signal		injects feedforward signals to the feedback loop when the circuit is operating, complex	<ul style="list-style-type: none"> main power supply of current mode control with modifiable compensation loop 	[3]–[5], [23], [34], [32], [35]
Load information availability	available (load-informed)	not related to power loss; but may affect total cost of the system [31]	needs a load level prediction signal	<ul style="list-style-type: none"> computer or other intelligent loads with advance step change information 	[30], [31]	
	not available		needs a wide bandwidth current sensor	<ul style="list-style-type: none"> no limitations on the load 	[3]–[5], [13]–[29], [32]–[35]	

In Table V, we provide a tabular comparison of the auxiliary circuits categorized under the proposed classification, i.e., types of power devices, connection styles, control methods, and load information availability, and make specific reference to their efficiency, complexity and possible applications. Our aim is to provide circuit designers a practical guideline for selecting auxiliary circuits and control methods for their specific applications. For instance, if a simple low-cost method is needed to enhance the transient response of a power supply feeding a non-computer load, a bridge-connected linear current source with non-intruding control would be adequate. On the other hand, a connect-connected switching current source with an intruding control would be very desirable for a microprocessor load that can provide load profile information and needs high efficiency.

VIII. CONCLUSION

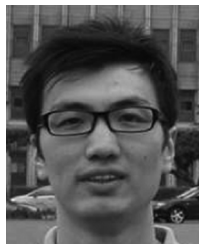
In the paper, we present a classification of auxiliary circuit schemes for tackling fast load transients in switching power supplies. We first consider the construction of auxiliary circuits in

terms of the way in which they are connected to the load and the main power supply, and also the interaction of the auxiliary circuit and the control loop of the main converter. Furthermore, we consider a classification based on a new design paradigm which has emerged from the recent research in load profile prediction in computer and microprocessor loads. Under this new paradigm, auxiliary circuits may receive advance load information and hence are able to tackle the transients by appropriately pre-energizing themselves. A comparison of the characteristics of the various schemes are discussed. Our study provides practical design pathways for selecting the appropriate kinds of auxiliary circuits for the applications concerned.

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