Pre-Energized Auxiliary Circuits for Very Fast Transient Loads: Coping With Load-Informed Power Management for Computer Loads

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***Abstract*—The recent development in computer science that the power demand and required time of code execution can be accurately predicted is paving a path that may lead to a new paradigm shift in power supply design. Specifically, while the design of power supplies now normally assumes that load current changes at random times and with unknown magnitudes (within a range), future computer loads may communicate with power supplies to provide information that facilitates power management. Such information would include the exact times of occurrence of load transients and their magnitudes. Following this trend of development where the power supply is "informed" by the load, we propose to use an auxiliary circuit that generates a slowly rising current prior to the occurrence of the actual transient. The slowly rising current can cause the power supply to shift its operation point to a new level slowly without exhibiting output voltage fluctuation. The actual load exhibits very fast current transient, but the combination of actual load and auxiliary circuit behaves as a slowly changing load which can be dealt with by an ordinary power supply capable of handling slowly changing load current. Thus, this method essentially buffers the power supply from large and fast transients. Our proposed approach involves the necessary algorithm for controlling the auxiliary circuit in accordance with the information provided by the microprocessor. The design of the auxiliary circuit is explained and experimental results for a 1.5 V load with 15 A step current are provided for verification.**

***Index Terms*—Auxiliary circuit, dc-dc converter, fast transient, large transient, load-informed power management, microprocessor power supply.**

I. Introduction

POWER supplies are indispensable parts of many electronic and electrical appliances. Advanced design of power supplies has developed over the past few decades around the so-called *switching technology*. Switching power conversion has become a mature technology that is now being used for the construction of high-performance power supply systems. Generally speaking, a switching power supply contains an assembly of components including power transistors, diodes, inductors and so on, which is designed to function as a controllable current source i_p. In addition, an energy storage element, i.e., C_o, is paralleled at the output to smooth the output voltage, as shown in Fig. 1. The usual consideration of the dynamic performance of a power supply assumes that the load changes are not known, though the ranges of the extents of load changes are normally specified. In other words, the power supply is always trying to cope with a variable load having random behavior. In a power supply employing a standard voltage feedback controller, the fundamental principle of regulating the operating point is based on the measured information at the output. Then, a negative feedback loop is employed to adjust the current source i_p in response to any change in the output, where time delays inevitably exist in the feedback network as well as the components involved.

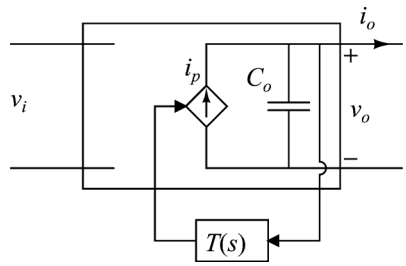

Fig. 1. Basic mechanism of a power supply to process the load dynamics.

Comparing with the linear voltage regulator, the switching power converter incurs a longer time delay to reach a new operating point following a load change. For instance, the process may physically involve a change in the current of an inductor. Referring to Fig. 1, during that delay period, the energy storage element (capacitor) will need to address the instantaneous imbalance of i_p and i_o, which will in turn incur overshoots or undershoots of v_o from the reference value. When the load varies at a low slew rate, a small capacitor would suffice to smooth out the output voltage. However, when the load varies at a high slew rate, a larger capacitor is needed to achieve the allowed small voltage fluctuation. However, large capacitors are undesirable as they add cost to and increase the size of the system.

A practical system where the above problem occurs is the power supply for microprocessors [1], [2]. A number of methods have been proposed for tackling this problem. An auxiliary circuit that deals with fast transients has been considered, and its implementation involves connecting an extra energy transfer path to the load [3]–[16], as shown in Fig. 2(a). This

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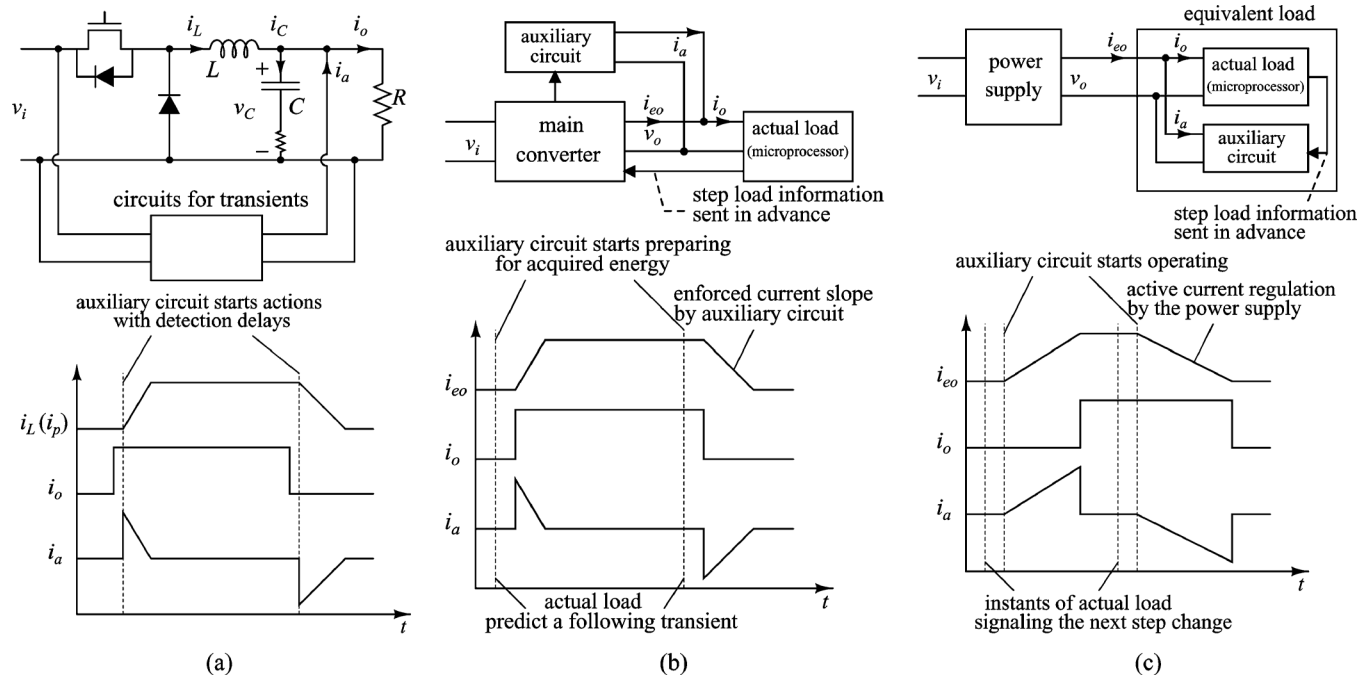


Fig. 2. Summary of three auxiliary circuits. (a) Previous auxiliary circuit used in a buck converter to assist load transients, (b) illustration of the paradigm of the auxiliary circuit cooperating with a behavior predictive load, and (c) proposed pre-energized scheme of the auxiliary circuit with load-informed power.

type of auxiliary circuits can significantly improve transient performance under high slew-rate output current conditions. However, such methods do have practical drawbacks. For the auxiliary circuit to generate the necessary current, the occurrence of the load step, either up or down, must be precisely detected. Techniques for detection of load steps are mainly based on voltage drop or large-signal change of the current. It is difficult to implement an accurate detection of the current step change due to the effect of voltage delay and the finite bandwidth of amplifier circuits. Furthermore, when the scheme is implemented using a switching circuit, it is impossible to generate an ideal step current to deal with very rapid transients [9]–[16]. Clearly, linear circuits and resistors can be used to achieve very rapid current steps [3]–[8], but the poor efficiency is often a price too high to pay.

Recently, a paradigm shift in the design of power supplies has begun to emerge as advance information about the load change may become available [17], [18], as illustrated in Fig. 2(b). Thus, we may conceive new concepts in the use of auxiliary circuits for providing very fast transient power, where the load may communicate with the power supply circuit about its future transient events. In practice, a signal may be sent from the load to inform the auxiliary circuit about the magnitude and the time of the next transient. The auxiliary circuit will then prepare the output current and take an appropriate action to tackle the transient. In these methods, a switching capacitor or resistance augmentation is utilized to achieve the energy supply or sink. Comparing with the switching mode auxiliary circuits mentioned earlier, these methods will offer very rapid current steps and generate perfect spike-free responses to fast load transients.

In this paper, we examine the new auxiliary circuit design paradigm where advance loading information is utilized for achieving very fast load transient response. We propose a practical approach to implementing such auxiliary circuits. Specifically, the auxiliary circuit will start sinking or sourcing current at a slow rate to pre-energize the power supply before the load transient occurs. Since the time instant and magnitude of the load current change are known, the auxiliary circuit may schedule a suitable start time of the pre-energizing process. At the instant of the application of the load transient, the output current of the power supply is hitting the new level to which the load is heading. At the same time the auxiliary circuit will remove i_a, switching i_o to the load, as shown in Fig. 2(c). It should be noted that in the whole process the power supply is operating independently. Compared with other auxiliary-circuit-based methods, no interaction between the power supply and the auxiliary circuit is required, implying a lower complexity of the system. In addition, as the load provides a synchronized signal at the instant of the application of each transient, exact predictions or detections of the times of the transients are unnecessary, thus greatly simplifying the design of the system and enhancing the transient performance.

II. Application Scenarios

As mentioned earlier, a likely consequence of the development of load-informed power management is that the microprocessor can communicate with the auxiliary circuit about the occurrence of a large current load step before it actually applies the step. With the prior information, interactions between the microprocessor and the auxiliary circuit would eliminate the requirement for fast transient capability of the power supply. The combined auxiliary circuit and load is then connected to an "ordinary" power supply which is capable of providing regulated voltage under small-signal perturbations.

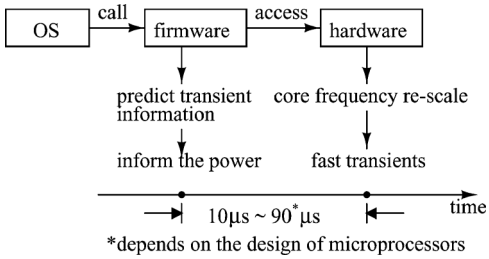


Fig. 3. The process of core frequency scaling from OS calling the firmware to the hardware implementation and transient predictions in small time scale.

A. Possibility of Microprocessor Informing Auxiliary Circuit

Dynamic voltage and frequency scaling (DVFS) in practical microprocessor systems allows the clock frequency and supply voltage to vary dynamically in response to computational load requirements. Hence, a microprocessor is able to predict its energy cost and time duration before the completion of one section of code execution [19]–[24].

Specifically, the dynamic frequency scaling (DFS) is generally realized in three stages. First, the operation system (OS) would send out a command to re-scale the core frequency when the CPU usage has changed in a significant scale. Second, the firmware or BIOS (Basic Output Input System) will reconfigure the clock generator and related registers. Finally, it will take the hardware circuit several tens of microseconds to change the clock rate [25]. An illustration of the interactions among OS, firmware and hardware is shown in Fig. 3. It can be seen that the whole system needs some time to respond to the power changing requirement from the OS. Hence, the microprocessor is able to accurately provide the transient information prior to the transient that occurs in a small time scale.

Furthermore, the OS may predict the transients in a large time scale, as shown in Fig. 4. The ending time of program executions can be estimated by the OS with the corresponding computational profile of different applications, i.e., arithmetic calculations, media playing or file copying. When the heavy computational load is finished, the computer may immediately enter the idle/sleep mode. Therefore, the step-down load transients can be predicted. Likewise, a step load transient will appear after the application program is triggered by some input signals. In that case, the OS still needs to prepare for the start-up, e.g., assigning software or hardware resources, accessing the source data and regulating the core frequency. The transient prediction for power management may also be triggered by the same input signal. The information would be sent to the auxiliary circuit with minimum latency.

Observation and estimation of computational requirement for power management would occupy part of computational resource. To address this problem, a special unit may be integrated in one chip with CPU cores to realize the power management functions discussed above, as shown in Fig. 5. Also, the control function of the auxiliary circuit may also be integrated together. In this case, the communication for load-informed power can be implemented within one chip.

On the other hand, it is possible to reserve several pins for communication with auxiliary circuits. For a microprocessor,

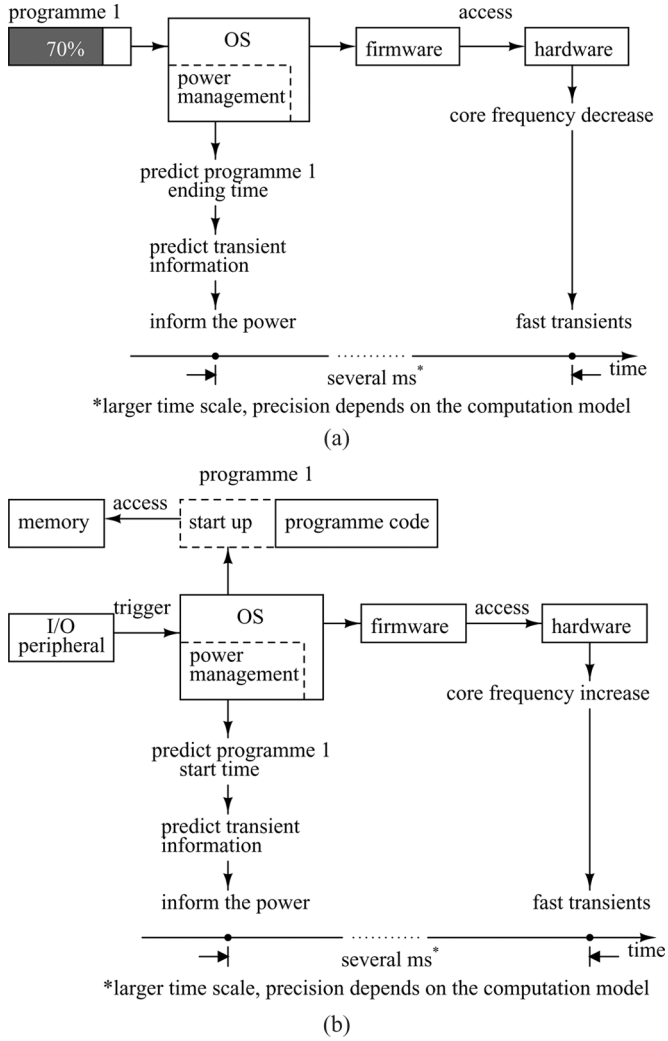


Fig. 4. Predict the real (a) ending and (b) starting time of the programme to give the advance transients information in a large time scale.

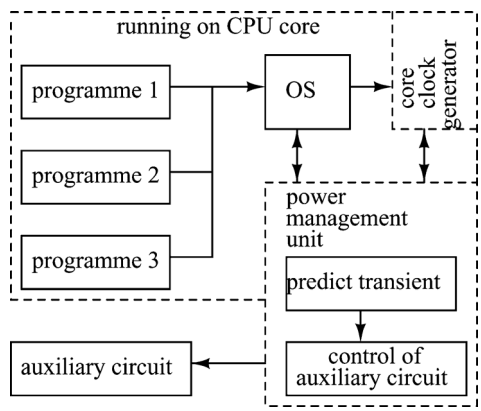


Fig. 5. A power management unit operating for load-informing is integrated with CPU cores.

interaction signals for voltage identifications (VID) are assigned for dynamic voltage scaling (DVS) in the traditional power management system of microprocessors [26]. This mechanism will facilitate the power supply in suppressing overshoots. If the VID scheme is removed and replaced by a

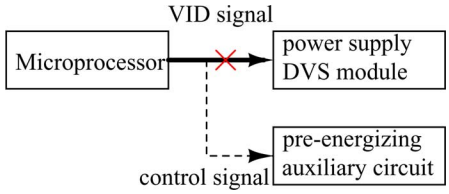


Fig. 6. Microprocessor pins for VID signals can be used for load-informed power management.

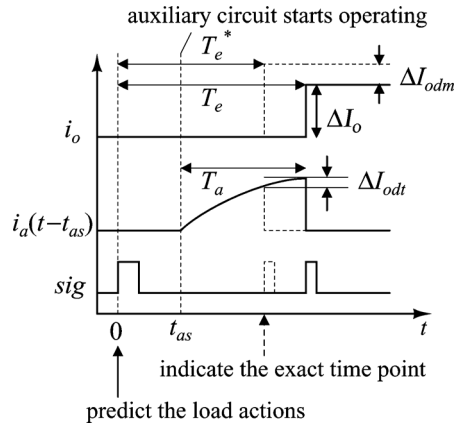


Fig. 7. Scheduling and implementing the auxiliary circuit action by the signal predicting and indicating transients.

pre-energizing scheme to compensate the transients, the reference of power supply can be constantly set to the lowest voltage value and about 10% energy saving may be achieved, assuming an average of 50% loading [18]. Hence, the pins reserved for VID function can be used instead to transmit control signals for the auxiliary circuit, as given in Fig. 6. Null response to large-signal transients will be tackled by the operation of the auxiliary circuit [5].

B. Interaction of Actual Load and Auxiliary Circuit

The equivalent load contains the actual load and an auxiliary circuit, as shown in Fig. 2(c). The current of the actual load, i_o, may exhibit an ultra high slew rate but can be predicted before it is applied. As discussed before, a key feature of the equivalent load is that the actual load sends a signal to the auxiliary circuit in advance of each occurrence of large load steps. After receiving that signal, the auxiliary circuit will schedule its action by calculations.

The instant when the predictive signal is received is defined as the time origin. From the signal it can be learned that at the instant T_e the load transient with ΔI_o magnitude will occur. Here, the characteristic of i_a vs time is known and denoted as $i_a(t-t_{as})$, where t_{as} is the start point of circuit actions. When $i_a(T_e-t_{as})=\Delta I_o$ is expected, then $t_{as}=T_e-T_a$ is obtained, where $T_a = i_a^{-1}(\Delta I_o)$. Hence, the auxiliary circuit starts its action at the time instant t_{as}, as given in Fig. 7. Also, $T_e > T_a$ must be satisfied to give sufficient time for i_a to rise. Here, the time consumption on calculations for scheduling is omitted.

Prior to the application of the step current in i_o, the auxiliary circuit will begin to sink current (denoted as i_a) during T_a. The slew rate of i_a must not exceed the allowed limit, denoted as $k_{p\max}$. When the actual load current step occurs, the power supply continues to deliver the load current but the auxiliary circuit ceases to sink instantly, resulting in the delivery of a very fast transient current to the actual load. Likewise for the case of opposite polarity, before i_o steps to a lower magnitude, i_a goes negative gradually and then is cut off simultaneously as i_o steps down. In other words, the equivalent load connecting to the power supply is designed to sink/source a controllable slowly ramping current, making use of an energy buffer circuit which has prior information about when a rapid load change would occur.

C. Synchronization Signal to Allow Inexact Prediction

In this prediction method, the actions of load transient and the auxiliary circuit must be aligned in time. A synchronization signal to indicate the occurrence of a load transient will allow inexact time prediction. The energy consumption of microprocessors depends on the operation frequency which is dynamically scaled and implemented by the hardware. Hence, the hardware is able to identify the instantaneous clock rates and naturally provides a synchronous signal with the occurrence of a transient.

Referring to Fig. 7, if the load generates a fast transient at T_e^* instead of T_e, the auxiliary circuit will be triggered by the synchronization signal to cut off i_a immediately. In this case, only residual transients, quantified as ΔI_{odt}, need to be taken care of by the power supply. Furthermore, letting the prediction inaccuracy of the magnitude be ΔI_{odm}, the load transient taken by the power supply becomes

$$\Delta I_{od}=\Delta I_{odt}+\Delta I_{odm}=-i_a(T_a+T_e^*-T_e)+\Delta I_o+\Delta I_{odm}. \tag{1}$$

If $T_e^*-T_e \ll T_a$ is obtained, then $\Delta I_{odt} \ll \Delta I_o$. The power supply only needs to address a much smaller amount of transient ΔI_{od}, as compared to ΔI_o.

III. Implementation of Auxiliary Circuit for Supplying Pre-Energizing Current

A. Auxiliary Circuit Topology

Our design of the auxiliary circuit is shown in Fig. 8 which consists of five switches, an inductor and a capacitor. Here, S_1 is implemented as a back-to-back MOSFET; S_3 and S_4 are general MOSFETs; S_2 and S_5 are diodes which may incur small power loss during the energy recovery cycles. Four operation stages can be identified, i.e., P_1, P_2, P_3 and P_4, for the two types of load steps, as explained in Fig. 9. Detailed waveforms of the auxiliary circuit are given in Fig. 10. Stages P_1 and P_2 are employed for step-up load currents, whereas P_3 and P_4 are for step-down load currents.

1) Stage $\mathrm{P}_1[T_1,T_2]$*:* At t_1, the auxiliary circuit, turning on S_1 and S_3 at the same time, begins to sink current gradually from the power supply and stores energy in L_A. Hence, the slew rate of $i_{a/eo}$ is programmable by choosing the inductance of L_A.

2) Stage $P_2[t_2,t_3]$*:* When i_a catches up with the load step (ΔI_o) with the same amount of step appearing in i_o, the circuit enters stage P_2. At t_2, which is the beginning of P_2, i_a drops to zero immediately, canceling out the positive transient of ΔI_o at

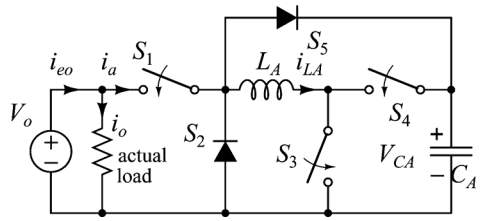


Fig. 8. Schematic diagram of auxiliary circuit to provide prior slow sloping current.

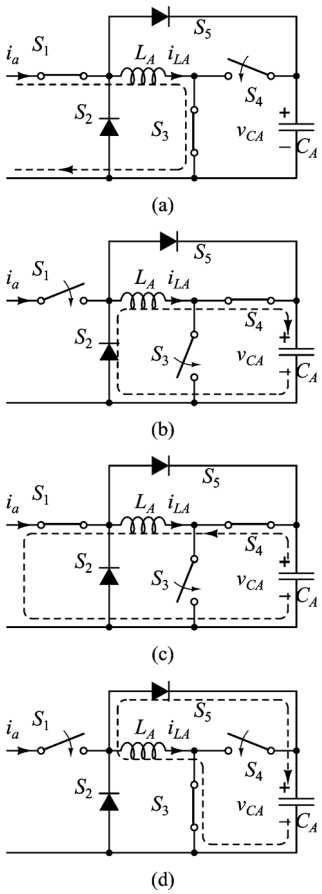


Fig. 9. Switch topologies of the auxiliary circuit. (a) Stage P_1 and (b) stage P_2 are for step-up load currents, and (c) stage P_3 and (d) stage P_4 are for step-down load currents.

i_o. In this stage, the energy stored in L_A during P_1 is transferring to C_A through S_2 and S_4. This stage will end at t_3, when i_{LA} has declined to zero.

3) Stage $P_3[t_4, t_5]$: The start time of this stage, t_4, can be calculated once the microprocessor has provided the prior information of negative load step. Similar to P_1, when the circuit enters stage P_3, the auxiliary circuit generates an increasingly negative i_a, while releasing energy from C_A. Different from P_1, however, the trajectory of i_a will never be quasi-linear, but becomes quasi-sinusoidal as a result of an RLC oscillation. The slew rate of i_a depends on the values of L_A and C_A, and the initial voltage of C_A at t_4.

4) Stage $P_4[t_5, t_6]$: At the start of this stage, i_a has reached the level of $-\Delta I_o$. Switch S_1 will be open to cut off i_a, and

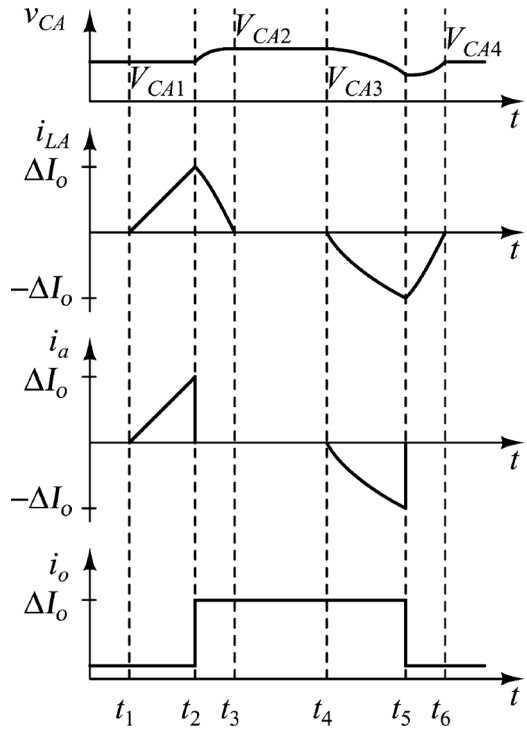


Fig. 10. Waveforms of the auxiliary circuit for the four operating stages for ΔI_o stepping up at t_2 and down at t_5.

hence current in L_A will start to flow through the closed switch S_5 to C_A. Hence, the transients in i_a and i_o counteract each other at t_5. Then, i_{LA} will decline to zero at t_6, which is the end of this stage.

B. Operating Principles

First, as presented in Section III-A1, in stage P_1, i_a is equal to i_{AL}, which is given as

$$i_{LA}(t) = V_o/R_{d1}\left[1 - e^{-R_{d1}/L_A(t-t_1)}\right] \quad (t_1 \le t \le t_2), \tag{2}$$

where R_{d1} is the dominant parasitic resistance in topology P_1 and equal to the sum of turn-on resistances of the two switches and the ESR of L_A. In stage P_3, i_{LA} flows through S_1 to the load giving a negative quasi-sinusoidal i_a, which is given by

$$\begin{aligned} i_{LA}(t) &= -i_{m3}\sin\omega_d(t-t_4) \\ &\approx -i_{m3}\sin\frac{t-t_4}{\sqrt{L_A C_A}} \quad (t_4 \le t \le t_5), \end{aligned} \tag{3}$$

where

$$i_{m3} = \frac{(V_{CA2} - V_o)\sqrt{C_A}}{\sqrt{L_A}} e^{\frac{-R_{d3}}{2L_A}(t-t_4)} \tag{4}$$

and R_{d3} is the dominant parasitic resistance in topology P_3. Since in P_3 the current starts from zero, $i_a(t)$ is in the phase range $[0, (t_5 - t_4)/\sqrt{L_A C_A}]$, as depicted in Fig. 11.

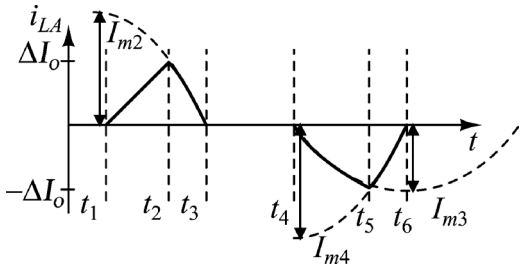


Fig. 11. Sinusoidal inductor current in the auxiliary circuit starts and ends at certain phase angle with different magnitudes.

TABLE I
PARAMETERS OF POWER SUPPLY AND LOAD FOR AUXILIARY CIRCUIT DESIGN

Symbols	Descriptions
V_o	Output voltage of the power supply
$\Delta I_{o\max}$	Maximum transient step of the actual load
$k_{U\max}$	Maximum slew rate of positive transient of the output current of power supply i_{eo} that does not cause output voltage fluctuation
$k_{D\max}$	Maximum slew rate (absolute value) of negative transient of output current of power supply i_{eo} that does not cause output voltage fluctuation
$k_{p\max}$	Maximum allowable slew rate of the varying i_{eo} that does not cause fluctuation of V_o exceeding $\pm 3\%$ reference value (see Fig. 12)

C. Parameters Constraints From $k_{U\max}$, $k_{D\max}$ and $\Delta I_{o\max}$

From the definitions of $k_{U\max}$ and $k_{D\max}$ shown in Table I, in order to achieve a null response to large load current transients, the auxiliary circuit should be designed to satisfy

$$di_a/dt \le k_{U\max} \tag{5}$$

and

$$di_a/dt \ge -k_{D\max} \tag{6}$$

in P_1 and P_3, respectively. When the auxiliary circuit is sinking current in P_1, the slew rate of i_a is given as

$$\frac{di_a}{dt} = (V_o/L_A)e^{-R_{d1}/L_A(t-t_1)} \le V_o/L_A \le k_{U\max}. \tag{7}$$

Thus, the inductance value should be limited as

$$L_A \ge V_o/k_{U\max}. \tag{8}$$

In P_3, releasing current to the load, the slew rate of i_a will take the form as

$$\begin{aligned}\frac{di_a}{dt} &= -\frac{V_{CA2}-V_o}{L_A}\cos\frac{t-t_4}{\sqrt{L_AC_A}}e^{-\frac{R_{d3}}{2L_A}(t-t_4)} \\ &\quad + \frac{V_{CA2}-V_o}{L_A}\sin\frac{t-t_4}{\sqrt{L_AC_A}}\frac{R_{d3}}{2L_A}e^{-\frac{R_{d3}}{2L_A}(t-t_4)} \\ &\ge -k_{D\max}(t_4 \le t \le t_5),\end{aligned} \tag{9}$$

from which the limitation for L_A can be derived as

$$-\frac{V_{CA2}-V_o}{L_A} \ge -k_{D\max} \tag{10}$$

and

$$L_A \ge (V_{CA2}-V_o)/k_{D\max}. \tag{11}$$

Moreover, considering $\Delta I_{o\max}$, (4) is limited as

$$I_{m3} = \frac{(V_{CA2}-V_o)\sqrt{C_A}}{\sqrt{L_A}}e^{-\frac{\pi R_{d3}\sqrt{C_A}}{4\sqrt{L_A}}} \ge \Delta I_{o\max}. \tag{12}$$

D. Determination of Parameters

The value of V_{CA2} determines the slew rate of i_a at P_3, as observed from (9). Hence, lowering V_{CA2} will reduce the interference of i_a for the power supply. However, a lower V_{CA2} means that a larger capacitor is required, since in P_3, the energy requirement will be covered by the energy released by C_A, which is given as $C_A(V_{CA2}^2 - V_{CA3}^2)/2$.

With V_{CA2} determined, (5) and (11) are used as the lower bound of L_A, i.e.,

$$L_A \ge \max\left\{\frac{V_{CA2}-V_o}{k_{D\max}}, \frac{V_o}{k_{U\max}}\right\}. \tag{13}$$

Furthermore, from (12), the constraint for C_A can be derived as

$$C_A \ge \frac{\Delta I_{o\max}^2 L_A}{(V_{CA2}-V_o)^2}e^{\frac{\pi R_{d3}\sqrt{C_A}}{2\sqrt{L_A}}}, \tag{14}$$

where R_{d3}/L_A needs to be sufficiently smaller than $1/\sqrt{L_AC_A}$ so as to make $e^{(\pi R_{d3}\sqrt{C_A})/(2\sqrt{L_A})}$ approach 1. To determine the time instants of the switching actions, we refer to Fig. 10. Specifically, the time instants t_2 and t_5 (duration being equivalent to T_e in Fig. 7) will be provided to the auxiliary circuit. The auxiliary circuit can readily calculate the switching time instant t_1 from (2) and t_4 from (3) (duration being equivalent to t_{as} in Fig. 7) using

$$t_1 = t_2 - \frac{L_A}{R_{d1}}\ln\left(\frac{V_o}{V_o - \Delta I_o R_{d1}}\right) \tag{15}$$

and

$$t_4 = t_5 - {i_{LA}}^{-1}(\Delta I_o), \tag{16}$$

where i_{LA}^{-1} represents the inverse function of $i_{LA}(t)$ in (3) which has no analytical solution. In practical applications, t_1 and t_4 can be obtained by using a look-up table that contains the off-line numerical calculation results of (2) and (3) to reduce the on-line calculations.

IV. ALTERNATIVE PRACTICAL IMPLEMENTATION

A. Practical Trade-Offs

The proposed pre-energizing strategy and auxiliary circuit scheme aims to achieve null response in V_o to fast current transients. In practice, most applications allow some voltage fluc-

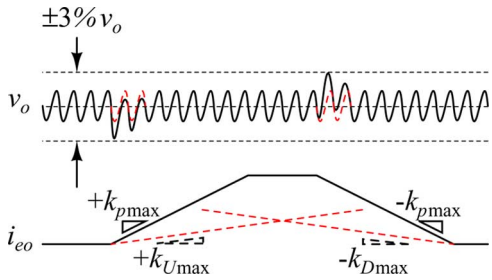


Fig. 12. Allowed fluctuation of V_o, e.g., ±3% band, incurred by the i_{eo} with the slew rate of $k_{p\max}$.

tuation in V_o, while size, cost and efficiency remain the key considerations.

The solution presented in Section III requires a large inductor and a large capacitor in order to achieve an ideal performance. Smaller values of $k_{U\max}$ and $k_{D\max}$ require larger capacitors, as can be seen from Fig. 13. For applications involving 15 A current transients, for instance, increasing V_{CA2} to 12 V may reduce the value of C_A to 0.3 mF, but it also increases L_A to 100 μH which would still take up a significant space. From (13), applying i_a with higher slew rates than $k_{U\max}$ and $k_{D\max}$ will necessitate a smaller inductance of L_A leading to an increase in the voltage deviation of v_o. Also, $k_{p\max}$ is used to define the fast load current which would control the maximum voltage deviation, as shown in Fig. 12. Moreover, applying a faster current slope (as determined by $k_{p\max}$) and increasing V_{CA2} may not decrease L_A to an accepted range.

To reduce the size of storage elements, a practical approach is to operate the auxiliary circuit in switching mode, emulating the linear ramping currents in stages P_1 and P_3 with switching ramps, as illustrated in Fig. 14 [27], [28]. Specific arrangements are explained in the next subsection.

B. Alternative Switching Scheme

In the two time durations $[t_1, t_2]$ and $[t_4, t_5]$, i_a should be ramping up and down, respectively, at a sufficiently low rate. The strategy described in Section III employs two topologies corresponding to stages P_1 and P_3 to achieve the required function.

As discussed above, implementing stages P_1 and P_3 in switching mode would reduce the size of L_A significantly. Our approach is to switch between P_1 and P_3, and the required ramping current (up or down, as appropriate) can be achieved in the average sense by controlling the duty cycle, as illustrated in Fig. 14. To avoid confusion, we denote the ramp-up stage (originally P_1) as P_{1-3}, and the ramp-down stage (originally P_3) as P_{3-1}. Also, for brevity, we denote di_a/dt given in (7) and (9) as k_{a1} and k_{a3}. It should be noted that even when k_{a1} and k_{a3} are much larger than what is required, the duty cycle (ratio of durations of P_1 and P_3) can be programmed to generate i_a with the needed slew rate of k_{a1-3} and k_{a3-1} for P_{1-3} and P_{3-1}, as illustrated by the dash line in Fig. 14. The original time durations $[t_1, t_2]$ and $[t_4, t_5]$ will be replaced by the durations of stages P_{1-3} and P_{3-1}, respectively.

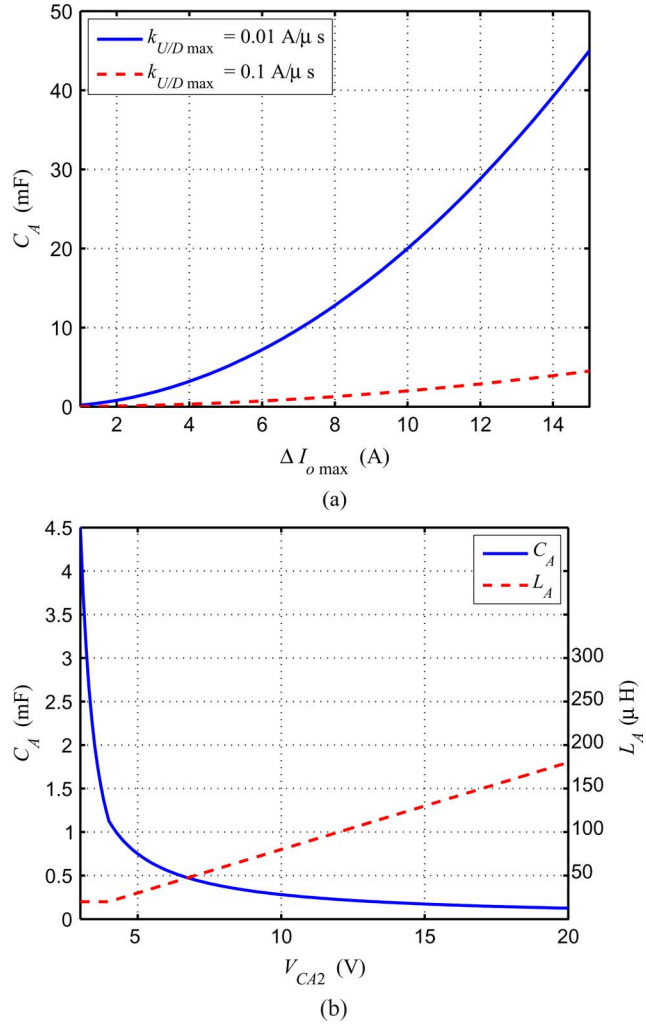


Fig. 13. Value of C_a versus (a) $\Delta I_{o\max}$ in $V_o = 2$ V and $V_{CA2} = 3$ V or (b) V_{CA2} in $V_o = 2$ V, $\Delta I_{o\max} = 15$ A and $k_{U/D\max} = 0.1$ A/μs.

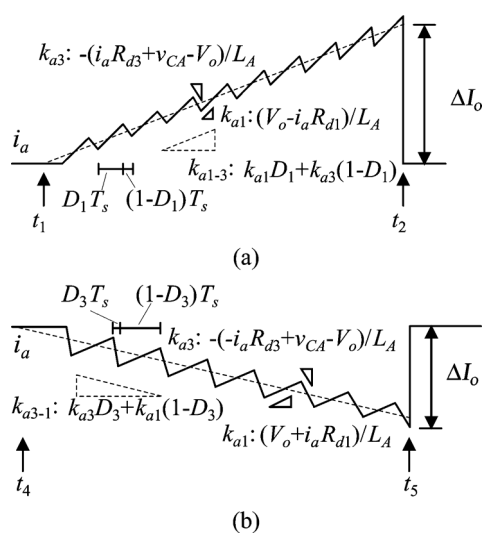


Fig. 14. Waveforms of i_a during (a) $[t_1, t_2]$ and (b) $[t_4, t_5]$ using high-frequency switching mode implementation.

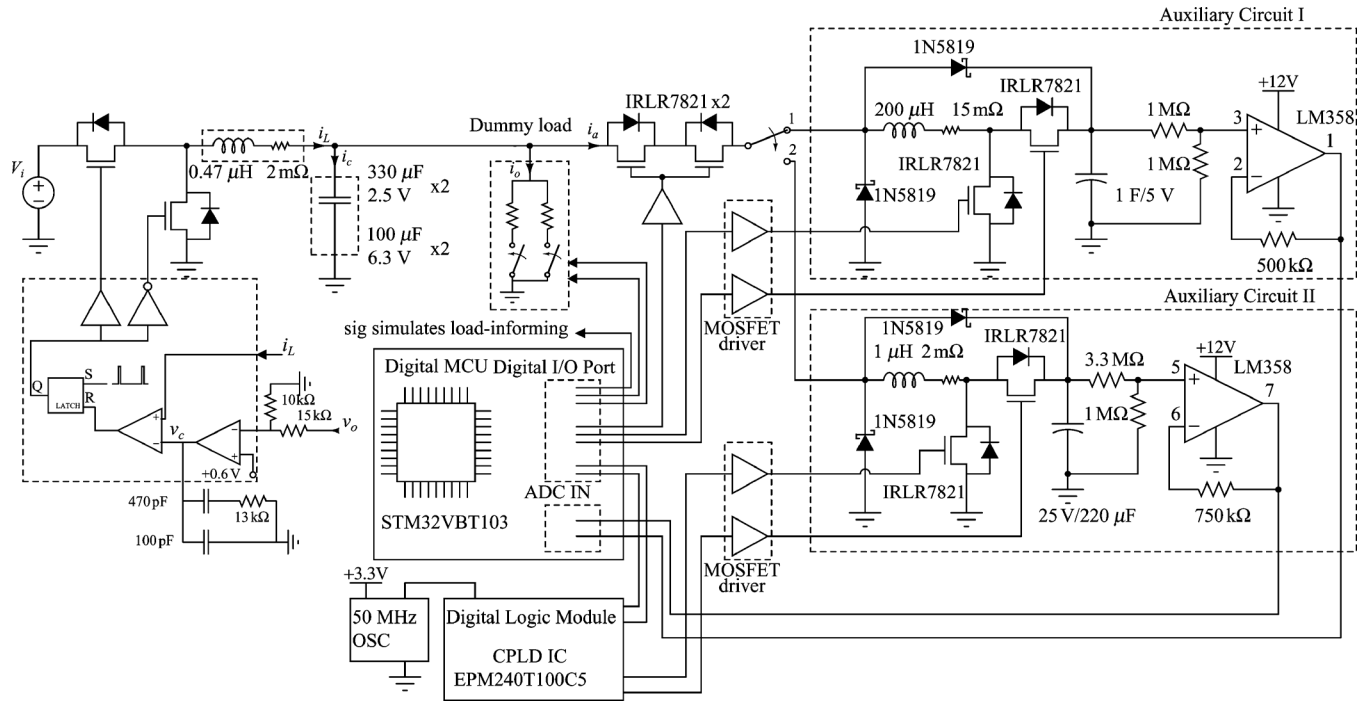


Fig. 15. Schematic diagram of experimental prototype.

During P_{1-3} and P_{3-1}, the duty cycles of the auxiliary circuit, D_1 and D_3, can be derived as

$$D_1 = \frac{k_{a1-3} - k_{a3}}{k_{a1} - k_{a3}} \approx 1 - \frac{V_o - L_A k_{a1-3} - i_a R_{d3}}{v_{CA}} \tag{17}$$

and

$$D_3 = \frac{k_{a3-1} - k_{a1}}{k_{a3} - k_{a1}} \approx \frac{V_o - L_A k_{a3-1} - i_a R_{d1}}{v_{CA}}, \tag{18}$$

assuming that $R_{d1} \approx R_{d3}$ and i_a is approximately constant during a switching cycle.

C. Circuit Design

In this alternative implementation of the auxiliary circuit, L_A and C_A are determined by the upper limits of the switching ripples, $\Delta I_{o\max}$, v_{CA}, and the expected value of k_{a1-3} and k_{a3-1}.

First of all, V_{CA2} is chosen as discussed in Section III-D. Second, the switching frequency is chosen according to the driving technique and devices used, and is normally several hundreds of kHz to one MHz. Third, L_A can be designed by considering the ripple magnitude of i_a which should be limited by the ripple band of the main converter. Fourth, C_A is designed to store sufficient energy that is released during P_{3-1}, i.e.,

$$\frac{1}{2}C_A\left(V_{CA2}^2 - V_{CA3}^2\right) \geq \frac{V_o \Delta {I_o}^2}{2k_{a3-1}} + \frac{1}{2}L_A \Delta {I_o}^2 + E_{\mathrm{cond\_loss}}, \tag{19}$$

where $E_{\mathrm{cond\_loss}} \approx (R_{d1} + R_{d3})/(6k_{a3-1})\Delta I_o^3$. Hence, C_A is given as

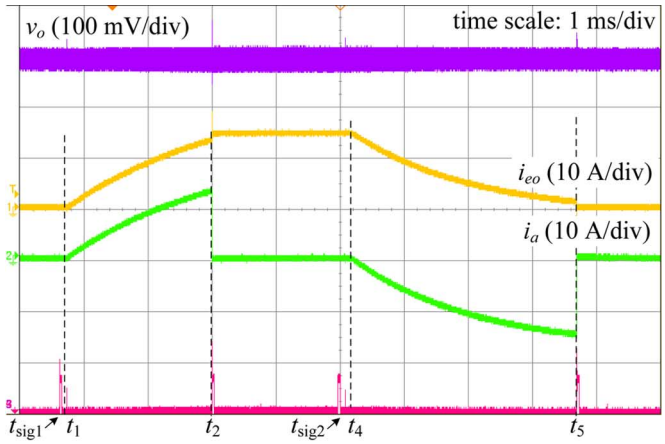
$$C_A \geq \frac{\frac{V_o \Delta {I_o}^2}{k_{a3-1}} + L_A \Delta {I_o}^2 + 2E_{\mathrm{cond\_loss}}}{(V_{CA2}^2 - V_{CA3}^2)}. \tag{20}$$

TABLE II
PARAMETERS OF THE DC-DC SYNCHRONIZED BUCK CONVERTER (WHICH SERVES AS THE EXTERNAL POWER SUPPLY TO THE LOAD)

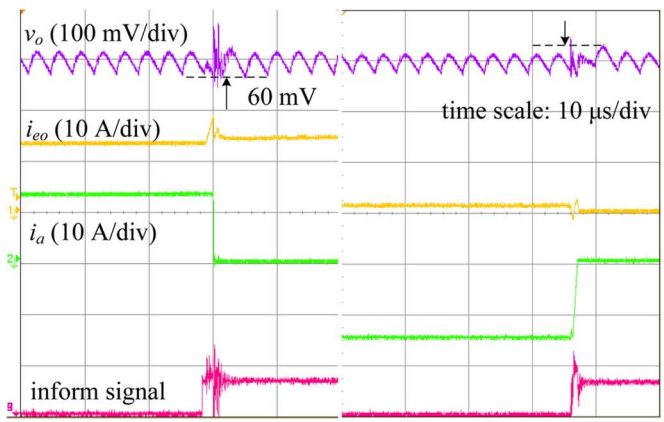
Parameters/Components	Values
Input voltage	12 V
Output voltage	1.5 V
Inductance	0.47 μH
Output capacitance	2 × 100 μF 2 × 330 μF
Maximum current	20 A
Switching frequency	300 kHz
Operation mode	Continuous mode
Control	Current mode control
$k_{U\max}$	8 A/ms
$k_{D\max}$	-8 A/ms
$k_{p\max}$	±100 A/ms

D. Voltage Control of C_A

As mentioned before, at the instant of t_4, the auxiliary circuit should guarantee that C_A is charged adequately for use in P_{3-1}. However, V_{CA3} is related to past operations of the auxiliary circuit. A worst case is that the load generates step-down transients and slow ramp-up currents. In that case, v_{CA} will get smaller due to operation for the step-down transients. Even in a general situation, the magnitudes of positive and negative fast transients are not always symmetrical, which would makes v_{CA} drift toward one direction. Applying P_1 or P_3 to generate small i_a is able to regulate v_{CA} to a suitable level, when the auxiliary circuit is not operating for transients. The suitable level for v_{CA} is related to the instantaneous load current. An effective scheme to set the suitable v_{CA} has been described in [29], and has been adopted in the prototype.



(a)



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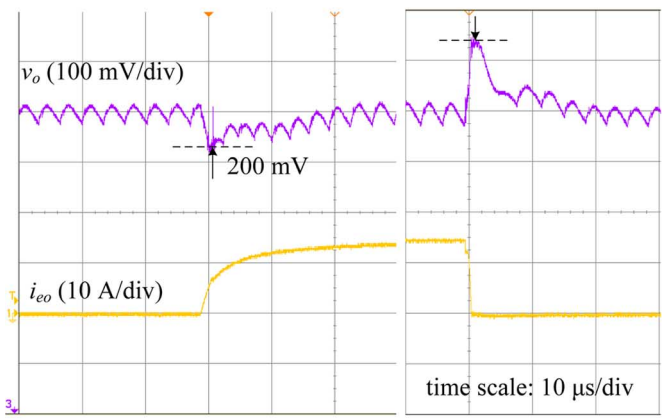

(c)

Fig. 16. Response comparisons for a 10 A transient between the system with and without using the proposed method. (a) Waveforms of the system with Auxiliary Circuit I, (b) enlargement of (a) near t_2 and t_5, and (c) waveforms of the system without the method.

V. Experimental Validation

In this section, an experimental prototype is constructed to validate the proposed method. A low voltage and high current load (1.5 V and 20 A (max)) is selected to emulate a practical microprocessor load. The power supply is a synchronous dc-dc buck converter, whose circuit parameters are shown in Table II. It is a high performance converter, and is capable of handling load current slew rates of up to $k_{U\max} = 8$ A/ms and $k_{D\max} = -8$ A/ms without voltage fluctuation, or $k_p = \pm 100$ A/ms with voltage fluctuation within $\pm 3\%$ of 1.5 V. In this paper, the original implementation with ideal performance but large components (*Auxiliary Circuit I*) and the switching implementation with small components but limited voltage spikes (*Auxiliary Circuit II*) are constructed to validate the method.

TABLE III
Parameters of **Auxiliary Circuit I**

Parameters/Components	Values
L_A	200 μH/15 A (max)
C_A	1 F/5 V
v_{CA}	3.0 V—2.8 V
k_{a1}	8 A/ms
k_{a3}	-8 A/ms
MOSFETs ($S_{1,3,4}$)	IRLR7821, $R_{\mathrm{DS(ON)}}$=10 mΩ
Diodes ($S_{2,5}$)	1N5819, V_F = 0.55 V

TABLE IV
Parameters of **Auxiliary Circuit II**

Parameters/Components	Values
L_A	1 μH/15 A (max)
C_A	220 μF
v_{CA}	9.5 V—4.5 V
k_{a1}	1500 A/ms
k_{a3}	-8000 A/ms
f_s	500 kHz for $P_{1\text{-}3}$ 1 MHz for $P_{3\text{-}1}$
$k_{a1\text{-}3}$,$k_{a3\text{-}1}$	$\pm$100 A/ms
ripple on i_a	1.5 A
MOSFETs ($S_{1,3,4}$)	IRLR7821, $R_{\mathrm{DS(ON)}}$=10 mΩ
Diodes ($S_{2,5}$)	1N5819, V_F = 0.55 V

A. Prototype Design

The prototype comprises a general converter, a dummy load, and a digital controller to emulate a computer load, and it also performs as the proposed power management unit to provide advance loading information and control the auxiliary circuit. The schematic diagram is shown in Fig. 15.

A traditional type-II compensation strategy is utilized in this converter. The dummy load is capable of generating 0–15 A transients at 20 A/μs by a resister bank. Switching actions of the resister bank are controlled by the digital micro-controller. When the load prediction signal comes, the digital controller will schedule time instants t_1, or t_4. When the switching actions are taken at t_2 or t_5, the auxiliary circuit will operate synchronously, and another indication signal is generated to represent the information from the load. In this prototype, the dummy load and the auxiliary circuit are controlled by one controller which validates the idea in Fig. 5 for integrating the power management unit with the computer. It should be noted that the information signal in Figs. 16(a) and (b) is used to demonstrate the load-informed power management and monitor the operation of the prototype.

Two auxiliary circuits are constructed. The parameters are given in Tables III and IV. In Auxiliary Circuit I, the minimum capacitor for $V_{CA2} = 3.0$ V is 0.02 F. To allow for conduction loss and current leakage, C_A is chosen as 1 F/5 V. Thus, the size of the capacitor is still very large. Hence, this solution remains illustrative but understandably impractical. The advantage for this circuit is that a high speed controller is not necessary, and

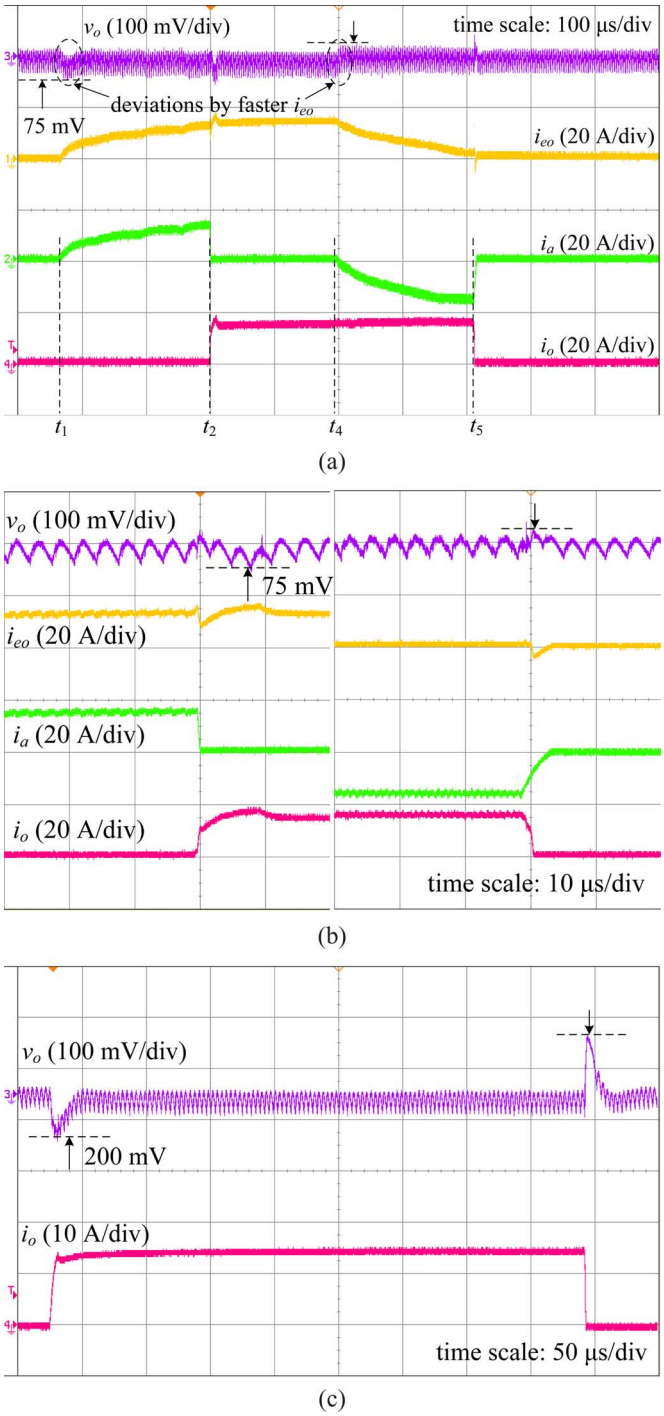

Fig. 17. Response comparisons for a 15 A transient between the system with and without using the proposed method. (a) Waveforms of the system with Auxiliary Circuit II, (b) enlargement of (a) near t_2 and t_5, and (c) waveforms of the system without the method but with an additional 220 μF filter capacitor.

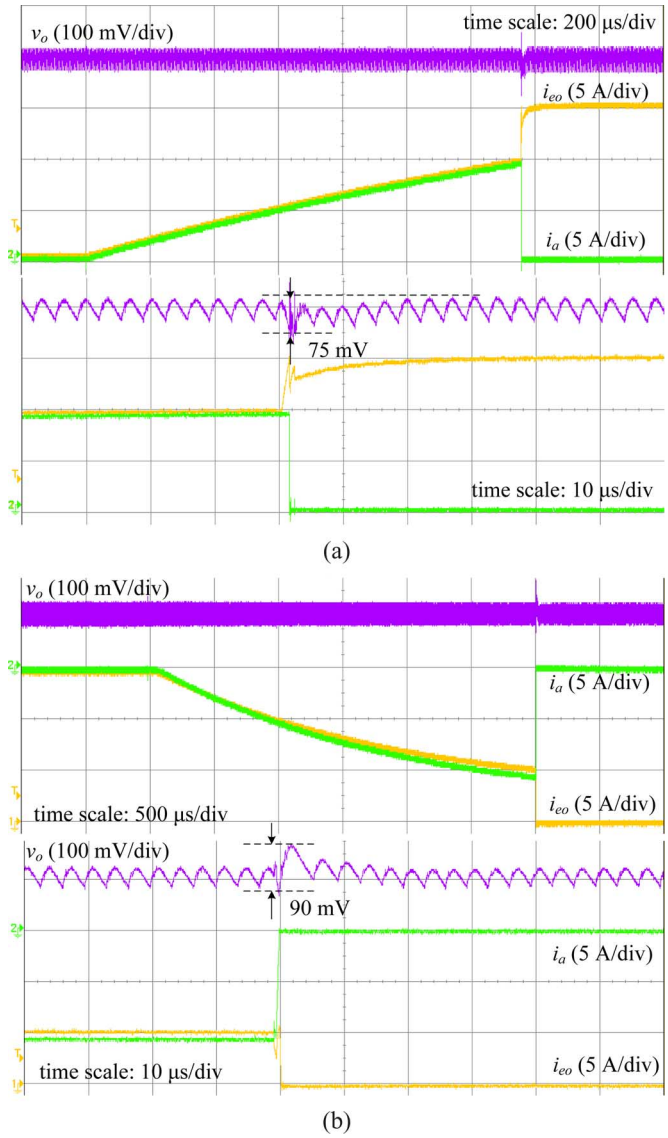

Fig. 18. Effects of the auxiliary circuit generating a magnitude mismatched current for (a) step-up load current, and (b) step-down load current.

the turn-on duration is several milliseconds for a 15 A transient. The driving loss is reduced but the conduction loss is increased due to the long operation time for a given transient.

In Auxiliary Circuit II, similar to Auxiliary Circuit I, the digital controller is responsible for providing S_1 and the enable signals of S_3 and S_4. The duty cycles in stages P_{1-3} and P_{3-1} are controlled by a digital logic module (CPLD in Fig. 15). Since v_{CA} is always varying during the above two stages, a strategy implemented within the digital logic module can be used to generate the incremental duty cycles, i.e., D_1 and D_3, during P_{1-3} and P_{3-1}. The digital controller will capture the voltage signal of v_{CA}, and whenever the voltage is running beyond the specified range, a voltage adjustment will be enabled. In this scenario, S_1 will be turned on first, then S_3 and S_4 are turned on alternately, charging or discharging C_A accordingly [29].

B. Experimental Results

The effectiveness of Auxiliary Circuit I is illustrated in Fig. 16. The use of the auxiliary circuit can effectively suppress the voltage fluctuation, reducing the magnitude of the output voltage fluctuation from 200 mV to 60 mV.

When Auxiliary Circuit II is applied, the voltage fluctuation is increased, as shown in Fig. 17. A faster rate of change in i_{eo}, both positive and negative, has been shown to cause about 15 mV of voltage fluctuation. In addition, the switching ripple of the auxiliary circuit generates very small voltage fluctuation in

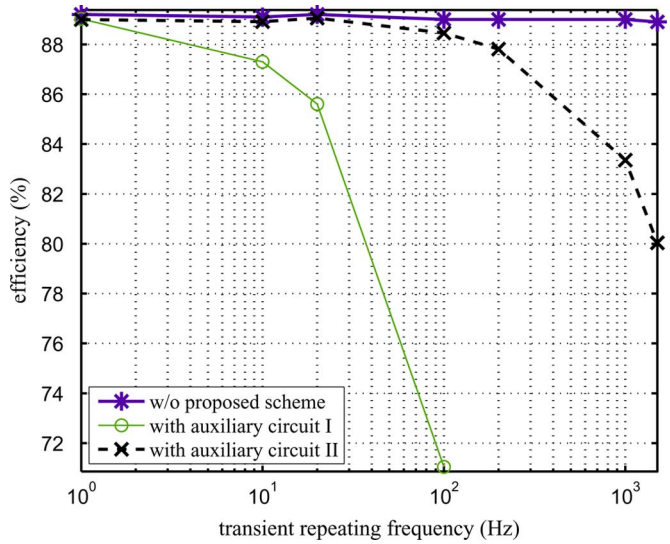

Fig. 19. Experimental measurements of efficiency degradation in the proposed method using Auxiliary Circuit I and II, where the magnitude of transients is 15 A and the mean load current is 7.5 A.

V_o. Here, Auxiliary Circuit II is able to suppress the magnitude of the output voltage fluctuation from 200 mV to 75 mV.

The analysis about the effect of inexact prediction has also been validated in this experiment. Specifically, we let the auxiliary circuit receive a prediction of 10 A step-up transient while a 15 A transient actually occurs. The same condition can be caused by a prediction error of the instant of the application of the transient, i.e., when the auxiliary circuit receives a prediction of 15 A transient while the transient occurs earlier than predicted, for instance, at the instant when i_a reaches 10 A. Therefore, in this case, a 5 A fast transient exists at i_{eo}, as reported in Fig. 18(a). Likewise, we can emulate a prediction error in the step-down transient. The result shows a 5 A mismatch in i_a and i_o, as shown in Fig. 18(b). For both cases, an acceptable voltage fluctuation of less than 90 mV is measured.

As with other auxiliary circuit schemes, the proposed method leads to converter efficiency degradation, as shown in Fig. 19. When the transient repetition rate is high, Auxiliary Circuit I incurs significantly more loss than Auxiliary Circuit II. The power losses are mainly from the conduction loss in the former scheme and additionally from the switching loss and magnetic components' loss in the latter scheme. Since the operation duration of Auxiliary Circuit I is much longer than that of Auxiliary Circuit II, the former has a poor efficiency. To solve this problem, two strategies are given. One is to apply MOSFETs with lower $R_{\mathrm{DS(ON)}}$ which is proportional to the amount of dissipation and replace $S_{2,5}$ by two MOSFETs in Auxiliary Circuit I, where these two switches are turned on for a relatively long duration. The other strategy is to use a high-performance main converter that can cope with fast dynamic response, i.e., with higher $k_{p\,\max}$, to reduce the operation duration of the auxiliary circuit.

In addition, we note that the power loss is independent of the mean load current level. For applications having a higher mean value of load current but same transient current, the effect on the efficiency degradation incurred by the auxiliary circuit would become insignificant.

In this experiment, although some characteristics (e.g., power and transient slew rate) of the prototype do not fully resemble the real microprocessor power system (e.g., hundreds of watts and hundreds of A/μs), the experimental result clearly validates the effectiveness of the proposed design in obtaining a response to large signal transients with insignificant voltage fluctuation.

VI. Conclusion

A method using auxiliary circuit to achieve null response to fast transients in a power supply system has been discussed in this paper. The idea has been inspired by a basic design paradigm shift requiring the load to provide real-time information about its power consumption dynamics. Then, the auxiliary circuit provides slowly rising current to pre-energize the power supply prior to actual load steps, cooperating with advance notice from the load. Such a development trend seems to be highly promising as the design of the associated power management circuits and systems can be desirably facilitated and the performance specifications can be more readily met. Thus, our idea transpires a possible future development of microprocessors which sees the inclusion of an auxiliary power circuit as a standard integrated part and the use of predictable load demand information for achieving the required power supply functions. In this paper we propose two specific implementations of the method and demonstrate their feasibility in a practical environment.

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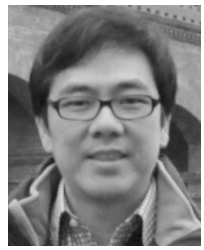

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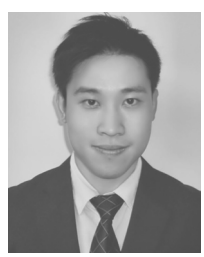

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