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# Improved Charge-Trapping Characteristics of $BaTiO_3$ by Zr Doping for Nonvolatile Memory Applications

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***Abstract*—The charge-trapping characteristics of $BaTiO_3$ film with and without Zr incorporation were investigated based on $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ capacitors. Compared with the device without Zr incorporation, the one with Zr incorporation showed a similar memory window (8.3 V at $\pm$12 V for 1 s), but higher program speed at low gate voltage (3.2 V at 100 $\mu$s + 6 V) and better endurance and data retention (charge loss of 6.4% at 150 °C for $10^4$ s), due to the Zr-doped $BaTiO_3$ exhibiting higher charge-trapping efficiency and higher density of traps with deeper energy levels.**

***Index Terms*—$BaTiO_3$, charge-trapping layer (CTL), nonvolatile memory, Zr incorporation.**

## I. Introduction

DUE to discrete charge-storage and coupling-free properties, metal–alumina–nitride–oxide–silicon (MANOS) NAND nonvolatile memory devices with dielectrics as charge-trapping layer (CTL) have been considered as a promising candidate to replace their floating-gate counterparts. Recently, high-$k$ dielectrics have been widely proposed to replace $Si_3N_4$ as CTL for continual downscaling of cell size and improving the charge-storage capacity [1]–[4]. Among various high-$k$ dielectrics, $BaTiO_3$ is well known for high dielectric constant ($k > 100$) with strong scaling ability [5], [6] and its negative band offset with respect to Si, thus leading to a large barrier height relative to $SiO_2$ ($\Delta E_c \sim 3.6$ eV) [7]. Therefore, it should be a promising candidate as CTL for nonvolatile memory applications. In addition, Zr-doped $BaTiO_3$ has also attracted increasing interest because the isovalent substitution of Ti with Zr in $BaTiO_3$ can shift the Curie temperature below room temperature, thus making the dielectric paraelectric at room temperature without fatigue problems [5]. Moreover, since $Zr^{4+}$ ion is chemically more stable than $Ti^{4+}$, Zr-doped $BaTiO_3$ has been demonstrated to have a lower leakage current than $BaTiO_3$ while maintaining a comparable dielectric constant [5]–[7]. However, there has been no report on Zr-doped $BaTiO_3$ as CTL for nonvolatile memory applications so far. Therefore, this letter aims to study the charge-trapping properties of $BaTiO_3$ film with and without Zr incorporation.

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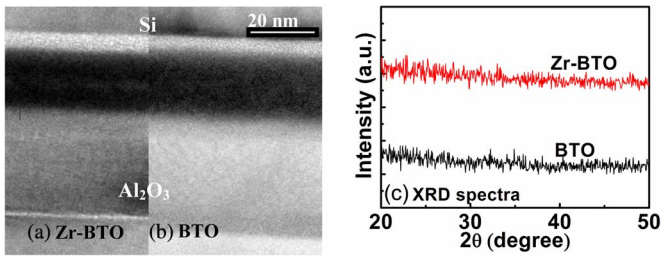


Fig. 1. Cross-sectional TEM images of (a) Zr-BTO and (b) BTO. (c) XRD spectra of $BaTiO_3/SiO_2$ with and without Zr incorporation on a Si substrate. The CTL thicknesses for the Zr-BTO and BTO samples are 9.5 and 10.6 nm, respectively.

## II. Experiment

A MANOS capacitor with $Al/Al_2O_3/$Zr-doped $BaTiO_3/SiO_2/Si$ structure (denoted as Zr-BTO) was fabricated on a p-type silicon substrate. After the RCA cleaning, 2-nm $SiO_2$ as tunneling layer (TL) was grown on the wafers by thermal dry oxidation. Then, 10-nm Zr-doped $BaTiO_3$ was deposited on the $SiO_2$ by reactive sputtering using $BaTiO_3$ and Zr targets in a mixed $Ar/O_2$ ambient, and the atomic ratio of Zr and Ti was determined to be 1/3 from X-ray photoelectron spectroscopy (XPS) analysis. This Zr/Ti ratio was close to the optimal value (1/4) in [5], which reported that the Zr-doped $BaTiO_3$ film degraded with further increase in the Zr/Ti ratio. $\Delta E_c$ also decreases with increasing Zr/Ti ratio [6], which is harmful to the data retention of the device. Following that, 15-nm $Al_2O_3$ as blocking layer (BL) was deposited by atomic layer deposition at 300 °C. Then, the sample went through postdeposition annealing in a $N_2$ ambient at 900 °C for 30 s. Finally, Al was evaporated and patterned as a gate electrode with a diameter of 100 $\mu$m, followed by forming gas annealing at 300 °C for 20 min. In addition, a control sample with $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ structure (denoted as BTO) was also fabricated by the same process for comparison.

## III. Results and Discussion

Fig. 1 shows the cross-sectional transmission electron microscopy (TEM) images of the MANOS capacitors with and without Zr incorporation, where both CTLs display an amorphous state. This is consistent with the observation of the X-ray diffraction (XRD) spectra shown in Fig. 1(c). The CTL with an amorphous state is favorable for data retention because charge loss via grain boundaries can be avoided [1]. Moreover, compared with the BTO sample, the Zr-BTO sample displays negligible interlayer between the TL/CTL/BL layers, which can

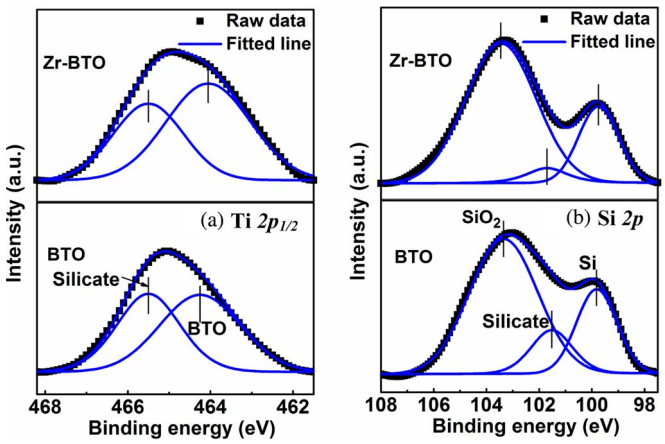


Fig. 2. XPS spectrum of $BaTiO_3/SiO_2$ on a Si substrate with and without Zr incorporation. (a) Ti $2p_{1/2}$. (b) Si $2p$.

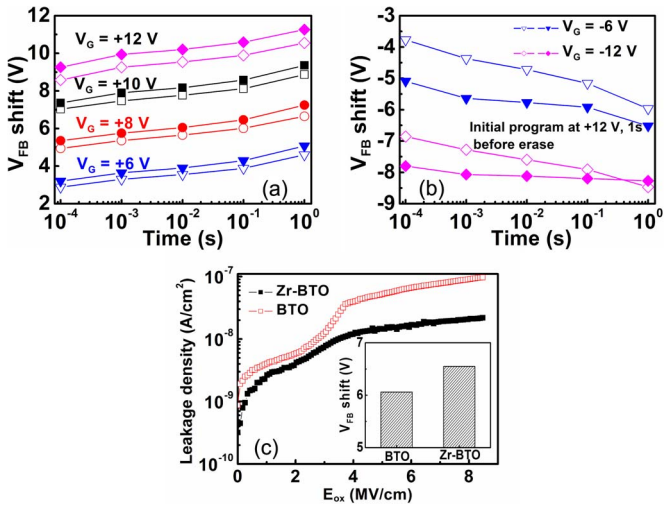


Fig. 3. (a) Program and (b) erase transient characteristics for the (solid symbol) Zr-BTO and (open symbol) BTO samples. (c) Gate leakage relative to $E_{\rm ox}$. (Inset) $V_{\rm FB}$ shift after sweeping. The equivalent oxide thickness and the initial $V_{\rm FB}$ for the Zr-BTO and BTO samples are 11.6 nm/−1.9 V and 11.8 nm/−1.8 V, respectively.

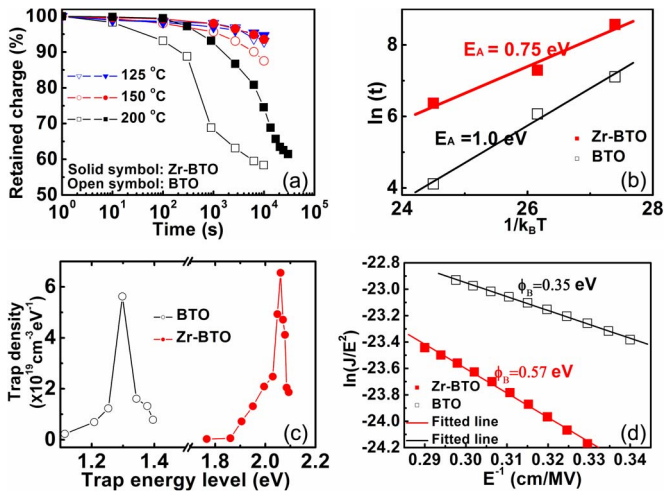


Fig. 4. (a) Data retention. (b) Arrhenius plot of the retention property. (c) Trap density relative to the energy level below the $BaTiO_3$ conduction-band edge. (d) Fowler–Nordheim plots for the MANOS (Al/CTL/TL/Si) capacitors under negative gate voltages, where $\ln(J/E^2)$ linearly varies with $E^{-1}$. $J$ is the current density, and $E$ is the electric field across the CTL. The barrier height $\Phi_B$ of the Al/CTL interface is extracted from the slope of the fitted line [12].

be further confirmed by XPS analysis. Fig. 2 shows the Ti $2p$ and Si $2p$ spectra, as well as the curve-fitting lines. For the BTO sample, the Ti $2p_{1/2}$ spectrum shows two peaks, where the stronger peak located at 464.3 eV agrees with the Ti–O bonding for $BaTiO_3$, whereas the weaker peak at 465.5 eV is assigned to Ti silicate formed by chemical reaction at the CTL/$SiO_2$ interface due to the poor thermodynamic stability of Ti [5], [8]. Compared with the BTO sample, the Ti $2p_{1/2}$ spectrum corresponding to the $BaTiO_3$ component in the Zr-BTO sample shifts to a lower binding energy by 0.2 eV, which is ascribed to oxygen vacancies generated by the substitution of Ti with Zr. Oxygen vacancies are normally associated with substitution at the Ti site, giving rise to deep traps, and are desirable for memory devices [9]. Fig. 2(b) shows the Si $2_p$ spectrum, where the three components for the BTO sample correspond to the Si substrate (∼99.8 eV), the silicate (∼101.5 eV), and the $SiO_2$ TL (∼103.4 eV), respectively [8]. The suppressed formation of silicate with negligible content is observed for the Zr-BTO sample due to the better stability of Zr than Ti [5], [7]. Note that an abrupt CTL/$SiO_2$ interface is beneficial for the memory device.

The program/erase (P/E) transient characteristics of the memory devices with and without Zr incorporation are shown in Fig. 3. The Zr-BTO sample displays a similar memory window (∼8.3 V) as the BTO one (∼8.5 V) under ±12 V for 1 s, but has higher P/E speeds than the latter. As the operating voltage $V_G$ increases from +6 to +12 V with a pulsewidth of 100 $\mu$s, the flatband voltage shift $\Delta V_{\rm FB}$ increases from 2.9 to 8.6 V for the BTO sample. For comparison, the $\Delta V_{\rm FB}$ of the Zr-BTO sample is from 3.2 to 9.3 V under the same conditions. The higher program speed for the Zr-BTO sample than the BTO one is mainly ascribed to the higher charge-trapping efficiency resulting from Zr incorporation. This can be further confirmed by the gate leakage as a function of $E_{\rm ox}$ (electric field across $SiO_2$), as shown in Fig. 3(c), where the BTO sample presents higher leakage than the Zr-BTO one, indicating that more electrons flow from the substrate into the gate electrode rather than being trapped in the CTL. Consequently, it shows a smaller $\Delta V_{\rm FB}$ (∼6.1 V) after sweeping than the Zr-BTO one (∼6.6 V). Moreover, due to the better stability of Zr than Ti [5], [7], Zr incorporated in $BaTiO_3$ can suppress the diffusion of Ti toward $Al_2O_3$ (or $SiO_2$) and the formation of interlayer at the BL/CTL (or CTL/TL) interface, as demonstrated in Figs. 1 and 2. This can reduce undesirable electron injection from the gate to the CTL under erase mode, thus contributing to higher erase speed for the Zr-BTO sample. This claim can be further supported by the larger leakage of the BTO sample under negative voltage (5.2 nA/cm$^2$ at $V_G = -2$ V) than that of the Zr-BTO one (4.0 nA/cm$^2$ at $V_G = -2$ V). Although the operating voltage here is lower than those with a single layer or a band-engineered structure as CTL [2]–[4], our sample even has higher operating speed, further demonstrating the merit of using Zr-doped $BaTiO_3$ as CTL for low-voltage high-performance memory applications.

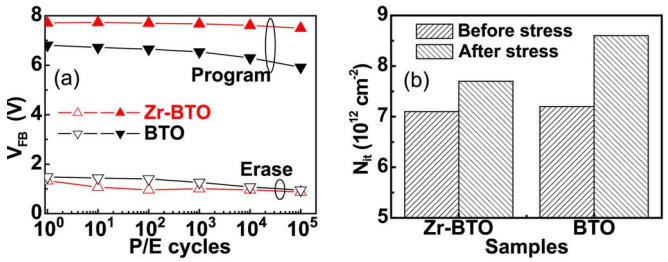


Fig. 5. (a) Endurance characteristics. (b) Interface-state density $N_{\rm it}$ before and after $10^5$-cycle P/E stress extracted by the method of Terman [14].

Fig. 4(a) displays the retention characteristics of the memory devices under high temperatures. As the temperature is from 125 °C to 200 °C, the corresponding charge loss rate after $10^4$-s baking time increases from 5.4% to 25.5% and from 7.0% to 41.6% for the Zr-BTO and BTO samples, respectively. The lower charge loss rate of the Zr-BTO sample demonstrates its better data retention. Moreover, the activation energy $E_A$ extracted from the Arrhenius plot of the retention property is also presented in Fig. 4(b) and is used to investigate the dependence of charge loss on testing temperature. The smaller $E_A(\sim 0.75$ eV) of the Zr-BTO sample than the BTO one ($\sim$1.0 eV) indicates lower charge loss expected under higher temperatures. The charge loss for both samples is sensitive to the temperature, which is consistent with the large $E_A$ here, implying that the charge loss mechanism is mainly due to a thermally activated process [10]. Considering the thermal activation as the dominant charge loss mechanism, the trap density profile as a function of trap energy can be extracted using the method in [11] and is plotted in Fig. 4(c), which shows that the traps in the BTO and Zr-BTO samples are mainly located at 1.3 and 2.1 eV below the $BaTiO_3$ conduction-band edge. This result shows that the Zr-BTO sample has more traps with deeper energy levels, which results in better data retention of the Zr-BTO sample.

Fig. 5 shows the endurance characteristics of the memory devices under a $\pm$12-V 100-$\mu$s stress pulse. For the BTO sample, the P/E window decreases from 5.3 to 5.0 V after $10^5$-cycle P/E stressing. On the contrary, the P/E windows of the Zr-BTO sample before and after the $10^5$-cycle stressing are 6.4 and 6.6 V, respectively, and negligible degradation happens. Both P/E $V_{\rm FB}$ levels shift downward with cycling, which is particularly severe for the BTO sample and is responsible for the degradation of its memory window under the stress. This suggests electron detrapping and/or hole trapping induced by the repetitive stress. As shown in Fig. 3(b), the erase transients of the Zr-BTO and BTO samples tend to saturate without an overerase phenomenon, indicating negligible hole trap sites in the CTL. Therefore, the better endurance of the Zr-BTO sample is partly due to its more deep traps because electrons located in deep traps are more difficult to escape via interface states induced by repeated P/E stress [13]. As shown in Fig. 5(b), the enhanced resistance of the Zr-BTO sample (negligible increase in interface-state density) against $10^5$-cycle stressing also contributes to its better endurance. The large memory window, high operating speed at low operating voltage, and good reliability of the Zr-BTO sample indicate its potential for multilevel cell operation with high data-storage capacity [4].

## IV. Conclusion

The charge-trapping characteristics of $BaTiO_3$ with and without Zr incorporation are investigated. The memory device with Zr-doped $BaTiO_3$ as CTL shows higher P/E speeds and better endurance and data retention than its counterpart without Zr incorporation. Therefore, Zr-doped $BaTiO_3$ is demonstrated to be a promising charge-trapping material for high-performance nonvolatile memory applications.

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