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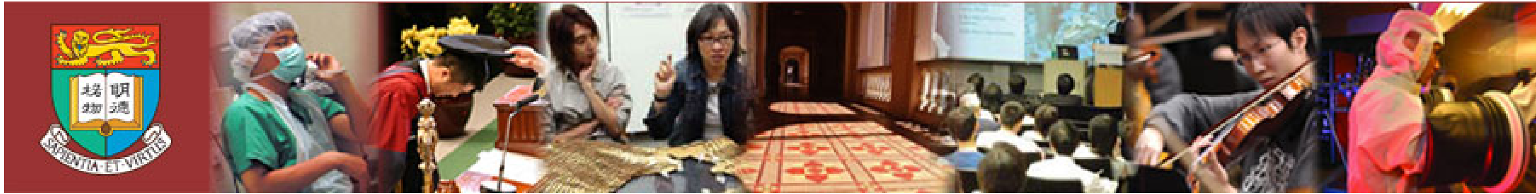

Title	Ga2O3(Gd2O3) as Charge-Trapping Layer for Nonvolatile Memory Applications
Author(s)	Huang, X; Sin, JKO; Lai, PT
Citation	IEEE Transactions on Nanotechnology, 2013, v. 12, p. 157-162
Issued Date	2013
URL	http://hdl.handle.net/10722/191389
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$Ga_2O_3(Gd_2O_3)$ as a Charge-Trapping Layer for Nonvolatile Memory Applications

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***Abstract*—The charge-trapping characteristics of Ga_2O_3 (Gd_2O_3) (denoted as GGO) with and without nitrogen incorporation were investigated based on Al/Al_2O_3/ GGO/SiO_2/Si (metal-alumina-nitride-oxide-silicon) capacitors. Compared with the capacitor without nitrogen incorporation, the one with nitrided GGO showed a larger memory window (10 V at $\pm$16 V, 1 s), a higher program speed with a low gate voltage (2.2V at +8 V, 100 μs), and a better retention property (charge loss of 9.7% after 10^4 s at 125 °C) mainly due to higher charge-trapping efficiency of the nitrided GGO film and the nitrogen-induced suppressed formation of the undesirable silicate interlayer at the GGO/SiO_2 interface, as confirmed by the transmission electron microscopy and the X-ray photoelectron spectroscopy.**

***Index Terms*—Charge-trapping layer, $Ga_2O_3(Gd_2O_3)$, high-k, nitridation, nonvolatile memory.**

I. Introduction

Conventional floating-gate flash memories with polysilicon as a charge-storage material are approaching their scaling limit mainly due to their difficulties in maintaining a high gate coupling ratio and suppressing crosstalk between neighboring cells. Metal-alumina-nitride-oxide-silicon (MANOS)-type nonvolatile memories with dielectrics as a charge-trapping layer (CTL) have been considered as a promising candidate to replace the floating-gate counterpart because of higher reliability and stronger scaling ability. Si_3N_4 was the first dielectric used as the CTL. The shortcomings of Si_3N_4 lie in its low dielectric constant ($k \sim 7$) and small conduction-band offset with respect to SiO_2 ($\Delta E_c = 1.2$ eV), which limit continual downscaling of the cell size [1], [2]. To solve these issues, extensive research works have been carried out to study high-k dielectrics for substituting Si_3N_4 as CTL [2]–[9]. Among various high-k dielectrics, $Ga_2O_3(Gd_2O_3)$ (denoted as GGO, $k \sim 14$ and $\Delta E_c \sim 1.9$ eV) is well known for its excellent thermodynamic stability and electrical properties on Si, Ge, and III–V compound semiconductor substrates, and is regarded as a promising dielectric material beyond the Si technology due to the excellent interface between GGO and high-mobility semiconductor substrate [10]–[13]. However, there has been no report focusing on the GGO film as CTL for nonvolatile memory applications so far. Moreover, nitrogen incorporation into dielectrics can induce deep-level traps in the band-gap, improve their thermal stability, and inhibit the interfacial reaction by nitrogen passivation [1]–[6]. Therefore, based on MANOS capacitors, this study aims to study the charge-trapping characteristics of GGO films with and without nitrogen incorporation. Experimental results demonstrated that this proposed device with nitrided GGO as CTL showed large memory window, high program speed, and good data retention even at 125 °C, all of which indicate its high potential for high-performance nonvolatile memory applications.

Manuscript received July 31, 2012; revised December 12, 2012; accepted December 17, 2012. Date of publication December 24, 2012; date of current version March 6, 2013. The review of this paper was arranged by Associate Editor M. De Vittorio.

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Digital Object Identifier 10.1109/TNANO.2012.2236350

II. Experiment

MANOS capacitors with an Al/Al_2O_3/$Ga_2O_3(Gd_2O_3)$/SiO_2/Si structure were fabricated on a p-type silicon substrate with a resistivity of 5 $\sim$ 10 Ω·cm and no n+ ring implant. After a standard Radio Corporation of America (RCA) cleaning, 2-nm SiO_2 as a tunneling layer (TL) was grown on the wafers by thermal dry oxidation. Then, 6-nm $Ga_2O_3(Gd_2O_3)$ film was deposited on the SiO_2 by cosputtering Ga_2O_3 and Gd targets in a mixed Ar/N_2 (1/1) or pure Ar ambient with a pressure of 4.5 and 2.4 mtorr, respectively, at a substrate temperature of 20 °C, and the corresponding MANOS capacitors were denoted as GGON and GGO. The substrate was not heated during the GGO film deposition in order to prevent the dielectric film from crystallization because grain boundaries in crystalline CTL could work as a leakage path to facilitate the charge loss, thus leading to reliability issues [5]. Following that, 15-nm Al_2O_3 as a blocking layer (BL) was deposited by means of atomic layer deposition using trimethyl-aluminum ($Al(CH_3)_3$) and H_2O as precursors at 300 °C. Then, both samples went through a postdeposition annealing in N_2 ambient at 900 °C for 30 s. Finally, Al was evaporated and patterned as a gate electrode with a diameter of 100 μm, followed by a forming-gas annealing at 300 °C for 20 min. The completed MANOS capacitors with and without nitrogen incorporation are shown in Fig. 1. The physical characteristics of the high-k dielectric films were determined by the transmission electron microscopy (TEM) and the X-ray photoelectron spectroscopy (XPS). The Fowler–Nordheim method was used to program/erase (P/E) the MANOS devices. All measurements were carried out under a light-tight and electrically shielded condition.

III. Results and Disscussion

Fig. 1 shows the TEM cross-sectional images of the MANOS capacitors with and without nitrogen incorporation, where the

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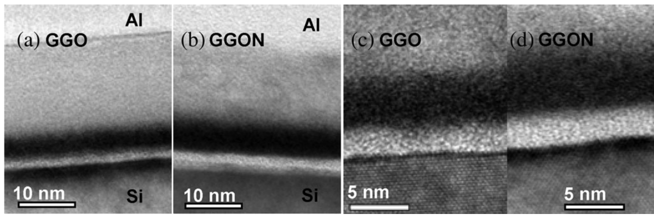
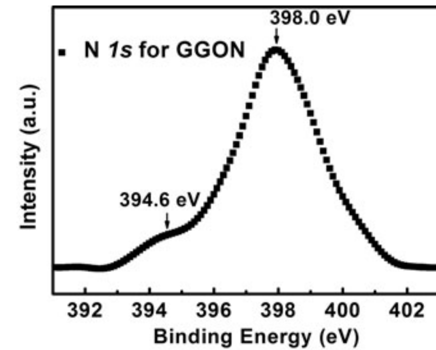


Fig. 1. Cross-sectional TEM images for the MANOS capacitors with Al/Al_2O_3/GGO(N)/SiO_2/Si. (a) Completed GGO sample. (b) Completed GGON sample. (c) High-resolution GGO TEM image compared with (d) high-resolution GGON TEM image.

physical thickness of the charge-trapping film for the GGO and GGON samples is determined to be 5.6 and 6.3 nm, respectively. Also, compared with the GGON sample, there is an obvious interlayer at the GGO/SiO_2 interface for the GGO sample, which can be further confirmed by the XPS analysis. Fig. 2 shows the N 1s, Gd 4d, and O 1s spectra of the stacked GGO/SiO_2 films with and without nitrogen incorporation. The atomic content of nitrogen in the nitrided GGO film is determined to be 10.8% by XPS analysis. A high nitrogen content in CTL is helpful to induce deep traps, thus improving the charge-trapping efficiency [4]. On the other hand, the high nitrogen content in the dielectric film can lead to the formation of metal nitride (e.g., GdN) with conductive property [3], [14], which can enhance the leakage of CTL thus deteriorating the dielectric quality. As shown in Fig. 2(a), the N 1s spectrum mainly includes two peaks located at 394.6 and 398.0 eV, which correspond to metal nitride (GdN) and oxynitride (GdON), respectively [3]. The weak intensity of the former peak (~394.6 eV) indicates only a small amount of metal nitride in the film, which is desirable for the reliability of the memory device. The nitrogen-doping process could be optimized further for better memory performance. For the GGO film, the Gd 4d spectrum shows two peaks located at 143.3 eV (Gd $4d_{5/2}$) and 149.1 eV (Gd $4d_{3/2}$) due to spin-orbit splitting. These two peaks are similar to the Gd component in Gd_2O_3 (Gd $4d_{5/2} \sim 143.1$ eV) [15], and the 0.2 eV shift to higher binding energy should be ascribed to the formation of silicate at the GGO/SiO_2 interface [16]. Compared with the Gd_2O_3 film, the peak of the Gd 4d spectrum (Gd $4d_{5/2} \sim 142.8$ eV) for the nitrided GGO film shifts to lower binding energy by 0.5 eV mainly due to nitrogen incorporation. The formation of silicate interlayer can be further confirmed by the O 1s spectrum as shown in Fig. 2(c), where the O 1s spectrum for the GGO one can be decomposed into three components corresponding to GGO (~531 eV), silicate (~ 532 eV), and SiO_2 (~533 eV), respectively [17]. Note that the area ratio of the O 1s component corresponding to SiO_2 and silicate is 9.6 and 3.7 for the GGON and GGO samples, respectively, demonstrating a smaller fraction of SiO_2 transformed into silicate for the GGON sample than the GGO one. This is consistent with the result from TEM images in Fig. 1, where an obvious interlayer is observed in the GGO sample as compared with an abrupt interface between the CTL and SiO_2 in the GGON one. The smaller silicate content in the GGON sample than the GGO one should be ascribed to suppressed elemental interdiffusion associated with nitrogen



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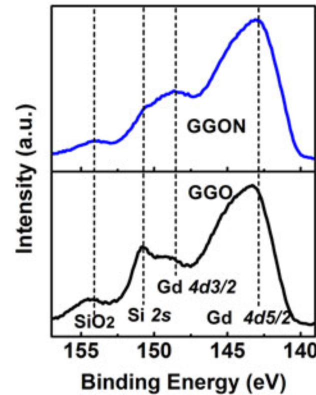

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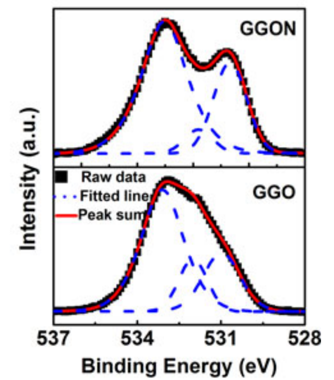


(c)

Fig. 2. XPS spectrum of the stacked GGO/SiO_2 films on the Si substrate with and without nitrogen incorporation. (a) N 1s spectrum. (b) Gd 4d spectrum. (c) O 1s spectrum (square symbol) as well as the curve-fitting lines (dashed line). Each curve-fitting line is assumed to follow the general shape of a Lorentzian–Gaussian function. The solid line (denoted as peak sum) denotes the convolution of each fitted line.

incorporation [1]. This nonstoichiometric interlayer normally has a smaller bandgap as well as more defects than the thermally grown SiO_2 TL. Consequently, an abrupt interface contributes to good data retention properties because the charge-loss process caused by the interlayer (e.g., trap-assisted tunneling) can be suppressed [18].

Fig. 3 shows the P/E transient characteristics of the two MANOS capacitors at various gate voltages V_G. The GGON sample displays higher P/E speeds than the GGO one under the same operating conditions. For the GGO sample, it has a $V_{\rm FB}$ shift ($\Delta V_{\rm FB}$, defined as $\Delta V_{\rm FB} = V_{\rm FB} - V_{FB0}$, where $V_{\rm FB}$ is the flat-band voltage under stress, and $V_{\rm FB0}$ is the flat-band voltage of the fresh device) of 4.8 and 5.9 V at +16 V for 100 μs and 1 s, respectively. For comparison, the GGON one shows a larger $\Delta V_{\rm FB}$ of 6.5 V at +16 V for 100 μs and increases to 10.5 V for 1 s, demonstrating its higher program speed and larger memory window, which are essential prerequisites for multilevel cell operations [9]. The high program performance of the GGON sample should be mainly due to its higher charge-trapping efficiency resulting from its higher deep-level trap density induced by nitrogen incorporation [2]–[6]. In addition, the $V_{\rm FB}$ of the GGO sample tends to saturate with time at V_G from +12 to +16 V, mainly due to the dynamic balance between electron trapping and detrapping. On the contrary, no

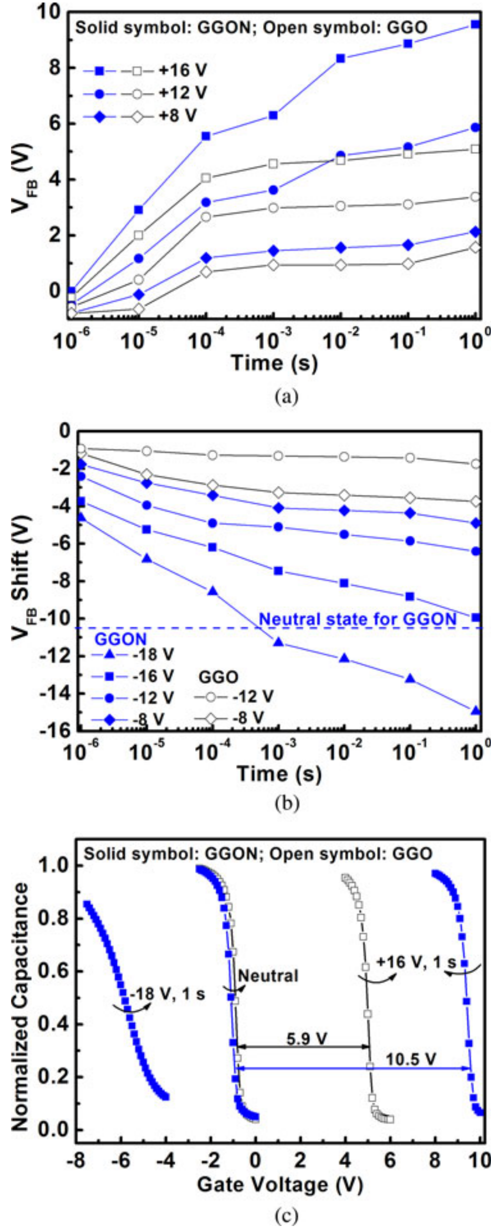


Fig. 3. (a) Program transient characteristics of the MANOS capacitors with and without nitrogen incorporation as a function of pulse width from 1 μs to 1 s at various V_G. (b) Erase transient characteristics of the MANOS capacitors. The samples are programmed at +16 V for 1 s before the erase test. The $V_{\rm FB}$ shift is defined as the difference of $V_{\rm FB}$ under erase stress and the initial $V_{\rm FB}$ programmed at +16 V, 1 s. (c) Normalized *C–V* curves for the MANOS capacitors under the neutral, program, and erase states. $V_{\rm FB}$ was extracted from the experimental *C–V* curve where the capacitance is equal to the calculated flat-band capacitance [20]. The neutral $V_{\rm FB}$ for the GGO and GGON samples is −0.79 and −0.96 V, respectively.

saturation phenomenon is observed for the GGON sample at V_G from +12 to +16 V as shown in Fig. 3(a), further supporting its higher charge-trapping efficiency. Moreover, the GGON sample still shows $\Delta V_{\rm FB}$ of 2.2 V even at a low gate voltage of +8 V for 100 μs, suggesting its potential for low-voltage high-performance memory applications. Compared with our previous sample with $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ structure (denoted as BTO, and BL/CTL/TL = 15.6 nm/10.6 nm/2.0 nm) which was fabricated on the same Si substrate and had the similar equivalent oxide thickness (EOT ∼ 10.8 nm) as the GGON one (EOT ∼ 10.4 nm), the GGON sample displays lower program speed ($\Delta V_{\rm FB}$ = 6.8 V at +12 V, 1 s; 10.5 V at +16, 1 s) than the BTO one ($\Delta V_{\rm FB}$ = 10.6 V at +12 V, 1 s) [19]. This should be ascribed to its lower charge-trapping efficiency resulting from the thinner CTL (∼6.3 nm) in the GGON sample. In addition, the higher program speed for the BTO sample indicates that the electron supply issue and hot electrons induced by high V_G play a minor role here. Otherwise, higher V_G (+16 V) for the GGON sample would lead to higher $\Delta V_{\rm FB}$ than the BTO sample operating at lower V_G (+12 V) because it can induce more electron injection from the substrate. Fig. 3(b) exhibits the erase transient characteristics of the two MANOS capacitors at various V_G, where the devices are prepared at +16 V for 1 s before erasing. For the GGON sample, $\Delta V_{\rm FB}$ increases with V_G and pulse time, which is typical for memory devices. Moreover, a large memory window of 10.0 V can be obtained at ±16 V for 1 s. On the contrary, for the GGO sample, one abnormal phenomenon occurs that its $\Delta V_{\rm FB}$ decreases as V_G increases from −8 V to −12 V, and then breaks down as V_G is up to −16 V with a significant leakage (1.8×10^{-8} and 0.39 A/cm^2 at $V_G = -3$ V before and after the stress. For comparison, 1.5×10^{-8} and 2.9×10^{-8} A/cm^2 at $V_G = -3$ V before and after the stress for the GGON sample). Also, the higher leakage of the GGO sample indicates its lower charge-trapping efficiency. It is also observed that $V_{\rm FB}$ erased at −18 V shifts more negatively than that of the neutral state, indicating net holes stored in the CTL. Because of the larger barrier height at the SiO_2/Si interface for hole tunneling (∼4.5 eV) than that for electron tunneling (∼3.2 eV), hole injection is usually less efficient than electrons [1], [5]. The thin tunneling oxide (∼2 nm) here is helpful for enhancing the hole injection. Therefore, both electron detrapping and hole trapping can happen under the erase transients. As shown later in Fig. 5, the GGO sample displays much worse data retention than the GGON one, suggesting that electron detrapping is much easier for the GGO sample. Therefore, the lower erase speed of the GGO sample should be mainly due to its lower hole-trapping efficiency. Due to the poor charge-trapping efficiency of the GGO sample, the increase of V_G will lead to a higher electrical field E across the dielectric films, thus enhancing holes tunneling from the Si substrate into the electrode rather than being trapped in the CTL film. This should be the reason that a smaller $\Delta V_{\rm FB}$ is obtained at $V_G = -12$ V than at $V_G = -8$ V for the GGO sample. The higher robustness for the GGON sample than the GGO one should be ascribed to its suppressed formation of the defective interlayer at the CTL/SiO_2 interface by nitrogen passivation [1]. It is noted that the GGON sample with a thinner interlayer at the CTL/SiO_2 interface shows higher trap density than the GGO one, indicating that the traps are mainly distributed in the bulk of the charge-trapping film rather than the interlayer. This is beneficial for the retention characteristics by avoiding electrons tunneling back to the substrate. The corresponding $C - V$ (gate capacitance versus gate voltage) curves under neutral, programmed, and erased states are shown in Fig. 3(c), where the GGON sample achieves a higher $V_{\rm FB}$ shift (10.5 V) than the GGO one (5.9 V) under the same

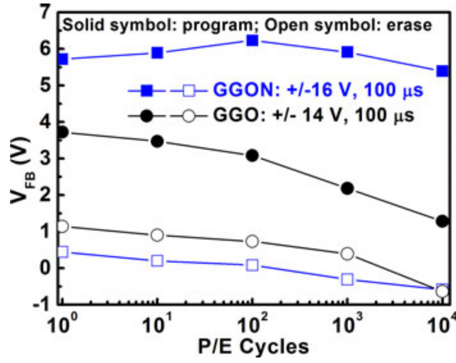
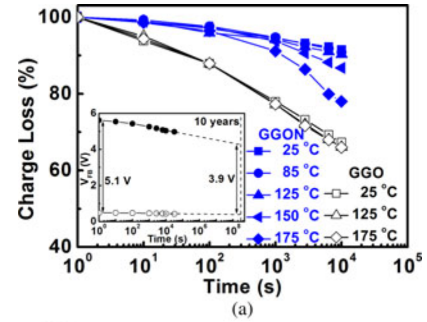


Fig. 4. Endurance characteristics of the GGON and GGO samples.

operating condition (+16 V, 1 s). Moreover, the GGO sample breaks down at $V_G = -16$ V. For comparison, the GGON sample can endure the stress up to -18 V, demonstrating its higher robustness against the stress. It is also observed that the *C–V* curve of the GGON sample at $V_G = -18$ V presents more severe stretch-out characteristics than the one under the neutral state, indicating extra interface states induced by the high stress.

Fig. 4 exhibits the endurance characteristic of the GGON sample under a $\pm$16-V 100-μs P/E stress. The P/E memory window before and after 10^4-cycle P/E stressing is 5.3 and 6.0 V, respectively, and no degradation of the P/E window is observed during the repeated stressing. On the contrary, the endurance data for the GGO sample under the same P/E stress cannot be obtained because breakdown happens at -16 V. Moreover, for the GGO sample under a lower P/E stress ($\pm$14 V, 100 μs), the P/E window degrades from 2.6 to 2.0 V after a 10^4-cycle P/E stressing, further demonstrating its worse endurance property than the GGON one. It is found that both P/E $V_{\rm FB}$ levels shift downward with cycling for the GGO sample, which causes the degradation of its memory window under the repeated P/E stress. This should be due to electron detrapping via the stress-induced defects [21]. Therefore, the better endurance property of the GGON sample should be due to its more deep traps because electrons located in deep traps are more difficult to escape from the CTL. In addition, the suppressed formation of the defective interlayer at the CTL/SiO_2 interface by nitrogen passivation also contributes to the enhanced hardness of the GGON sample against the stress.

Fig. 5(a) displays the retention characteristics of the MANOS capacitors with and without nitrogen incorporation, where the GGON sample shows better data retention than the GGO one over a wide temperature range from 25 to 175 °C (e.g., charge loss of 9.71% versus 36.9% after 10^4 s at 125 °C). For fair comparison, both samples are prepared with the same initial $\Delta V_{\rm FB}$ ($\sim$4.1 V). For the GGON sample, it shows a similar data retention with a little charge loss from 25 to 125 °C, and then obvious degradation begins as the baking temperature T is beyond 150 °C. For comparison, the retention data of the GGO sample coincides well, but with severe charge loss for the whole testing temperature range from 25 to 175 °C. The inset of Fig. 5(a) shows the data retention of the GGON sample prepared at $\pm$16 V for 100 μs at 85 °C, from which the P/E window after ten years



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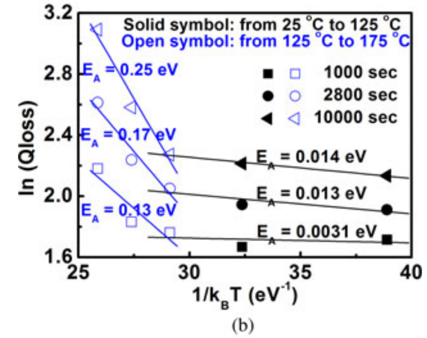

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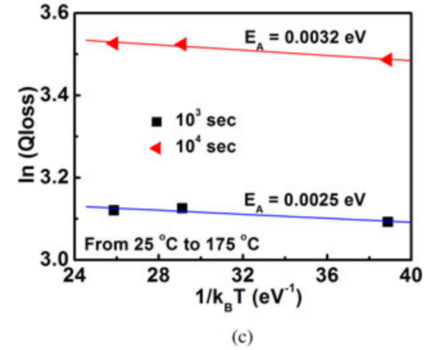

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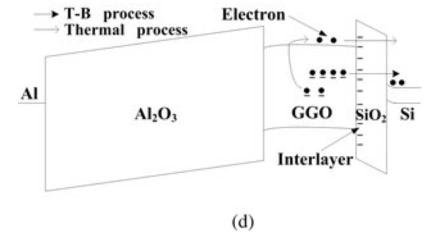

(d)

Fig. 5. (a) Retention characteristics of the MANOS capacitors with and without nitrogen incorporation with an initial $V_{\rm FB}$ shift of 4.1 V. The inset shows the data retention of the GGON sample programmed/erased at $\pm$16 V for 100 μs measured at 85 °C. (b) Arrhenius plot of the charge-loss characteristics for the GGON sample and (c) for the GGO sample, where k_B is the Boltzmann constant and T is the absolute temperature. (d) Energy-band diagram under the retention mode with an electric field of +4 MV/cm across the tunneling oxide. The interlayer acting as a medium to accelerate the charge loss is represented by traps at the GGO/SiO_2 interface.

is evaluated by extrapolation to be 3.9 V, corresponding to a charge loss of 23.5%. On the contrary, the GGO sample cannot achieve similar window as the GGON one (5.1 V) under high temperature even when high V_G with a long pulse width is used, further supporting its poor charge-trapping ability. To gain more insight on the charge-loss mechanism, the activation energy E_A extracted from the Arrhenius plot of the charge-loss rate [$Q_{\rm loss}$,

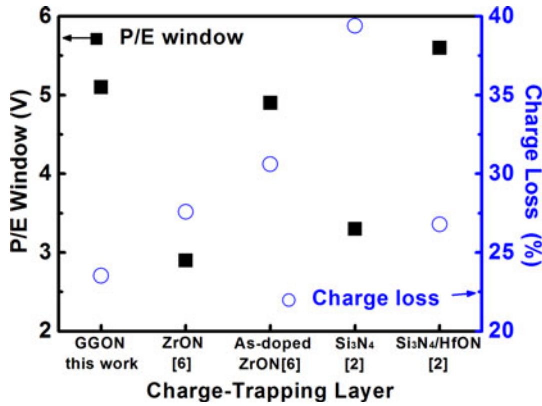

Fig. 6. Performance comparison of the GGON film with other typical dielectric films as CTL. All the samples are operated at ±16 V, 100 μs and measured at 85 °C. The charge loss is defined as $(W_0 - W_1)/W_0 \times 100\%$, where W_0 is the initial P/E memory window, and W_1 is the P/E window after ten years.

from Fig. 4(a)] is also shown in Fig. 5(b) [8], where the GGON sample exhibits two distinctive E_A for the low-T range from 25 to 125 °C (0.0031–0.014 eV) and for the high-T range from 125 to 175 °C (0.13–0.25 eV), implying different charge-loss mechanisms in the low- and high-temperature ranges. On the contrary, the GGO sample shows only one single E_A (∼0.003 eV) for the whole temperature range from 25 to 175 °C as shown in Fig. 5(c). The smaller E_A (0.0031 eV–0.014 eV) suggests that the trap-to-band (T–B) tunneling mechanism dominates the charge loss, which is a nonthermal process and is insensitive to temperature, while the larger E_A (0.13–0.25 eV) suggests that the charge-loss mechanism is related to a thermally activated process in the high-T range, which can be further illustrated by the energy-band diagram in Fig. 5(d) [22], [23]. Consequently, the severe charge loss caused by the T–B tunneling in the GGO sample should be due to more shallow traps in the GGO film as well as the thinner tunneling oxide resulting from the interfacial reaction at the GGO/SiO_2 interface, because the tunneling probability decreases with the tunneling path and barrier height. In addition, the nonstoichiometric interlayer can also act as a medium to facilitate electrons escaping from the CTL to the substrate [18]. It is also found that the E_A closely depends on $Q_{\rm loss}$. For the GGON sample, E_A with $Q_{\rm loss}$ extracted at 10^3, 2800, and 10^4 s increases from 0.0031 to 0.014 eV in the low-T range, and from 0.13 to 0.25 eV in the high-T range, respectively. It is reported that electrons located in shallow traps are easier to escape into the substrate, which is responsible for the retention degradation in the early stage [24]. Therefore, thermal energy as the driving force to accelerate charge loss has little impact on the retention degradation caused by shallow traps, thus leading to a smaller E_A with $Q_{\rm loss}$ extracted at earlier stage. For the GGO sample, E_A with $Q_{\rm loss}$ extracted at 10^3 and 10^4 s is 0.0025 and 0.0032 eV, respectively. The smaller E_A difference for the GGO sample than the GGON one indicates that shallow traps are dominant in the GGO film.

Fig. 6 shows the performance comparison of the GGON film in this study with other typical dielectrics acting as CTL. All the samples are programmed/erased at ±16 V for 100 μs and measured at 85 °C. Compared with other materials, the GGON sample shows good performance in terms of its large P/E window and excellent data retention, where its charge loss of 23.5% is the smallest among the devices in Fig. 6, even though the tunneling oxide is only 2 nm thick.

IV. Conclusion

In summary, the charge-trapping characteristics of the $Ga_2O_3(Gd_2O_3)$ film with and without nitrogen incorporation are investigated based on MANOS-type capacitors. The MANOS capacitor with nitrided GGO as CTL shows better electrical characteristics in terms of larger memory window, higher P/E speeds, and better data retention than the one without nitridation. Therefore, a $Ga_2O_3(Gd_2O_3)$ film with nitrogen incorporation is a promising candidate as the CTL for high-performance nonvolatile memory applications.

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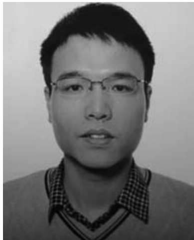

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