A Practical Regularization Technique for Modified Nodal Analysis in Large-Scale Time-Domain Circuit Simulation

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***Abstract*—Fast full-chip time-domain simulation calls for advanced numerical integration techniques with capability to handle the systems with (tens of) millions of variables resulting from the modified nodal analysis (MNA). General MNA formulation, however, leads to a differential algebraic equation (DAE) system with singular coefficient matrix, for which most of explicit methods, which usually offer better scalability than implicit methods, are not readily available. In this paper, we develop a practical two-stage strategy to remove the singularity in MNA equations of large-scale circuit networks. A topological index reduction is first applied to reduce the DAE index of the MNA equation to one. The index-1 system is then fed into a systematic process to eliminate excess variables in one run, which leads to a nonsingular system. The whole regularization process is devised with emphasis on exact equivalence, low complexity, and sparsity preservation, and is thus well suited to handle extremely large circuits.**

***Index Terms*—Explicit method, graph theory, index reduction, modified nodal analysis (MNA), singular matrix.**

I. Introduction

THE EVER-INCREASING integration density of modern integrated circuit (IC) designs has made the runtime of SPICE-like simulation [1] a bottleneck in the IC design flow. A circuitry modeled by modified nodal analysis (MNA) with millions of variables usually takes days, even weeks, to complete a time-domain simulation. The major reason is that mainstream circuit simulators adopt implicit numerical integration methods, e.g., backward Euler, for the sake of stability. The scalability, however, is to some extent sacrificed since solving large systems of differential equations is costly and difficult for parallelization.

The explicit methods (e.g., forward Euler), on the other hand, eliminate the need of actually solving a large linear system, and thus provide a much better scalability. Despite the well-known stability problem, the explicit methods have recently become a revived research area owing to the potential to respond to the demand of simulating million-scale problems. Previous efforts include adaptive time step for better stability [2], telescopic projective integration [3], and recent work on matrix exponential method, which allows the usage of even larger time step than implicit methods [4], [5].

One hurdle of explicit methods, on top of the stability issue (and kind of "overlooked" in the past), is the singular matrix problem associated with the MNA formulation. Recall that in MNA a circuit network is described by a system of differential algebraic equations (DAEs)

$$\mathbf{C}\dot{\mathbf{x}}(t) = -\mathbf{G}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{1}$$

where matrix $\mathbf{C}$ collects the effects of capacitances and inductances, matrix $\mathbf{G}$ collects the effects of resistance and the incidence matrix for current variable vector, vector $\mathbf{x}(t)$ consists of all node voltages and some branch currents, and vector $\mathbf{u}(t)$ denotes the independent sources.

Before most explicit methods can actually get started, (1) should preferably be convertible to a system of ordinary differential equations (ODEs) (for which these methods were developed in the first place)

$$\dot{\mathbf{x}}(t) = -\mathbf{C}^{-1}\mathbf{G}\mathbf{x}(t) + \mathbf{C}^{-1}\mathbf{B}\mathbf{u}(t) \tag{2}$$

which naturally requires the coefficient matrix $\mathbf{C}$ to be nonsingular. Implicit methods, on the other hand, relax the restriction on matrix invertibility. In backward Euler, for instance, only the matrix $\mathbf{C}/h + \mathbf{G}$ needs to be nonsingular, where h is the time step size.

The most common causes of singular $\mathbf{C}$ in MNA formulation are the empty rows corresponding to the nodes in the absence of capacitances, and the currents of independent and controlled voltage sources of which no time differential terms are present in (1). On top of this "explicit" singularity, it is often the case that some "hidden" dependence among MNA variables exists in a given circuit, rendering the $\mathbf{C}$ matrix singular or ill-conditioned even none of its rows are empty [6].

In this paper, we develop an effective method to regularize the DAE (1), i.e., to derive an equivalent equation with a nonsingular $\mathbf{C}$. In control theory, this amounts to converting the descriptor representation [7] of a circuit to an explicit state-space representation. To handle the large sparse matrices from real IC designs, our technique consists of two stages. By analyzing the topology with graph theory, an index reduction technique is first applied to reduce the DAE index of the MNA

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equation; then a systematic elimination is employed to remove the dependence among variables in one run ending up with a nonsingular system.

Our motivation is to offer a practical and cost-effective regularization solution for the majority of the real-world problems, without appealing to complete but complicated mathematics. In other words, we recognize the fact that most problems we have to deal with do not require so much generality, and instead can be resolved by less rigorous approaches in a more efficient manner. The rationale behind our method is to avoid (to most extent) certain matrix operations, such as (iterative) LU decompositions and matrix-matrix multiplications, which tend to damage the sparsity of MNA matrices. This is crucial for any practical techniques in large-scale circuit simulation considering the giant problem sizes. We achieve this goal by preprocessing the DAE index and the floating capacitors before systematic elimination, and using topology analysis to guide the preprocessing so that it affects only a small portion of the matrices. The proposed method also sheds some lights on relevant problems in other areas such as model order reduction [8].

II. Systematic Elimination

One widely used regularization method in previous work (e.g. [9]) is to reorder all nonzero entries of $\mathbf{C}$ to the upper left corner and partition (1) into two sets of equations

$$\begin{bmatrix} \mathbf{C}_{11} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \end{bmatrix} = - \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12} \\ \mathbf{G}_{21} & \mathbf{G}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \end{bmatrix} + \begin{bmatrix} \mathbf{B}_1 \\ \mathbf{B}_2 \end{bmatrix} \mathbf{u}. \quad (3)$$

Provided the submatrix $\mathbf{G}_{22}$ is invertible, (3) can be converted to an equation of $\mathbf{x}_1$ by the substitution of $\mathbf{x}_2$. Once $\mathbf{C}_{11}$ is also nonsingular, the whole system becomes regular. In spite of the simplicity, the applicability of this approach is rather limited. It relies upon the invertibility of both $\mathbf{C}_{11}$ and $\mathbf{G}_{22}$, which is generally not guaranteed in MNA formulation.

Chua and Lin in their classic book [6] provided a generic approach to obtain the state-space model for a circuit network with an arbitrarily high DAE index. The triplet $[\mathbf{C}, \mathbf{G}, \mathbf{B}]$ is reduced to the row echelon form recursively, and during each reduction some excess variables are eliminated. A method based on similar idea but specific to MNA formulation was developed by Natarajan [10], in which the nonzero entries are concentrated on the entire upper part of $\mathbf{C}$ (instead of only the top left corner) by the row echelon reduction

$$\begin{bmatrix} \mathbf{C}_{11} & \mathbf{C}_{12} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \end{bmatrix} = - \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12} \\ \mathbf{G}_{21} & \mathbf{G}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \end{bmatrix} + \begin{bmatrix} \mathbf{B}_{01} \\ \mathbf{B}_{02} \end{bmatrix} \mathbf{u}. \quad (4)$$

After (4) is obtained, another row echelon transform is applied to the submatrix of $[\mathbf{G}_{21}\ \mathbf{G}_{22}]$ from the bottom row, which is essentially a UL decomposition [11]. The columns of $\mathbf{G}$ and $\mathbf{C}$ are rearranged to ensure $\mathbf{G}_{22}$ is lower triangular. Finally, block Gaussian elimination (GE) is used to obtain a reduced system of equations

$$\mathbf{C}_r \dot{\mathbf{x}}_1 = -\mathbf{G}_r \mathbf{x}_1 + \mathbf{B}_{0r} \mathbf{u} + \mathbf{B}_{1r} \dot{\mathbf{u}} \quad (5)$$

where

$$\mathbf{C}_r = \mathbf{C}_{11} - \mathbf{C}_{12}\mathbf{G}_{22}^{-1}\mathbf{G}_{21} \quad \mathbf{G}_r = \mathbf{G}_{11} - \mathbf{G}_{12}\mathbf{G}_{22}^{-1}\mathbf{G}_{21} \quad (6a)$$

$$\mathbf{B}_{0r} = \mathbf{B}_{01} - \mathbf{G}_{12}\mathbf{G}_{22}^{-1}\mathbf{B}_{02} \quad \mathbf{B}_{1r} = -\mathbf{C}_{12}\mathbf{G}_{22}^{-1}\mathbf{B}_{02} \quad (6b)$$

$$\mathbf{x}_2 = -\mathbf{G}_{22}^{-1}\left(\mathbf{G}_{21}\mathbf{x}_1 - \mathbf{B}_{02}\mathbf{u}\right). \quad (6c)$$

Note that the derivative term of source $\mathbf{u}$ in (5) arises from the cross-coupling term $\mathbf{C}_{12}\dot{\mathbf{x}}_2$. The substitution of the latter differentiates the lower set of equations in (4), leading to the differentiation of the source term. Provided $\mathbf{C}_r$ is invertible, a variable transform of $\mathbf{x}_r = \mathbf{x}_1 - \mathbf{C}_r^{-1}\mathbf{B}_{1r}\mathbf{u}$ is applied to absorb the derivative of $\mathbf{u}$, yielding a regular ODE as in (2)

$$\mathbf{C}_r \dot{\mathbf{x}}_r = -\mathbf{G}_r \mathbf{x}_r + \mathbf{B}_r \mathbf{u} \quad (7)$$

with $\mathbf{B}_r = \mathbf{B}_{0r} - \mathbf{G}_r \mathbf{C}_r^{-1} \mathbf{B}_{1r}$.

The systematic elimination described in (4)–(7) is a component of our regularization framework. The direct application of this processs, however, has two bottlenecks: 1) reducing $\mathbf{C}$ to the row echelon form is costly (LU decomposition with row pivoting), and will introduce fill-ins into $\mathbf{G}$ during concurrent elementary operations (matrix-matrix multiplications); and 2) the matrix $\mathbf{C}_r$ can remain singular after the first round of regularization, and if so, the process has to be repeated to eliminate more variables from $\mathbf{x}_1$ until a nonsingular $\mathbf{C}_r$ is achieved. This situation arises when the system of DAE has an index higher than one, i.e., the output equation contains derivatives of the source terms, which can appear in the systematic elimination only after the second cycle [10]. Such iterative check and elimination of singularity is unfavorable for computational efficiency and sparsity preservation.

Note that the DAE index of a circuit can be arbitrarily high depending on its topology, but is usually no higher than 2 in practice. Index-3 (or higher) circuits are generally not suitable for computer simulation [6]. In this paper, we restrict our focus to index-2 circuits that represent the majority of the designs of practical interest. These index-2 systems in most cases result from the presence of CV-loops and LI-cutsets in the topology [12]. Hence, the key to address the second bottleneck lies in reducing an index-2 circuit to its index-1 equivalent *prior to* the elimination process of (4) by breaking all CV-loops and LI-cutsets in the topology. The index-1 system is then fed into (4) which is guaranteed to stop after the first iteration.

III. Topological Index Reduction

Generic index reduction of DAEs can be realized by the spectral projector technique [13]. Provided that the MNA matrices are known, the spectral projector can be constructed analytically through a lengthy matrix computation [14]. However, this construction process does not preserve sparsity, i.e., the projected matrices tend to be dense. Alternatively, an element-based topological index reduction method is proposed in [15] and [16] based on the concept of minimal extension. The virtue is that no algebraic (matrix) transformation is required; only the netlist needs to be augmented. Nevertheless,

$$\left[\begin{array}{cc|c} C_{kk} & C_{kl} & 0 \\ C_{lk} & C_{ll} & 0 \\ \hline 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \hline \dot{i}_v \end{array}\right] = - \left[\begin{array}{cc|c} G_{kk} & G_{kl} & 1 \\ G_{lk} & G_{ll} & -1 \\ \hline -1 & 1 & 0 \end{array}\right] \left[\begin{array}{c} v_k \\ v_l \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} 0 \\ 0 \\ \hline 1 \end{array}\right] [Vs] \tag{8a}$$

$$\left[\begin{array}{cc|c} C_{kk} & C_{kl} & 0 \\ C_{kk}+C_{lk} & C_{kl}+C_{ll} & 0 \\ \hline 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \hline \dot{i}_v \end{array}\right] = - \left[\begin{array}{cc|c} G_{kk} & G_{kl} & 1 \\ G_{kk}+G_{lk} & G_{kl}+G_{ll} & 0 \\ \hline -1 & 1 & 0 \end{array}\right] \left[\begin{array}{c} v_k \\ v_l \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} 0 \\ 0 \\ \hline 1 \end{array}\right] [Vs] \tag{8b}$$

$$\left[\begin{array}{cc|c} C_{kk} & C_{kl} & 0 \\ C_{kk}+C_{lk} & C_{kl}+C_{ll} & 0 \\ \hline 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \hline \dot{i}_v \end{array}\right] = - \left[\begin{array}{cc|c} G_{kk} & G_{kl} & 1 \\ 0 & G_{kk}+G_{lk}+G_{kl}+G_{ll} & 0 \\ \hline -1 & 1 & 0 \end{array}\right] \left[\begin{array}{c} v_k \\ v_l \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} 0 \\ G_{kk}+G_{lk} \\ \hline 1 \end{array}\right] [Vs] \tag{8c}$$

$$\left[\begin{array}{cc|c} C_{kk} & C_{kl} & 0 \\ C_{kk}+C_{lk} & C_{kl}+C_{ll} & 0 \\ \hline -1 & 1 & 0 \end{array}\right] \left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \hline \dot{i}_v \end{array}\right] = - \left[\begin{array}{cc|c} G_{kk} & G_{kl} & 1 \\ 0 & G_{kk}+G_{lk}+G_{kl}+G_{ll} & 0 \\ \hline 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} v_k \\ v_l \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} 0 \\ G_{kk}+G_{lk} \\ \hline 0 \end{array}\right] [Vs] + \left[\begin{array}{c} 0 \\ 0 \\ \hline 1 \end{array}\right] \left[\dot{V}s\right] \tag{8d}$$

$$\left[\begin{array}{cc|c} C_{kk} & C_{kl} & 0 \\ 0 \quad C_{kk}+C_{lk}+C_{kl}+C_{ll} & & 0 \\ \hline -1 & 1 & 0 \end{array}\right] \left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \hline \dot{i}_v \end{array}\right] = - \left[\begin{array}{cc|c} G_{kk} & G_{kl} & 1 \\ 0 & G_{kk}+G_{lk}+G_{kl}+G_{ll} & 0 \\ \hline 0 & 0 & 0 \end{array}\right] \left[\begin{array}{c} v_k \\ v_l \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} 0 \\ G_{kk}+G_{lk} \\ \hline 0 \end{array}\right] [Vs] + \left[\begin{array}{c} 0 \\ C_{kk}+C_{lk} \\ \hline 1 \end{array}\right] \left[\dot{V}s\right] \tag{8e}$$

$$[C_{kk}+C_{lk}+C_{kl}+C_{ll}]\,[\dot{v}_l] = -\,[G_{kk}+G_{lk}+G_{kl}+G_{ll}]\,[v_l] + [G_{kk}+G_{lk}]\,[Vs] + [C_{kk}+C_{lk}]\left[\dot{V}s\right] \tag{8f}$$

this method adds two unknowns into the system for every capacitor to be replaced. For networks with a large number of capacitor loops, e.g., with many capacitors mounted in parallel, this will increase the problem size considerably [17].

The index reduction method we develop here combines topology analysis and algebraic transformation in such a way that the algebraic transformation (mostly elementary row operations) is only applied to a small portion of the original system selected by the topology analysis. Modifications are made on the matrix equation instead of the netlist for better adaptability. One key observation is that a loop with capacitors only does not lead to an index-2 system in MNA; only when voltage source(s) come into the loop will the circuit become index-2 [18]. This is different from LI-cutsets where inductors alone can form a cutset leading to an index-2 system (because inductor currents are state variables in MNA).

A. Elimination of Voltage Sources

The first step of our topological index reduction is to eliminate all voltage sources. One (nondatum) node voltage and the branch current are eliminated for each (independent and controlled) voltage source regardless of whether it is part of a CV-loop. The intention of this elimination to break all *potential* CV-loops *in one shot*, which takes advantage of the (usually) small number of voltage sources in a given circuit. The MNA stamp of an independent voltage source is shown in (8a) and the corresponding elimination procedure is described in (8b)–(8f) (suppose v_k and i_v are eliminated). In (8b), the KCL of node k is applied to eliminate i_v at node l. In (8c), v_k is eliminated using the branch constitutive equation (BCE) of the independent voltage source. We enforce the implicit constraint in (8d) by differentiating the BCE, after which the derivative of Vs appears in the RHS. With the implicit constraint, $\dot{v}_k$ is eliminated in (8e). After deleting the rows and columns of v_k and i_v, we obtain the reduced equation (8f). The eliminations of the two types of controlled voltage sources, VCVS and CCVS, are described in the Appendix.

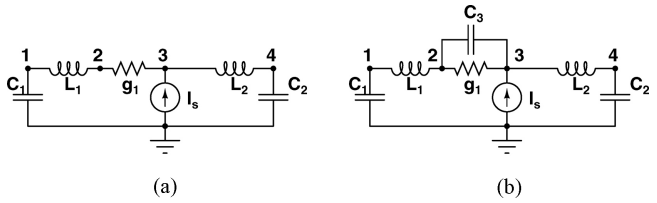

Fig. 1. LI-cutset examples. (a) Simple example of LI-cutset. (b) All terminals of inductors are connected to capacitors.

Note that when a voltage source is connected to a large number of elements at the same node, the elimination of this "supernode" has a chance to generate some rows/columns with a large number of nonzeros, with the total amount of nonzeros staying roughly the same or even becoming smaller. The dense rows/columns may affect the performance of sparse solvers in finding a good reordering for the sparse matrix. Hence, it is advisable to monitor the sparsity change in rows/columns involved in the elimination process during the implementation, and issue a warning if highly dense rows/columns are generated.

B. Breaking of LI-Cutsets

The second step is to break all LI-cutsets. The procedure is similar to the elimination of voltage sources, except that one inductor (not current source) per LI-cutset must be selected for elimination. A proper selection of the target inductors

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & 0 & & & & \\ & & 0 & & & \\ & & & C_2 & & \\ \hline & & & & L_1 & K \\ & & & & K & L_2 \end{array}\right]\left[\begin{array}{c}\dot{v}_1\\ \dot{v}_2\\ \dot{v}_3\\ \dot{v}_4\\ \hline \dot{i}_{L_1}\\ \dot{i}_{L_2}\end{array}\right] = -\left[\begin{array}{cccc|cc} & & g_1 & -g_1 & 1 & \\ & & -g_1 & g_1 & -1 & 1 \\ \hline -1 & 1 & & & & \\ & & -1 & 1 & & \end{array}\right]\left[\begin{array}{c}v_1\\ v_2\\ v_3\\ v_4\\ \hline i_{L_1}\\ i_{L_2}\end{array}\right] + \left[\begin{array}{c}1\\ \\ \hline \\ \\ \hline \\ \end{array}\right][Is] + \left[\begin{array}{c}\\ \\ \hline -\\ \\ \hline \\ \end{array}\right]\left[\dot{I}s\right] \tag{9a}$$

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & 0 & & & & \\ & & 0 & & & \\ & & & C_2 & & \\ \hline & & & & L_1 & K \\ & & & & K & L_2 \end{array}\right]\left[\begin{array}{c}\dot{v}_1\\ \dot{v}_2\\ \dot{v}_3\\ \dot{v}_4\\ \hline \dot{i}_{L_1}\\ \dot{i}_{L_2}\end{array}\right] = -\left[\begin{array}{cccc|cc} & & g_1 & -g_1 & 0 & \mathbf{1} \\ & & -g_1 & g_1 & 0 & \mathbf{-1} \\ & & & & 1 & -1 \\ \hline -1 & 1 & & & & \\ & & -1 & 1 & & \end{array}\right]\left[\begin{array}{c}v_1\\ v_2\\ v_3\\ v_4\\ \hline i_{L_1}\\ i_{L_2}\end{array}\right] + \left[\begin{array}{c}\mathbf{1}\\ \mathbf{-1}\\ 1\\ \\ \hline \\ \end{array}\right][Is] + \left[\begin{array}{c}\\ \\ \hline -\\ \\ \hline \\ \end{array}\right]\left[\dot{I}s\right] \tag{9b}$$

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & 0 & & & & \\ & & 0 & & & \\ & & & C_2 & & \\ \hline & & & & 0 & \mathbf{L_1+K} \\ & & & & 0 & \mathbf{L_2+K} \end{array}\right]\left[\begin{array}{c}\dot{v}_1\\ \dot{v}_2\\ \dot{v}_3\\ \dot{v}_4\\ \hline \dot{i}_{L_1}\\ \dot{i}_{L_2}\end{array}\right] = -\left[\begin{array}{cccc|cc} & & g_1 & -g_1 & 0 & 1 \\ & & -g_1 & g_1 & 0 & -1 \\ & & & & 1 & -1 \\ \hline -1 & 1 & & & & \\ & & -1 & 1 & & \end{array}\right]\left[\begin{array}{c}v_1\\ v_2\\ v_3\\ v_4\\ \hline i_{L_1}\\ i_{L_2}\end{array}\right] + \left[\begin{array}{c}1\\ -1\\ 1\\ \\ \hline \\ \end{array}\right][Is] + \left[\begin{array}{c}\\ \\ \\ \\ \hline \mathbf{L_1}\\ \mathbf{K}\end{array}\right]\left[\dot{I}s\right] \tag{9c}$$

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & 0 & & & & \\ & & 0 & & & \\ & & & C_2 & & \\ \hline & & & & 0 & \mathbf{-g_1(L_1+K)} \\ & & & & 0 & \mathbf{g_1(L_1+K)} \\ \hline & & & & 0 & L_1+K \\ & & & & 0 & L_2+K \end{array}\right]\left[\begin{array}{c}\dot{v}_1\\ \dot{v}_2\\ \dot{v}_3\\ \dot{v}_4\\ \hline \dot{i}_{L_1}\\ \dot{i}_{L_2}\end{array}\right] = -\left[\begin{array}{cccc|cc} & \mathbf{g_1} & -g_1 & & 0 & 1 \\ & \mathbf{-g_1} & g_1 & & 0 & -1 \\ & & & & 1 & -1 \\ \hline -1 & 1 & & & & \\ & & -1 & 1 & & \end{array}\right]\left[\begin{array}{c}v_1\\ v_2\\ v_3\\ v_4\\ \hline i_{L_1}\\ i_{L_2}\end{array}\right] + \left[\begin{array}{c}1\\ -1\\ 1\\ \\ \hline \\ \end{array}\right][Is] + \left[\begin{array}{c}\mathbf{-L_1g_1}\\ \mathbf{L_1g_1}\\ \\ \hline L_1\\ K\end{array}\right]\left[\dot{I}s\right] \tag{9d}$$

$$\left[\begin{array}{ccc|c} C_1 & & & g_1(L_1+K) \\ & 0 & & \\ & & C_2 & \\ \hline & & & L_2+K \end{array}\right]\left[\begin{array}{c}\dot{v}_1\\ \dot{v}_3\\ \dot{v}_4\\ \hline \dot{i}_{L_2}\end{array}\right] = -\left[\begin{array}{ccc|c} -g_1 & g_1 & & 1 \\ & & & 1 \\ & & & -1 \\ \hline & -1 & 1 & \end{array}\right]\left[\begin{array}{c}v_1\\ v_3\\ v_4\\ \hline i_{L_2}\end{array}\right] + \left[\begin{array}{c}1\\ 1\\ \\ \hline \\ \end{array}\right][Is] + \left[\begin{array}{c}L_1g_1\\ \\ \hline K\end{array}\right]\left[\dot{I}s\right] \tag{9e}$$

$$\left[\begin{array}{ccc|c} C_1 & & & \\ & C_2 & & \\ \hline & & & \mathbf{L_1+L_2+2K} \end{array}\right]\left[\begin{array}{c}\dot{v}_1\\ \dot{v}_4\\ \hline \dot{i}_{L_2}\end{array}\right] = -\left[\begin{array}{ccc|c} & & & 1 \\ & & & -1 \\ \hline \mathbf{-1} & 1 & & \frac{1}{\mathbf{g_1}} \end{array}\right]\left[\begin{array}{c}v_1\\ v_4\\ \hline i_{L_2}\end{array}\right] + \left[\begin{array}{c}1\\ \\ \hline \frac{1}{\mathbf{g_1}}\end{array}\right][Is] + \left[\begin{array}{c}0\\ 0\\ \hline \mathbf{L_1+K}\end{array}\right]\left[\dot{I}s\right] \tag{9f}$$

relies on deriving a reduced graph from the original network with only inductive branches and current sources. Then the inductors belonging to the tree branches of the reduced graph are selected [16]. For each selected inductor, the selection of nodes for elimination depends on the capacitors attached to the terminals of the inductor. Generally, at least one terminal of the inductor has no attached capacitors, and this node will be the one to eliminate. An example of LI-cutset is shown in Fig. 1(a) and the corresponding procedure to eliminate i_{L1} and v_2 (the node without capacitors) is shown in (9). A mutual inductance K between L_1 and L_2 is also included. The altered entries at each step are highlighted in bold.

In (9b), i_{L_1} is eliminated from $\mathbf{G}$ by the current law of the LI-cutset (10a). The differential current $\dot{i}_{L_1}$ is eliminated from $\mathbf{C}$ in (9c) using the differential current law (10b) of the LI-cutset

$$i_{L_1} - i_{L_2} + Is = 0 \tag{10a}$$

$$\dot{i}_{L_1} - \dot{i}_{L_2} + \dot{I}s = 0. \tag{10b}$$

In (9d), the dependence of v_2 in the second and third rows of $\mathbf{G}$ is eliminated by the BCE of L_1 (the fifth row). By removing the rows and columns corresponding to v_2 and i_{L_1} we get (9e). Notice that the second column of $\mathbf{C}$ is empty, which indicates the KCL at node 3 is an algebraic constraint despite the nonempty row in $\mathbf{C}$. In this case, one could either eliminate $g_1(L_1 + K)$ by the fourth row of $\mathbf{C}$ to illuminate the algebraic nature of the KCL, or simply eliminate v_3 by algebraic substitution. Equation (9f) is resulted from the elimination of v_3.

One exception arises when all terminals of the selected inductor are connected to capacitors. An example of this exception is shown in Fig. 1(b), where a parallel capacitor C_3 is added. In such a case, the $\mathbf{C}$ matrix in (9c) becomes

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & \mathbf{C_3} & \mathbf{-C_3} & & & \\ & \mathbf{-C_3} & \mathbf{C_3} & & & \\ & & & C_2 & & \\ \hline & & & & 0 & L_1+K \\ & & & & 0 & L_2+K \end{array}\right]. \tag{11}$$

Due to the dependence of $\dot{v}_2$ in $\mathbf{C}$, we can no longer use the BCE of L_1 to eliminate v_2 from the unknown list as done in (9d). However, one can prove the following lemma related to the concept of floating capacitors, which is defined as a

Algorithm 1: Breaking procedure of LI-cutset

Input: matrices $\mathbf{C}$, $\mathbf{G}$, $\mathbf{B}_0$, $\mathbf{B}_1$
Identify all LI-cutsets via topology analysis;
Select one inductor L_e from each cutset for elimination;
Eliminate i_{L_e} and $\dot{i}_{L_e}$ using the algebraic and differential KCL of the cutset;
if *one terminal n_e of L_e has no capacitor* **then**
  Eliminate v_{n_e} using the BCE of L_e;
else
  Invoke floating capacitor routine to eliminate one redundant node voltage;
end
Remove corresponding rows and columns from the MNA equations.

group of connected capacitors that have no path of capacitors to the ground node.

Lemma 1: If any inductor in a LI-cutset has all its terminals attached to capacitors, there is at least one terminal that all the attached capacitors are (part of) a set of floating capacitors.

Proof: A LI-cutset refers to a set of inductor and current source branches on which the algebraic sum of currents is zero all the time. If any inductor in an LI-cutset is connected to nonfloating capacitors at all its terminals, one (neither inductor nor current source) current bypass will form and the LI-cutset will be broken. In other words, at least one set of terminal capacitors of the inductor must all locate within the generalized node (a subcircuit) isolated by the inductors and current sources, and hence must be floating. ■

To deal with this exception, a special treatment for floating capacitors will be invoked to eliminate one node voltage, which will be detailed in the next section. The whole procedure of LI-cutset elimination is summarized in Algorithm 1.

IV. Treatment for Floating Capacitors

An index-1 system results, after eliminating all voltage sources and the selected inductors from the topology

$$\hat{\mathbf{C}}\dot{\hat{\mathbf{x}}} = -\hat{\mathbf{G}}\hat{\mathbf{x}} + \hat{\mathbf{B}}_{0r}\mathbf{u} + \hat{\mathbf{B}}_{1r}\dot{\mathbf{u}}. \tag{12}$$

The matrix $\hat{\mathbf{C}}$ may still be singular, due to the hidden (algebraic) singularity in $\hat{\mathbf{C}}$ caused by floating capacitors, i.e., in each group of floating capacitors one node voltage is dependent on the others. To reveal such singularity, an LU decomposition is needed to reduce $\hat{\mathbf{C}}$ to the row echelon form as in (4). Nevertheless, if this singularity can be detected and eliminated in advance via topology analysis, the LU decomposition can actually be replaced by a simple permutation of all nonzero rows to the upper part of $\hat{\mathbf{C}}$, which is much more desirable in terms of speed and sparsity.

To this end, we represent each group of floating capacitors by a connected component in a derived graph comprising only capacitive nodes and branches. The MNA stamp of a 3-node floating capacitors group is given in (13a). The algebraic constraint of the floating capacitors implies the relevant rows

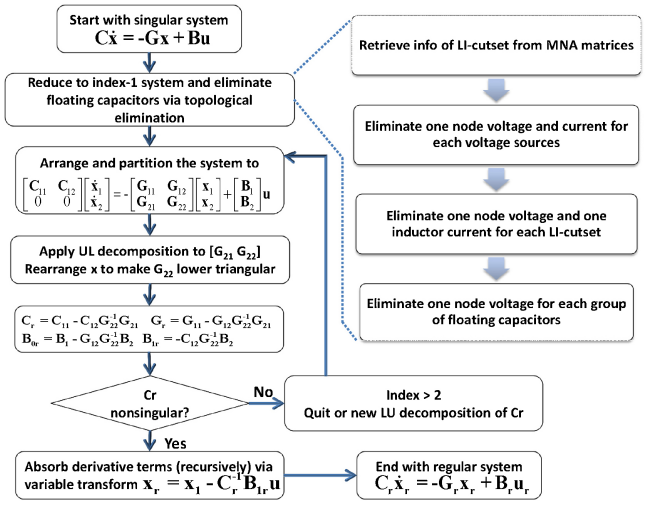

Fig. 2. Flow of the regularization process.

in $\hat{\mathbf{C}}$ add up to zero as shown in (13b). Provided the row summation in $\hat{\mathbf{G}}$ leads to at least one nonzero pivot entry for voltage (assuming $\sum \hat{G}_{*k}$ for $\hat{v}_k$), $\hat{v}_k$ (and $\dot{\hat{v}}_k$) can then be eliminated by the algebraic (and differential) KCL at node k. The nonzero pivoting appears when the subgraph of connected component has at least one outgoing branch of resistor

$$\begin{bmatrix} \hat{C}_{kk} & \hat{C}_{kl} & \hat{C}_{km} \\ \hat{C}_{lk} & \hat{C}_{ll} & \hat{C}_{lm} \\ \hat{C}_{mk} & \hat{C}_{ml} & \hat{C}_{mm} \end{bmatrix} \begin{bmatrix} \dot{\hat{v}}_k \\ \dot{\hat{v}}_l \\ \dot{\hat{v}}_m \end{bmatrix} = - \begin{bmatrix} \hat{G}_{kk} & \hat{G}_{kl} & \hat{G}_{km} \\ \hat{G}_{lk} & \hat{G}_{ll} & \hat{G}_{lm} \\ \hat{G}_{mk} & \hat{G}_{ml} & \hat{G}_{mm} \end{bmatrix} \begin{bmatrix} \hat{v}_k \\ \hat{v}_l \\ \hat{v}_m \end{bmatrix} + \begin{bmatrix} \hat{I}_{s_k} \\ \hat{I}_{s_l} \\ \hat{I}_{s_m} \end{bmatrix} \tag{13a}$$

$$\begin{bmatrix} 0 & 0 & 0 \\ \hat{C}_{lk} & \hat{C}_{ll} & \hat{C}_{lm} \\ \hat{C}_{mk} & \hat{C}_{ml} & \hat{C}_{mm} \end{bmatrix} \begin{bmatrix} \dot{\hat{v}}_k \\ \dot{\hat{v}}_l \\ \dot{\hat{v}}_m \end{bmatrix} = - \begin{bmatrix} \sum \hat{G}_{*k} & \sum \hat{G}_{*l} & \sum \hat{G}_{*m} \\ \hat{G}_{lk} & \hat{G}_{ll} & \hat{G}_{lm} \\ \hat{G}_{mk} & \hat{G}_{ml} & \hat{G}_{mm} \end{bmatrix} \begin{bmatrix} \hat{v}_k \\ \hat{v}_l \\ \hat{v}_m \end{bmatrix} + \begin{bmatrix} \sum \hat{I}_{s_*} \\ \hat{I}_{s_l} \\ \hat{I}_{s_m} \end{bmatrix}. \tag{13b}$$

If all row pivotings in $\mathbf{G}$ for voltages are zero after the summation, i.e., the resistor group also forms a connected component isolated by current variable branches (inductors or voltage sources), a general treatment based on transforming node voltages to branch voltages can be exploited [19]. The rationale is to transform the node voltages $[v_1, v_2, ..., v_n]^T$ in each set of floating capacitors, to the "branch" voltage with reference to v_n, namely, $[v_1 - v_n, v_2 - v_n, ..., v_n]^T$. The new "reference voltage" v_n is then eliminated to reduce the number of unknowns by one.

Taking (11) as an example, the node-branch transform procedure is shown in (14). Suppose v_3 is selected as the new reference node, then in the remaining nodes, there must be one node (v_2 in this case) having at least one outgoing current variable branch (i_{L_1}). The BCE of this current branch is used to eliminate the dependence of v_2 (except the v_2 row itself), then the node-branch voltage transformation is carried out to transform v_2 to $v_2 - v_3$. The *partial* elimination of v_2 in (14a) is to ensure the nonzero pivot element of v_3 in $\mathbf{G}$ after the node-branch transformation [see (14c)]. The empty column in $\mathbf{C}$ at the same step results from the algebraic

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & C_3 & -C_3 & & & \\ & -C_3 & C_3 & & & \\ & & & C_2 & & \\ \hline & & & & 0 & L_1+K \\ & & & & 0 & L_2+K \end{array}\right] \left[\begin{array}{c} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_4 \\ \hline \dot{i}_{L_1} \\ \dot{i}_{L_2} \end{array}\right] = - \left[\begin{array}{cccc|cc} & & g_1 & -g_1 & 0 & 1 \\ & & -g_1 & g_1 & 0 & -1 \\ & & & & 0 & 1 \\ & & & & 0 & -1 \\ \hline -1 & 1 & & & & \\ & & -1 & 1 & & \end{array}\right] \left[\begin{array}{c} v_1 \\ v_2 \\ v_3 \\ v_4 \\ \hline i_{L_1} \\ i_{L_2} \end{array}\right] + \left[\begin{array}{c} 1 \\ -1 \\ 1 \\ \hline \\ \\ \end{array}\right] [Is] + \left[\begin{array}{c} \\ \\ \\ \\ \hline L_1 \\ K \end{array}\right] \left[\dot{I}s\right] \tag{14a}$$

$$\left[\begin{array}{cccc|c} C_1 & & & & \\ & C_3 & -C_3 & & \\ & -C_3 & C_3 & & 0\ \mathbf{g_1}\,(\mathbf{L_1}+\mathbf{K}) \\ & & & C_2 & \\ \hline & & & & L_1+K \\ & & & & L_2+K \end{array}\right] \left[\begin{array}{c} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_4 \\ \hline \dot{i}_{L_1} \\ \dot{i}_{L_2} \end{array}\right] = - \left[\begin{array}{cccc|cc} & & g_1 & -g_1 & 0 & 1 \\ & & -\mathbf{g_1} & 0 \quad g_1 & 0 & -1 \\ & & & & 0 & 1 \\ & & & & 0 & -1 \\ \hline -1 & 1 & & & & \\ & & -1 & 1 & & \end{array}\right] \left[\begin{array}{c} v_1 \\ v_2 \\ v_3 \\ v_4 \\ \hline i_{L_1} \\ i_{L_2} \end{array}\right] + \left[\begin{array}{c} 1 \\ -1 \\ 1 \\ \hline \\ \\ \end{array}\right] [Is] + \left[\begin{array}{c} \mathbf{L_1 g_1} \\ \\ \hline L_1 \\ K \end{array}\right] \left[\dot{I}s\right] \tag{14b}$$

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & C_3 & \mathbf{0} & & & \\ & -C_3 & \mathbf{0} & & & \\ & & & C_2 & & \\ \hline & & & & 0 & L_1+K \\ & & & & 0 & L_2+K \end{array}\right] \left[\begin{array}{c} \dot{v}_1 \\ \mathbf{\dot{v}_2-\dot{v}_3} \\ \dot{v}_3 \\ \dot{v}_4 \\ \hline \dot{i}_{L_1} \\ \dot{i}_{L_2} \end{array}\right] = - \left[\begin{array}{cccc|cc} & & g_1 & \mathbf{0} & 0 & 1 \\ & & -g_1 & 0 \quad \mathbf{g_1} & 0 & -1 \\ & & & & 0 & 1 \\ & & & & 0 & -1 \\ \hline -1 & 1 & \mathbf{1} & & & \\ & & & -1 \quad 1 & & \end{array}\right] \left[\begin{array}{c} v_1 \\ \mathbf{v_2-v_3} \\ v_3 \\ v_4 \\ \hline i_{L_1} \\ i_{L_2} \end{array}\right] + \left[\begin{array}{c} 1 \\ -1 \\ 1 \\ \hline \\ \\ \end{array}\right] [Is] + \left[\begin{array}{c} L_1 g_1 \\ \\ \hline L_1 \\ K \end{array}\right] \left[\dot{I}s\right] \tag{14c}$$

$$\left[\begin{array}{cccc|cc} C_1 & & & & & \\ & C_3 & 0 & & & \\ & -C_3 & 0 & & & \\ & & & C_2 & & \\ \hline & & & & 0 & L_1+K \\ -\frac{\mathbf{C_3}}{\mathbf{g_1}} & & & & 0\ \mathbf{L_1+L_2+2K} & \end{array}\right] \left[\begin{array}{c} \dot{v}_1 \\ \dot{v}_2-\dot{v}_3 \\ \dot{v}_3 \\ \dot{v}_4 \\ \hline \dot{i}_{L_1} \\ \dot{i}_{L_2} \end{array}\right] = - \left[\begin{array}{cccc|cc} & & g_1 & 0 & 0 & 1 \\ & & -g_1 & 0 \ g_1 & 0 & -1 \\ & & & & 0 & 1 \\ & & & & 0 & -1 \\ \hline -1 & 1 & 1 & & & \\ -\mathbf{1} & & \mathbf{0} & 1 & \frac{\mathbf{1}}{\mathbf{g_1}} & \end{array}\right] \left[\begin{array}{c} v_1 \\ v_2-v_3 \\ v_3 \\ v_4 \\ \hline i_{L_1} \\ i_{L_2} \end{array}\right] + \left[\begin{array}{c} 1 \\ -1 \\ 1 \\ \hline \frac{\mathbf{1}}{\mathbf{g_1}} \end{array}\right] [Is] + \left[\begin{array}{c} L_1 g_1 \\ \\ \hline L_1 \\ \mathbf{L_1+K} \end{array}\right] \left[\dot{I}s\right] \tag{14d}$$

$$\left[\begin{array}{ccc|c} C_1 & & & \\ & C_3 & & \\ & & C_2 & \\ \hline -\frac{C_3}{g_1} & & & L_1+L_2+2K \end{array}\right] \left[\begin{array}{c} \dot{v}_1 \\ \dot{v}_2-\dot{v}_3 \\ \dot{v}_4 \\ \hline \dot{i}_{L_2} \end{array}\right] = - \left[\begin{array}{ccc|c} & g_1 & & 1 \\ & & & -1 \\ & & & -1 \\ \hline -1 & 0 & 1 & \frac{1}{g_1} \end{array}\right] \left[\begin{array}{c} v_1 \\ v_2-v_3 \\ v_4 \\ \hline i_{L_2} \end{array}\right] + \left[\begin{array}{c} 1 \\ -1 \\ \\ \hline \frac{1}{g_1} \end{array}\right] [Is] + \left[\begin{array}{c} \\ \\ \\ \hline L_1+K \end{array}\right] \left[\dot{I}s\right] \tag{14e}$$

constraint of floating capacitors. Then the excess voltage v_3 is eliminated, resulting in (14d). Equation (14e) is obtained after relevant variables are removed. Note that, different from [19], our node-branch voltage transformation does not require the generation of normal tree, which can be prohibitive for large-scale circuit networks. The elimination procedure for floating capacitors is summarized in Algorithm 2. The complete flow of the regularization is demonstrated in Fig. 2.

V. Applicability, Complexity, and Implementation

A. Applicability

The proposed method is not a universal way out of the singular problem associated with MNA formulation in circuit simulation. By breaking CV-loops and LI-cutsets, one can cure most of the index-2 circuits, but not all of them. In active circuits with controlled sources, CV-loops and LI-cutsets may not be the only causes of index-2 systems; the complex actions of controlled sources and negative elements can also give rise to intricate dependence that leads to higher DAE indices. Some such examples can be found in [6, p. 335]. In these cases the regularized matrix $\mathbf{C}_r$ will be singular after the first cycle, where a simple check of condition number can reveal the problem. Then another cycle of systematic elimination, if affordable, can be carried out to eliminate more variables. Designers can also return to check whether the circuit has been designed as desired. To the authors' knowledge, no practical approach has been reported in literatures to regularize index-2 circuits with millions of variables, and with the high DAE index arising from controlled sources.

On the other hand, the proposed method is effective for the circuits where CV-loops and LI-cutsets are the only causes of index-2 DAEs, e.g., RLCM networks. Notice that in [20] Tischendorf remarks that the networks containing voltage controlled current sources, which is a vital component in common linearized models of nonlinear devices, also belong to this category provided a mild constraint is satisfied. This implies that our regularization approach is also applicable to nonlinear circuit simulation with common device models. Note that the current regularization technique is applicable

Algorithm 2: Elimination procedure of floating capacitors

Input: matrices $\mathbf{C}$, $\mathbf{G}$, $\mathbf{B}_0$, $\mathbf{B}_1$
Identify all floating capacitors via topology analysis;
For each group of floating capacitors, add up all rows in $\mathbf{G}$ corresponding to the nodes;
if *At least one node voltage (e.g., v_1) with nonzero pivoting in* $\mathbf{G}$ *after the summation* **then**
  Eliminate v_1 from $\mathbf{C}$ and $\mathbf{G}$;
else
  Eliminate v_1 using the BCE of the current branch (except the v_1 row itself);
  Apply node-branch transformation, leading to empty row in $\mathbf{C}$ and nonempty row in $\mathbf{G}$;
  Eliminate v_n from $\mathbf{G}$;
end
Remove corresponding rows and columns from the MNA equations.

TABLE I
SPECIFICATIONS OF TEST CASES

Design	Function	Type	Nodes	Nodes w/o Cap	Index
D1	Trans. line	L	5.6K	431	2
D2	Power grid	L	1.6M	0.6M	2
D3	Power amp.	NL	342	105	2
D4	ALU	NL	10K	373	1

for standard MNA formulation only. Extension to charge/flux MNA will be a topic of future work.

B. Complexity and Implementation Issues

The computational cost of the regularization can be divided into two parts: the cost of topology analysis and the cost of algebraic transformation. The complexity of the two main graph theory algorithms, finding minimal spanning tree and searching for connected components, are $O(N_g)$ and $O\left(N_g log(N_g)\right)$, respectively [21], where N_g refers to the number of "nodes" in the corresponding graphs. Since these algorithms work on reduced graphs, N_g is usually much smaller than the number of MNA variables, e.g., a subcircuit consisting of only capacitors or resistors, regardless of its real size, will be seen as one node in the graph to find LI-cutsets. Therefore, the CPU time devoted to the topology analysis part is insignificant. The algebraic transformation includes the row-wise eliminations and the LU decomposition of $[\mathbf{G}_{21}\ \mathbf{G}_{22}]$ in the systematic elimination stage, of which costs are generally topology-dependent. The expense in row-wise eliminations rests with the number of voltage sources, LI-cutsets and floating capacitors in a topology. In our experiments, the number of these "trouble makers" is usually less than 0.1% for million-scale designs. The cost of factorizing $[\mathbf{G}_{21}\ \mathbf{G}_{22}]$ depends on the number of nodes in absence of capacitances. A circuit having many nodes without capacitances (which is uncommon) will require a longer processing time. Note that the reduction of $[\mathbf{G}_{21}\ \mathbf{G}_{22}]$ to the row echelon form does not affect the sparsity of $\mathbf{C}$.

For linear networks, the regularization procedure is implemented as a one-time preprocessing step. Owing to its reduction nature, the expense of regularization can be amortized by the saving of solving a smaller system in each time step during the subsequent transient simulation. This is in contrast to the expansion nature of [15] wherein the later time integration is carried out with an augmented system.

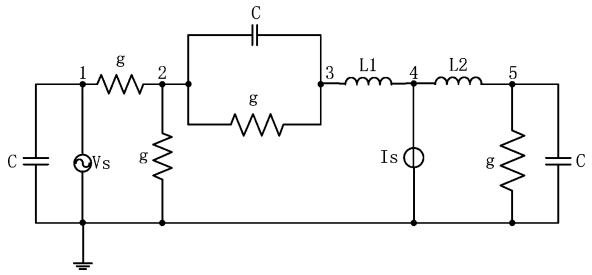

Fig. 3. Schematic of a simple circuit example.

For nonlinear circuits, the regularization may have to be repeated whenever the (linearized) MNA matrices are modified by the nonlinear device evaluation. A positive side is that the device evaluation does not alter the topology after linearization, which is fixed in the first place when the device models are chosen. Hence, the topology analysis can remain as a one-time preprocessing. The row-wise GE can also be made symbolic as in (8f) to enable a fast computation. What has to be repeated then boils down to the processing of (4)–(7), essentially several sparse block GEs. Again, this part of cost should not be "sneered at" purely as an extra cost; it is actually proportional to the saving one can benefit later from solving a smaller system in downstream simulations.

To ensure a right implementation, a proper design of error checking and exception handling is necessary. For instance, "nonzero pivoting" assertions (or "zero pivoting" if no fill-ins should be generated) can be used to guarantee the validity of every row-wise elimination. Condition number checking can be applied before matrix inverse or linear solve. This way, one can guarantee the correctness in the regularization process (no erroneous systems will be generated), even though it may not stop in one cycle. Again, instead of a universal algorithm that covers all possible situations, the aim of this paper is to provide a framework of regularization with sufficient flexibility that allows users to design their own codes with different coverage according to their needs, which span from analysis of specific types of circuits (power-ground networks, and so on) to general-purpose circuit simulation.

VI. EXPERIMENTAL RESULTS

We prototype the regularization technique in MATLAB and integrate the codes into a SPICE-like circuit simulator SMORES developed in MIT [22]. Experiments are carried out on a server with Intel Xeon 3.0 GHz CPU and 16 GB memory.

A. Simple Example

Fig. 3 shows a simple index-2 circuit. The MNA formulation is given in (15a) (for simplicity we assume uniform values of $g = 1$, $C = 1$, and $L = 1.5$). The $\mathbf{C}$ matrix is singular because of: 1) the fourth and the last zero rows; and 2) the linear dependence between the second and third rows.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1.5 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1.5 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_4 \\ \dot{v}_5 \\ \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_V \end{bmatrix} = - \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 1 \\ -1 & 3 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ i_{L1} \\ i_{L2} \\ i_V \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} I_s \\ V_s \end{bmatrix} \tag{15a}$$

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 3 \end{bmatrix} \begin{bmatrix} \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_5 \\ \dot{i}_{L2} \end{bmatrix} = - \begin{bmatrix} 3 & -1 & 0 & 0 \\ -1 & 1 & 0 & 1 \\ 0 & 0 & 1 & -1 \\ 0 & -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ v_3 \\ v_5 \\ i_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} I_s \\ V_s \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 1.5 & 0 \end{bmatrix} \begin{bmatrix} \dot{I}_s \\ \dot{V}_s \end{bmatrix} \tag{15b}$$

$$\begin{bmatrix} 1 & 0 & 0.5 \\ 0 & 1 & 0 \\ 0 & 0 & 3 \end{bmatrix} \begin{bmatrix} \dot{v}'_3 \\ \dot{v}'_5 \\ \dot{i}'_{L2} \end{bmatrix} = - \begin{bmatrix} 1 & 0 & 1.5 \\ 0 & 1 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v'_3 \\ v'_5 \\ i'_{L2} \end{bmatrix} + \begin{bmatrix} 0.5 & 0 \\ 0.5 & 0 \\ 0.25 & 0.5 \end{bmatrix} \begin{bmatrix} I_s \\ V_s \end{bmatrix} \tag{15c}$$

TABLE II

TOPOLOGY ANALYSIS RESULTS AND PERFORMANCE OF REGULARIZATION (TIME UNIT: SECOND)

Case	Vs	LI	FC	cond($\mathbf{C}_r$)	nnz($\mathbf{C}+\mathbf{G}$)	nnz($\mathbf{C}_r+\mathbf{G}_r$)	t_{TP}	t_{GE}	t_{SE}	t_{All}
D1	18	3	1	1.1×10^7	0.9M	0.9M	0.3	0.5	5.1	5.9
D2	0	181	0	1.4×10^6	5.4M	4.8M	46.8	144.4	8.9	191.2
D3	2	0	0	2.4×10^3	2.2K	2.1K	0.02	0.02	0.01	0.05
D4	11	0	0	4.4×10^5	44K	43K	0.24	0.91	0.02	1.2

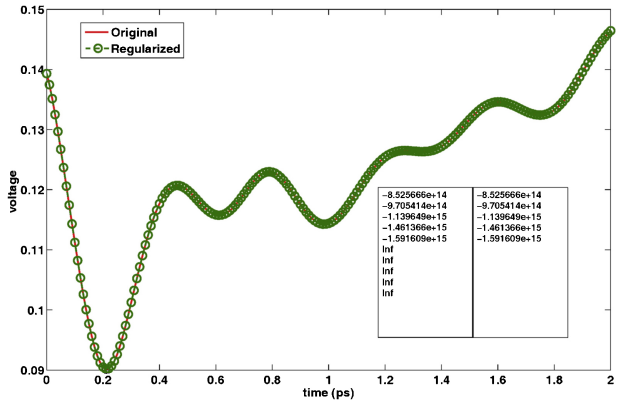

Fig. 4. Accuracy of regularization process.

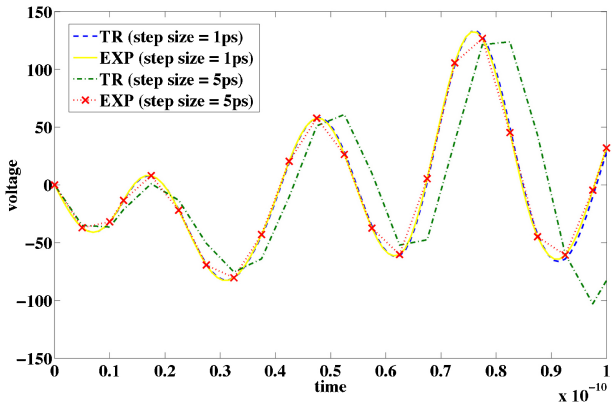

Fig. 5. Transient simulation results of EXP and TR methods with different step sizes.

The topological index reduction eliminates v_1 and i_V to break the CV-loop, and v_4 and i_{L1} to break the LI-cutset, resulting in an index-1 DAE (15b). The final equation after the floating capacitor removal, systematic elimination and variable transformation is given in (15c). Note that the variables are different from those in (15b) due to the variable transformation.

B. Practical Examples

The regularization technique is also tested with a set of large designs. Table I details the functionality, type (linear and nonlinear), size (up to 1.6M nodes), DAE index of MNA system and the number of nodes without capacitances of the benchmark circuits.

First, the transient response (by trapezoidal method) of D1 before and after the regularization are compared in Fig. 4. Since no approximation is introduced, the regularization maintains the accuracy quite well (the relative mismatch between the two curves is 4.3×10^{-11}). The five largest (in magnitude) generalized eigenvalues of the matrix pencils $(-\mathbf{G}, \mathbf{C})$ and $(-\mathbf{G}_r, \mathbf{C}_r)$ are also shown in Fig. 4. The five INF eigenvalues are removed by the regularization and the remaining normal eigenvalues are preserved, which guarantees the exact equivalence between the original and regularized systems.

Table II lists the primary data of interest for regularization. With the tested cases, several observations can be made: 1) the number of "troublemaker" elements to be eliminated before

$$\left[\begin{array}{cccc|c} z & z & z & z & 0 \\ z & z & z & z & 0 \\ z & z & z & z & 0 \\ z & z & z & z & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \end{array}\right]\left[\begin{array}{c} \dot{v}_j \\ \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \\ \hline \dot{i}_v \end{array}\right] = -\left[\begin{array}{cccc|c} z & z & z & z & -1 \\ z & z & z & z & 1 \\ z & z & z & z & 0 \\ z & z & z & z & 0 \\ \hline 1 & -1 & -K & K & 0 \end{array}\right]\left[\begin{array}{c} v_j \\ v_k \\ v_l \\ v_m \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} z \\ z \\ z \\ z \\ \hline 0 \end{array}\right][u] + \left[\begin{array}{c} z \\ z \\ z \\ z \\ \hline 0 \end{array}\right][\dot{u}] \tag{16a}$$

$$\left[\begin{array}{cccc|c} z & z & z & z & 0 \\ \mathbf{z_1} & \mathbf{z_1} & \mathbf{z_1} & \mathbf{z_1} & 0 \\ z & z & z & z & 0 \\ z & z & z & z & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \end{array}\right]\left[\begin{array}{c} \dot{v}_j \\ \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \\ \hline \dot{i}_v \end{array}\right] = -\left[\begin{array}{cccc|c} z & z & z & z & -1 \\ \mathbf{z_1} & \mathbf{z_1} & \mathbf{z_1} & \mathbf{z_1} & 0 \\ z & z & z & z & 0 \\ z & z & z & z & 0 \\ \hline 1 & -1 & -K & K & 0 \end{array}\right]\left[\begin{array}{c} v_j \\ v_k \\ v_l \\ v_m \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} z \\ \mathbf{z_1} \\ z \\ z \\ \hline 0 \end{array}\right][u] + \left[\begin{array}{c} z \\ \mathbf{z_1} \\ z \\ z \\ \hline 0 \end{array}\right][\dot{u}] \tag{16b}$$

$$\left[\begin{array}{cccc|c} z & z & z & z & 0 \\ z_1 & z_1 & z_1 & z_1 & 0 \\ z & z & z & z & 0 \\ z & z & z & z & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \end{array}\right]\left[\begin{array}{c} \dot{v}_j \\ \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \\ \hline \dot{i}_v \end{array}\right] = -\left[\begin{array}{cccc|c} z & z & z & z & -1 \\ \mathbf{0} & \mathbf{z_2} & \mathbf{z_2} & \mathbf{z_2} & 0 \\ \mathbf{0} & \mathbf{z_2} & \mathbf{z_2} & \mathbf{z_2} & 0 \\ \mathbf{0} & \mathbf{z_2} & \mathbf{z_2} & \mathbf{z_2} & 0 \\ \hline 1 & -1 & -K & K & 0 \end{array}\right]\left[\begin{array}{c} v_j \\ v_k \\ v_l \\ v_m \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} z \\ z_1 \\ z \\ z \\ \hline 0 \end{array}\right][u] + \left[\begin{array}{c} z \\ z_1 \\ z \\ z \\ \hline 0 \end{array}\right][\dot{u}] \tag{16c}$$

$$\left[\begin{array}{cccc|c} z & z & z & z & 0 \\ \mathbf{0} & \mathbf{z_3} & \mathbf{z_3} & \mathbf{z_3} & 0 \\ \mathbf{0} & \mathbf{z_3} & \mathbf{z_3} & \mathbf{z_3} & 0 \\ \mathbf{0} & \mathbf{z_3} & \mathbf{z_3} & \mathbf{z_3} & 0 \\ \hline 1 & -1 & -K & K & 0 \end{array}\right]\left[\begin{array}{c} \dot{v}_j \\ \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \\ \hline \dot{i}_v \end{array}\right] = -\left[\begin{array}{cccc|c} z & z & z & z & -1 \\ 0 & z_2 & z_2 & z_2 & 0 \\ 0 & z_2 & z_2 & z_2 & 0 \\ 0 & z_2 & z_2 & z_2 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 \end{array}\right]\left[\begin{array}{c} v_j \\ v_k \\ v_l \\ v_m \\ \hline i_v \end{array}\right] + \left[\begin{array}{c} z \\ z_1 \\ z \\ z \\ \hline 0 \end{array}\right][u] + \left[\begin{array}{c} z \\ z_1 \\ z \\ z \\ \hline 0 \end{array}\right][\dot{u}] \tag{16d}$$

$$\left[\begin{array}{ccc} z_3 & z_3 & z_3 \\ z_3 & z_3 & z_3 \\ z_3 & z_3 & z_3 \end{array}\right]\left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \end{array}\right] = -\left[\begin{array}{ccc} z_2 & z_2 & z_2 \\ z_2 & z_2 & z_2 \\ z_2 & z_2 & z_2 \end{array}\right]\left[\begin{array}{c} v_k \\ v_l \\ v_m \end{array}\right] + \left[\begin{array}{c} z_1 \\ z \\ z \end{array}\right][u] + \left[\begin{array}{c} z_1 \\ z \\ z \end{array}\right][\dot{u}] \tag{16e}$$

$$\left[\begin{array}{cccc|cc} z & z & z & z & 0 & 0 \\ z & z & z & z & 0 & 0 \\ z & z & z & z & 0 & 0 \\ z & z & z & z & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & z & z & 0 & z \end{array}\right]\left[\begin{array}{c} \dot{v}_j \\ \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \\ \hline \dot{i}_v \\ \dot{i}_c \end{array}\right] = -\left[\begin{array}{cccc|cc} z & z & z & z & -1 & 0 \\ z & z & z & z & 1 & 0 \\ z & z & z & z & 0 & -1 \\ z & z & z & z & 0 & 1 \\ \hline 1 & -1 & 0 & 0 & 0 & -K \\ 0 & 0 & z & z & 0 & z \end{array}\right]\left[\begin{array}{c} v_j \\ v_k \\ v_l \\ v_m \\ \hline i_v \\ i_c \end{array}\right] + \left[\begin{array}{c} z \\ z \\ z \\ z \\ \hline 0 \\ z \end{array}\right][u] + \left[\begin{array}{c} z \\ z \\ z \\ z \\ \hline 0 \\ 0 \end{array}\right][\dot{u}] \tag{17a}$$

$$\left[\begin{array}{ccc|c} z_3 & z_1 & z_1 & z_3 \\ z_3 & z & z & z_3 \\ z_3 & z & z & z_3 \\ \hline & z & z & z \end{array}\right]\left[\begin{array}{c} \dot{v}_k \\ \dot{v}_l \\ \dot{v}_m \\ \hline \dot{i}_c \end{array}\right] = -\left[\begin{array}{ccc|c} z_2 & z_1 & z_1 & z_2 \\ z_2 & z & z & z_2 \\ z_2 & z & z & z_2 \\ \hline 0 & z & z & z \end{array}\right]\left[\begin{array}{c} v_k \\ v_l \\ v_m \\ \hline i_c \end{array}\right] + \left[\begin{array}{c} z_1 \\ z \\ z \\ \hline z \end{array}\right][u] + \left[\begin{array}{c} z_1 \\ z \\ z \\ \hline 0 \end{array}\right][\dot{u}]. \tag{17b}$$

systematic elimination is only a negligible percentage (<0.5%) of the total number of variables; 2) the regularized matrix $\mathbf{C}_r$ is invertible with a reasonable condition number; 3) the matrix sparsity is not much affected by the regularization (the numbers of nonzeros stay roughly the same); and 4) in terms of CPU time, the cost of topology analysis (t_{TP}) depends on the sizes of MNA matrices. The expense in row-wise GE (t_{GE}) rests with the number of topological elements to be eliminated. The time spent on systematic elimination (t_{SE}) depends on the number of nodes in absence of capacitances. Overall, these results confirm the proposed regularization process can address the singular $\mathbf{C}$ problem for large-scale designs within a reasonable time (e.g., 191.2 s for the 1.6M case).

C. Application in Explicit Method

To show the application of the proposed regularization technique, we apply a recently developed explicit method, matrix exponential method (EXP) [5], to simulate the 1.6M case (D2). The EXP method requires the matrix-vector product of $\mathbf{C^{-1}(Gv)}$, which is not possible without the application of regularization. The transient responses calculated by the EXP method and the implicit trapezoidal method (TR) are compared in Fig. 5. It shows that the EXP method can use large step sizes while maintaining a good accuracy. The performance data of the two methods in Table III show that the explicit EXP method is 12× faster than the implicit TR method [note that EXP(5 ps) has a comparable accuracy with TR(1 ps)].

TABLE III
CPU TIMES OF TR AND EXP METHODS FOR D3 (TIME SPAN = 100 PS, UNIT: SECOND)

Step Size	TR	EXP
1 ps	2907.1	1190.2
5 ps	853.2	233.8

VII. CONCLUSION

We proposed a two-stage regularization technique to address the singular matrix problem commonly encountered in explicit numerical integration methods. Combining topological index

reduction and systematic elimination, our method is able to regularize large-scale circuit networks with a reasonable efficiency, and maintain the sparsity of the resultant matrices. Numerical experiments have confirmed the accuracy and performance of the proposed technique with examples featuring up to 1.6 million nodes.

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APPENDIX

The MNA stamp of a VCVS, with the BCE of $v_j - v_k = K(v_l - v_m)$, is shown in (16a). Entries z can have arbitrary values and the subscript indicates the step where the entry is updated. Suppose v_j and i_v are selected for elimination. In (16b), the dependence of i_v is first removed from row k in $\mathbf{G}$ using the row of v_j. We eliminate v_j and $\dot{v}_j$ in (16c) and (16d), respectively, using the algebraic and differential BCE. After removing relevant rows and columns, we obtain (16e).

The MNA stamp of a CCVS with the BCE of $v_j - v_k = Ki_c$ is shown in (17a). Two current variables are introduced and only the current of (controlled) voltage source i_v is eliminated. The elimination procedure is similar to that of VCVS. The reduced stamp is shown in (17b).

REFERENCES

[1] L. Nagel, *SPICE2: A Computer Program to Simulate Semiconductor Circuits*. Berkeley, CA: Univ. California, May 1975.
[2] A. Devgan and R. A. Rohrer, "Event driven adaptively controlled explicit simulation of integrated circuits," in *Proc. ICCAD*, 1993, pp. 136–140.
[3] W. Dong and P. Li, "Parallelizable stable explicit numerical integration for efficient circuit simulation," in *Proc. DAC*, 2009, pp. 382–385.
[4] S. H. Weng, P. Du, and C. K. Cheng, "A fast and stable explicit integration method by matrix exponential operator for large scale circuit simulation," in *Proc. ISCAS*, 2011, pp. 321–327.
[5] S. H. Weng, Q. Chen, and C. K. Cheng, "Time-domain analysis of large-scale circuits by matrix exponential method with adaptive control," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, to be published.
[6] L. O. Chua and P. M. Lin, *Computer-Aided Analysis of Electronic Circuits*. Englewood Cliffs, NJ: Prentice-Hall, 1975.
[7] A. Varga, "A descriptor systems toolbox for MATLAB," in *Proc. CACSD Symp.*, 2000, pp. 150–155.
[8] P. Miettinen, M. Honkala, J. Roos, and M. Valtonen, "Improving model-order reduction methods by singularity exclusion," in *Proc. SCEE Book Abstracts*, 2010, pp. 137–138.
[9] Q. Su, V. Balakrishnan, and C.-K. Koh, "Efficient approximate balanced truncation of general large-scale RLC systems via Krylov methods," in *Proc. ASP-DAC*, 2002, pp. 311–316.
[10] S. Natarajan, "A systematic method for obtaining state equations using MNA," *IEE Proc. G Circuits Devices Syst.*, vol. 138, no. 3, pp. 341–346, Jun. 1991.
[11] G. W. Stewart, *Matrix Algorithms: Basic Decompositions*. Philadelphia, PA: SIAM, 1998, p. 185.
[12] D. E. Schwarz and C. Tischendorf, "Structural analysis for electric circuits and consequences for MNA," *Int. J. Circuits Theor. Appl.*, vol. 28, no. 2, pp. 131–162, Mar. 2000.
[13] Z. Zhang and N. Wong, "An efficient projector-based passivity test for descriptor systems," *IEEE Trans. Comput.-Aided Des.*, vol. 29, no. 8, pp. 1203–1214, Aug. 2010.
[14] T. Reis and T. Stykel, "PABTEC: Passivity-preserving balanced truncation for electrical circuits," *IEEE Trans. Comput.-Aided Des.*, vol. 29, no. 9, pp. 1354–1367, Sep. 2010.
[15] S. Bächle and F. Ebert, "Element-based topological index reduction for differential-algebraic equations in circuit simulation," Inst. Math., TU Berlin, Berlin, Germany, Tech. Rep. 05-246, 2005.
[16] S. Bächle and F. Ebert, "Graph theoretical algorithms for index reduction in circuit simulation," Inst. Math., TU Berlin, Berlin, Germany, Tech. Rep. 05-245, 2005.
[17] S. Bächle and F. Ebert, "Index reduction by element-replacement for electrical circuits," *SCEE*, vol. 11, pp. 191–197, 2007.
[18] M. Güther and U. Feldmann, "The DAE-index in electric circuit simulation," *Math. Comput. Simul.*, vol. 39, nos. 5–6, pp. 573–582, Nov. 1995.
[19] L. Mandache, D. Topan, and I. G. Sirbu, "Improved modified nodal analysis of nonlinear analog circuits in the time domain," in *Proc. World Congr. Eng.*, 2010, pp. 905–908.
[20] C. Tischendorf, "Topological index calculation of DAEs in circuit simulation," *Surv. Math. Ind.*, vol. 8, nos. 3–4, pp. 187–199, 1999.
[21] D. Joyner, M. V. Nguyen, and N. Cohen. (2012). *Graph-Theory-Algorithms-Book* [Online]. Available: http://code.google.com/p/graph-theory-algorithms-book
[22] B. N. Bond. (2010). *SMORES: A MATLAB Tool for Simulation and Model Order Reduction of Electrical Systems* [Online]. Available: http://bnbond.com/software/smores

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