Effects of fluorine incorporation on the electrical properties of silicon MOS capacitor with La_2O_3 gate dielectric

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***Abstract* — In this work, the effects of fluorine incorporation by using plasma on the electrical properties of Si MOS capacitor with La_2O_3 gate dielectric are investigated. From the capacitance-voltage (C-V) curve and gate leakage current, it is demonstrated that the F-plasma treatment can effectively suppress the growth of interfacial layer, and thus improve the electrical properties of the device in terms of accumulation capacitance, interface-state density and break-down voltage.**

***Index Terms* — fluorine, high-k dielectric, interfacial layer , lanthanum oxide, MOS.**

I. Introduction

With the continual downscaling of the dimensions of complementary metal-oxide-semiconductor (CMOS) devices in integrated circuit, high-dielectric constant (high-k) metal oxides have been widely investigated in order to replace the conventional dielectric of Si dioxide (SiO_2) for suppressing the increase of gate leakage current [1]. Among them, lanthanum oxide (La_2O_3) is considered to be a promising candidate because of its high dielectric constant and large conduction band offset from Si substrate [2]. However, the properties of La_2O_3 still need to be improved due to growth of low-k interfacial layer of SiO_x.

It has been reported that fluorine incorporation can passivate the Si surface and improve the interface quality between HfO_2 and Si substrate [3]. Hence, this work aims to study the effects of fluorine incorporation on the electrical properties of Si MOS capacitor with La_2O_3 gate dielectric.

II. Experiment

P-type (100) Si wafers were selected to act as the substrate of MOS capacitors. The wafers were cleaned by the conventional RCA method. Subsequently, a film of La_2O_3 with a thickness of 11.5 nm was deposited on the wafers by sputtering La_2O_3 at a radio-frequency (RF) power of 30 W in a mixed ambient of Ar plus O_2. Then, two samples (F-150s, F-300s) received a treatment of $CHF_3 + O_2$ plasma at a RF power of 20 W at 5 °C for 150 s and 300 s respectively. Besides, the flow rate of CHF_3 and O_2 was 10 sccm and 1 sccm respectively. Then, the two samples together with the control sample (non-F) without F-plasma treatment were annealed at 900 °C in an ambient of N_2 at a flow rate of 500 ml/min for 30 s. After that, aluminum was thermally evaporated and patterned as gate electrodes. Eventually, forming-gas annealing was carried out at 300 °C for 20 min so as to improve the ohmic contact of the electrodes.

The physical thickness of the La_2O_3 film was measured by an ellipsometer. Furthermore, the high-frequency (1-MHz) C-V characteristics of the samples were measured by HP4284A LCR meter. Moreover, their gate leakage current was monitored by means of HP4156A semiconductor parameter analyzer. All the measurements were carried out under a light-tight and electrically-shielded condition and at room temperature.

III. Results and discussion

The 1-MHz C-V curves of the samples are shown in Fig. 1. It is found that the accumulation capacitances of the two plasma-treated samples are larger than that of the untreated sample. Moreover, the accumulation capacitance of the sample F-300s is the largest among all. It shows that the fluorine incorporation after the deposition of La_2O_3 can effectively suppress the growth of low-k interfacial layer of SiO_x during the subsequent high-temperature annealing. This is possibly because fluorine has higher electro-negativity than oxygen and thus can passivate the interface between the high-k material and Si substrate. Besides, no significant hysteresis can be found from the 1-MHz C-V curves swept in two directions (from inversion to accumulation and from accumulation to inversion) for each sample. This is mainly ascribed to the sufficiently high annealing temperature of 900 °C after the La_2O_3 deposition and the F-plasma treatment.

From the C-V curves shown in Fig. 1, the electrical parameters, such as capacitance equivalent dielectric thickness (CET), flat-band voltage (V_{fb}), oxide-charge density (Q_{ox}) and interface-state density near mid-gap (D_{it}), are extracted and listed in Table 1. Besides, the dielectric constant (k_{die}) of each sample is also calculated and listed in the table.

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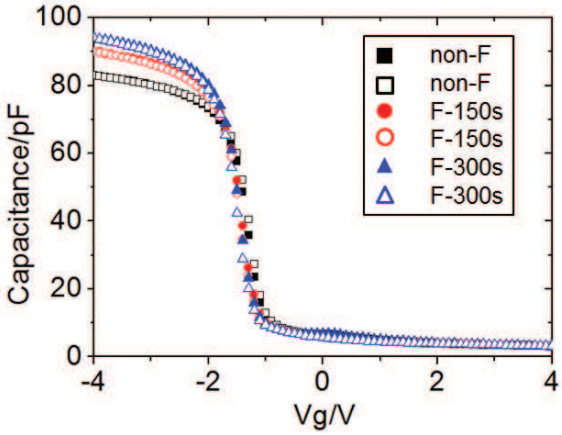

Fig. 1. High-frequency (1-MHz) C-V curves of the samples with different F-plasma treatment conditions (solid symbol for the swept direction from inversion to accumulation; hollow symbol for the swept direction from accumulation to inversion).

In Table 1, the control sample (non-F) has the largest CET value while the sample F-300s has the smallest one. Meanwhile, the k_{die} value of the control sample is smaller than the other two samples. It indicates that the fluorine incorporation can help suppress the growth of low-k SiO_x interfacial layer during annealing at high temperature, and thus increase the effective dielectric constant. Moreover, the D_{it} values of the samples with the plasma treatment are smaller than that of the control sample. This shows that the incorporation of fluorine can effectively passivate the interface between La_2O_3 and Si substrate, and thus reduce the interface state. Besides, the V_{fb} values of all the samples are negative while their Q_{ox} values are positive. Compared with the control sample, the F-150s and F-300s samples have larger magnitudes for these two parameters. It is probably because that fluorine incorporation can cause the reduction of negative charge [4].

Table 1. Electrical parameters extracted from C-V curves.

sample	CET (nm)	V_{fb} (V)	Q_{ox} (cm^{-2})	D_{it} ($cm^{-2}eV^{-1}$)	k_{die}
non-F	3.3	-1.31	3.8×10^{12}	1.3×10^{12}	13.6
F-150s	3.1	-1.40	4.8×10^{12}	6.0×10^{11}	14.5
F-300s	3.0	-1.43	5.2×10^{12}	8.0×10^{11}	15.0

Fig. 2. shows the gate leakage current density (J_g) of the samples. On one hand, the leakage of the non-F sample is the lowest due to the growth of the SiO_x interfacial layer, which could help suppress the gate leakage current to some extent. This further supports that the fluorine incorporation can cause the suppression of the interfacial layer. On the other hand, dielectric breakdown does not happen until the gate voltage (V_g) reaches about -6 V for the F-150s and F-300s samples, while it occurs at about -5 V for the control sample. This is probably due to plasma-induced formation of La-F bonds in the dielectric which are stronger than the original La-O bonds.

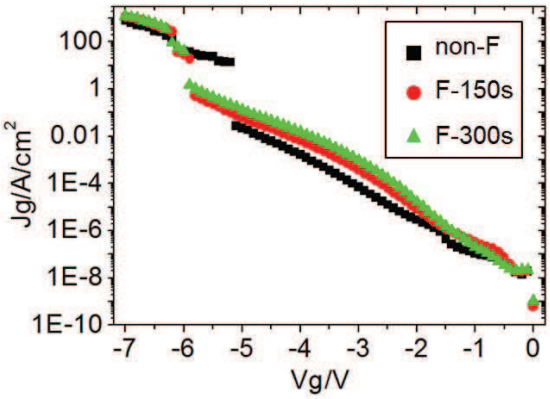

Fig. 2. Gate leakage current density of the samples with different F-plasma treatment conditions.

IV. Conclusion

In this work, Si MOS capacitors with high-k La_2O_3 as gate dielectric were fabricated. Based on the comparison of the samples, the effects of F-plasma treatment after the La_2O_3 deposition on the electrical properties of the devices were investigated. The experimental result shows that fluorine incorporation can effectively passivate the interface between La_2O_3 and Si substrate, thus suppressing the growth of low-k SiO_x interfacial layer and improving the electrical properties of the devices.

References

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