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Computer-Aided Design and Optimization of High-Efficiency LLC Series Resonant Converter

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***Abstract*—High conversion efficiency is desired in switch mode power supply converters. Computer-aided design optimization is emerging as a promising way to design power converters. In this work a systematic optimization procedure is proposed to optimize LLC series resonant converter full load efficiency. A mode solver technique is proposed to handle LLC converter steady-state solutions. The mode solver utilizes numerical nonlinear programming techniques to solve LLC-state equations and determine operation mode. Loss models are provided to calculate total component losses using the current and voltage information derived from the mode solver. The calculated efficiency serves as the objective function to optimize the converter efficiency. A prototype 300-W 400-V to 12-V LLC converter is built using the optimization results. Details of design variables, boundaries, equality/inequality constraints, and loss distributions are given. An experimental full-load efficiency of 97.07% is achieved compared to a calculated 97.4% efficiency. The proposed optimization procedure is an effective way to design high-efficiency LLC converters.**

***Index Terms*—Computer-aided design, efficiency, LLC resonant converter, optimization, power converter.**

NOMENCLATURE

a, b, c	Curve fitting factor.
a_{DF}, b_{DF}	Curve fitting factor.
A_e	Effective cross-sectional area of transformer.
A_{e_Lr}	Effective cross-sectional area of resonant inductor.
b_{xl}	Lower bound vector of design variables.
b_{xu}	Upper bound vector of design variables.
B_{m_XF}	Peak-to-peak swing of transformer flux density.
ΔB_{m_XF}	Amplitude of transformer flux density swing.
ΔB_{m_Lr}	Amplitude of resonant inductor flux density swing.
C_r	Value of resonant capacitor.
d_{AWG}	Diameter of AWG wire in transformer primary winding.
d_{Lr_AWG}	Diameter of AWG wire in resonant inductor winding.
D_F	Dissipation factor.
E_{off}	Turn-off energy consumed by primary MOSFET.
f	Frequency.
f_r	Resonant frequency ($L_r C_r$).
f_s	Switching frequency.
F	Normalized frequency.
F_R	Ratio of AC–DC resistance.
F_{R_pri}	Transformer primary side F_R.
F_{R_sec}	Transformer secondary side F_R.
F_{Rn_Lr}	Resonant inductor F_{Rn}.
h_{foil}	Thickness of foils in transformer secondary winding.
i_{Lr}	Resonant inductor current.
I_{base}	Base current for normalization.
I_{n_pri}	nth harmonic component of primary RMS current.
I_{n_sec}	nth harmonic component of secondary RMS current.
I_{Lr_MAX}	Maximum resonant inductor current.
I_{off}	Turn-off current of primary MOSFET.
$I_{\mathrm{rip\_in}}$	Input ripple current.
$I_{\mathrm{rip\_out}}$	Output ripple current.
$I_{\mathrm{RMS\_pri}}$	Primary side RMS current.
$I_{\mathrm{RMS\_sec}}$	Secondary side RMS current.
j_{Lr}	Normalized resonant inductor current.
j_{Lm}	Normalized magnetizing current.
j_{out}	Normalized output current.
j_{rec}	Normalized secondary rectified current.
k	Steinmetz coefficient.
k_1	Ratio of two resonant frequencies.
k_{off}	Ratio of turn-off energy and turn-off voltage.
L_r	Resonant inductor value.
L_m	Nagnetizing inductor value.
m_1, m_2	Normalized input/output voltage.
m_c	Normalized resonant capacitor voltage.
m_{Lr}	Normalized resonant inductor voltage.
m_m	Normalized transformer voltage.
m_{m2}	Normalized transformer voltage (mode indicator).
M	Normalized conversion ratio.
n	Order of harmonic frequency.
n_{C_in}	Number of input capacitor parallelled.

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n_{C_out}	Number of output capacitor parallelled.
n_{layer}	Number of layers in transformer primary winding.
n_{Lr}	Number of turns in resonant inductor.
n_{Lr_layer}	Number of layers in resonant inductor.
n_{sample}	Number of samples in each switching cycle.
n_p	Number of transformer primary turns.
n_s	Number of transformer secondary turns.
p	Number of layers in magnetic component winding.
P_{cd_pri}	Conduction loss of primary MOSFET.
P_{cd_SR}	Conduction loss of synchronous rectifier.
$P_{cu\_XF\_\mathrm{pri}}$	Copper loss of transformer primary side.
$P_{cu\_XF\_\mathrm{sec}}$	Copper loss of transformer secondary side.
P_{cu_Lr}	Copper loss of resonant inductor.
P_{core_XF}	Core loss of transformer.
P_{core_Lr}	Core loss of resonant inductor.
P_{Cr}	Loss of resonant capacitor.
P_{C_in}	Loss of input capacitor.
P_{C_out}	Loss of output capacitor.
P_{g_SR}	Gate-drive loss of synchronous rectifier.
P_{g_pri}	Gate-drive loss of primary MOSFET.
P_{loss}	Sum of all losses.
P_{out}	Output power.
P_{sw_pri}	Loss of primary MOSFET.
P_{sw_SR}	Switching-loss of synchronous rectifier.
Q_{g_pri}	Gate-drive charge of power MOSFET.
Q_{g_SR}	Gate-drive charge of secondary SR.
Q_{oss_SR}	Output capacitance charge of secondary SR.
r_L	Normalized value of output load.
R_{Cr}	ESR of resonant capacitor.
R_{ds_pri}	On-state resistance of primary MOSFET.
R_{ds_SR}	On-state resistance of synchronous rectifier.
R_L	Value of output load.
R_{Lr}	DC resistance of resonant inductor.
R_{XF_pri}	Transformer DC resistance of the primary side.
R_{XF_sec}	Transformer DC resistance of the secondary side.
t	Time.
v_c	Voltage of resonant capacitor.
v_{Lm}	Voltage of magnetizing inductor.
V_1	Input voltage of LLC equivalent circuit.
V_2	Output voltage of LLC equivalent circuit.
V_{base}	Base voltage in normalization.
V_{g_pri}	Gate-drive voltage of primary MOSFET.
V_{g_SR}	Gate-drive voltage of synchronous rectifier.
V_{e_Lr}	Volume of inductor core.
V_{e_XF}	Volume of transformer core.
V_{in}	Input voltage.
V_{out}	Output voltage.
x	Vector of design variables.
Z_{base}	Base impedance.
α, β	Normalized angles.
$\alpha_{\mathrm{core}}, \beta_{\mathrm{core}}$	Steinmetz coefficients.
γ	Normalized half period of switching cycle.
θ	Normalized angle (time based).
λ	Ratio of L_r/L_m.
$\delta(n)$	Skin depth of $n\mathrm{th}$ harmonic frequency.
ρ_{cu}	Electrical resistivity of copper.
μ_0	Vacuum permeability.
Ω	Optimization constraint set.
ω_0	Resonant frequency ($L_r C_r$).
ω_1	Resonant frequency ($L_r + L_M C_r$).

I. Introduction

ENERGY efficiency is a hot topic that has drawn the attention of researchers and engineers for decades. Numerous research works have focused on improving power converter efficiency. Computer-aided design optimization is one of the methods used to achieve high-energy conversion efficiency, and it has been applied widely in conventional PWM converter design. Early research work [1] utilized the sequential unconstrained minimization technique (SUMT) or the augmented Lagrangian (ALAG) penalty function technique to optimize the converter mass. A practical converter optimization approach was developed in [2] for industrial applications, which utilized the nonlinear optimization program to optimize converter design. Design optimization of interleaved converter for automobile applications was investigated in [3]. A Monte Carlo searching method was applied to handle a large number of design variables. Fuel cell system mass was minimized in [4] under a certain duration constraint. The Pareto-front of power converter multiobject optimization was investigated by [5]. The Pareto-front of converter volume and efficiency were obtained, which means no further efficiency improvement can be achieved under certain constraints, such as converter volume or mass. Converter volume and efficiency were included in the weighted objective function to determine the degree of optimized efficiency or volume. The Pareto-front curve of power density versus efficiency showed that the optimized efficiency was limited by a certain volume constraint. A similar optimization approach was applied to phase-shift PWM converter design in [6] to achieve 99% efficiency.

LLC series resonant converter is emerging to meet the high-efficiency requirements of offline converter and it is becoming increasingly popular in industrial applications. It has zero-voltage switching (ZVS) at primary side and zero-current switching (ZCS) at secondary side. Design methodology of 1-MHz 1-kW LLC converter was investigated in [7]. Details of design procedure were presented in a digital control LLC converter [8]. The LLC converter efficiency can be further improved by using synchronous rectifiers [9]–[11]. Actually, it is more sensible to design and optimize the LLC converter and synchronous rectifiers as an entire system. Adaptive control methodology was proposed to improve the performance of LLC converter [12]. The application of LLC converter in photovoltaic (PV) system was developed in [13]. The advantage of high efficiency from light load to full load shows performance improvements of the entire PV system. Design procedures for wide range LLC converter and dead-time of LLC converter were presented in [14], [15], respectively.

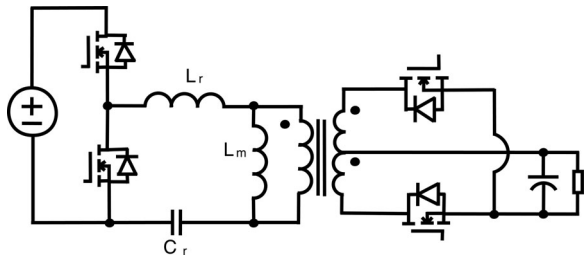


Fig. 1. Half-bridge LLC series resonant DC/DC converter.

So far, there is minimal work on the optimization of LLC converter. The optimization of LLC converter is more difficult than conventional PWM converters. This is because of the following reasons: First, there are multiple modes of operations; each mode has different resonant characteristics. Second, the nonlinear behavior of LLC converter does not have closed-form solutions.

One of the conventional methods used to predict LLC operation behavior is the fundamental harmonic approximation method [16]. However, this method only considers the fundamental frequency harmonic and produces errors when the switching frequency is not at resonant frequency. An improved LLC model was proposed in [17] to present more accurate waveforms. The key equations were solved by numerical method, but this LLC model still assumed that the resonant current is sinusoidal. The steady-state solutions based on state-variable equation were developed in [18]. This method can accurately predict LLC resonant behaviors. However, the nonlinear equations do not have closed-form solutions. With the development of numerical computational techniques, the present research work utilizes nonlinear programming techniques to solve LLC converter steady-state equations. A mode solver is proposed to accurately predict LLC resonant behaviors. Such mode solver is a numerical procedure that considers LLC resonances at different modes. Hence, the proposed mode solver is suitable for handling LLC design variables.

Loss models are presented to predict converter losses that serve as the objective function to optimize LLC efficiency. A prototype 400 V to 12 V/25 A LLC converter is built to verify optimization results. The measured efficiency of optimized LLC converter is 97.07% at full load.

II. LLC Converter Models

A. LLC Mode Solver

A mode solver is proposed to compute the multiple-mode steady-state operation of the LLC converter. The half-bridge LLC converter topology is shown in Fig. 1. There are two resonant inductors and a resonant capacitor in the resonant tank. Hence, the name LLC represents these three resonant elements. Power MOSFETs are applied as the half-bridge switches, which are operated in complementary manner with nearly 50% duty. Output voltage is regulated by variable frequency control. A dead-time is applied during the transition of switching to achieve zero voltage switching and to avoid cross conduction from high-side to low-side switches.

The proposed LLC mode solver serves as a function block in the main optimization procedure. The input variables of the LLC steady-state solver are the values of resonant parameters, such as L_r, C_r, and L_m and the excitations, such as the switching frequency, load, and input/output voltage. The state equations are solved numerically and the output of this function block are vectors containing particular waveform information of current and voltage. The LLC converter has several modes of operation. These modes include the continuous conduction mode below or above resonance, discontinuous conduction mode below or above resonance, and cut-off mode. Continuous conduction mode is defined as a state in which the secondary diode conducts throughout the switching cycle. Discontinuous conduction mode is defined as the state in which secondary diode has certain periods not conducting. The mode solver presented can tackle different modes, which are determined by the nonlinear relationship of the switching frequency, load, and input/output voltage. The detailed procedures of the LLC mode solver are in Fig. 2.

B. Normalization

The solver procedures start with normalization, as shown in Fig. 2 (a1) and (a2). The resonant characteristics of the tank circuit are normalized for the sake of uniformity. We use ω_0 and ω_1 to denote the two resonant frequencies

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} = 2\pi f_r, \omega_1 = \frac{1}{\sqrt{(L_r + L_m)C_r}}. \quad (1)$$

The operation angle θ is given by

$$\theta = \omega_0 t. \quad (2)$$

Denote F the ratio of two frequencies

$$F = \frac{f_s}{f_r}. \quad (3)$$

A half period of switching cycle γ is defined by

$$\gamma = \frac{\omega_0}{2f_s} = \frac{\pi}{F}. \quad (4)$$

The conversion ratio M is defined as

$$M = \frac{V_2}{V_1}. \quad (5)$$

We define some normalized parameters in the following :

$$V_{\text{base}} = V_2 = \frac{n_p}{n_s} V_{\text{out}}, m_2 = \frac{V_2}{V_{\text{base}}} = 1 \quad (6)$$

$$m_1 = \frac{1}{M} \quad (7)$$

$$Z_{\text{base}} = \sqrt{\frac{L_r}{C_r}} \quad (8)$$

$$I_{\text{base}} = \frac{V_{\text{base}}}{Z_{\text{base}}} \quad (9)$$

where V_{base} is defined as the V_2 so that m_2 is normalized to unity, and m_1 is the normalized input voltage. The base impedance Z_{base} and base current I_{base} are given by (8) and (9), respectively.

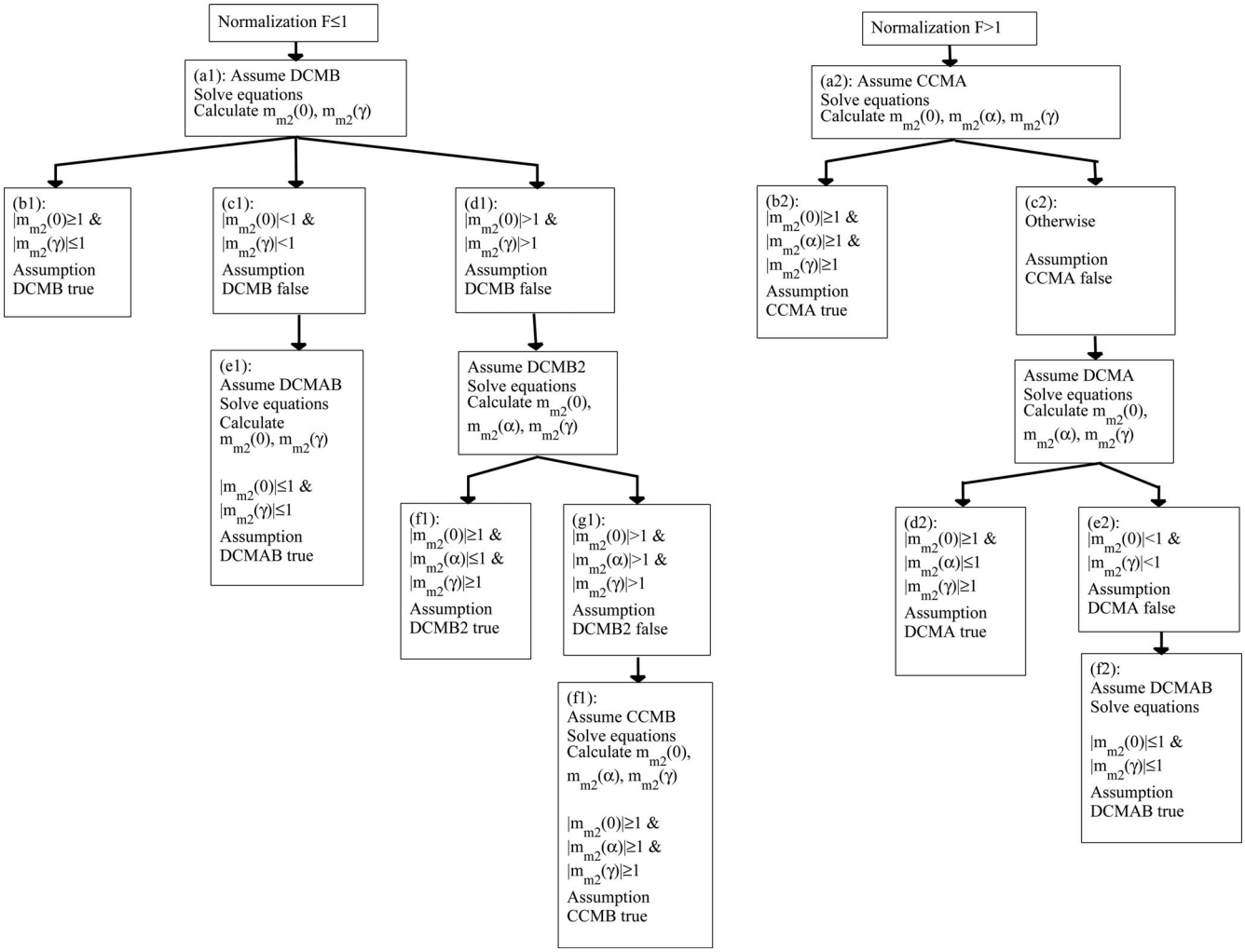


Fig. 2. Flow chart of LLC mode solver.

The normalized voltage on resonant capacitor $m_c(\theta)$ and normalized current through resonant inductor $j_{Lr}(\theta)$ are, respectively, given by

$$m_c(\theta) = \frac{v_c(\frac{\theta}{\omega_0})}{V_{\text{base}}} \tag{10}$$

$$j_{Lr}(\theta) = \frac{i_{Lr}(\frac{\theta}{\omega_0})}{I_{\text{base}}}. \tag{11}$$

Similar expressions are applied to $m_m(\theta)$, $m_{m2}(\theta)$, $m_{Lr}(\theta)$ $j_{Lm}(\theta)$ and j_{out}.

The ratio of two resonant inductance λ and the ratio of two resonant frequencies k_1 are, respectively, given by

$$\lambda = \frac{L_r}{L_m} = \frac{m_{Lr}(\theta)}{m_m(\theta)} \tag{12}$$

$$k_1 = \frac{\omega_1}{\omega_0}. \tag{13}$$

The normalized output load resistance r_L is defined as

$$r_L = \frac{n_p^2 R_L}{n_s^2 Z_{\text{base}}}. \tag{14}$$

C. Operation Below Resonant Frequency

1) Discontinuous Conduction Mode Below Resonance: If $F < 1$, the LLC is assumed to operate in discontinuous conduction mode below resonance (DCMB) first, as shown in Fig. 2 (a1). DCMB is one of the popular designed operation modes. In DCMB mode, the LLC converter voltage conversion ratio M is larger than unity ($M > 1$). Typical waveforms in DCMB mode are shown in Fig. 3(b). The equivalent circuit of DCMB mode in $\theta \in [0, \alpha)$ is shown in Fig. 4(b). The dead-time transition is ignored for simplified analyses. The state equations are given by (15)

$$\theta \in [0, \alpha)$$

$$\begin{cases} m_c(\theta) = [m_c(0) - \frac{1}{M} + 1]\cos(\theta) + j_{Lr}(0)\sin(\theta) \\ \quad + \frac{1}{M} - 1 & \text{(15a)} \\ m_m(\theta) = 1 & \text{(15b)} \\ j_{Lr}(\theta) = [-m_c(0) + \frac{1}{M} - 1]\sin(\theta) \\ \quad + j_{Lr}(0)\cos(\theta) & \text{(15c)} \\ j_{Lm}(\theta) = j_{Lm}(0) + \lambda\theta. & \text{(15d)} \end{cases}$$

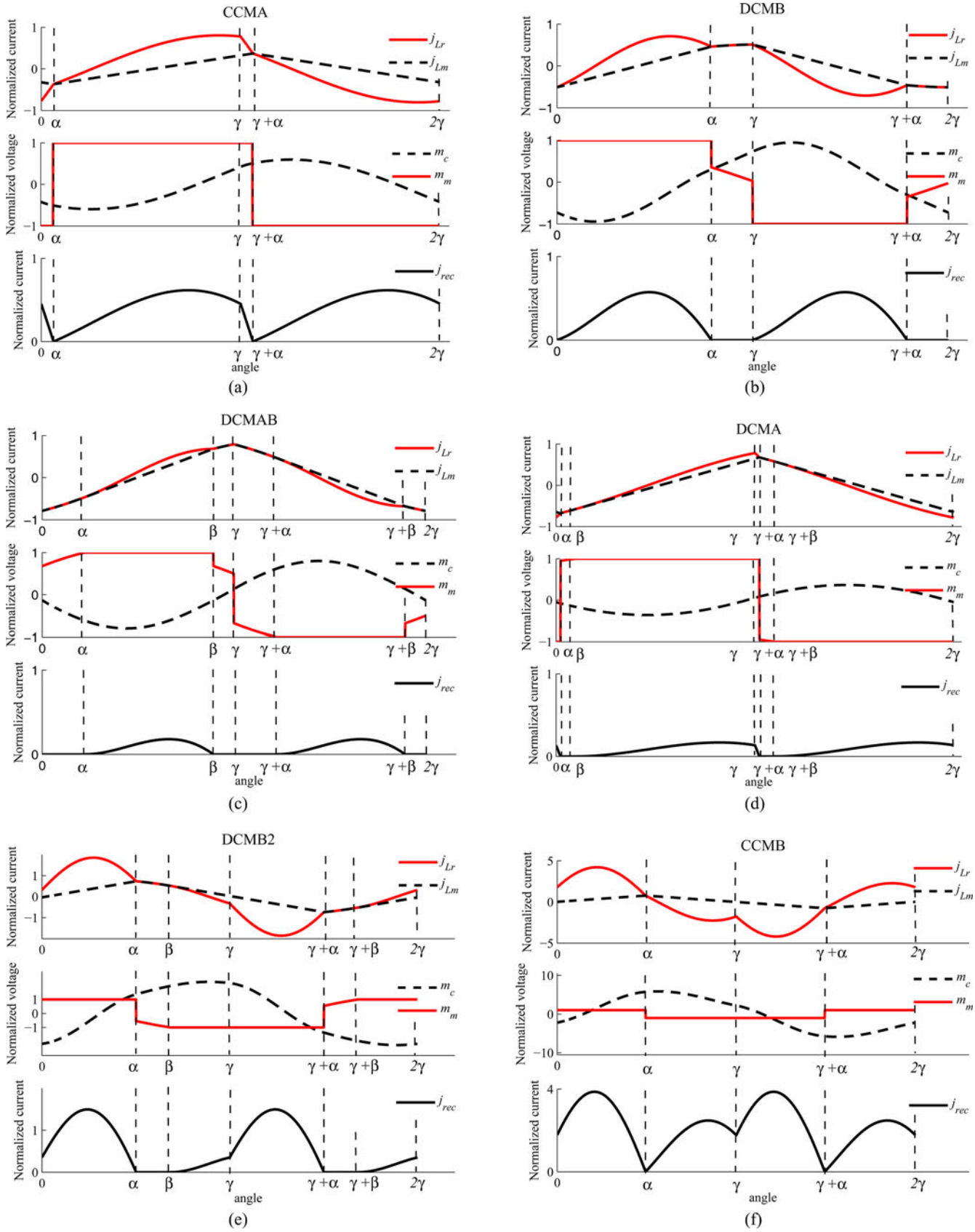


Fig. 3. LLC operation modes.

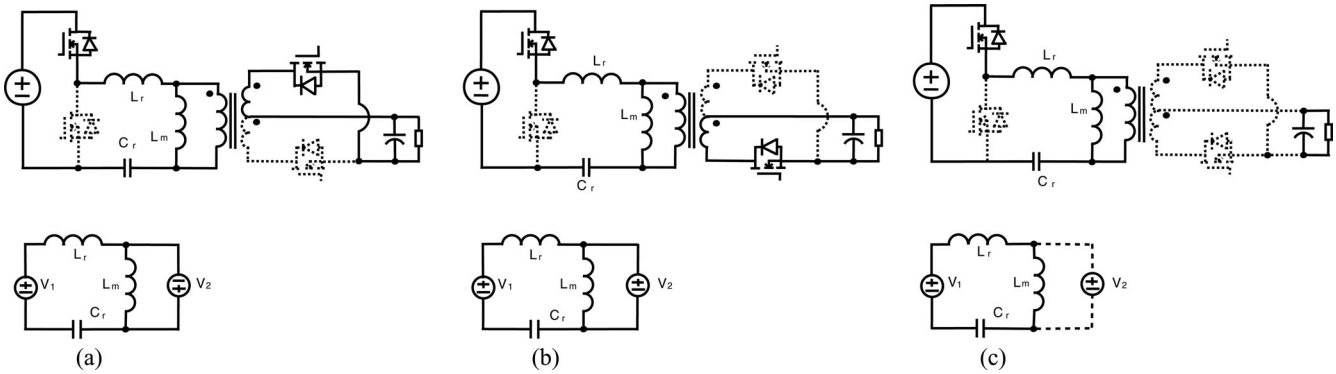


Fig. 4. Equivalent circuits of LLC converter.

The equivalent circuit in $\theta \in [\alpha, \gamma)$ is shown in Fig. 4(c). The state equations are given by (16)

$$\theta \in [\alpha, \gamma)$$

$$\begin{cases} m_c(\theta) = [m_c(\alpha) - \frac{1}{M}]\cos[k_1(\theta-\alpha)] \\ \quad + \frac{j_{Lr}(\alpha)}{k_1}\sin[k_1(\theta-\alpha)] + \frac{1}{M} & (16a) \\ m_m(\theta) = \{[-m_c(\alpha) + \frac{1}{M}]\cos[k_1(\theta-\alpha)] \\ \quad - \frac{j_{Lr}(\alpha)}{k_1}\sin[k_1(\theta-\alpha)]\}/(1+\lambda) & (16b) \\ j_{Lr}(\theta) = [-m_c(\alpha) + \frac{1}{M}]k_1\sin[k_1(\theta-\alpha)] \\ \quad + j_{Lr}(\alpha)\cos[k_1(\theta-\alpha)] & (16c) \\ j_{Lm}(\theta) = j_{Lr}(\theta). & (16d) \end{cases}$$

The average output current j_{out} is given by

$$\begin{aligned} j_{\text{out}} &= \frac{1}{\gamma}\int_0^{\gamma} |j_{Lr}(\theta) - j_{Lm}(\theta)|\,d\theta \\ &= \frac{1}{\gamma}\int_0^{\alpha} [j_{Lr}(\theta) - j_{Lm}(\theta)]\,d\theta \\ &= \frac{1}{\gamma}\left\{\left[-m_c(0) + \frac{1}{M} - 1\right](1-\cos\alpha)\right. \\ &\quad \left. + j_{Lr}(0)\sin\alpha - j_{Lr}(0)\alpha - \frac{1}{2}\lambda\alpha^2\right\}. \end{aligned} \quad (17)$$

The steady-state solution in DCMB $[j_{Lr}(0), m_c(0), \alpha, M]$ can be solved by

$$\begin{cases} m_c(0) + m_c(\gamma) = 0 & (18a) \\ j_{Lr}(0) + j_{Lr}(\gamma) = 0 & (18b) \\ j_{Lr}(\alpha) - j_{Lm}(\alpha) = 0 & (18c) \\ j_{\text{out}} r_L - 1 = 0. & (18d) \end{cases}$$

These four equations become the basis of the solver, and which adequately describe the waveforms of the resonant operation. The initial condition $m_c(0)$ is equal to $-m_c(\gamma)$, as shown in Fig. 3(b), given by (18a). The same reasoning can be applied to $j_{Lr}(0)$ and $-j_{Lr}(\gamma)$ in (18b). The diode stops conducting at angle α, where the resonant current equals to the magnetizing current. Hence, (18c) is formulated that $j_{Lr}(\alpha) = j_{Lm}(\alpha)$. Finally, the unity output voltage is equal to $j_{\text{out}} r_L$, given by (18d). These four equations have four unknowns $[j_{Lr}(0), m_c(0), \alpha, M]$. Two unknowns are the normalized boundary value of resonant inductor current $j_{Lr}(0)$ and resonant capacitor voltage $m_c(0)$. The third unknown is the normalized time α that the secondary diode stops conducting. The fourth unknown is the conversion ratio M. Since these unknowns do not have the analytical closed-form solution, the equations are solved by MATLAB function `fsolve`(x), which is a numerical-based search function.

After solving the above four equations, the following procedures are carried out to validate the assumption of DCMB. At the time when $j_{Lr}(\theta) = j_{Lm}(\theta)$ (the moment $\theta = 0$ or interval $\theta \in [\alpha, \gamma]$ in DCMB), the voltage on L_m determines whether the diodes start to conduct or not. A mode indicator $m_{m2}(\theta)$ is defined as the normalized voltage on L_m, based on the equivalent circuit Fig. 4 (c), when $\theta = 0$ or $\theta \in [\alpha, \gamma]$. According to Kirchhoff's Voltage Law, we obtain

$$m_{Lr}(\theta) + m_{m2}(\theta) + m_c(\theta) = m_1. \quad (19)$$

The solution of $m_{m2}(\theta)$ can be derived by inserting (7) and (12) into (19). To simplify the analyses, we only consider the instants 0 and γ

$$m_{m2}(\theta) = \frac{-m_c(\theta) + \frac{1}{M}}{1+\lambda}_{|\theta=0,\gamma}. \quad (20)$$

($\theta = 0$): If $|m_{m2}(0) \geq 1|$ (the output voltage is normalized to 1), the secondary diode conducts and clamps the $m_m(0)$ to 1 (DCMB true).

Otherwise, if $|m_{m2}(0)| < 1$, the secondary diode is OFF and it is no longer DCMB (DCMB false) but in another mode, discontinuous conduction mode above and below resonance (DCMAB), as shown in Fig. 2 (c1) and Fig. 3(c). Since the LLC converter is assumed operating at DCMB at this moment, DCMAB should be considered later.

($\theta = \gamma$): At the end of DCMB first half cycle γ, if $|m_{m2}(\gamma)| \leq 1$, diode is OFF (DCMB true). Otherwise, if $|m_{m2}(\gamma)| > 1$, the assumption of DCMB is violated (DCMB false).

Summaries are listed as below:

Flow chart Fig. 2 (b1) shows, if $|m_{m2}(0)| \geq 1$ and $|m_{m2}(\gamma)| \leq 1$, the assumption of DCMB is true.

If $|m_{m2}(0)| < 1$ and $|m_{m2}(\gamma)| < 1$, the assumption of DCMB is false then LLC converter is assumed to operate at DCMAB, as shown in Fig. 2 (c1).

If $|m_{m2}(0)| > 1$ and $|m_{m2}(\gamma)| > 1$, the assumption of DCMB is false and then LLC converter is assumed to operate at DCMB2, as shown in Fig. 2 (d1).

2) Discontinuous Conduction Mode Above or Below Resonance: Flow chart Fig. 2 (c1) shows that the converter may operate at DCMAB. Procedures to solve DCMAB are presented later. The secondary diodes do not conduct in $\theta \in [0, \alpha)$ or $[\beta, \gamma)$ when the LLC converter operates at DCMAB, as shown in Fig. 3(c). The equivalent circuit in DCMAB mode $\theta \in [0, \alpha)$ and $[\beta, \gamma)$ is the circuit (c) of Fig. 4. The equivalent circuit in $\theta \in [\alpha, \beta)$ is the circuit (a) of Fig. 4. Five equations are formulated to solve DCMAB given by

$$\begin{cases} m_c(0) + m_c(\gamma) = 0 & \text{(21a)} \\ j_{Lr}(0) + j_{Lr}(\gamma) = 0 & \text{(21b)} \\ j_{Lr}(\alpha) - j_{Lm}(\alpha) = 0 & \text{(21c)} \\ j_{Lr}(\beta) - j_{Lm}(\beta) = 0 & \text{(21d)} \\ j_{\text{out}} r_L - 1 = 0. & \text{(21e)} \end{cases}$$

Similar to the procedure in DCMB equivalent circuit, the mode indicator $m_{m2}(0)$ and $m_{m2}(\gamma)$ can be calculated by (20).

The assumption of DCMAB is true when $|m_{m2}(0)| < 1$ and $|m_{m2}(\gamma)| < 1$, as shown in Fig. 2 (e1).

3) Other Modes Below Resonant Frequency: Two other modes below the resonant frequency are discontinuous conduction mode below resonance "2" (DCMB2) and continuous conduction mode below resonance (CCMB). Typical operation waveforms of the two modes are shown in Fig. 3(e) and (f). Although these two modes are not widely designed in the LLC converter, their operations are still included in the solver for the sake of completeness. The blocks (d1), (f1), (g1), and (h1), in the flow chart in Fig. 2, states the procedures to solve DCMB2 and CCMB.

D. Operation Above Resonant Frequency

1) Continuous Conduction Mode Above Resonance (CCMA): If the $F > 1$, the LLC is assumed to operate in continuous conduction mode above resonance (CCMA), as shown in Fig. 2 (a2). CCMA is a popular mode in LLC converter operation. In this mode, the LLC converter voltage conversion ratio is less than unity ($M < 1$). Typical waveforms in CCMA mode are shown in Fig. 3(a). The equivalent circuit in CCMA mode in $\theta \in [0, \alpha)$ is the circuit (b) of Fig. 4. The state equations are given by

$\theta \in [0, \alpha)$

$$\begin{cases} m_c(\theta) = [m_c(0) - \frac{1}{M} - 1]\cos(\theta) + j_{Lr}(0)\sin(\theta) \\ \quad + \frac{1}{M} + 1 & \text{(22a)} \\ m_m(\theta) = -1 & \text{(22b)} \\ j_{Lr}(\theta) = [-m_c(0) + \frac{1}{M} + 1]\sin(\theta) \\ \quad + j_{Lr}(0)\cos(\theta) & \text{(22c)} \\ j_{Lm}(\theta) = j_{Lm}(0) - \lambda\theta. & \text{(22d)} \end{cases}$$

The equivalent circuit in $\theta \in [\alpha, \gamma)$ is the circuit (a) in Fig. 4. The state equations are presented as follows:

$\theta \in [\alpha, \gamma)$

$$\begin{cases} m_c(\theta) = [m_c(\alpha) - \frac{1}{M} + 1]\cos(\theta - \alpha) \\ \quad + j_{Lr}(\alpha)\sin(\theta - \alpha) + \frac{1}{M} - 1 & \text{(23a)} \\ m_m(\theta) = 1 & \text{(23b)} \\ j_{Lr}(\theta) = [-m_c(\alpha) + \frac{1}{M} - 1]\sin(\theta - \alpha) \\ \quad + j_{Lr}(\alpha)\cos(\theta - \alpha) & \text{(23c)} \\ j_{Lm}(\theta) = j_{Lm}(\alpha) + \lambda\theta. & \text{(23d)} \end{cases}$$

The normalized average output current is given by

$$\begin{aligned} j_{\text{out}} &= \frac{1}{\gamma}\int_0^{\gamma} |j_{Lr}(\theta) - j_{Lm}(\theta)| d\theta \\ &= \frac{1}{\gamma}\int_0^{\alpha} [j_{Lm}(\theta) - j_{Lr}(\theta)] d\theta \\ &\quad + \frac{1}{\gamma}\int_{\alpha}^{\gamma} [j_{Lr}(\theta) - j_{Lm}(\theta)] d\theta \\ &= \frac{1}{\gamma}\Bigg\{ \alpha j_{Lm}(0) - \frac{1}{2}\lambda\alpha^2 - \left[- m_c(0) + \frac{1}{M} + 1 \right] \\ &\quad \times (1 - \cos\alpha) - j_{Lr}(0)\sin\alpha + \left[- m_c(\alpha) + \frac{1}{M} - 1 \right] \\ &\quad \times [1 - \cos(\gamma - \alpha)] + j_{Lr}(\alpha)\sin(\gamma - \alpha) \\ &\quad - j_{Lm}(\alpha)(\gamma - \alpha) - \frac{1}{2}\lambda(\gamma - \alpha)^2 \Bigg\}. \end{aligned} \quad \text{(24)}$$

Four equations are formulated to solve CCMA given by

$$\begin{cases} m_c(0) + m_c(\gamma) = 0 & \text{(25a)} \\ j_{Lr}(0) + j_{Lr}(\gamma) = 0 & \text{(25b)} \\ j_{Lr}(\alpha) - j_{Lm}(\alpha) = 0 & \text{(25c)} \\ j_{\text{out}} r_L - 1 = 0. & \text{(25d)} \end{cases}$$

Similar validation procedures are carried out. The $m_{m2}(0)$, $m_{m2}(\alpha)$ and $m_{m2}(\gamma)$ can be calculated by (20).

If $|m_{m2}(0)| \geq 1$ and $|m_{m2}(\gamma)| \geq 1$, and $|m_{m2}(\alpha)| \geq 1$, the assumption of CCMA is true, as shown in flow chart Fig. 2 (b2).

Otherwise the assumption of CCMA is false [Fig. 2 (c2)]. The assumption of operating mode changes to discontinuous conduction modes above resonance (DCMA) in this case, as shown in Fig. 2 (d2).

2) Other Modes above Resonance: DCMA and DCMAB are two modes operating above resonant frequency. Typical operation waveforms are shown in Fig. 3(c) and (d). The blocks (d2), (f2), and (g2), in the flow chart in Fig. 2, state the procedures to solve DCMA and DCMAB equations.

Table I is presented to summarize the LLC converter operation modes, angles, and their equivalent circuits. Table II reveals the key characteristics used for validating the operation modes.

III. Loss Models

The current waveforms of LLC converter are determined by the operation mode and calculated by the proposed mode solver. Current harmonics are calculated to predict losses. A numerical method is used to sample a switching cycle with n_{sample} points. The current harmonics are calculated by fast Fourier transform, as shown in Fig. 5.

TABLE I
OPERATION MODES OF LLC CONVERTER

$F \leq 1$			
MODE	Angle	Equivalent circuit	Unknows
DCMB	$[0, \alpha)$	(b)	$[j_{Lr}(0), m_c(0), \alpha, M]$
	$[\alpha, \gamma)$	(c)	
DCMAB	$[0, \alpha)$	(c)	$[j_{Lr}(0), m_c(0), \alpha, \beta, M]$
	$[\alpha, \beta)$	(b)	
	$[\beta, \gamma)$	(c)	
DCMB2	$[0, \alpha)$	(b)	$[j_{Lr}(0), m_c(0), \alpha, \beta, M]$
	$[\alpha, \beta)$	(c)	
	$[\beta, \gamma)$	(a)	
CCMB	$[0, \alpha)$	(b)	$[j_{Lr}(0), m_c(0), \alpha, M]$
	$[\alpha, \gamma)$	(a)	

$F > 1$			
CCMA	$[0, \alpha)$	(a)	$[j_{Lr}(0), m_c(0), \alpha, M]$
	$[\alpha, \gamma)$	(b)	$[j_{Lr}(0), m_c(0), \alpha, M]$
DCMA	$[0, \alpha)$	(a)	$[j_{Lr}(0), m_c(0), \alpha, \beta, M]$
	$[\alpha, \beta)$	(c)	
	$[\beta, \gamma)$	(b)	
DCMAB	$[0, \alpha)$	(c)	$[j_{Lr}(0), m_c(0), \alpha, \beta, M]$
	$[\alpha, \beta)$	(b)	
	$[\beta, \gamma)$	(c)	

TABLE II
VALIDATIONS OF LLC OPERATION MODES

$F \leq 1$		
	$m_{m2}(0) \geq 1$	$m_{m2}(0) \leq 1$
$m_{m2}(\gamma) \geq 1$	$m_{m2}(\alpha) \leq 1$ DCMB2 true $m_{m2}(\alpha) \geq 1$ CCMB true	N.A.
$m_{m2}(\gamma) \leq 1$	DCMB true	DCMAB true

$F > 1$		
	$m_{m2}(0) \geq 1$	$m_{m2}(0) \leq 1$
$m_{m2}(\gamma) \geq 1$	$m_{m2}(\alpha) \geq 1$ CCMA true $m_{m2}(\alpha) \leq 1$ DCMA true	N.A.
$m_{m2}(\gamma) \leq 1$	N.A.	DCMAB true

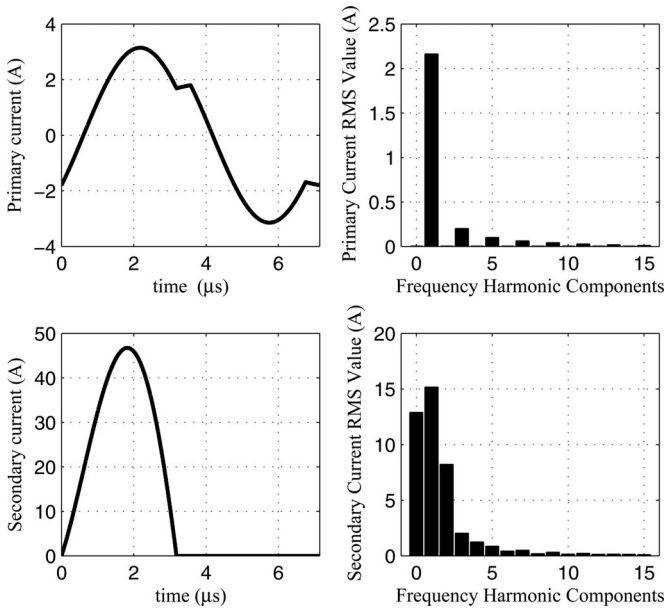


Fig. 5. Transformer current waveform and harmonic components.

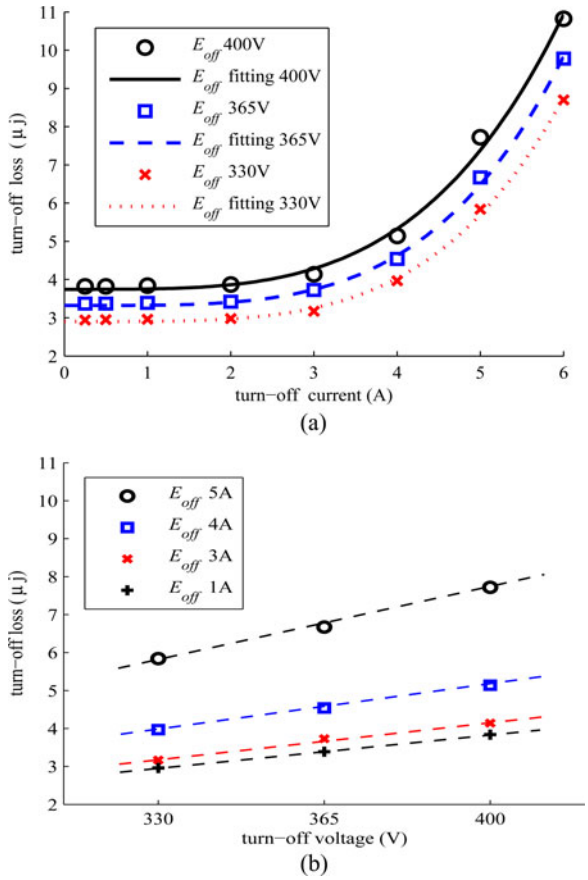


Fig. 6. PSPICE-simulated primary MOSFET turn-off loss.

A. Primary MOSFET

The most promising feature of the LLC converter is zero voltage switching turn-on and small turn-off current for primary side MOSFETs. A simple and effective MOSFET switching loss model is proposed for the prediction of turn-off switching loss at different turn-off currents, as shown in Fig. 6(a). This proposed model utilizes a curve-fitting method to record SPICE simulation results of turn-off switching loss $E_{\rm off}(I_{\rm off})$. The input voltage is fixed at 330, 365, and 400 V in SPICE simulation, as shown in Fig. 6(a). $E_{\rm off}$ is nearly linearly increasing with $V_{\rm in}$ from 330 to 400 V at a certain turn-off current level, as shown in Fig. 6(b). The parameter $k_{\rm off}$ is defined as the ratio of $E_{\rm off}$ increasing value from 330 to 400 V divided by the voltage increasing value 70 V. The actual energy dissipated during switching is $E_{\rm off}(I_{\rm off}, V_{\rm in})$

$$E_{\rm off}(I_{\rm off}) = ae^{bI_{\rm off}} + c \tag{26}$$

$$k_{\rm off}(I_{\rm off}) = \frac{E_{\rm off}(I_{\rm off}, 400\ {\rm V}) - E_{\rm off}(I_{\rm off}, 330\ {\rm V})}{400\ {\rm V} - 330\ {\rm V}} \tag{27}$$

$$E_{\rm off}(I_{\rm off}, V_{\rm in}) = E_{\rm off}(I_{\rm off}, 330\ {\rm V}) + k_{\rm off}(I_{\rm off})(V_{\rm in} - 330). \tag{28}$$

It should be noted that during turn-off, there are two currents flowing through the MOSFET and the total energy value is

$E_{\rm off}(I_{\rm off}, V_{\rm in})$. One current is to charge the output capacitance of MOSFET to $V_{\rm in}$ with the energy $E_{\rm off}(0, V_{\rm in})$, the other current produces energy dissipation (cannot be recovered) in the MOSFET channel with the energy $E_{\rm off}(I_{\rm off}, V_{\rm in}) - E_{\rm off}(0, V_{\rm in})$. During the dead-time, the energy stored in the output capacitance of MOSFET $E_{\rm off}(0, V_{\rm in})$ is recovered to the input capacitor (the drain source voltage of MOSFET drops from $V_{\rm in}$ to 0, soft switching achieved).

The switching loss and conduction loss of the high side and the low side primary MOSFETs (assuming the same type of MOSFETs at the high side and the low side) are denoted as $P_{sw\_\rm pri}(I_{\rm off}, V_{\rm in})$ and $P_{cd\_\rm pri}$, respectively. The gate driving loss of primary MOSFETs is denoted as $P_{g\_\rm pri}$

$$P_{sw\_\rm pri}(I_{\rm off}, V_{\rm in}) = 2f_s[E_{\rm off}(I_{\rm off}, V_{\rm in}) - E_{\rm off}(0, V_{\rm in})] \tag{29}$$

$$P_{cd\_\rm pri} = I^2_{\rm RMS\_pri} R_{ds\_\rm pri} \tag{30}$$

$$P_{g\_\rm pri} = Q_{g\_\rm pri} V_{g\_\rm pri} f_s. \tag{31}$$

B. Isolation Transformer

Transformer design of LLC converter is an important task toward achieving high efficiency. Here, sandwich winding is implemented in order to reduce the AC resistance of the transformer. A center tap configuration is applied at secondary with copper foils for high current low voltage applications. Magnetizing inductance is integrated in the isolation transformer with a certain air gap. A typical transformer structure is shown in Fig. 7. The primary and secondary DC resistance $R_{XF\_\rm pri}$ and $R_{XF\_\rm sec}$ can be directly calculated by the winding geometry. The skin depth of the nth harmonics frequency is given by

$$\delta(n) = \sqrt{\frac{2\rho_{cu}}{2\pi n f_s \mu_0}}. \tag{32}$$

The AC-to-DC resistance ratio F_R at nth harmonic frequency is calculated by Dowell's equation [20], [21], given by

$$F_R(n,p,X) = X\frac{e^{2X} - e^{-2X} + 2\sin(2X)}{e^{2X} + e^{-2X} - 2\cos(2X)} + 2X\frac{p^2-1}{3}\frac{e^{X} - e^{-X} - 2\sin(X)}{e^{X} + e^{-X} + 2\cos(X)}. \tag{33}$$

We have: $F_{R\_\rm pri}(n) = F_R(n,p,X)$ is for primary round conductors with $p = n_{\rm layer}$, $X = \frac{\sqrt{\pi} d_{\rm AWG}}{2\delta(n)}$ [21].

$F_{R\_\rm sec}(n) = F_R(n,p,X)$ is for secondary foils with $p = \frac{n_s}{2}$ and $X = \frac{h_{\rm foil}}{\delta(n)}$.

The AC copper loss at each harmonic frequency is calculated by summing the losses from DC to 32nd harmonics. The primary side and secondary copper losses of the transformer are given by

$$P_{cu\_XF\_\rm pri} = R_{XF\_\rm pri} \sum_{n=0}^{32} F_{R\_\rm pri}(n) I^2_{n\_\rm pri} \tag{34}$$

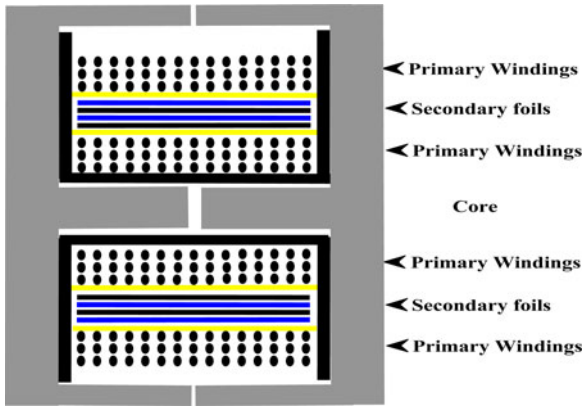


Fig. 7. Winding structure of transformer.

$$P_{cu\_XF\_\rm sec} = R_{XF\_\rm sec} \sum_{n=0}^{32} F_{R\_\rm sec}(n) I^2_{n\_\rm sec} \tag{35}$$

where $I_{n\_\rm pri}$ and $I_{n\_\rm sec}$ denote the nth order harmonic current at the primary side and the secondary side of the transformer. Flux swing of the half-bridge LLC converter is bidirectional. The peak-to-peak flux density is given by

$$B_{m\_XF} = \frac{\int_0^{\frac{t_s}{2}} |v_{Lm}(t)| dt}{n_p A_{e\_XF}}. \tag{36}$$

The empirical Steinmetz equation [19] is applied to calculate the core loss of the transformer, given by

$$P_{\rm core\_XF} = V_{e\_XF} k f_s^{\alpha_{\rm core}} \Delta B_{m\_XF}^{\beta_{\rm core}} \tag{37}$$

where $\Delta B_{m\_XF} = \frac{1}{2} B_{m\_XF}$ is the flux swing, and k, $\alpha_{\rm core}$, and $\beta_{\rm core}$ are the Steinmetz coefficients provided by the manufacturer [22].

C. Resonant Inductor

A separate resonant inductor is applied in the LLC converter. The separate inductor is used because it simplifies the resonance design process. Integrated transformer may lead to totally different loss models, designs, and optimization procedures.

The losses in the resonant inductor are copper loss and core loss. The DC resistance of resonant inductor is calculated according to its geometry. Dowell's equation (33) is also applied to calculate AC resistance. $F_{R\_Lr}(n) = F_R(n,p,X)$ is for resonant inductor, with $p = n_{Lr\_\rm layer}$, $X = \frac{\sqrt{\pi} d_{Lr\_\rm AWG}}{2\delta(n)}$. The copper loss of resonant inductor is given by

$$P_{cu\_Lr} = R_{Lr} \sum_{n=0}^{32} F_{R\_Lr}(n) I^2_{n\_\rm pri}. \tag{38}$$

Core loss of resonant inductor is given by

$$P_{\rm core\_Lr} = V_{e\_Lr} k f_s^{\alpha_{\rm core}} \Delta B_{m\_Lr}^{\beta_{\rm core}} \tag{39}$$

where $\Delta B_{m\_Lr} = \frac{L_r I_{Lr\_\max}}{n_{Lr} A_{e\_Lr}}$ is the flux swing of resonant inductor.

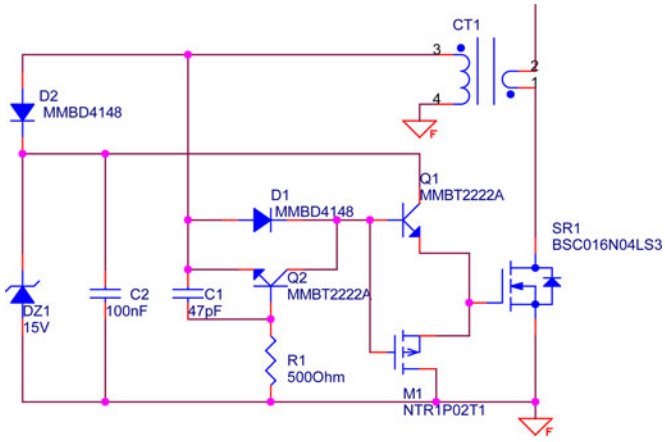


Fig. 8. Current-driven synchronous rectifiers driver.

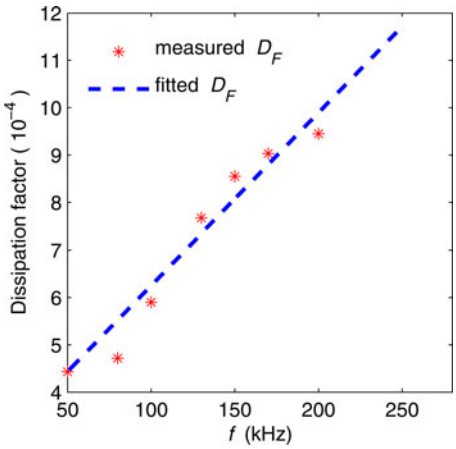


Fig. 9. Dissipation factor of resonant capacitor.

D. Synchronous Rectifier

Synchronous rectification (SR) is implemented at the secondary side to achieve high efficiency at the low-voltage high-current output condition. The current driven synchronous rectifier driving scheme [23], [24] is implemented. The SR driver is shown in Fig. 8. We assume that the SR works under a timing scheme that current does not flow through synchronous rectifier body diode. The major losses for the synchronous rectifier are the conduction loss, turn-off switching loss, and the gate-drive loss. Turn-off switching loss is the energy stored in the stray inductance and being dissipated by the circuit [25]. The simplified model for the turn-off loss and the gate-driving loss of SR are denoted as P_{sw_SR} and $P_{g\_SR,}$, respectively. The conduction loss of SRs is denoted as P_{cd_SR}

$$P_{sw\_SR} = \frac{n_s V_{\text{in}} Q_{oss\_SR} f_s}{2n_p} \tag{40}$$

$$P_{g\_SR} = Q_{g\_SR} V_{g\_SR} f_s \tag{41}$$

$$P_{cd\_SR} = I^2_{\text{RMS\_sec}} R_{ds\_SR}. \tag{42}$$

E. Capacitors

1) Resonant Capacitor: The resonant capacitor in series with the power path carries high RMS current and high voltage. A low-loss capacitor is used to achieve high efficiency and low temperature. A metalized polypropylene capacitor is selected because of its low dissipation factor and low cost. Typically, the dissipation factor (or loss angle $\tan\delta$) of polypropylene capacitor increases with the increasing of frequency up to 10 MHz. Same as before, the curve-fitting method is applied to record the dissipation factor of the resonant capacitor Fig. 9

$$D_F = a_{DF} f + b_{DF} \tag{43}$$

$$R_{Cr} = \frac{D_F}{2\pi f C_r} \tag{44}$$

$$P_{Cr} = I^2_{\text{RMS\_pri}} R_{Cr} \tag{45}$$

where D_F is the dissipation factor with fitting parameter $a_{DF} = 0.03642$ and $b_{DF} = 2.611$. The equivalent series resistance (ESR) of the resonant capacitor R_{Cr} is calculated according to the dissipation factor and the capacitance, given by (44), and the loss of resonant capacitor P_{Cr} is given by (45).

2) Input/output capacitors: Attention should be paid to the output capacitor selection. The output ripple current of LLC converter is higher than that of PWM converters (such as forward, half-bridge, and Cuk converter). The actual ripple currents are calculated by summing frequency harmonic components (DC component excluded) from fundamental frequency to $32nd$ frequency, given by

$$I^2_{\text{rip\_in}} = \sum_{n=1}^{32} I^2_{n\_\text{pri}} \tag{46}$$

$$I^2_{\text{rip\_out}} = \sum_{n=1}^{32} I^2_{n\_\text{sec}} \tag{47}$$

Large capacitance to volume ratio and low cost make aluminum electrolytic capacitors a suitable choice for the input/output capacitor. One has to parallel sufficient number of output capacitors to share ripple current. Low ESR series output capacitor is preferred to avoid excessive power dissipation. Such excessive power dissipation results in significant life degrading. The power dissipations of input/output capacitors are given by

$$P_{C\_\text{in}} = I^2_{\text{rip\_in}} \frac{R_{C\_\text{in}}}{n_{C\_\text{in}}} \tag{48}$$

$$P_{C\_\text{out}} = I^2_{\text{rip\_out}} \frac{R_{C\_\text{out}}}{n_{C\_\text{out}}}. \tag{49}$$

IV. Optimization Procedures

An optimization procedure is presented in this section. The optimization program in this paper is developed under MATLAB environment. The LLC efficiency optimization involves nonlinear, constrained, continuous optimization problems. The `fmincon`(x) function of MATLAB optimization toolbox is applied as the optimizer to solve such problems. The "active-set" algorithm is used in the `fmincon`(x) function. Detailed

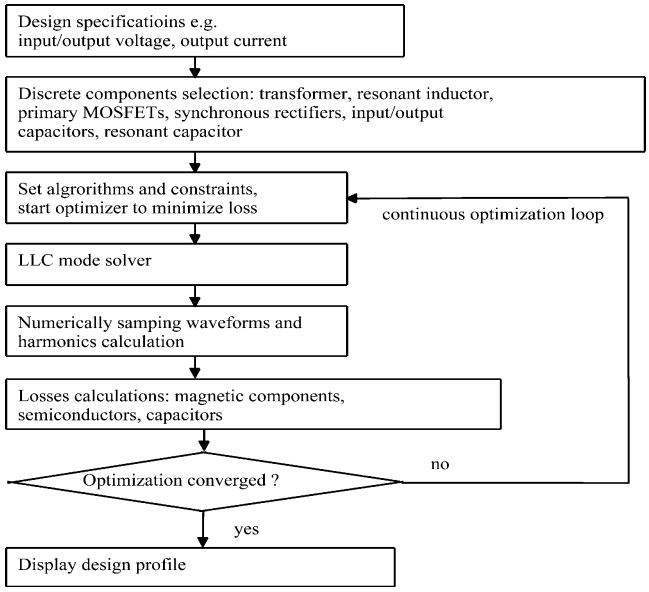


Fig. 10. Flow chart of LLC efficiency optimization procedure.

optimization procedures can be found in [26]. The aim of the optimization is to minimize the loss at a certain loading condition. The flow chart of the optimization procedure is presented in Fig. 10. The characteristics of the power components are discrete, such as the primary MOSFETs, transformer core and bobbin size. The continuous optimization methods cannot handle such discrete values, so we pre-select the discrete components at the discrete component selection stage. In the continuous optimization stage, the discrete components and their related parameters are fixed.

Let x denote a vector containing all the design variables, such as switching frequency, primary turns, secondary turns, value of L_r, L_m, and C_r, etc.

$$x = [f_s, n_p, n_s, L_m, C_r, L_r, d_{\mathrm{AWG}}, n_{\mathrm{layer}}, h_{\mathrm{foil}}, n_{Lr}, d_{\mathrm{AWG\_}Lr}, n_{Lr\_\mathrm{layer}}] \quad (50)$$

The objective function $P_{\mathrm{loss}}(x)$ is the converter loss at full load condition. The optimization problem is to minimize the loss $P_{\mathrm{loss}}(x)$ subject to constraints set Ω, given by

$$\min_{x\in\Omega} P_{\mathrm{loss}}(x) \quad (51)$$

where Ω is given by

$$\Omega = \{x | b_{xl} \leq\leq x \leq\leq b_{xu}, 0.3 - \Delta B_{m\_Lr} \geq 0, 0.3 - \Delta B_{m\_XF} \geq 0, V_{\mathrm{out}} = 12\}. \quad (52)$$

The lower bound vector b_{xl} and the upper bound vector b_{xu} of design variables give the searching range, where the expression "$x \geq\geq b_{xl}$" denotes "$x - b_{xl}$" to be a vector with non-negative entries. "$0.3 - \Delta B_{m\_Lr} \geq 0$" and "$0.3 - \Delta B_{m\_XF} \geq 0$" denote that the resonant inductor and the transformer do not saturate (0.3 is assumed to be the ferrite flux saturation level).

TABLE III
OPTIMIZED RESULTS

Design variables	Lower bound	Upper bound	Optima results	Stopping at boundary
$f_s(kHz)$	50	250	152	No
N_p	10	60	33	No
N_s	1	3	2(integer)	No
$L_m(\mu H)$	100	300	300	Yes
$C_r(nF)$	10	100	39.0	No
$L_r(\mu H)$	30	90	30	Yes
$d_{XF\_AWG}(mm)$	0.1	0.5	0.1	Yes
n_{XF_layer}	1	20	5.56	No
$d_{Lr\_AWG}(mm)$	0.1	0.2	0.1	Yes
n_{Lr}	1	50	13	No
$h_{foil}(mm)$	0.1	0.2	0.2	Yes
n_{Lr_layer}	1	20	8	No
Optimized efficiency: 97.4% (calculated)				

TABLE IV
LOSSES PROFILE

Components	Losses Profile	(W)
Transformer	Primary copper	0.71
	Secondary copper	0.68
	Core	0.87
Resonant inductor	copper	0.39
	Core	0.28
Primary MOSFETs	Conduction	0.71
	Switching	0.02
	Gate driving	0.26
SRs	Conduction	1.56
	Switching	0.10
	SR driver	1.02
Capacitors	input capacitor	0.09
	Output capacitor	0.41
	Resonant capacitor	0.08
Others	PCB	0.81
Total losses (calculated)		7.99
Efficiency (calculated)		97.4%

The output voltage V_{out} given by (53) is required to satisfy the equality constraint and given by

$$V_{\mathrm{out}} = \frac{n_s M V_{\mathrm{in}}}{2n_p}. \quad (53)$$

This means that the output voltage should be regulated at 12 V. This equality constraint is nonlinearly related to many design variables, such as f_s, n_p, n_s, L_r, C_r, L_m, and the operation mode. The optimizer algorithm searches the optimum result that satisfies the constraint set.

V. OPTIMIZATION AND EXPERIMENTAL RESULTS

A. Optimization Results

The optimization program aims to optimize a 400 V input voltage, 12 V output voltage, and 25 A output current LLC resonant converter. The optimized design variables and lower/upper bounds are presented in Table III. The lower/upper bounds are predefined. It can be seen that some of the design variables converge to their boundaries. These boundaries are limited by physical factors such as size. This table also indicates those boundaries that can be improved to have even higher efficiency.

The loss distributions are also presented in Table IV. The optimized efficiency is calculated to be 97.4%, where the calculated efficiency is (output power)/[(all losses)+(output power)]. The loss table indicates the loss distribution and facilitates the

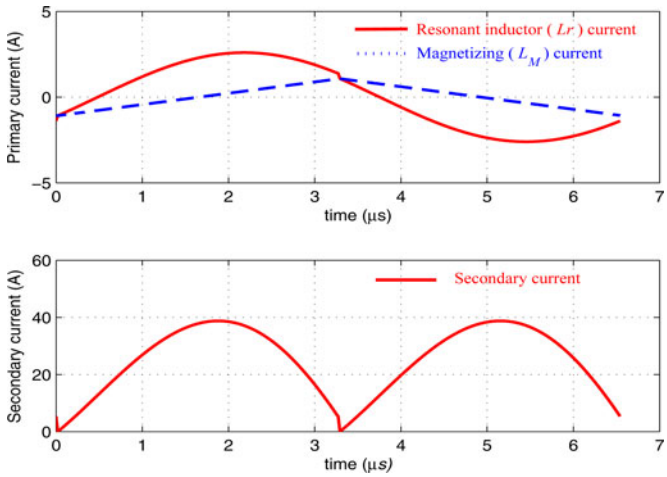


Fig. 11. Calculated waveforms at optimized efficiency.

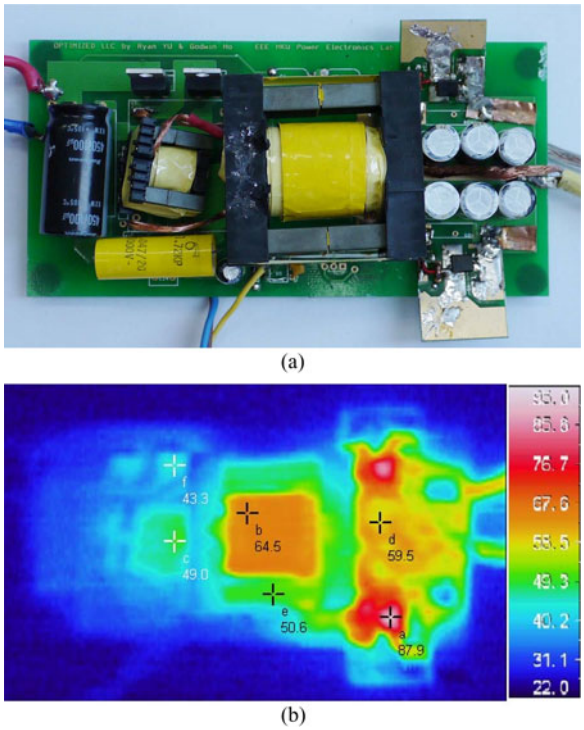


Fig. 12. Prototype converter and thermal images. (a) Prototype LLC converter. (b) Thermal image of prototype converter.

thermal design for components. The table can also direct the choice of individual components. The calculated waveforms of the optimized converter are presented in Fig. 11. The optimized LLC converter operates in CCMA and the switching frequency is only slightly higher than resonant frequency. The results are very similar to previous research works [7], [8] that good efficiency of LLC converter occurs at resonant frequency.

B. Experimental Results

A prototype LLC converter is built as shown in Fig. 12(a). The converter is designed to be naturally cooled. The circuit parameters are listed in Table V. The synchronous rectifier modules are

TABLE V
COMPONENT LIST

Optimized LLC resonant converter $V_{in} = 400V$, $V_{out} = 12V$, $I_{out} = 25A$		
Primary MOSFET	IPP50R140CP	
Synchronous rectifier	BSC016N04LS3	Current driven SRs
Isolation transformer	Turn ratio 34:2 ETD44/22/15 3C90	Primary: AWG40*50 Secondary: 0.2mm foils Leakage inductance: 8μH Lm : 300μH
Resonant inductor	22μH PQ20/16 3C96	AWG44*60 N_{Lr}=12
Resonant Capacitor	47 nF 1000V	Metalized polypropylene 1.72KP .047/20 1000V
Input Capacitor	100μF 450V	RUBYCON KXW (400$m\Omega$ @100kHz)
Output Capacitor	6*1800μF 16V	CHEMI-CON (7$m\Omega$ @100kHz) KZJ16VB182M10X25LL

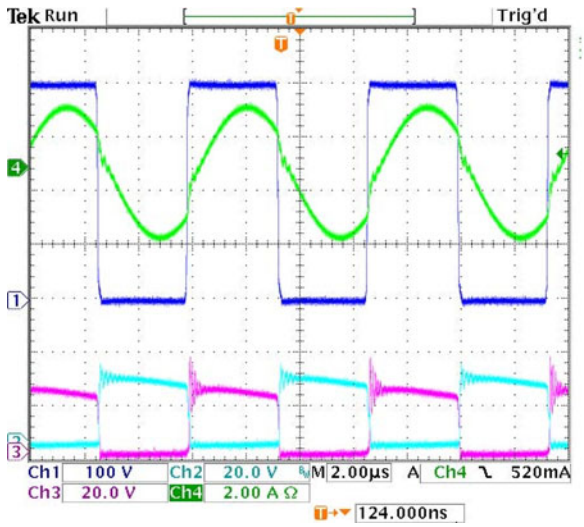


Fig. 13. Experimental waveform of prototype converter.

placed vertically with the heat sinks in the original design. However, it is placed horizontally and the heat sinks are removed in order to take thermal inferred images. The thermal infrared image of the prototype converter operating at full load 12 V 25 A (for 2 h) is also shown in Fig. 12(b). The ambient temperature is 25 °C and there is no air flow. The prototype LLC converter operates at CCMA during full-load conditions, shown in Fig. 13. The Ch1 of Fig. 13 is the drain-source voltage of primary low side MOSFET. Ch2 and Ch3 are the drain-source voltages of secondary SRs. Ch4 is the resonant inductor current. The measured efficiency is 97.07% at full load where the efficiency is calculated by [(output voltage)*(output current)]/[(input voltage)*(input current)]. The average input voltage, input current, and output voltage are measured by the DC voltage meters. The average output current is measured by the DC current meter of the electronic load. The efficiency curve of prototype converter is shown in Fig. 14. The 50%-load-efficiency is higher than 97% and 20%-load-efficiency is higher than 96%. The calculated full-load loss is 7.99 W and the experimental full-load loss is (input power)-(output power), which is 9.05 W. The error of loss calculation is 11.8%, which is calculated by [(experimental loss)-(calculated loss)]/(experimental loss).

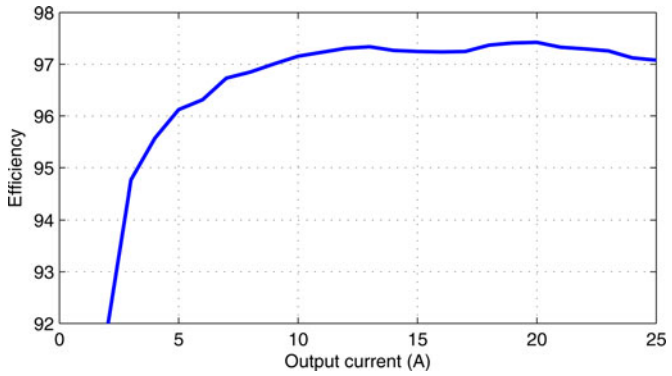


Fig. 14. Measured efficiency of prototype converter.

VI. Conclusion

In this research work a systematic optimization procedure is proposed to optimize the LLC converter full-load efficiency. A mode solver technique is proposed to handle the LLC converter steady-state solutions. The mode solver utilizes numerical nonlinear programming techniques to solve LLC state equations and determine the operation mode. Loss models are provided to calculate the total component losses using the current and voltage information derived from the mode solver. The calculated efficiency serves as the objective function to optimize the converter efficiency. A prototype 300-W 400-V to 12-V LLC converter is built using the optimization results. The details of design variables, boundaries, equality/inequality constraints, and loss distributions are given. A measured full-load efficiency of 97.07% is achieved compared to the calculated 97.4% efficiency. The proposed optimization procedure is an effective way to design high-efficiency LLC converters.

References

[1] S. Balachandran and F. C. Lee, "Algorithms for power converter design optimization," *IEEE Trans. Aerosp Electron. Syst.*, vol. AES–17, no. 3, May 1981.

[2] R. B. Ridley, C. Zhou, and F. C. Lee, "Application of nonlinear design optimization for power converter components," *IEEE Trans. Power Electron.*, vol. 5, no. 1, pp. 29–40, Jan. 1990.

[3] T. C. Neugebauer and D. J. Perreault, "Computer-Aided optimization of DC/DC converters for automotive applications," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 775–783, May 2003.

[4] N. Benavides and P. L. Chapman, "Mass-optimal design methodology for DC–DC converters in low-power portable fuel cell applications," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1545–1555, May 2008.

[5] J. W. Kolar, J. Biela, and J. Minibock, "Exploring the Pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency versus 7 kW/dm^3 power density," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, May, 2009, pp. 1–21.

[6] U. Badstuebner, J. Biela, and J. W. Kolar, "Design of an 99%-efficient, 5kW, phase-shift PWM DC-DC converter for telecom applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2010, pp. 773–780.

[7] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2006, pp. 533–538.

[8] H. de Groot, E. Janssen, R. Pagano, and K. Schetters, "Design of a 1-MHz LLC resonant converter based on a DSP-driven SOI half-bridge power MOS module," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2307–2320, Nov. 2007.

[9] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[10] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current driven synchronous rectifier for series-parallel resonant (LLC) DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 289–297, Jan. 2010.

[11] C. Zhao, M. Chen, G. Zhang, X. Wu, and Z. Qian, "A novel symmetrical rectifier configuration with low voltage stress and ultralow output-current ripple," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1820–1831, Jun. 2010.

[12] B. C. Kim, K. B. Park, C. E. Kim, B. H. Lee, and G. W. Moon, "LLC resonant converter with adaptive link-voltage variation for a high-power-density adapter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2248–2252, Sep. 2010.

[13] Z. Liang, R. Guo, J. Li, and A. Q. Huang, "A high-efficiency PV module-integrated DC/DC converter for PV energy harvest in FREEDM systems," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 897–909, Mar. 2011.

[14] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Optimizing the normalized dead-time and maximum switching frequency of a wide-adjustable-range LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 462–472, Feb. 2011.

[15] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using LLC resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1746–1756, May 2011.

[16] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–1781, Apr. 1988.

[17] M. P. Foster, C. R. Gould, A. J. Gilbert, D. A. Stone, and C. M. Bingham, "Analysis of CLL voltage-output resonant converters using describing functions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1772–1781, Jul. 2008.

[18] J. F. Lazar and R. Martinelli, "Steady-state analysis of the LLC series resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2001, vol. 2, pp. 728–735.

[19] C. P. Steinmetz, "On the law of hysteresis," *Trans. AIEE*, vol. 9, pp. 3–64, 1892.

[20] P. L. Dowell, "Effect of eddy currents in transformer windings," *IEE Proc.*, vol. 113, no. 8, pp. 1387–1394, Aug. 1966.

[21] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 127–131, Jan. 1994.

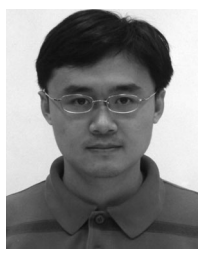
[22] Ferroxcube application note, "Design of planar power transformers," [Online]. Available: www.ferroxcube.com.

[23] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "A novel high frequency current driven synchronous rectifier applicable to most switching topologies," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 635–648, Sep. 2001.

[24] F. N. K. Poon, J. C. P. Liu, and M. H. Pong, "Current driven synchronous rectifier with energy recovery using hysterisis driver," U.S. Patent 6 597 587 B1, Jul. 22, 2003.

[25] Infineon Application Note. (2009, Jun.). "Improving efficiency of synchronous rectification by analysis of the MOSFET power loss mechanism," [Online]. Available: www.infineon.com.

[26] S. P. Han, "A globally convergent method for nonlinear programming," *J. Optim. Theory Appl.*, vol. 22, p. 297, 1977.



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