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Nitrided La_2O_3 as Charge-Trapping Layer for Nonvolatile Memory Applications

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Abstract—Charge-trapping characteristics of La_2O_3 with and without nitrogen incorporation were investigated based on $\text{Al}/\text{Al}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_2/\text{Si}$ (MONOS) capacitors. The physical properties of the high- k films were analyzed by X-ray diffraction and X-ray photoelectron spectroscopy. Compared with the MONOS capacitor with La_2O_3 as charge-trapping layer, the one with nitrided La_2O_3 showed a larger memory window (4.9 V at ± 10 -V sweeping voltage), higher program speed (4.9 V at 1-ms +14 V), and smaller charge loss (27% after 10 years), due to the nitrided La_2O_3 film exhibiting less crystallized structure and high trap density induced by nitrogen incorporation, and suppressed leakage by nitrogen passivation.

Index Terms—Charge-trapping layer (CTL), high- k dielectric, metal-oxide-nitride-oxide-silicon (MONOS), nitrided La_2O_3 , non-volatile memory.

Metal-oxide-nitride-oxide-silicon (MONOS)-type flash memories with dielectrics as charge-trapping layer (CTL) have many advantages over their floating-gate counterparts, such as lower power consumption, higher reliability, and stronger scaling ability. These are mainly ascribed to their physically discrete-trapping characteristics, which can avoid the whole charge leakage even via one single defect happened in the floating-gate memory devices. Si_3N_4 ($k \sim 7$) was the first dielectric used as the CTL. Recently, extensive researches have been carried out to study high- k dielectrics for substituting Si_3N_4 as CTL, mainly due to their higher charge-trapping efficiency and stronger scaling ability [1]–[7]. Among various high- k dielectrics, rare-earth metal oxides, such as Y_2O_3 ($k \sim 18$) [4], Pr_2O_3 ($k \sim 15$) [5], Nd_2O_3 ($k \sim 16$) [5], Er_2O_3 ($k \sim 13$) [5], Gd_2O_3 ($k \sim 14$) [6], La_2O_3 ($k \sim 25$) [7], have received much interest as CTL, mainly due to their relatively high dielectric constants, appropriate conduction-band offsets with respect to Si and good electrical properties [8]. Moreover, La_2O_3 seems more suitable for CTL due to its high dielectric constant and deep-level traps [9], which contribute to high program/erase (P/E) speeds and good retention property. Unfortunately, only a small memory window (0.5 V at +13 V for 1 s [7]) was obtained for the MONOS memory with La_2O_3

as CTL due to the low trap density of the La_2O_3 film. It has been widely reported that nitrogen incorporation into dielectrics can induce traps in the bandgap [1], [2]. In addition, nitrogen incorporation can improve thermal stability [8]. Therefore, based on MONOS capacitors, this work aims to study the charge-trapping characteristics of the La_2O_3 film with and without nitrogen incorporation.

MONOS capacitors with an $\text{Al}/\text{Al}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_2/\text{Si}$ structure were fabricated on p-type silicon substrate. After a standard RCA cleaning, 2-nm SiO_2 was grown on the wafers by thermal dry oxidation. Then, 4-nm La_2O_3 was deposited on the SiO_2 by reactive sputtering using a La_2O_3 target in a mixed Ar/N_2 or Ar/O_2 ambient, and the corresponding MONOS capacitors were denoted as LaON and LaO, respectively. It is noted that both samples have similar thickness for fair comparison. Following that, 14-nm Al_2O_3 as blocking layer was deposited by means of atomic layer deposition using trimethyl-aluminum ($\text{Al}(\text{CH}_3)_3$) and H_2O as precursors at 300 °C. Then, both samples went through a postdeposition annealing (PDA) in N_2 ambient at 850 °C for 30 s. The high-temperature annealing was used to imitate the thermal budget for activating the source/drain of memory transistors after the film deposition [10]. Finally, Al was evaporated and patterned as gate electrode, followed by a forming-gas annealing at 300 °C for 20 min. The cross-sectional transmission electron microscopy (TEM) image of the LaON sample is shown in the inset of Fig. 1(a). To investigate the physical and electrical characteristics of the La_2O_3 film, $\text{Al}/\text{La}_2\text{O}_3/\text{SiO}_2/\text{Si}$ (MNOS) capacitors with and without nitrogen incorporation were also fabricated by the same process mentioned above. The thickness of the dielectrics was determined using ellipsometry and confirmed by TEM. The physical characteristics of the high- k dielectric films were determined by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS). The electrical characteristics of the memory devices were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer at room temperature. The flatband voltage (V_{FB}) was extracted from the experimental C - V curve where the capacitance is equal to the calculated flatband capacitance [11].

The atomic content of nitrogen in the LaON film is determined to be 2.7% by the XPS analysis shown in Fig. 1(a). Fig. 1 also shows the La 3d and Si 2s spectra of the stacked $\text{La}_2\text{O}_3/\text{SiO}_2$ films with and without nitrogen incorporation. For the La_2O_3 film, the La 3d spectrum shows two strong peaks located at 833.0 eV (La $3d_{5/2}$) and 849.9 eV (La $3d_{3/2}$) with a spin-orbit splitting energy of 16.9 eV. These two peaks are in accordance with the La component in La_2O_3 [12]. Compared with the La_2O_3 film, the peak of the La 3d spectrum for the

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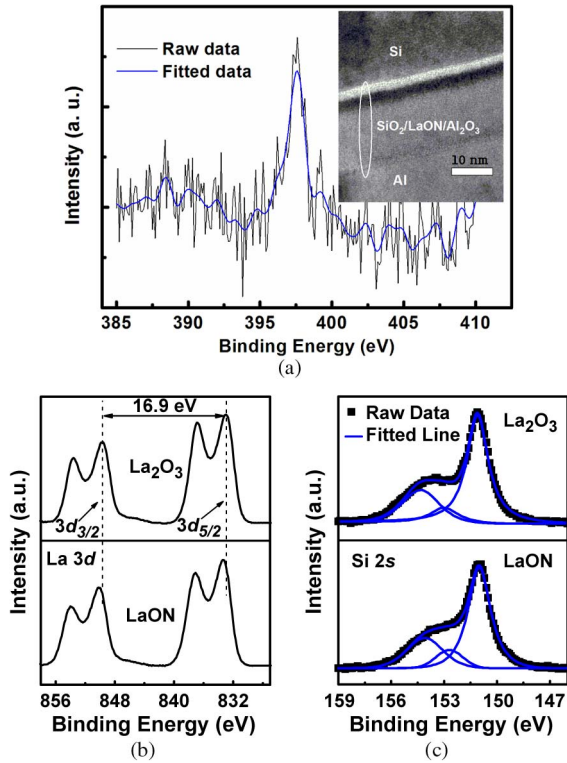


Fig. 1. XPS spectrum of the stacked $\text{La}_2\text{O}_3/\text{SiO}_2$ films with and without nitrogen incorporation. (a) N $1s$ spectrum. (b) La $3d$ spectrum. (c) Si $2s$ spectrum. The inset of Fig. 1(a) is the cross-sectional TEM image of the LaON sample.

nitrided La_2O_3 film shifts to higher binding energy by 0.4 eV, which should be mainly due to the presence of more La-silicate content in the film resulting from the chemical reaction at the $\text{SiO}_2/\text{La}_2\text{O}_3$ interface [13], [14]. The presence of La silicate can be further confirmed by the Si $2s$ spectrum shown in Fig. 1(c), where the Si $2s$ spectrum of the La_2O_3 film can be decomposed into three components located at 151.0 eV, 153.6 eV and 154.3 eV, respectively. The component located at 151.0 eV with a full width at half maximum of 1.4 eV can be assigned to the Si substrate [14], while the component located at 154.3 eV agrees with the bonding structure of SiO_2 [15]. For comparison, the component located at 153.6 eV lying between SiO_2 and Si can be associated with La silicate at the $\text{SiO}_2/\text{La}_2\text{O}_3$ interface. The ratio of Si component corresponding to SiO_2 and silicate (SiO_2 versus silicate) is evaluated to be 2.67 and 2.30 for the La_2O_3 and LaON films, respectively. Combined with the TEM result that no obvious interlayer between the SiO_2 and LaON films as shown in Fig. 1(a), it can be concluded that only a small fraction of SiO_2 is transformed into the silicate for both the LaON and LaO samples. One possible reason for less La-silicate content in the La_2O_3 film than the nitrided one is that reoxidation may happen in the La_2O_3 film during the PDA, because oxygen is easier to diffuse through its more polycrystalline structure, which can be confirmed by the XRD patterns as shown in Fig. 2 later.

The crystalline structures of the stacked $\text{La}_2\text{O}_3/\text{SiO}_2$ films on Si substrate with and without nitrogen incorporation are investigated by XRD and shown in Fig. 2. For the La_2O_3 film, it shows an intense peak at $2\theta = 56.5^\circ$ and three weak peaks

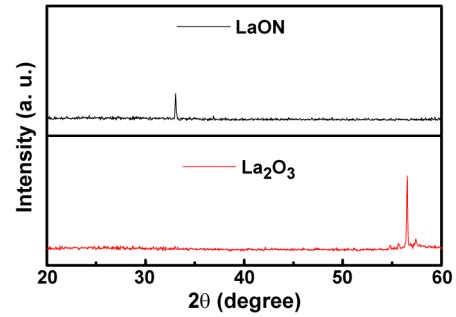


Fig. 2. XRD pattern of the stacked $\text{La}_2\text{O}_3/\text{SiO}_2$ films on Si substrate with and without nitrogen incorporation.

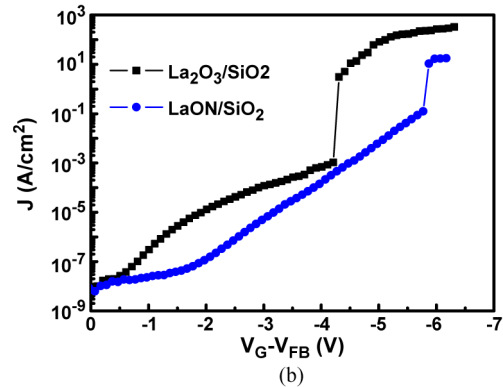
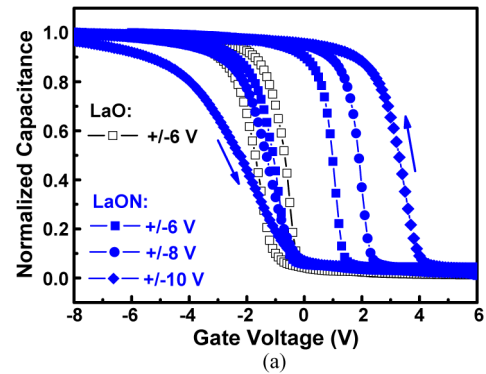


Fig. 3. (a) $C-V$ hysteresis curve of the MONOS capacitors with and without nitrogen incorporation. (b) $J-V_G$ characteristic of the MNOS samples with and without nitrogen incorporation.

located at $2\theta = 54.8^\circ, 55.7^\circ, 57.3^\circ$, respectively, indicating its polycrystalline nature. For comparison, the nitrided La_2O_3 film only exhibits a single peak at $2\theta = 30.0^\circ$, indicating its less crystallized structure. This peak is in accordance with the (411) reflection of the cubic La_2O_3 phase ($2\theta = 30.3^\circ$). Furthermore, compared with the La_2O_3 film, the nitrided La_2O_3 film exhibits lower peak intensity in the XRD diffraction spectrum, suggesting its less crystallized structure due to nitrogen incorporation, which can suppress the crystallization of the dielectric film [8]. Based on the Scherrer equation, the grain size of the La_2O_3 and LaON films is calculated to be 1.35 nm and 1.10 nm, respectively. The La_2O_3 film with polycrystalline structure and larger grain size indicates its more defects along the grain boundaries, which can be further confirmed by the $I-V$ characteristics as shown in Fig. 3(b) later.

Fig. 3(a) shows the 1-MHz $C-V$ hysteresis characteristics of the MONOS capacitors with and without nitrogen incorporation. Sweep starts from inversion region to accumulation region, and back to inversion region again. As the sweeping voltage increases from ± 6 V to ± 10 V, the memory window of the LaON sample increases from 2.0 V to 4.9 V. For comparison, the memory window of the LaO sample is only 0.9 V under ± 6 V sweeping voltage. A larger memory window for the LaON sample indicates its higher trap density due to nitrogen incorporation. Furthermore, when the sweeping voltage increases to ± 8 V, the LaO sample is damaged with a high conductance G of 1.1 mS at $V_G = -8$ V ($G = 12 \mu\text{S}$ for the LaON one), demonstrating the nitridation-induced hardened structure of the nitrated La_2O_3 film. To gain deeper insight into the above phenomenon, the gate-current density as a function of negative gate voltage ($J-V_G$) of the MNOS capacitors ($\text{Al}/\text{La}_2\text{O}_3/\text{SiO}_2/\text{Si}$) with and without nitrogen incorporation is also shown in Fig. 3(b). The MNOS sample without nitrogen incorporation shows much larger gate leakage by two orders of magnitude at $V_G - V_{\text{FB}} = -2$ V as well as lower breakdown voltage than the one with nitrogen incorporation. Electrons injected from the gate electrode can be divided into two parts: some are trapped in the charge-trapping film, and others will pass through the charge-trapping film into the substrate. Consequently, a smaller gate leakage for the nitrated MNOS sample than the one without nitrogen incorporation demonstrates its higher trapping efficiency. This should be mainly ascribed to its fewer defects due to its less crystallized structure and nitrogen passivation. The nitrogen incorporation not only can improve the thermal stability of the dielectric, but also passivates its defects, both of which are beneficial for the dielectric quality of the La_2O_3 film. In addition, since there is only a slight difference in silicate content between the LaO and LaON samples, it is reasonable to assume that this silicate interlayer has similar influence on the gate leakage. Compared with the La_2O_3 film, the dielectric constant of the LaON one can also be improved due to nitrogen incorporation (15 versus 12 from the CV measurement). The lower dielectric constant for the LaO(N) film than the reported value (~ 25) for pure La_2O_3 should be ascribed to the formation of silicate.

Fig. 4 shows the P/E transient characteristics of the MONOS capacitors with and without nitrogen incorporation. The LaON sample displays higher P/E speeds than the LaO one under the same operating conditions. For the LaON sample, it has a V_{FB} shift of 4.9 V and 6.8 V at +14 V for 1 ms and 1 s, respectively, demonstrating its high program speed and large memory window. Moreover, the LaON sample still shows a V_{FB} shift of 3.4 V even at +10 V for 1 ms, which is larger than the value (3.1 V) for the LaO sample at +14 V for 1 s, further supporting its high trapping efficiency resulting from the nitrogen incorporation. In addition, a high erase speed for the LaON sample can be demonstrated by a V_{FB} shift of 3.6 V at -10 V for 100 μs as shown in Fig. 4(b). It is noted that the erase speed can be further improved by using electrodes with high work function (e.g., Pt) because the gate injection due to electrons tunneling from the gate under erase state can be suppressed. The nitrogen incorporation can induce deep-level traps in the charge-trapping film. Meanwhile, the defects

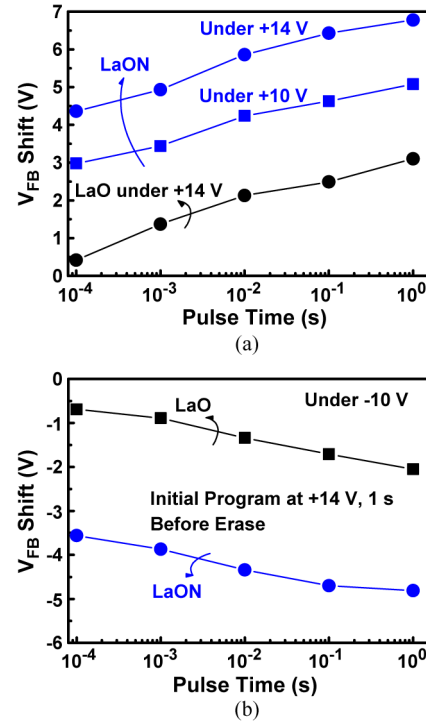


Fig. 4. (a) Program and (b) erase transient characteristics for the MONOS capacitors with and without nitrogen incorporation.

along the grain boundaries can also be suppressed in the LaON sample due to its less crystallized structure as well as nitrogen passivation [16]. It is worth pointing out that the deep-level traps and defects along the grain boundaries play different roles in the charge-trapping characteristics. Charges stored in the defects along the grain boundaries are easy to escape, resulting in low charge-trapping efficiency. These defects can also act as a medium to accelerate charge leakage. Therefore, they should not be considered as effective traps, but as degraders on the reliability of the devices. This is consistent with the conclusion based on the $I-V$ characteristics shown in Fig. 3(b). The higher charge-trapping efficiency for the LaON sample than the LaO one contributes to its higher P/E speeds. In addition, the higher dielectric constant of the LaON film is also beneficial for higher P/E speeds due to higher electric field across SiO_2 under the same operating voltage.

Fig. 5(a) displays the retention characteristics of the MONOS capacitors with and without nitrogen incorporation measured at room temperature. To achieve an approximately the same initial memory window, the LaON sample is programmed at +10 V for 100 μs , while the LaO one is programmed at +14 V for 1 s. The V_{FB} shift decreases with time during the retention mode, which is mainly due to the loss of electrons stored in the CTL via tunneling back to the substrate and gate electrode or hole tunneling from the substrate into the CTL as shown in the inset of Fig. 5(a)[8]. The retained charge rate after 10 years is evaluated by extrapolation to be 72.8% and 65.8% for the LaON and LaO samples, respectively. A more serious charge loss rate for the LaO sample should be ascribed to its more defects in the polycrystalline structure of the La_2O_3 film, because the leakage path via the defects along the grain boundaries can degrade the retention performance. This is consistent with the

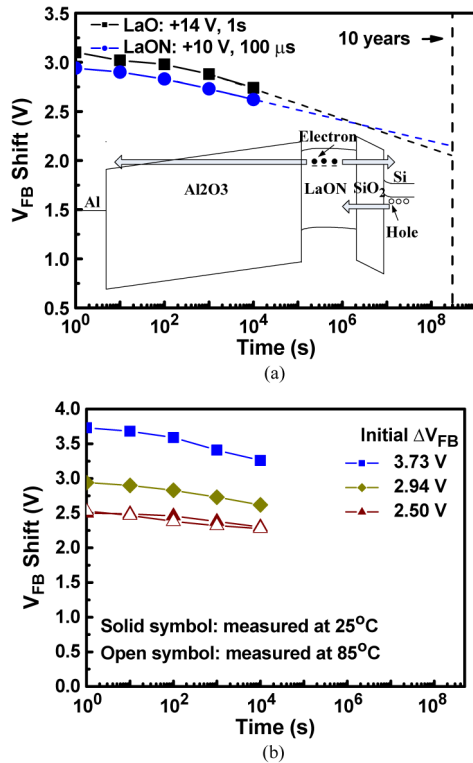


Fig. 5. (a) Retention characteristics of the MONOS capacitors with and without nitrogen incorporation measured at 25 °C. The inset shows the energy-band diagram under the retention mode with $E_{ox} = 4$ MV/cm. The arrays represent possible charge-loss processes. (b) Retention characteristics of the LaON sample with different initial V_{FB} shifts measured at 25 °C. The retention data measured at 85 °C are also shown.

conclusions from the J - V_G characteristics in Fig. 3(b). It is also noted that even the LaO sample shows acceptable retention performance, even though the tunneling layer (SiO_2) is only 2-nm thick. A thin SiO_2 contributes to high P/E speeds for the MONOS-type memories. However, the thin SiO_2 deteriorates the data retention characteristics because charges stored into the charge-trapping film are easy to escape into the substrate during the retention mode. Therefore, there is a tradeoff between P/E speeds and data retention. The acceptable retention characteristics for the LaO sample should be due to the deep-level traps in the La_2O_3 film [9]. Moreover, even though the LaON sample has higher silicate content than the LaO one, it exhibits better retention property, indicating that nitrogen incorporation plays a key role in the performance of the memory devices. To investigate the contributions of electron or hole tunnelings to the degradation of data retention, the retention properties of the LaON sample with different initial V_{FB} shifts (ΔV_{FB}) are also shown in Fig. 5(b). If the hole tunneling dominates under the retention mode, the retention properties should be closely related to the electric field across SiO_2 (E_{ox}) induced by the charges stored in the CTL because the hole-tunneling current by direct-tunneling mechanism (or Fowler-Nordheim mechanism) increases exponentially with E_{ox} . The retained charge after 10^4 s is 87.4%, 89.1%, and 92.0% with initial ΔV_{FB} of 3.73 V ($E_{ox} = 4.75$ MV/cm), 2.94 V ($E_{ox} = 3.74$ MV/cm) and 2.50 V ($E_{ox} = 3.18$ MV/cm), respectively. Only a slight difference of the charge loss under different initial ΔV_{FB} indicates that the

hole tunneling plays a negligible role on the degradation of data retention, mainly due to the good SiO_2/Si interface and large valence-band offset between SiO_2 and Si [8]. The retention property of the LaON sample measured at 85 °C is also shown in Fig. 5(b), where the retained charge after 10^4 s is 90.0% (versus 92.0% at room temperature), further supporting its good data retention property.

In conclusion, the charge-trapping characteristics of La_2O_3 film with and without nitrogen incorporation are investigated based on MONOS-type capacitors. The nitrated La_2O_3 film shows a less crystallized structure and smaller surface roughness compared with the La_2O_3 film. Moreover, the MONOS capacitor with nitrated La_2O_3 as CTL shows better electrical characteristics (larger memory window, higher P/E speeds, and smaller charge loss) than the sample with La_2O_3 as CTL because the nitrated La_2O_3 film exhibits a larger quantity of traps induced by nitrogen incorporation and suppressed leakage through nitrogen passivation. Therefore, the nitrated La_2O_3 film is a promising CTL for high-performance nonvolatile memory applications.

REFERENCES

- [1] H. J. Yang, C. F. Cheng, W. B. Chen, S. H. Lin, F. S. Yeh, S. P. McAlister, and A. Chin, "Comparison of MONOS memory device integrity when using $\text{Hf}_{1-x-y}\text{N}_x\text{O}_y$ trapping layers with different N compositions," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1417–1423, Jun. 2008.
- [2] Y.-H. Wu, L.-L. Chen, J. R. Wu, M. L. Wu, C. C. Lin, and C. H. Chang, "Nonvolatile memory with nitrogen-stabilized cubic-phase ZrO_2 as charge-trapping layer," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 1008–1010, Sep. 2010.
- [3] H. W. You and W. J. Cho, "Charge trapping properties of the HfO_2 layer with various thicknesses for charge trap flash memory applications," *Appl. Phys. Lett.*, vol. 96, no. 9, pp. 093 506-1–093 506-3, Mar. 2010.
- [4] T. M. Pan and W. W. Yeh, "High-performance high-k Y_2O_3 SONOS-type flash memory," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2354–2360, Sep. 2008.
- [5] T. M. Pan and T. Y. Yu, "Comparison of the structural properties and electrical characteristics of Pr_2O_3 , Nd_2O_3 and Er_2O_3 charge trapping layer memories," *Semicond. Sci. Technol.*, vol. 24, no. 9, pp. 095 022-1–095 022-3, Sep. 2009.
- [6] J. C. Wang, C. T. Lin, C. S. Lai, and J. L. Hsu, "Nanostructure band engineering of gadolinium oxide nanocrystal memory by CF_4 plasma treatment," *Appl. Phys. Lett.*, vol. 97, no. 2, pp. 023 513-1–023 513-3, Mar. 2010.
- [7] H. J. Kim, S. Y. Cha, and D. J. Choi, "Memory characteristics of $\text{Al}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Al}_2\text{O}_3$ multi-layer films with various blocking and tunnel oxide thicknesses," *Mater. Sci. Semicond. Process.*, vol. 13, no. 1, pp. 9–12, Feb. 2010.
- [8] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High- κ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001.
- [9] B. Sen, H. Wong, J. Molina, H. Iwai, J. A. Ng, K. Kakushima, and C. K. Sarkar, "Trapping characteristics of lanthanum oxide gate dielectric film explored from temperature dependent current-voltage and capacitance-voltage measurements," *Solid State Electron.*, vol. 51, no. 3, pp. 475–480, Mar. 2007.
- [10] C. Y. Tsai, T. H. Lee, and A. Chin, "Arsenic-implanted HfON charge-trapping flash memory with large memory window and good retention," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 381–383, Mar. 2011.
- [11] Z. Q. Liu, S. Y. Chiam, W. K. Chim, J. S. Pan, and C. M. Ng, "Thermal stability improvement of the lanthanum aluminate/silicon interface using a thin yttrium interlayer," *J. Electrochem. Soc.*, vol. 157, no. 12, pp. G250–G257, Oct. 2010.
- [12] K. Kakushima, K. Okamoto, T. Koyanagi, M. Kouda, K. Tachi, T. Kawanago, J. Song, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Selection of rare earth silicates for highly scaled gate dielectrics," *Microelectron. Eng.*, vol. 87, no. 10, pp. 1868–1871, Oct. 2010.
- [13] D. Eom, S. Y. No, C. S. Hwang, and H. J. Kim, "Deposition characteristics and annealing effect of La_2O_3 films prepared using $\text{La}(\text{iPrCp})_3$ precursor," *J. Electrochem. Soc.*, vol. 154, no. 3, pp. G49–G53, Jan. 2007.

- [14] L. Shi, Y. Yuan, X. F. Liang, Y. D. Xia, J. Yin, and Z. G. Liu, "Microstructure and dielectric properties of La_2O_3 doped amorphous SiO_2 films as gate dielectric material," *Appl. Surf. Sci.*, vol. 253, no. 7, pp. 3731–3735, Sep. 2006.
- [15] H. Seyama and M. Soma, "Bonding-state characterization of the constituent elements of silicate minerals by x-ray photoelectron spectroscopy," *J. Chem. Soc., Faraday Trans. 1*, vol. 81, no. 2, pp. 485–495, 1985.
- [16] Y. H. Wu, L. L. Chen, Y. S. Lin, M. Y. Li, and H. C. Wu, "Nitrided tetragonal ZrO_2 as the charge-trapping layer for nonvolatile memory application," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1290–1292, Dec. 2009.

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