Analysis and Design of a High-Voltage-Gain Hybrid Switched-Capacitor Buck Converter

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***Abstract*—This paper presents an analysis on the effect of having different number of capacitors n in the first-stage switched-capacitor circuit of an improved hybrid switched-capacitor buck converter for high-voltage-gain conversion. Various aspects of the topology, operation, and efficiency are investigated. It is shown both analytically and experimentally that a higher n in the step-down capacitor stage does not necessarily lead to an overall improved power efficiency. A design and optimization method is thus proposed for the improved SC-buck converter.**

***Index Terms*—High voltage gain converter, hybrid switch-capacitor buck converter.**

I. Introduction

HIGH-VOLTAGE-GAIN dc-dc converters are commonly used for electronic applications. To save energy, the supply voltage of modern electronics is decreased to an ultra-low voltage level of less than 1 V. Meanwhile, the intermediate dc supply voltage, especially that of renewable power sources [1], is at a relatively high level of above 12 V [2]–[6]. This prompts the power electronics community to investigate high-voltage-gain dc-dc converters which have a low-voltage output and a high bandwidth regulation.

At present, the electronic industry is still using simple and easy-to-control converters based on conventional buck converter topologies, for achieving such kind of voltage step-down conversions [2]–[5]. However, to achieve high-voltage-gain conversions, the buck converter has to be operated with a very small duty ratio ($D = (V_{\rm out})/(V_{\rm in})$ being very small), which not only complicates its implementation due to the limits of the duty ratio and the switching frequency [6], but also deteriorates its dynamic performance and reduces its efficiency due to the very-short on time and very-long freewheeling time within the switching cycle [7]. For this kind of conversion, converters with transformers would be a better choice. However, this increases size and cost, which makes them less acceptable for applications that do not need isolation [6].

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Switched-capacitor (SC) dc-dc converters, which consist exclusively of power switches and capacitors, can efficiently perform high-voltage-gain conversion [6]–[8]. As there is no magnetic component in the topologies, they are suitable for integrated circuit (IC) implementation in microelectronic form. Besides, they also have advantages of small size, light weight, high efficiency and high power density [9]–[17]. These advantages make them useful in modern electronic products such as portable digital assistant, MP3 players, digital cameras, FLASH, and LED lighting applications [18], [19]. However, SC dc-dc converter cannot get a high efficiency if they are used for the purpose of voltage regulation, which limits their applications [9]–[20].

The limitations of the conventional converters have spurred the interests in developing a new kind of high-voltage-gain hybrid SC dc-dc converters [6]–[8], [21]–[25], of which the converter is made up of a first-stage SC converter, followed by a second-stage buck converter. For this two-stage SC-buck converter, the first-stage SC converter steps down the input voltage to a low level while the second-stage buck converter mainly performs the voltage regulation. An overall high efficiency is achievable with such two-stage hybrid SC-buck converter because the first-stage SC converter is used only for voltage transformation and not voltage regulation. As mentioned, for performing only voltage transformation, a very high efficiency SC converter is achievable. Industrial SC converter products of higher than 98% efficiency (e.g., LTC1044, MAX1044, SI7660, GS7660, etc.) is available. Once the input voltage is converted to a low unregulated voltage by the high efficiency SC converter, the second-stage buck converter will perform a small voltage transformation and the voltage regulation operation at a high efficiency. This is also possible because the input voltage to the buck converter is already at a low level making its duty ratio relatively normal. Recall that the reason why a single buck converter when used for high-voltage-gain conversion is lossy is because the buck converter has to do both the voltage conversion and regulation and that its duty ratio being the function of the input voltage and the output voltage, is very small.

Interestingly, while the concept of such converters have been widely reported [6], [7], [21]–[23], the effect of having different number of capacitors n in the first-stage switched-capacitor circuit has not being studied. In this paper, using an improved hybrid SC-buck converter as an illustrative example, we introduce a systematic way of modifying n for high-voltage-gain conversion that will result in an optimal way of designing and configuring such a hybrid SC-buck converter. Various aspects of the topology, operation, and efficiency will be discussed.

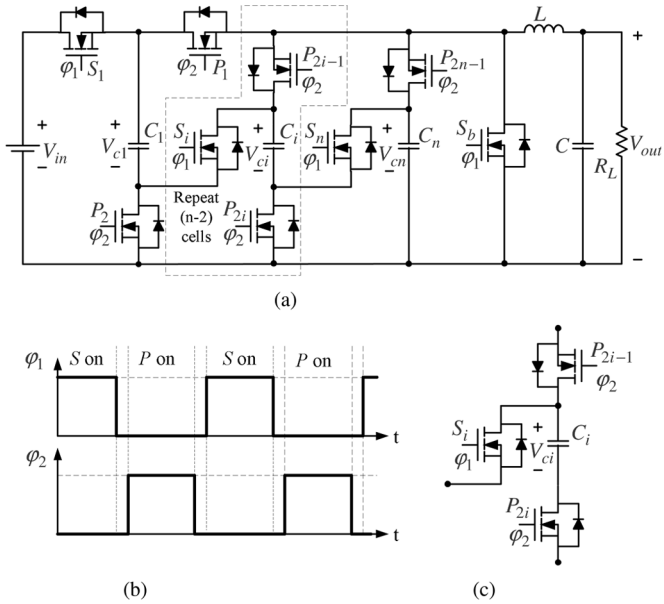


Fig. 1. Overview of the modified SC-buck converter. (a) Topology. (b) Timing diagram. (c) Single cell.

This paper is organized as follows. Section II shows the modified topology of the SC-buck converter and its working principle. Section III gives an analysis on the efficiency of the converter using an energy-flow approach. Section IV describes the control mechanism of the SC-buck converter. Section V shows the experimental results of the modified circuit. Section VI gives a guideline on the design of the SC-buck converter. Section VII gives the conclusions to this paper.

II. Hybrid Switched-Capacitor Buck Converter

A modified version of the hybrid SC-buck converter that was originally reported in [24] is illustrated in this paper. Using the proposed hybrid SC-buck converter with n flying capacitors (hereon known only as SC-buck converter), the effect of having a different step-down conversion ratio in the first-stage SC converter on the SC-buck converter is theoretically investigated in this section and experimentally verified in Section V. Some insights to the design of the converter can be obtained from this analysis.

Fig. 1 shows the SC-buck converter and its timing diagram. Fig. 2 shows its three operating states.

In State 1, all S switches are "ON" and all P switches are "OFF." $V_{\rm in}$ charges the flying capacitors $C_1, C_2, \ldots, C_n$, which are connected in series as illustrated in Fig. 2(a). Concurrently, the buck stage of the converter is in freewheeling mode, of which the current in L freewheels through S_b.

In State 2, all S switches are "OFF" and all P switches are "ON." All the flying capacitors are connected in parallel and discharge to the buck stage of the converter as shown in Fig. 2(b).

In State 3, all switches are "OFF" as indicated in Fig. 2(c). Flying capacitors are neither charging nor discharging. The current in L freewheels through the body diode of S_b.

The equivalent circuits of State 1 and State 2 shown in Fig. 3 can be illustrated as given in Fig. 3(a) and (b), respectively, where $r_{\rm dson}$ is the turn-on resistance of the switch, $r_{\rm esr}$ is the resistance of each flying capacitor, $r_{\rm esr\_C}$ is the resistance of the output capacitor C, and $r_{\rm esr\_L}$ is the resistance of L.

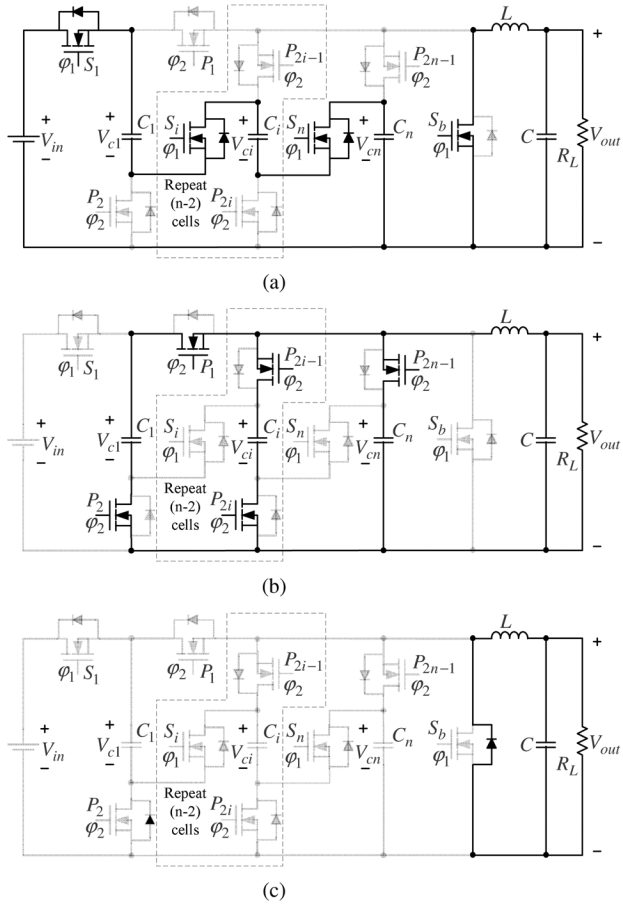


Fig. 2. Operating states of the modified SC-buck converter. (a) State 1. (b) State 2. (c) State 3.

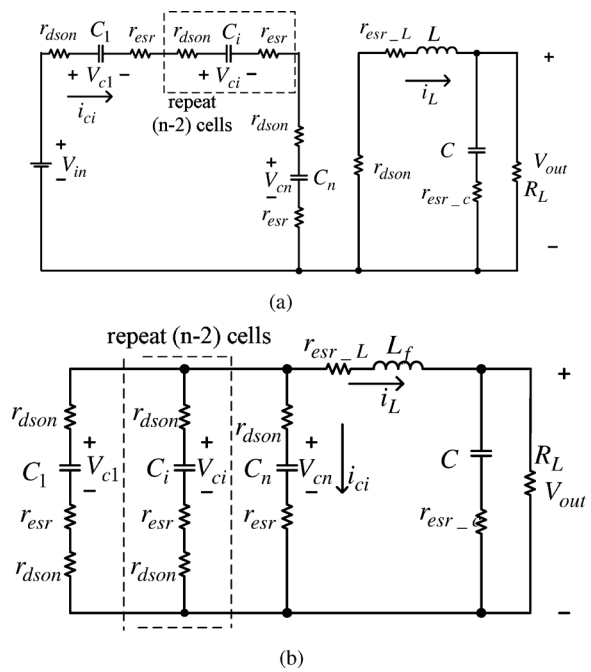


Fig. 3. Equivalent circuit of the converter. (a) State 1: Charging equivalent circuit. (b) State 2: Discharging equivalent circuit.

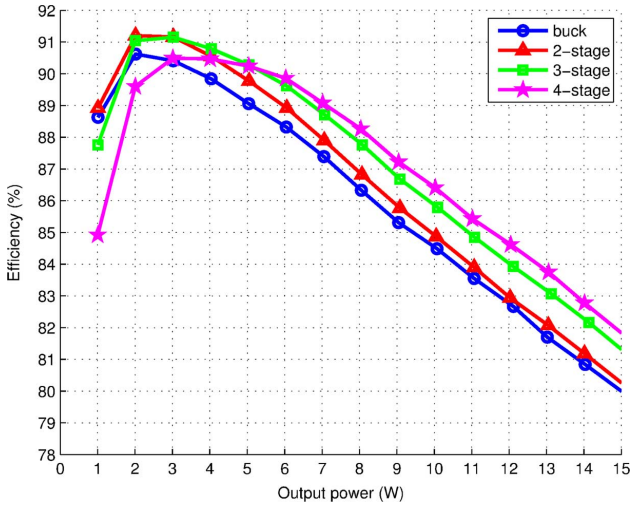


Fig. 4. Comparison of experimentally measured efficiencies among SC-buck converters with $n = 2, 3, 4$ and a buck converter (i.e., $n = 1$).

TABLE I
PARAMETERS OF SC-BUCK CONVERTER

$V_{\rm in}$ & $V_{\rm out}$	f_S	MOSFET
12 V & 1 V	200 kHz	Si7356ADP
$C_1, C_2 \cdots C_n$	L	C
94 μF	13 μH	410 μF

A prototype based on the SC-buck topology ($n = 2, 3, 4$) given in Fig. 1(a) and parameters given Table I is constructed. The number n can be modified by connecting or bypassing the single-cell structure depicted in Fig. 1(c). Experiment is performed to compare the performance of this converter against a conventional buck converter. Both the buck converters have the same C and f_S. Operating at the same 12 V input and 1 V output condition, it can be seen from Fig. 4 that the SC-buck converters gives a better efficiency than the conventional buck converter, except when it is at very light-load condition, similar to what has been reported in [7] and [22]. From Fig. 4, it is observed that a higher n of SC-buck converter always give a better efficiency at heavy load. However, depending on the loading condition, there is an optimal n that allows the SC-buck converter to achieve the best possible efficiency. In the next section, the efficiency of the SC-buck converter will be studied.

III. EFFICIENCY ANALYSIS

From Fig. 2, the energy-flow mechanism of the SC-buck converter can be seen as having two parts as depicted in Fig. 5. First, in State 1, energy is transferred from the power source $V_{\rm in}$ to the flying capacitors through the SC-stage with a "charging efficiency" of η_C. In this state, energy is temporarily stored in the flying capacitors. Then, in State 2, the energy stored in the capacitors will be transferred to the load through the buck-stage with a "discharging efficiency" of η_D. Averaged over a switching period, the energy in the flying capacitors is kept constant during steady state. The overall efficiency of SC-buck converter is the product of the charging efficiency and the discharging efficiency, i.e., $\eta_{\rm overall} = \eta_C \cdot \eta_D$.

The circuit in Fig. 3(a) can be further simplified into equivalent circuits representing the charging, discharging and free-

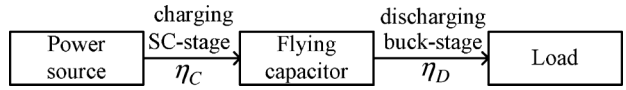


Fig. 5. Energy-flow diagram of a SC-buck converter.

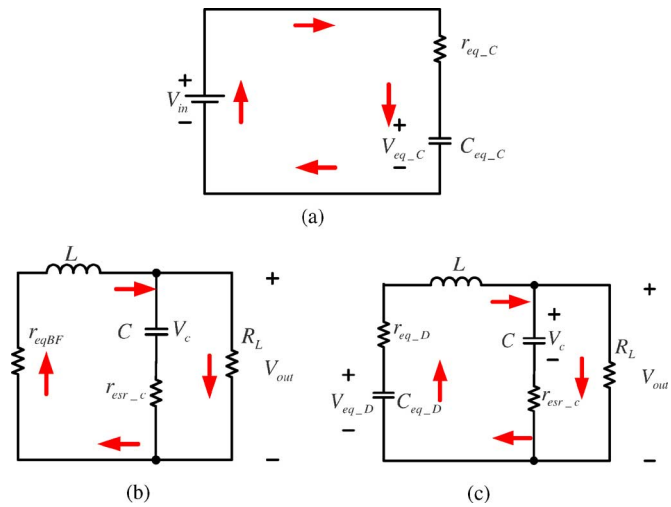


Fig. 6. Simplified equivalent circuits of the charging, discharging and free-wheeling operations of the SC-buck converter. (a) Charging operation. (b) Free-wheeling operation. (c) Discharging operation.

wheeling operations as given in Fig. 6(a)–(c), respectively. For Fig. 6(a), $C_{\rm eq\_C} = C_1/n = C_{\rm sum}/n^2$ and $r_{\rm eq\_C} = n \cdot (r_{\rm dson} + r_{\rm esr})$. For Fig. 6(b), $r_{\rm eqBF} = r_{\rm dson} + r_{\rm esr\_L}$. For Fig. 6(c), $C_{\rm eq\_D} = n \cdot C_1 = C_{\rm sum}/n$ and $r_{\rm eq\_C} = (r_{\rm dson} + r_{\rm esr})/n$. Here, $C_{\rm sum} = C_1 + \cdots + C_n$.

A. Charging Efficiency η_C

The charging efficiency η_C given in the energy-flow diagram in Fig. 5 can be obtained by analyzing the RC circuit given in Fig. 6(a). In this state, the energy stored in the flying capacitors will be transferred to the buck stage in the following state. The energy change would have an influence on the charging efficiency. The key point of calculating charging efficiency is to obtain the initial voltage of the flying capacitors. The method of deriving the charging efficiency of an equivalent RC circuit of an SC converter is given in [8]. Here, we apply the method to this converter.

First, the voltage across $C_{\rm eq\_C}$ is

$$V_{\rm eq\_C}(t) = V_{\rm in}\left[1 - (1-b)e^{-\frac{t}{\tau}}\right], \tag{1}$$

where $b = V_{\rm eq\_C(i)}/V_{\rm in}$, $\tau = r_{\rm eq\_C}C_{\rm eq\_C}$, and that $V_{\rm eq\_C(i)}$ is the initial voltage of the equivalent flying capacitor. The total energy stored in $C_{\rm eq\_C}$ in each switching period is

$$\Delta E_C(t) = \frac{1}{2}C_{\rm eq\_C}\left(V^2_{\rm eq\_C}(t) - V^2_{\rm eq\_C(i)}\right). \tag{2}$$

This stored energy will be discharged into the buck stage. We denote ΔE_T as the energy consumed by the buck stage in one period. Therefore, $\Delta E_C(T_{\rm on}) = \Delta E_T$.

Assume the input power of the buck stage of the SC-buck converter is $P_{\rm bin}$. In one switching period, the input energy is

$$\Delta E_T = P_{\rm bin}T = P_{\rm bin}/f_S. \tag{3}$$

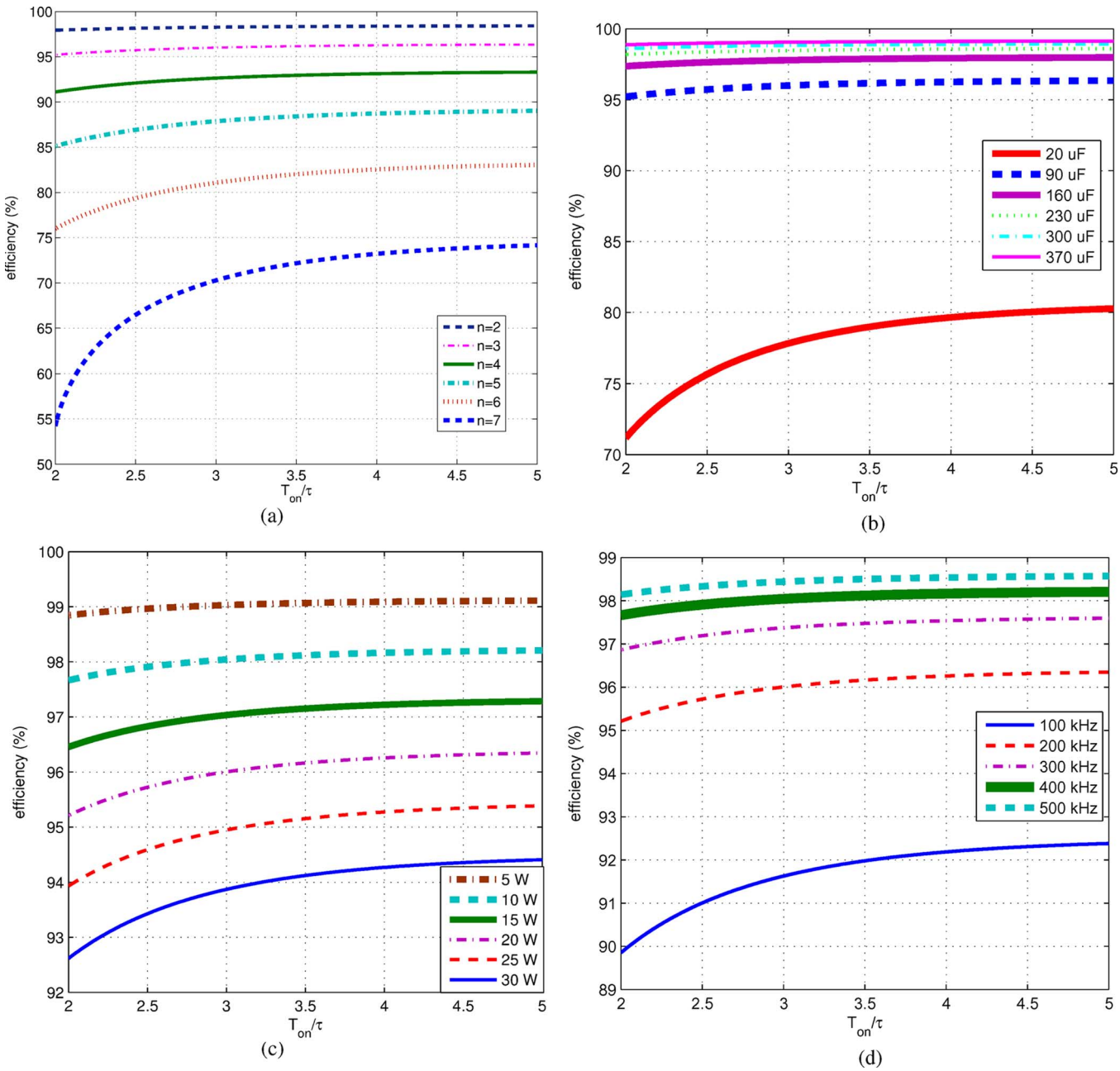


Fig. 7. Properties of SC-stage charging efficiency. (a) Plot of calculated charging efficiency for different n. (b) Plot of calculated charging efficiency for different $C_{\rm sum}$. (c) Plot of calculated charging efficiency for different $P_{\rm bin}$. (d) Plot of calculated charging efficiency for different switching frequency f_s.

At steady state, for each period, the energy stored in $C_{\rm eq\_C}$ is equal to this input energy, i.e., $\Delta E_C(T_{\rm on}) = \Delta E_T$, giving

$$V_{\rm eq\_C}^2(T_{\rm on}) - V_{\rm eq\_C(i)}^2 = \frac{2P_{\rm bin}}{f_S C_{\rm eq\_C}}. \tag{4}$$

By substituting (1) into (4) and solving the equation, the initial voltage can be derived as

$$b = \frac{1}{1+e^{-\frac{T_{\rm on}}{\tau}}} \times \left[e^{-\frac{T_{\rm on}}{\tau}} + \sqrt{1 - \frac{2P_{\rm bin}\left(1+e^{-\frac{T_{\rm on}}{\tau}}\right)}{f_S C_{\rm eq\_C} V_{\rm in}^2\left(1-e^{-\frac{T_{\rm on}}{\tau}}\right)}}\right]. \tag{5}$$

By substituting $V_{\rm eq\_C(i)} = b \cdot V_{\rm in}$ into the charging efficiency equation in [8] where $\eta_C = (V_{\rm eq\_C}(t) + V_{\rm eq\_C(i)})/(2V_{\rm in})$, we get

$$\eta_C = \frac{(1+b) - (1-b)e^{-\frac{T_{\rm on}}{\tau}}}{2}. \tag{6}$$

Fig. 7(a) gives the charging efficiency plot obtained from (6) for different n of which the total capacitance is kept constant with $C_{\rm sum} = 90\ \mu$F at $P_{\rm bin} = 20$ W and $f_S = 200$ kHz. Fig. 7(b) illustrates the charging efficiency for different values of $C_{\rm sum}$ at $f_s = 200$ kHz, $P_{\rm bin} = 20$ W, $n = 3$, $V_{\rm in} = 12$ V, and $V_o = 1$ V. Fig. 7(c) shows the charging efficiency for different $P_{\rm bin}$ at $f_s = 200$ kHz, $C_{\rm sum} = 90\ \mu$F, $n = 3$, $V_{\rm in} = 12$ V, and $V_o = 1$ V. Fig. 7(d) shows the charging efficiency for different

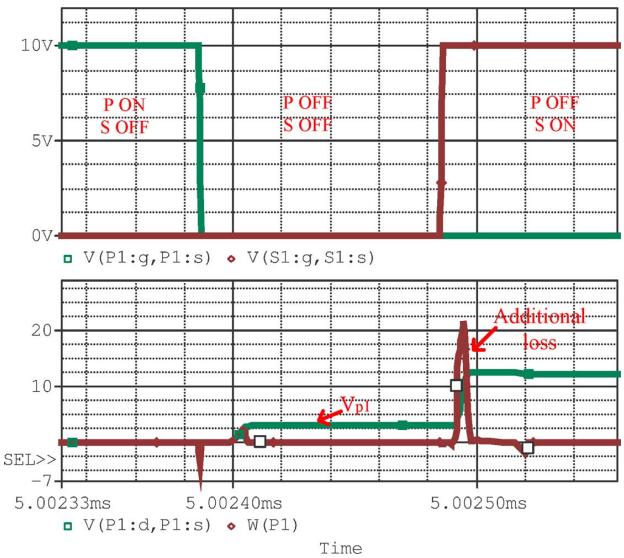


Fig. 8. Waveforms of P switches during the transition from State 3 to State 1.

switching frequency f_s with $C_{\rm sum} = 90\ \mu$F, $P_{\rm bin} = 20$ W, $n = 3$, $V_{\rm in} = 12$ V and $V_o = 1$ V.

From the calculated results, the following conclusions can be deduced:

1) When the value of capacitor $C_{\rm sum}$ is fixed, having more flying capacitors gives a lower charging efficiency.
2) With a longer charging time $T_{\rm on}$ in (6), the charging efficiency η_C is higher.
3) A bigger $C_{\rm sum}$ value leads to a higher charging efficiency. However, the rate of increase in charging efficiency decreases with an increasing $C_{\rm sum}$.
4) A heavier load gives a lower charging efficiency.
5) A faster switching frequency leads to a higher charging efficiency.

B. Discharging Efficiency η_D

The discharging efficiency of the SC-buck converter is mainly influenced the buck stage of the converter, of which it is being used to process and deliver energy from the flying capacitors to the output. Our study shows that the buck-stage efficiency of the SC-buck converter is dominantly the efficiency of a conventional buck converter plus an additional parasitic capacitor charging loss that is not present in the buck converter. The power loss of buck converter is well documented in many papers. It includes the conduction loss, switching loss, and the ESR loss. In the SC-buck converter, the power loss includes the following losses.

1) Conduction Loss:

i. Conduction loss on each branch's switches:

$$\begin{cases} P_{\rm c\_sw\_up} = R_{\rm dson} D \left(I_o^2 + \frac{\Delta I_L^2}{12} \right) & \text{(upper switch)} \\ P_{\rm c\_sw\_dn} = R_{\rm dson} D \left(I_o^2 + \frac{\Delta I_L^2}{12} \right) & \text{(lower switch)}, \end{cases} \tag{7}$$

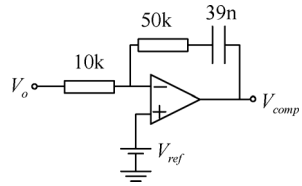


Fig. 9. Compensation circuit of the controller in the experimental prototype.

where I_o is the output current and ΔI_L is the inductor current ripple.

ii. Conduction loss on the buck-stage switch:

$$P_{\rm c\_sw\_Sb} = R_{\rm dson} \left(1 - D - \frac{2T_{\rm dt}}{T} \right) \left(I_o^2 + \frac{\Delta I_L^2}{12} \right). \tag{8}$$

iii. Conduction loss on the body diode of buck-stage switch:

$$P_{\rm c\_diode\_Sb} = 2 f_S V_{\rm fd} I_o T_{\rm dt}, \tag{9}$$

where $V_{\rm fd}$ is the forward diode voltage of S_b and $T_{\rm dt}$ is the dead time. Thus, the total conduction loss is

$$P_c = nP_{\rm c\_sw\_up} + (n-1)P_{\rm c\_sw\_up} + P_{\rm c\_sw\_Sb} + P_{\rm c\_diode\_Sb}. \tag{10}$$

2) Switching Loss:

i. Switching loss on switches of each branch, which includes the switching loss on the upper switches:

$$\begin{cases} P_{\rm sw\_on\_up} = f_S V_{\rm C\_on} I_{\rm d\_on} \frac{t_{ri}+t_{fu}}{2} \\ P_{\rm sw\_off\_up} = f_S V_{\rm C\_off} I_{\rm d\_off} \frac{t_{ru}+t_{fi}}{2}, \end{cases} \tag{11}$$

and the switching loss on the lower switches:

$$\begin{cases} P_{\rm sw\_on\_dn} = f_S V_{\rm C\_on} I_{\rm d\_on} \frac{t_{ri}+t_{fu}}{2} \\ P_{\rm sw\_off\_dn} = f_S V_{\rm fd} I_{\rm d\_off} \frac{t_{ru}+t_{fi}}{2}, \end{cases} \tag{12}$$

where $I_{\rm d\_on}$ and $I_{\rm d\_off}$ are respectively the branch current of the capacitor when P is turned on and off.

ii. Switching loss of the body diode of buck-stage switch:

$$P_{\rm sw\_diode\_Sb} = f_S C_{\rm oss} V_{\rm inb\_on}^2, \tag{13}$$

where $V_{\rm inb\_on}$ is the voltage of flying capacitor when P is turned on. Thus, the total switching loss is

$$P_{\rm sw} = n(P_{\rm sw\_on\_up} + P_{\rm sw\_off\_up}) + (n+1) \times (P_{\rm sw\_on\_dn} + P_{\rm sw\_off\_dn}) + P_{\rm sw\_diode\_Sb}. \tag{14}$$

3) ESR Loss:

i. Loss on the ESR of inductor:

$$P_{\rm esr\_L} = r_{\rm esr\_L} \left(I_o^2 + \frac{\Delta I_L^2}{12} \right). \tag{15}$$

ii. Loss on the ESR of a flying capacitor:

$$P_{\rm esr\_C} = r_{\rm esr\_C} D \left(I_o^2 + \frac{\Delta I_L^2}{12} \right). \tag{16}$$

Thus, the total ESR loss is

$$P_{\rm esr} = P_{\rm esr\_L} + nP_{\rm esr\_C}. \tag{17}$$

4) Parasitic Capacitor Charging Loss: When the SC-buck converter switches from State 3 to State 1, the voltage across all the P switches will change. This causes the parasitic capacitor of the P switches to charge up to a certain voltage level, generating an additional charging loss. Fig. 8 shows the simulation voltage and current waveforms of the SC-buck converter during the transition from State 3 to State 1, which introduces the additional power loss.

The equation describing the parasitic capacitor charging loss of each P switch is given as

$$\begin{cases} P_{\rm ad\_up} = f_s C_{\rm oss} V_{\rm sw\_up}^2 \\ P_{\rm ad\_dn} = f_s C_{\rm oss} V_{\rm sw\_dn}^2, \end{cases} \tag{18}$$

where $V_{\rm sw\_up}$ and $V_{\rm sw\_dn}$ are respectively the voltages of the upper and lower switches of each branch. For n number of P switches, the parasitic capacitor charging loss is

$$P_{\rm ad} = P_{\rm ad\_up\_1} + \cdots + P_{\rm ad\_up\_}n + P_{\rm ad\_dn\_1} + \ldots + P_{\rm ad\_dn\_(n-1)}. \tag{19}$$

Finally, the overall power loss of the buck-stage is

$$P_{\rm dis\_loss} = P_c + P_{\rm sw} + P_{\rm esr} + P_{\rm ad}. \tag{20}$$

Then, the discharging efficiency of the SC-buck converter is

$$\eta_D = \frac{P_o}{P_o + P_{\rm dis\_loss}} \times 100\%. \tag{21}$$

IV. Control Mechanism of the SC-Buck Converter

As the buck stage of the SC-buck converter is switching between the freewheeling and the discharging operation [see Fig. 6(b) and (c)], it behaves similarly to a simple duty-cycle controlled buck converter. Hence, only an ordinary voltage-mode controller will be needed for the control of the buck stage of the SC-buck converter. With this controller, the compensator can be designed using the pole placement approach. For this work, the adopted controller has a compensation network with the transfer function $G_c(s) = 5 + (1)/(0.00039s)$. Fig. 9 shows the implementation circuit of the compensation network used in the experimental prototype.

V. Experimental Results

In order to verify the calculation method and the properties of the topology, a prototype has been built. The parameters are shown in Table I. Fig. 10 shows the output voltage waveform of a SC-buck converter with 5 flying capacitors ($n = 5$) under a constant load of 15 A. In comparison to the flying capacitor voltage of the first-stage SC converter, the final output voltage waveform of the SC-buck converter contains a much smaller voltage ripple.

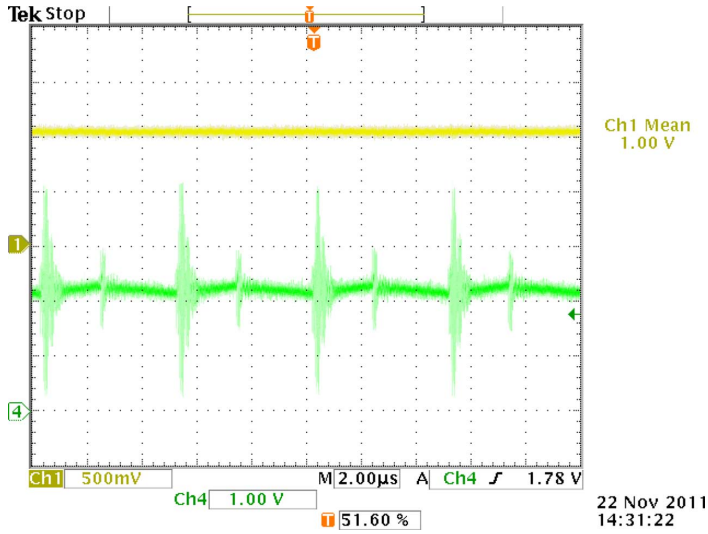


Fig. 10. Output voltage waveform of a SC-buck converter with 5 flying capacitors ($n = 5$) (Ch1: buck output voltage; Ch4: SC flying capacitor voltage).

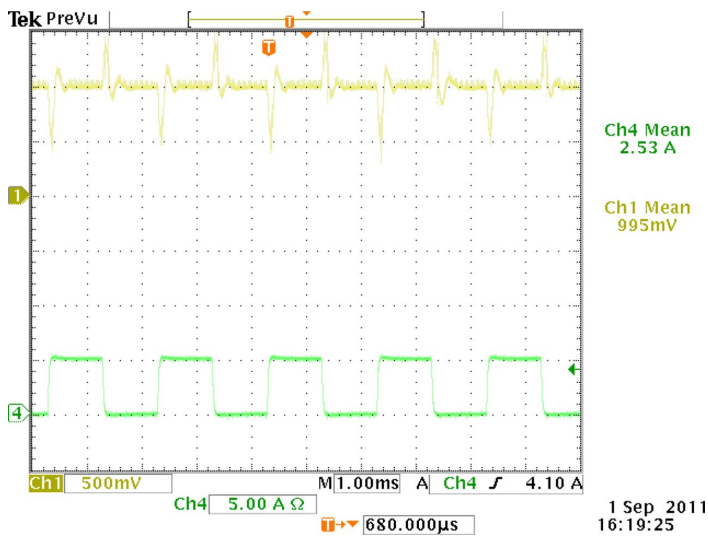


Fig. 11. Output voltage waveform of the proposed converter with closed-loop control with an active load switching between 0 A and 5 A (Ch1: Output voltage; Ch4: Output current).

Fig. 11 depicts the closed-loop output voltage waveforms of the SC-buck converter operating with an active load switching between 0 A and 5 A, showing that ordinary voltage-mode control can be applied to the SC-buck converter with good result.

Fig. 12 gives a comparison of the calculated efficiencies and the experimental efficiencies at various output power levels and value of n. The efficiency curves fit well at higher power levels. The small discrepancy at lower power levels may be due to the relative higher measurement error at the lower power levels.

Fig. 13 gives the experimental efficiency curves at various output power levels using a different n. The results show that

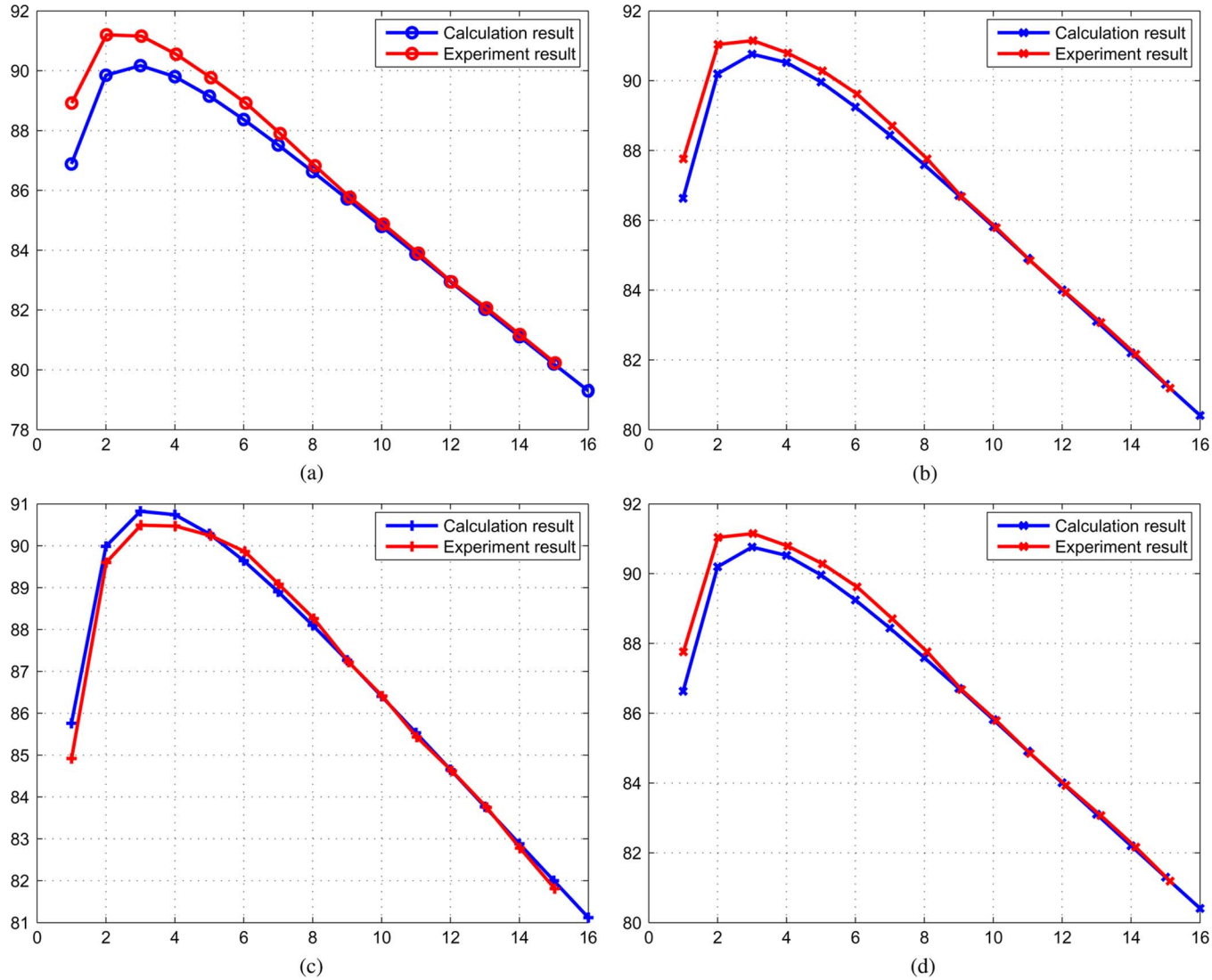


Fig. 12. Plots of the experimentally measured efficiencies and calculated efficiencies for the SC-buck converter with (a) $n = 2$, (b) $n = 3$, (c) $n = 4$, and (d) $n = 5$.

there is a best n to achieve a highest efficiency at different loading conditions.

VI. Circuit Design and Optimization

Four parameters are needed to start a design: input voltage ($V_{\rm in}$), output voltage (V_o), maximum output current ($I_{o\_{\rm Max}}$) and the switching frequency (f_s). With these parameters, the component design of the converter circuit can be carried out based on the number of capacitor n chosen, as given in the following subsection.

A. Components Selection

i. *Inductor:* Assuming that the switch of the buck is ideal, then

$$L = V_o \cdot \left(1 - \frac{V_o}{V_{\rm in}}\right) \cdot \frac{1}{f_s} \frac{1}{\Delta I_L}. \tag{22}$$

where $\Delta I_L = p \cdot I_{o\_{\rm Max}}$, and p is typically chosen as 0.3.

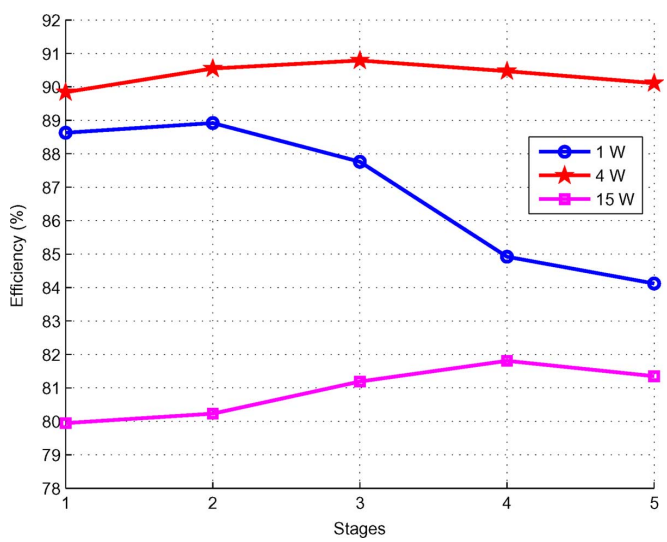


Fig. 13. Experimental result of the SC-buck converter for 1 W, 4 W, and 15 W loading with different n.

TABLE II
VOLTAGES OF PARALLEL SWITCHES AT DIFFERENT STATES

	$S_{off}P_{on}$	$S_{off}P_{off}$	$S_{on}P_{off}$	$S_{off}P_{off}$
$V(P_1)$	0	V_{c1}	$V_{\rm in}$	$V_{\rm in}$
$V(P_3)$	0	V_{c2}	$V_{\rm in}-V_{c1}$	$V_{\rm in}-V_{c1}$
$\cdots$	0	$\cdots$	$\cdots$	$\cdots$
$V(P_{2n-1})$	0	V_{cn}	$V_{\rm in}-V_{c1}-\cdots-V_{cn}$	$V_{\rm in}-V_{c1}-\cdots-V_{cn}$
$V(P_2)$	0	V_D	$V_{c2}+\cdots+V_{cn}$	$V_{c2}+\cdots+V_{cn}$
$V(P_4)$	0	V_D	$V_{c3}+\cdots+V_{cn}$	$V_{c3}+\cdots+V_{cn}$
$\cdots$	0	V_D	$\cdots$	$\cdots$
$V(P_{2n})$	0	V_D	V_{cn}	V_{cn}

ii. *Output capacitor:* The output capacitor dictates the ripple of output voltage. The output voltage ripple is

$$\Delta V_o = \Delta I_L \cdot (\mathrm{ESR} + \Delta T/C_o). \tag{23}$$

Rearranging (23), we have

$$C_o = \frac{\Delta T}{\frac{\Delta V_o}{\Delta I_L} - \mathrm{ESR}}, \tag{24}$$

where $\Delta T = \max\{(V_o)/(V_{\rm in}) \cdot (1)/(f_s), (1-(V_o)/(V_{\rm in})) \cdot (1)/(f_s)\}$, and ESR is the equivalent series resistance of output capacitor. Using (24), the value of the output capacitor is determined. Typically, the output voltage ripple is mainly contributed by the ESR of output capacitor.

iii. *Flying capacitor:* A proper value of the flying capacitor will improve the charging efficiency. Equation (5) gives the initial voltage b, which indicates the minimum voltage of the flying capacitors. Furthermore, it also dictates the charging efficiency. To obtain a high charging efficiency, b should be higher than 0.95. Although (5) can give an exact value of the flying capacitor, it is difficult to solve. A simplified version of this equation is desired. Assume the discharging efficiency is 100%. Then,

$$P_{o\_\rm Max} = \frac{1}{2} f_s \cdot C_{\rm sum} \cdot \left(\frac{V_{\rm in}}{n} - \Delta V_f\right) \cdot \Delta V_f, \tag{25}$$

where ΔV_f is the voltage drop of flying capacitors. In (25), ΔV_f is relatively low compared with $(V_{\rm in})/(n)$. So, (25) can be simplified as

$$P_{o\_\rm Max} = \frac{1}{2} f_s \cdot C_{\rm sum} \cdot \frac{V_{\rm in}}{n} \cdot \Delta V_f. \tag{26}$$

By rearranging (26) and setting $\Delta V_f = (1-b)\cdot(V_{\rm in}/(n)$, the flying capacitor can be simplified as

$$C_{\rm sum} = \frac{2 \cdot n^2 \cdot V_o \cdot I_{o\_\rm Max}}{(1-b) \cdot f_s \cdot V_{\rm in}^2}. \tag{27}$$

iv. *Switch:* Essentially, the maximum voltage and current ratings of the switches can be determined using a scaling function of n multiplied by $V_{\rm in}$ or I_o, as shown in Table IV. Most of the scaling functions are simple factors of n. However, the charging currents passing through the switches $(S_1 \ldots S_n)$ are controlled by the circuit. The maximum current passing through these switches is

$$I_{\rm max} = \frac{\Delta V_f}{R_{\rm dson}}. \tag{28}$$

TABLE III
COMPARISON OF DIFFERENT STAGES SC-BUCK CONVERTER COMPONENTS USED

Stages	Buck	2-stage	3-stage	$\cdots$	n-stage
Switches	2	6	6	$\cdots$	$3n$
Flying capacitors	none	2	3	$\cdots$	n
Inductor	1	1	1	$\cdots$	1
Output Capacitor	1	1	1	$\cdots$	1

The parameter $R_{\rm dson}$ not only affects the maximum charging current, but also dictates the time constant τ, which affects the charging time. In order to have a high charging efficiency, the charging time should be at least three times higher than the time constant τ. So,

$$R_{\rm dson} = \frac{n}{3} \cdot \frac{1}{C_{\rm sum}} \cdot \left(1 - \frac{n \cdot V_o}{V_{\rm in}}\right) \cdot \frac{1}{f_s}. \tag{29}$$

Substitute (29) into (28), the maximum current passing through the switches $(S_1 \ldots S_n)$ is given as

$$I_{\rm max} = \frac{3 f_s C_{\rm sum} \Delta V_f}{n \cdot \left(1 - \frac{n \cdot V_o}{V_{\rm in}}\right)}. \tag{30}$$

B. Design and Optimization of the SC-Buck Converter

In the previous subsection, methods of selecting the components are introduced. Here, the design and optimization procedure will be given as follows.

1) Preset the four design specifications of input voltage $(V_{\rm in})$, output voltage (V_o), maximum output current $(I_{o\_\rm Max})$ and the switching frequency (f_s).
2) The maximum number of stages $n_{\rm max} = \mathrm{floor}(V_{\rm in}/V_{\rm out})$ is calculated.
3) For $n = 2$ to $n_{\rm max}$, components are selected as illustrated in Section VI-A. A best efficiency of this n at a particular loading condition can be found as illustrated in Section III.
4) Based on the results of different n's, an optimal n can be obtained.

VII. CONCLUSION

This paper presents an analysis on the effect of having different number of flying capacitors n in the first-stage SC circuit of an improved SC-buck converter for high-voltage-gain conversion. The analysis shows that a higher n in the SC stage with the same overall capacitance leads to a lower charging efficiency. On the other hand, the buck-stage efficiency is dependent on the operating conditions and design parameters. A higher n leads to a higher discharging efficiency. Since the overall efficiency is the multiplication of the charging efficiency and the discharging efficiency, there will be an optimal n in terms of efficiency for each switched-capacitor buck converter at a particular load. The experimental results confirms the analytical findings. As such, a design and optimization procedure is developed for the hybrid switched-capacitor buck converter for choosing the optimal n. It is also shown that the converter can easily be controlled using ordinary voltage-mode control for buck converter.

TABLE IV
COMPONENTS' PARAMETERS

	Stages	2-stage	3-stage	⋯	n-stage
	Inductor	$V_o \cdot (1-\frac{2\cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}$	$V_o \cdot (1-\frac{3\cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}$	⋯	$V_o \cdot (1-\frac{n\cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}$
	Output Capacitor	$\frac{\max\{\frac{V_o}{V_{\text{in}}}\cdot\frac{1}{f_s},(1-\frac{V_o}{V_{\text{in}}})\cdot\frac{1}{f_s}\}}{\frac{\Delta V_o}{\Delta I_L}-ESR}$	$\frac{\max\{\frac{V_o}{V_{\text{in}}}\cdot\frac{1}{f_s},(1-\frac{V_o}{V_{\text{in}}})\cdot\frac{1}{f_s}\}}{\frac{\Delta V_o}{\Delta I_L}-ESR}$	⋯	$\frac{\max\{\frac{V_o}{V_{\text{in}}}\cdot\frac{1}{f_s},(1-\frac{V_o}{V_{\text{in}}})\cdot\frac{1}{f_s}\}}{\frac{\Delta V_o}{\Delta I_L}-ESR}$
	Flying Capacitors	$\frac{4\cdot V_o\cdot I_{o\ Max}}{(1-b)\cdot f_s\cdot V_{\text{in}}^2}$	$\frac{6\cdot V_o\cdot I_{o\ Max}}{(1-b)\cdot f_s\cdot V_{\text{in}}^2}$	⋯	$\frac{2\cdot n\cdot V_o\cdot I_{o\ Max}}{(1-b)\cdot f_s\cdot V_{\text{in}}^2}$
Switch S_1:	$V_{\max}$	$\frac{1}{2}\cdot V_{\text{in}}$	$\frac{2}{3}\cdot V_{\text{in}}$	⋯	$\frac{n-1}{n}\cdot V_{\text{in}}$
	$I_{\max}$	$\frac{3f_sC_{sum}\Delta V_f}{2\cdot(1-\frac{2\cdot V_o}{V_{\text{in}}})}$	$\frac{f_sC_{sum}\Delta V_f}{(1-\frac{3\cdot V_o}{V_{\text{in}}})}$	⋯	$\frac{3f_sC_{sum}\Delta V_f}{n\cdot(1-\frac{n\cdot V_o}{V_{\text{in}}})}$
Switch S_i, $(i=2\cdots n)$.	$V_{\max}$	$\frac{1}{2}\cdot V_{\text{in}}$	$\frac{1}{2}\cdot V_{\text{in}}$	⋯	$\frac{1}{n}\cdot V_{\text{in}}$
	$I_{\max}$	$\frac{3f_sC_{sum}\Delta V_f}{2\cdot(1-\frac{2\cdot V_o}{V_{\text{in}}})}$	$\frac{f_sC_{sum}\Delta V_f}{(1-\frac{3\cdot V_o}{V_{\text{in}}})}$	⋯	$\frac{3f_sC_{sum}\Delta V_f}{n\cdot(1-\frac{n\cdot V_o}{V_{\text{in}}})}$
Switch S_b:	$V_{\max}$	$\frac{1}{2}\cdot V_{\text{in}}$	$\frac{1}{3}\cdot V_{\text{in}}$	⋯	$\frac{1}{n}\cdot V_{\text{in}}$
	$i_{\max}$	I_o	I_o	⋯	I_o
Switch P_1:	$V_{\max}$	V_{in}	V_{in}	⋯	V_{in}
	$I_{\max}$	$\frac{1}{2}\cdot I_o$	$\frac{1}{3}\cdot I_o$	⋯	$\frac{1}{n}\cdot I_o$
Switch P_{2i-1}, $(i=2\cdots n)$.	$V_{\max}$	$\frac{n-i+1}{2}\cdot V_{\text{in}}$	$\frac{n-i+1}{3}\cdot V_{\text{in}}$	⋯	$\frac{n-i+1}{n}\cdot V_{\text{in}}$
	$I_{\max}$	$\frac{1}{2}\cdot I_o$	$\frac{1}{3}\cdot I_o$	⋯	$\frac{1}{n}\cdot I_o$
Switch P_2:	$V_{\max}$	$\frac{1}{2}\cdot V_{\text{in}}$	$\frac{2}{3}\cdot V_{\text{in}}$	⋯	$\frac{n-1}{n}\cdot V_{\text{in}}$
	$I_{\max}$	$\frac{1}{2}\cdot I_o$	$\frac{1}{3}\cdot I_o$	⋯	$\frac{1}{n}\cdot I_o$
Switch P_{2i}, $(i=2\cdots n-1)$.	$V_{\max}$	$\frac{n-i}{2}\cdot V_{\text{in}}$	$\frac{n-i}{3}\cdot V_{\in}$	⋯	$\frac{n-i}{n}\cdot V_{\text{in}}$
	$I_{\max}$	$\frac{1}{2}\cdot I_o$	$\frac{1}{3}\cdot I_o$	⋯	$\frac{1}{n}\cdot I_o$

REFERENCES

[1] [Online]. Available: http://www.itrs.net/Links/2005ITRS/Home2005.htm

[2] J. Wei, P. Xu, H. P. Wu, F. C. Lee, K. Yao, and M. Ye, "Comparison of three topology candidates for 12 V VRM," in *IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2001, pp. 245–251.

[3] P. Xu, J. Wei, and F. C. Lee, "Multiphase coupled-buck converter—A novel high efficient 12 V voltage regulator module," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 74–82, Jan. 2003.

[4] J. Agrawal, D. Kastha, and B. Culpepper, "An improved control scheme for multiphase buck converter circuits used in voltage regulator modules," in *Proc. IEEE Conf. Power Electron. Drives Syst. (PEDS)*, Apr. 2006, pp. 418–423.

[5] J. J. Sun, Y. Qiu, M. Xu, and F. C. Lee, "High-frequency dynamic current sharing analyses for multiphase buck VRs," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2424–2431, Nov. 2007.

[6] R. Guo, Z. Liang, and A. Huang, "A multi-modes charge-pump based high efficiency wide input range DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2010, pp. 2706–2712.

[7] M. Xu, J. Sun, and F. C. Lee, "Voltage divider and its application in the two-stage power architecture," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2006, vol. 2, pp. 499–505.

[8] C. K. Cheung, S. C. Tan, Y. M. Lai, and C. K. Tse, "A new visit to an old problem in switched-capacitor converters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2010, pp. 3192–3195.

[9] S. V. Cheong, H. S. H. Chung, and A. Ioinovici, "Inductorless DC-DC converter with high power density," *IEEE Trans. Ind. Electron.*, vol. 41, no. 2, pp. 208–215, Apr. 1994.

[10] G. Zhu and A. Ioinovici, "Implementing IC based designs for 3.3 V supplies," *IEEE Circuits Devices Mag.*, vol. 11, no. 5, pp. 27–29, Sep. 1995.

[11] C. K. Tse, S. C. Wong, and M. H. L. Chow, "On lossless switched-capacitor power converters," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 286–291, May 1995.

[12] G. Zhu and A. Ioinovici, "DC-to-DC converter with no magnetic elements and enhanced regulation," *IEEE Trans. Aerosp. Electron. Sys.*, vol. 33, no. 2, pp. 499–506, Apr. 1997.

[13] D. Maksimovic and S. Dhar, "Switched-capacitor DC-DC converters for low-power on-chip applications," in *IEEE Power Electron. Specialists Conf. (PESC)*, Jul. 1999, vol. 1, pp. 54–59.

[14] G. Zhu, H. Wei, I. Batarseh, and A. Ioinovici, "A new switched-capacitor DC-DC converter with improved line and load regulation," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 1999, pp. 234–237.

[15] W. Chen, W. H. Ki, P. K. T. Mok, and M. Chan, "Switched-capacitor power converters with integrated low dropout regulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2001, pp. 293–296.

[16] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC-DC converters with a very high DC line-to-load voltage ratio," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2003, vol. 3, pp. 435–438.

[17] J. Han, A. V. Jouanne, and G. C. Temes, "A new approach to reducing output ripple in switched-capacitor-based step-down DC-DC converter," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1548–1555, Nov. 2006.

[18] J. Liu, Z. Chen, and Z. Du, "Switched capacitor DC-DC converters enable electronic products to become more compact," in *Proc. Int. Conf. Softw. Eng. (ICSE)*, Nov. 1996, pp. 234–237.

[19] J. Liu, Z. Chen, and Z. Du, "A new design of power supplies for pocket computer systems," *IEEE Trans. Ind. Electron.*, vol. 45, no. 2, pp. 228–235, Apr. 1998.

[20] Y. H. Chang, "Variable-conversion-ratio switched-capacitor-voltage-multiplier/divider DC-DC converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, pp. 1944–1957, Aug. 2011.

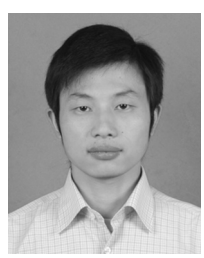
[21] R. D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," *IEEE Trans. Power Elect.*, vol. 3, no. 4, pp. 484–488, Oct. 1988.

[22] J. Sun, M. Xu, Y. Ying, and F. C. Lee, "High power density high efficiency system two-stage power architecture for laptop computers," in *IEEE Power Electron. Specialists Conf. Rec. (PESC)*, Jun. 2006, pp. 4008–4015.

[23] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *IEEE Power Electron. Specialists Conf. Rec. (PESC)*, Jun. 2008, pp. 4008–4015.

[24] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[25] S. Xiong, S. C. Tan, and S. C. Wong, "Analysis of a high-voltage-gain hybrid switched-capacitor buck converter," in *Proc., IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 1616–1619.



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